COMBINATION MOTOR DRIVERS WITH DC-DC CONVERTERS

Check for Samples: DRV8809, DRV8810

FEATURES

- **Configurable to Eight Modes of Combination Motor Driver**
  - **Bipolar Stepper Motor Driver**
    - **16-Step Current-Mode Control**
    - **800-mA Average Output Current as Stepper Motor Drive**
  - **DC Motor Driver**
    - **800-mA Maximum Continuous Current and 8-A/500-ns or 3-A/100-ms Peak Current for Each DC Motor Drive**
  - **Low ON resistance $R_{ds(ON)}$ = 0.55 Ω at T_J = 25°C (Typ)**
- **Three Integrated DC-DC Converters**
  - **On/Off Selectable Using C_SELECT Pin and Serial Interface**
  - **Outputs Programmable With External Resistor Network From 1.5 V to VDIN × 0.8**
  - **1.5-A Output Capability for All Three Channels**
- **7-V to 40-V Operating Voltage Range for DC-DC Converters**
- **Two Serial Interfaces for Communications**
- **Thermally-Enhanced Surface-Mount 64-Pin QFP PowerPAD™ Package (Eco-Friendly – RoHS and No Sb/Br)**
- **Power-Down Function (Deep-Sleep Mode)**
- **Reset Signal Output (Active Low)**
- **Reset (All Clear) Control Input**

DESCRIPTION/ORDERING INFORMATION

The DRV8809/DRV8810 provides an integrated motor driver solution. The chip has four H-bridges internally and is configurable to eight different modes of combination motor driver control.

The output driver block for each H-bridge consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The stepper motor control has a 16-step mode programmable through the three-wire serial interface (SPI). The SPI input pins are 3.3-V compatible and 5-V tolerant.

The DRV8809/DRV8810 has three DC-DC switch-mode buck converters to generate a programmable output voltage from 1.5 V to 80% of VDIN (Channel A) or up to 10 V (for Channel B and Channel C), with up to 1.5-A load current capability. The outputs are selected using the C_SELECT terminal at start-up or using serial interface during operation.

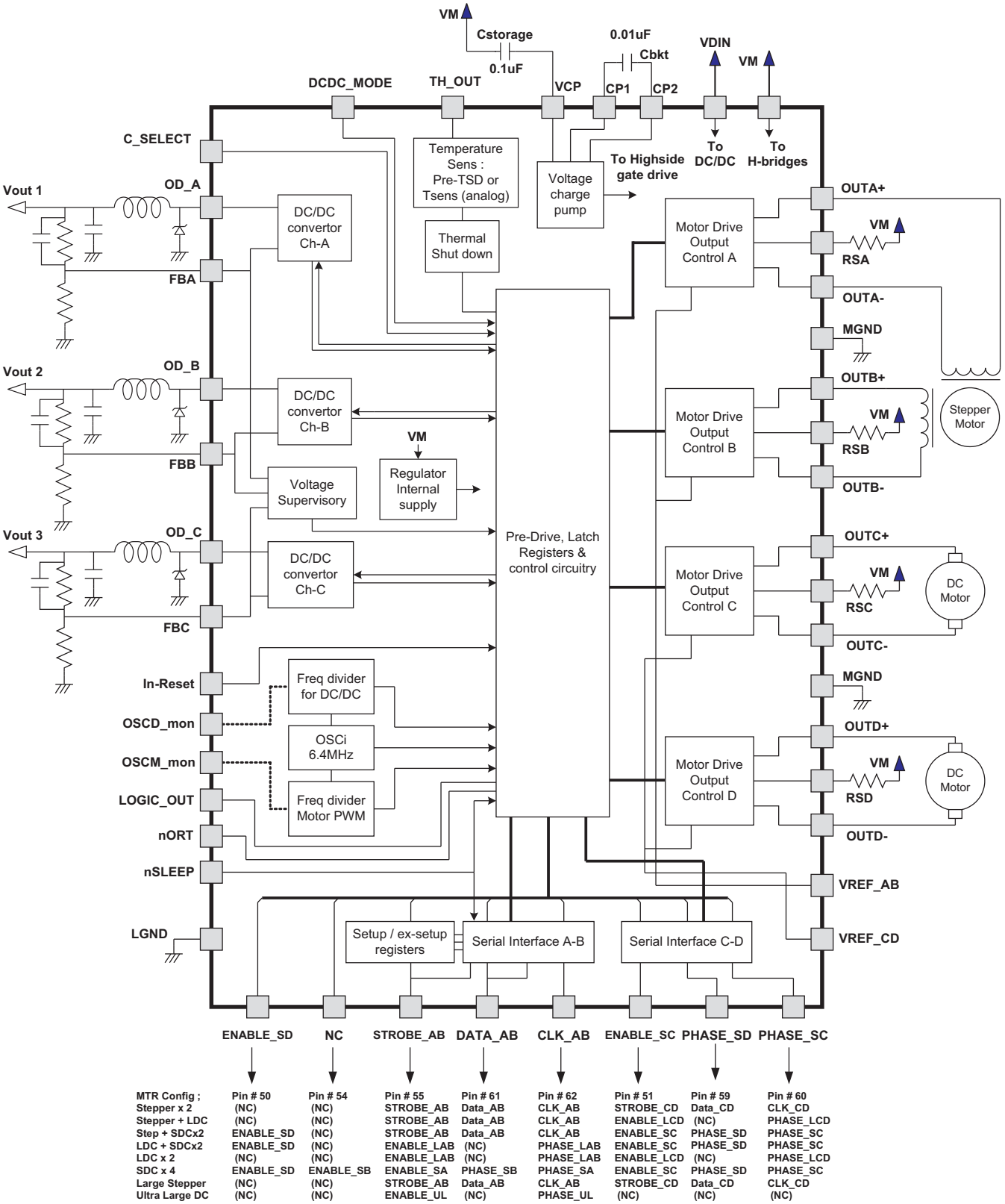
An internal shutdown function is provided for overcurrent protection (OCP), short-circuit protection, overvoltage/undervoltage lockout (UVLO), and thermal shutdown (TSD). Also, the device has a reset function that operates at power on and at input to the In-Reset pin.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 50°C	Plastic QFP 64 (S-PQFP-G64)	DRV8809A0PAP	DRV8809A0PAP
		DRV8810A0PAP	DRV8810A0PAP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM
(One Stepper Motor and Two DC Motor Drives)



MTR Config ;	Pin # 50	Pin # 54	Pin # 55	Pin # 61	Pin # 62	Pin # 51	Pin # 59	Pin # 60
Stepper x 2	(NC)	(NC)	STROBE_AB	Data_AB	CLK_AB	STROBE_CD	Data_CD	CLK_CD
Stepper + LDC	(NC)	(NC)	STROBE_AB	Data_AB	CLK_AB	ENABLE_LCD	(NC)	PHASE_LCD
Step + SDCx2	ENABLE_SD	(NC)	STROBE_AB	Data_AB	CLK_AB	ENABLE_SC	PHASE_SD	PHASE_SC
LDC + SDCx2	ENABLE_SD	(NC)	ENABLE_LAB	(NC)	PHASE_LAB	ENABLE_SC	PHASE_SD	PHASE_SC
LDC x 2	(NC)	(NC)	ENABLE_LAB	(NC)	PHASE_LAB	ENABLE_LCD	(NC)	PHASE_LCD
SDC x 4	ENABLE_SD	ENABLE_SB	ENABLE_SA	PHASE_SB	PHASE_SA	ENABLE_SC	PHASE_SD	PHASE_SC
Large Stepper	(NC)	(NC)	STROBE_AB	Data_AB	CLK_AB	STROBE_CD	Data_CD	CLK_CD
Ultra Large DC	(NC)	(NC)	ENABLE_UL	(NC)	PHASE_UL	(NC)	(NC)	(NC)

PAP PACKAGE
(TOP VIEW)

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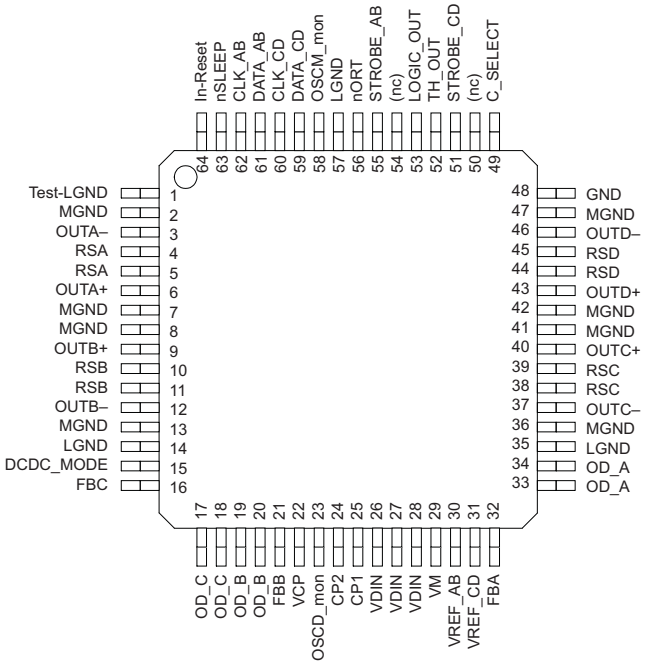
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL			I/O	PULLUP/ PULLDOWN	SHUNT RESISTOR	DESCRIPTION
NO.	NAME IN SETUP MODE	NAME IN OPERATION				
1	Test-LGND	Test-LGND	-			Low power or analog ground
2	MGND	MGND	-			Power ground for motor
3	OUTA-	OUTA-	O			Motor-drive output for winding A–
4	RSA	RSA	I			Channel A current-sense resistor
5	RSA	RSA	I			Channel A current-sense resistor
6	OUTA+	OUTA+	O			Motor-drive output for winding A+
7	MGND	MGND	-			Power ground for motor
8	MGND	MGND	-			Power ground for motor
9	OUTB+	OUTB+	O			Motor-drive output for winding B+
10	RSB	RSB	I			Channel B current-sense resistor
11	RSB	RSB	I			Channel B current-sense resistor
12	OUTB-	OUTB-	O			Motor-drive output for winding B–
13	MGND	MGND	-			Power ground for motor
14	LGND	LGND	-			Low-power or analog ground
15	DCDC_MODE	DCDC_MODE	I	Up	200 kΩ	DC-DC Ch-B/Ch-C operation mode select
16	FBC	FBC	I			Feedback signal for DC-DC converter C
17	OD_C	OD_C	O			Output for DC-DC switch mode regulator C
18	OD_C	OD_C	O			Output for DC-DC switch mode regulator C
19	OD_B	OD_B	O			Output for DC-DC switch mode regulator B
20	OD_B	OD_B	O			Output for DC-DC switch mode regulator B
21	FBB	FBB	I			Feedback signal for DC-DC converter B

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	PULLUP/ PULLDOWN	SHUNT RESISTOR	DESCRIPTION
NO.	NAME IN SETUP MODE	NAME IN OPERATION				
22	VCP	VCP	-			Charge pump capacitor
23	OSCD_mon	OSCD_mon	O			OSCD clock monitoring
24	CP2	CP2	-			Charge-pump bucket capacitor (high side)
25	CP1	CP1	-			Charge-pump bucket capacitor (low side)
26	VDIN	VDIN				Voltage supply for DC-DC converter
27	VDIN	VDIN				Voltage supply for DC-DC converter
28	VDIN	VDIN				Voltage supply for DC-DC converter
29	VM	VM	-			Voltage supply for motors
30	VREF_AB	VREF_AB	I			Voltage reference for maximum stepper motor current through A and B bridges
31	VREF_CD	VREF_CD	I			Voltage reference for maximum stepper motor current through C and D bridges
32	FBA	FBA	I			Feedback signal for DC-DC converter A
33	OD_A	OD_A	O			Output for DC-DC switch mode regulator A
34	OD_A	OD_A	O			Output for DC-DC switch mode regulator A
35	LGND	LGND	-			Low-power or analog ground
36	MGND	MGND	-			Power ground for motor
37	OUTC–	OUTC–	O			Motor-drive output for winding C–
38	RSC	RSC	I			Channel C current-sense resistor
39	RSC	RSC	I			Channel C current-sense resistor
40	OUTC+	OUTC+	O			Motor-drive output for winding C+
41	MGND	MGND	-			Power ground for motor
42	MGND	MGND	-			Power ground for motor
43	OUTD+	OUTD+	O			Motor-drive output for winding D+
44	RSD	RSD	I			Channel D current-sense resistor
45	RSD	RSD	I			Channel D current-sense resistor
46	OUTD–	OUTD–	O			Motor drive output for winding D–
47	MGND	MGND	-			Power ground for motor
48	GND	GND	-			Must be grounded
49	C_SELECT	C_SELECT	I	Up	200 kΩ	DC-DC converter selector
50	-	ENABLE_SD	I	Down	100 kΩ	Enable input for DC motor D control
50	-	Reserved	I	Down	100 kΩ	Reserved for DC motor operation
51	STROBE_CD	ENABLE_SC	I	Down	100 kΩ	Enable for DC motor C control
51	STROBE_CD	ENABLE_LCD	I	Down	100 kΩ	Enable for large DC motor CD control
51	STROBE_CD	STROBE_CD	I	Down	100 kΩ	Serial interface data strobe for H-bridge C, D stepper motor drive (latch on rising edge)
52	TH_OUT	TH_OUT	O	Open drain		Temperature-sensing output
53	LOGIC OUT	LOGIC OUT	O	Open drain		Protection-monitoring output
54	-	Reserved	I	Down	100 kΩ	Reserved for four DC motor operation
54	-	ENABLE_SB	I	Down	100 kΩ	Enable for DC motor B control
55	STROBE_ AB	STROBE_ AB	I	Down	100 kΩ	Serial interface data strobe for H-bridge A, B stepper motor drive (latch on rising edge)
55	STROBE_AB	ENABLE_LAB	I	Down	100 kΩ	Enable for large DC motor AB control
55	STROBE_AB	ENABLE_SA	I	Down	100 kΩ	Enable for DC motor A control
56	nORT	nORT	O	Open drain		Reset output (open drain)
57	LGND	LGND	-			Low power or analog ground
58	OSCM_mon	OSCM_mon	O	Open drain		OSCM clock monitoring

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	PULLUP/ PULLDOWN	SHUNT RESISTOR	DESCRIPTION
NO.	NAME IN SETUP MODE	NAME IN OPERATION				
59	DATA_CD	PHASE_SD	I	Down	100 kΩ	Serial input data for H-bridge C and D control
59	DATA_CD	DATA_CD	I	Down	100 kΩ	Serial input data for H-bridge C and D control
60	CLK_CD	PHASE_SC	I	Down	100 kΩ	Phase input for DC motor C control
60	CLK_CD	CLK_CD	I	Down	100 kΩ	Clock input synchronization for serial data CD
60	CLK_CD	PHASE_LCD	I	Down	100 kΩ	Phase input for large DC motor CD control
61	DATA_AB	DATA_AB	I	Down	100 kΩ	Serial input data for H-bridge A and B control
61	DATA_AB	PHASE_SB	I	Down	100 kΩ	Phase input for DC motor B control
62	CLK_AB	CLK_AB	I	Down	100 kΩ	Clock input synchronization for serial data AB
62	CLK_AB	PHASE_LAB	I	Down	100 kΩ	Phase input for large DC motor AB control
62	CLK_AB	PHASE_SA	I	Down	100 kΩ	Phase input for DC motor A control
63	nSLEEP=L	nSLEEP	I	Down	100 kΩ	Enable/disable (part can be in sleep state)
64	In-Reset	In-Reset	I	Up	200 kΩ	Reset (L: Reset, H/open: Normal operation)

Table 1. Alternate Functions of Select Pins By Operation Mode

CONFIG	PIN							
	50	51	54	55	59	60	61	62
Default Name	ENABLE_SD	ENABLE_SC	ENABLE_SB	STROBE_AB	PHASE_ SD	PHASE_SC	DATA_AB	CLK_AB
Dual Stepper	-	STROBE_CD	-	STROBE_AB	DATA_CD	CLK_CD	DATA_AB	CLK_AB
Stepper + Large DC	-	ENABLE_LCD	-	STROBE_AB	-	PHASE_LCD	DATA_AB	CLK_AB
Stepper + Dual Small DC	ENABLE_SD	ENABLE_SC	-	STROBE_AB	PHASE_SD	PHASE_SC	DATA_AB	CLK_AB
Large DC + Dual Small DC	ENABLE_SD	ENABLE_SC	-	ENABLE_LAB	PHASE _SD	PHASE_SC	-	PHASE_LAB
Dual Large DC	-	ENABLE_LCD	-	ENABLE_LAB	-	PHASE_LCD	-	PHASE_LAB
Quad Small DC	ENABLE_SD	ENABLE_SC	ENABLE_SB	ENABLE_SA	PHASE_SD	PHASE_SC	PHASE_SB	PHASE_SA
Large Stepper	-	STROBE_CD	-	STROBE_AB	DATA_CD	CLK_CD	DATA_AB	CLK_AB
Ultra-Large DC	-	-	-	ENABLE_UL	-	-	-	PHASE_UL

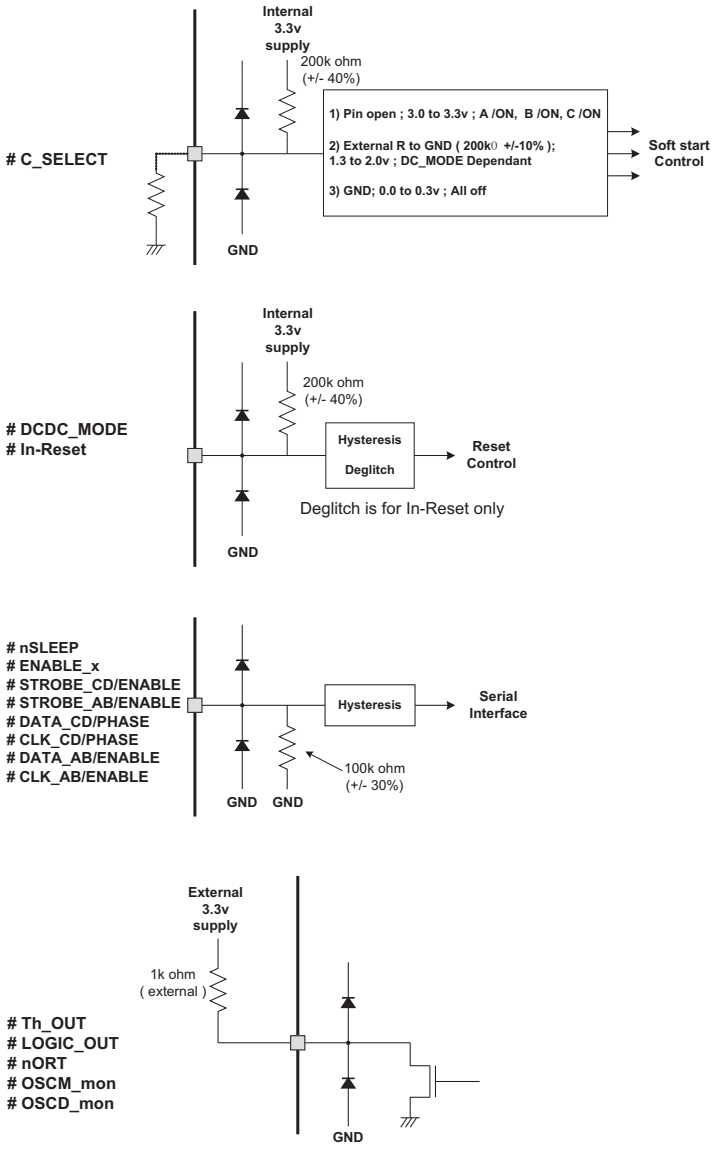


Figure 1. Input Pin Configurations

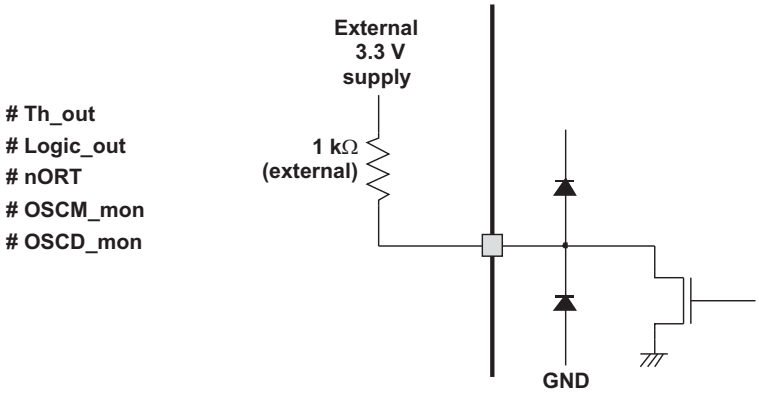


Figure 2. Open-Drain Output Pin Configurations

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

V_M	Supply voltage(1)	50 V
	Logic input voltage range, serial I/F inputs, and reset (2)	–0.3 V to 5.5 V
	Continuous total power dissipation (θ_{JA} = 20°C/W)	4 W
	Continuous motor-drive output current for each H-bridge (100 ms)	3 A
	Peak motor-drive output current for each H-bridge (500 ns)	8 A
	Continuous DC-DC converter output current	1.5 A
	Continuous DC-DC converter output current ODB, C in parallel mode	3.0 A
T_J	Operating junction temperature range (1 h)	0°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s	260°C
	ESD levels on every pin, Human-Body Model (HBM)	2 kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The negative spike less than –5 V and narrower than 50-ns duration should not cause any problem.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_M for motor control	18	27	40	V
Supply voltage for DC-DC converter (VDIN)	7	27	40	V
Average output current for motor driver for each H-bridge			800	mA
DC output current for DC-DC converter			1.2	A
DC output current for DC-DC in Ch-B/C parallel mode			2.4	A
Operating ambient temperature(1)	–40		50	°C
Operating junction temperature	0		120	°C

(1) If the total power is less than 4 W, then the operating ambient temperature range is -40°C to 60°C.

ELECTRICAL CHARACTERISTICS

T_J = 0°C to 120°C, V_M = 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply (Sleep) Current						
I_{SLEEP1}	Supply (sleep) current 1	nSLEEP = L, DC-DC all off		4	5	mA
I_{SLEEP2}	Supply (sleep) current 2	nSLEEP = L, V_M = 8 V, Full duty cycle		7	10	mA
I_{SLEEP3}	Supply (sleep) current 3	nSLEEP = L, V_M = 40 V, Full duty cycle		8	10	mA

ELECTRICAL CHARACTERISTICS

T_J = 0°C to 120°C, V_M = 7 V to 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Interface Circuit						
V_{IH}	Digital high-level input voltage	Digital inputs(1)	2		5	V
I_{IH}	Digital high-level input current	Digital inputs			100	µA
V_{IL}	Digital low-level input voltage	Digital inputs			0.8	V
I_{IL}	Digital low-level input current	Digital inputs			100	µA
V_{hys}	Digital input hysteresis	Digital inputs	0.3	0.45	0.6	V
T_{degl}	Digital input deglitch time	In-Reset	2.5		7.5	µs

(1) Absolute maximum rating for charge-pump circuit is 60 V.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 120°C, V_M = 7 V to 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Charge-Pump VCP (C_P = 0.1 µF to 0.47 µF, C_{bk} = 0.01 µF ± 10%)							
V_O(CP)	Output voltage	I_{LOAD} = 0 mA,	$V_M > VthV_{M2}$	V_M + 10		V_M + 13	V
$f_{(CP)}$	Switching frequency				1.6		MHz
t_{start}	Start-up time	CStorage = 0.1 µF,	$V_M \geq 16$ V		0.5	2	ms
Internal Clock OSCi							
f_{OSCi}	System clock frequency			5.76	6.4	7.04	MHz
VREF Input							
V_{REF}	Reference voltage input			0.8	2.5	3.6	V
$I_{leak-vr}$	Input leak current					1	µA
C_SELECT for DC-DC Start-Up Selection (DCDC_MODE = L)							
Vcs0	DC-DC all off			0		0.3	V
Vcs1	DC-DC all off	Pull down by external 200-kΩ resistor		1.3		2	V
Vcs2	Turn on ODA then ODB and ODC	As pin open		3		3.3	V
C_SELECT for DC-DC Start-Up Selection (DCDC_MODE = H or Open, Ch-B/C Parallel Mode)							
Vcs0	DC-DC all off			0		0.3	V
Vcs1	Turn on ODB/C then ODA	Pull down by external 200-kΩ resistor		1.3		2	V
Vcs2	Turn on ODA then ODB/C	As pin open		3		3.6	V
Three DC-DC Converters(2)							
V_{DINOPE}	Operating supply voltage	Ratio to V_{OUT}(DC)			1.25 = V_O		V
ODA ODB ODC	VoutA = 1.5 V – 30 V, VoutB/C = 1.5 V – 10 V, Programmable with external reference on FBX × VDIN > 1.25 × Vout (largest)	20 V ≤ VDIN < 40 V		–3	V_O	3	%
		6.5 V ≤ VDIN < 20 V		–3	V_O	5	
		Vth_{VM-} < VDIN < 6.5 V,	$V_O \leq 3.3$ V	–3	V_O	5	
V_{FB}	FBX feedback voltage	For ODA/B/C			1.50		V
$I_{O\ ODx}$	ODx output current (dc)	With external L and C				1.5	A
$I_{O\ ODBC}$	OD_{BC} output current (DC) in Ch-B/Ch-C parallel mode	With external L and C DCDC_MODE = H				3	A
$I_{O\ ODx2}$	Output current (dc) at low VDIN	VDIN = 7 V,	V_O = 5 V			0.8	A
$I_{O\ ODx3}$	Output current (dc) at low VDIN	VDIN = 7 V,	V_O = 3.3 V			1.5	A
f_{OSCD}	Switching (chopping frequency)	f_{OSCD} = (0,0)		90	100	110	kHz
$R_{ds(ON)}$	FET ON resistance at 0.8 A for OD_x	T_J = 25°C			0.35		Ω
		T_J = 120°C				0.50	
5 V-Low	5.5-V V_O at VDIN = VthV_	VDIN = VthV_, VthV_ = 5-V load (dc) = 0.5 A(3)		4			V
	V_O voltage to 5.5 V			–30			%
	V_O voltage drop from VDIN					1	V
Vo_min6	V_O setting without kick UVP when VDIN = $VthV_{M+}$ (V_O setting at VDIN = 10 V)	$VthV_{M+}$ = 6-V load (DC) = 0.5 A(4)		6			V

(2) DCDC_MODE = H, Ch-B and Ch-C are in parallel driving mode.
(3) Lower VDIN decrease gate drive and the voltage drop is increased. Specified by bench characterization only.
(4) V_{OUT} (at VDIN = $VthV_{M+}$) is lower than V_O setting. When VDIN is down to $VthV_{M+}$, undervoltage protection (UVP) shuts down the device, in case the V_O is set as V_O > 7 V. Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 120°C, V_M = 7 V to 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Three DC-DC Converter Protection						
$I_{O\ DD\ ODx}$	Overcurrent detect for OD_x source	Peak current in each ON cycle	1.8		3	A
$tFILT_{OCP}$	OCP filtering time	By OSCi cycles		2		cycles
t_{ODSD}	DC-DC shutdown filter	Number of subsequent chopping cycles with OCP detection		4		chop cycles
Vovpx	Overvoltage protection (OVP)	Percentage of nominal Voutx detected at VFB	25	30	35	%
Vuvpx	Undervoltage protection (UVP)	Percentage of nominal Voutx detected at VFB (VFB decreasing)	-25	-30	-35	%
tVfilter	OVP/UVP filtering time		3	8	13	us
t_{sst}	Start-up time with soft start				56	ms
V_{stover}	Start-up overshoot	Ratio to V_O			3	%
V_M Supervisory						
$VthV_{M–}$	nORT for V_M low threshold	V_M decreasing	4.5	5	6	V
$VthV_{M+}$	nORT for V_M high threshold	V_M increasing	5.5	6	7	V
$VthV_{Mh}$	nORT for V_M detect hysteresis	($VthV_{M+}$) - (VthV_)	0.5	1		V
$VthV_{M2}$	For motor driver off (5)				15	V
t_{VM} filt	V_M monitor filtering time	For V_M threshold detect	10		30	µs
Thermal Shutdown (TSD)						
T_{TSD}	Thermal shutdown set points		150	170	190	°C
Temperature Sense, Pre TSD (See Extended Setup Register Definition)						
T_{TSD0}	Temperature sense point 0	Register selectable, Assert logic H at TH_OUT	130	150	170	°C
T_{TSD1}	Temperature sense point 1	Register selectable, Assert logic H at TH_OUT	120	140	160	°C
Tc_sens	TH_OUT (analog out) temperature coefficient	Specified by design		6		mV/°C
RESET/nORT: Open-Drain Outputs (nORT, LOGIC_OUT, TH_OUT)						
V_{OH}	High-state voltage	R_L = 1 kΩ to 3.3 V	3			V
V_{OL}	Low-state voltage	R_L = 1 kΩ to 3.3 V			0.3	V
I_{OL}	Low-state sink current	V_O = 0.4 V	3			mA
t_r	Rise time	10% to 90%			1	µs
t_f	Fall time	90% to 10%			50	ns
RESET/nORT Delay: Start-Up Sequence						
t_{ord1}	nORT delay 1	Reset deassertion from $VthV_{M+}$ < VDIN for DC-DC wake up falling		300	390	ms
t_{ord3}	DC-DC turnon delay	From one DC-DC wake up to following DC-DC to go soft-start sequence		1.7		ms
t_{ord4}	nORT delay 4	Reset deassertion from 2nd DC-DC wake up		120	180	ms
In-Reset						
t_{reset}	In-Reset assertion to nORT assertion delay	In-Reset falling to nORT failing		5	10	µs

(5) No nORT assertion to $VthV_{M2}$ detection

ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 120°C, V_M = 7 V to 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
H-Bridge Drivers (OUTx+ and OUTx–)						
I_{OUT1}(max)	Peak output current 1	Less than 500-ns period			8	A
I_{OUT2}(max)	Peak output current 2	Less than 100-ms period			3	A
I_{OUT}(max)	Average continuous output current				0.8	A
$R_{ds(ON)}$	FET ON resistance at 0.8 A	T_J = 25°C		0.55		Ω
		T_J = 120°C			1	
I_{CEX}	Output leakage current	V_{OUTX} = 0 V or 10 V			10	µA
I_{RS}	Sense resistor supply current	nORT = Low			15	µA
$I_{OC\ Motor}$	Motor overcurrent threshold for each H-bridge(6)		3		5	A
$t_{filterM}$	Motor overcurrent filter time		2.5	5	8.5	µs
f_{OSCM}	Motor oscillator frequency	F_OSCM = (0,0)	720	800	880	kHz
f_{chop}	Motor chopping frequency = f_{OSCM}/8	F_OSCM = (0,0)	90	100	110	kHz
Stepper Motor Drive (Parameters Are Tested Without Motor Loading)						
$I_{STEPMOTORAVG}$	Average stepper motor current for H-bridge	V_M = 40 V		800		mA
$I_{STEPMOTORPeak}$	Peak stepper motor current for H-bridge	V_M = 40 V		1.3		A
	Stepper motor current limit threshold (internal reference)(7)	VL_{16} , Phase angle = 90°		100		%
		VL_{15} , Phase angle = 84°		100		
		VL_{14} , Phase angle = 79°		98		
		VL_{13} , Phase angle = 73°		96		
		VL_{12} , Phase angle = 68°		92		
		VL_{11} , Phase angle = 62°		88		
		VL_{10} , Phase angle = 56°		83		
		VL_9 , Phase angle = 51°		77		
		VL_8 , Phase angle = 45°		71		
		VL_7 , Phase angle = 40°		63		
		VL_6 , Phase angle = 34°		56		
		VL_5 , Phase angle = 28°		47		
		VL_4 , Phase angle = 23°		38		
		VL_3 , Phase angle = 17°		29		
		VL_2 , Phase angle = 11°		20		
		VL_1 , Phase angle = 6°		10		
		VL_0 , Phase angle = 0°		0		
I_{OUT}	Output current accuracy at 100% setting(7)	Excludes VREF and RSENS errors, I_{OUT} > 1 A(7) (8)	–5		5	%
$Isw_{Leakage}$	Switch (driver MOSFET) leakage current	Outputs off	–10		10	µA
t_{ab}	Stepper motor blanking time	By OSCi cycles	8		9	cycles

(6) When the overcurrent is detected, all H-bridges are shut down and assert nORT pulse (40 ms).
(7) This is not measured directly, checked by Itrip amplifier gain without motor loading
(8) This device may show current setting error when motor current is less than 1 A, due to noise filter delay at the Itrip comparator.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 120°C, V_M = 7 V to 40 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stepper and DC Motor Drivers						
t_r	Rise time	V_M = 27 V	100		300	ns
t_f	Fall time	20% to 80%	100		300	ns
t_{PDOFF}	Enable or strobe detection to sink or source gate off delay		50	150	400	ns
t_{COD}	Crossover delay time, to prevent shoot through		100	600	1000	ns
t_{PDON}	Enable or strobe detection to sink or source gate on delay			750		ns
DC Motor Drivers						
t_{blank}	Blanking time	TBLNK = (0,0) for Min, (1,1) for Max, f_{CHOP} = 100 kHz	1.6		5.65	µs
t_{wPminp}	Minimum pulse duration (phase)				1	µs
t_{wPmine}	Minimum pulse duration (enable)				1	µs
Serial Interface						
$f_{(CLK)}$	Clock frequency		1		25	MHz
$t_{wh(CLK)}$	Minimum high-level pulse width		10			ns
$t_{wl(CLK)}$	Minimum low-level pulse width		10			ns
t_{su}	Setup time, data to CLK↓		10			ns
t_h	Hold time, CLK↓ to data		10			ns
t_{cs}	CLK↓ to STROBE↑		10			ns
t_{sc}	STROBE↓ to CLK↑		10			ns
$t_{w(STRB)}$	Minimum strobe pulse duration		20			ns
t_{ss_min}	Strobe mask time from nSLEEP		1.5		4	µs
Serial Interface: ID Monitor Function at LOGIC_OUT, Extended Setup Mode						
t_{ODL}	0 data output delay bit 3 to bit 0 (ext-setup) = (1100)	From strobe rise to LOGIC_OUT, 1 kΩ to external 3.3 V			4000	ns
t_{ODH}	1 data output delay bit 3 to bit 0 (ext-setup) = (1111)	From strobe rise to LOGIC_OUT, 1 kΩ to external 3.3 V			4000	ns

Serial Interface

The device has two serial interface circuit blocks for stepper motor driving control. These two serial interfaces provide controls to each motor driver independently.

CLKAB	Serial clock for H-bridge A, B
DATAAB	Serial data for H-bridge A, B
STROBEAB	Strobe input for H-bridge A, B

CLKCD	Serial clock for H-bridge C, D
DATACD	Serial data for H-bridge C, D
STROBECD	Strobe signal for H-bridge C, D

Sixteen bits serial data is shifted into the least significant bit (LSB) of the serial data input (DATA) shift register on the falling edge of the serial clock (CLK). After 16 bits of data transfer, the strobe signal (Strobe) rising edge latches all the shifted data. During data transfer, Strobe voltage level is acceptable high or low.

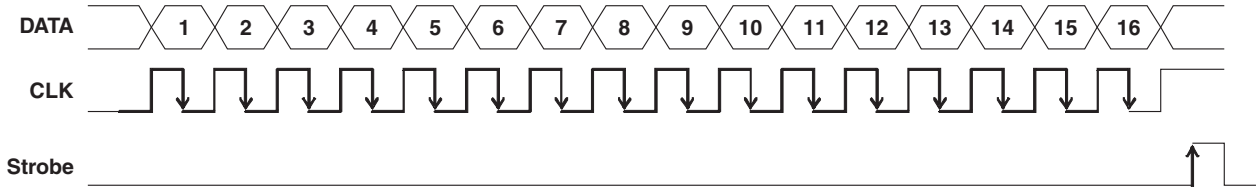


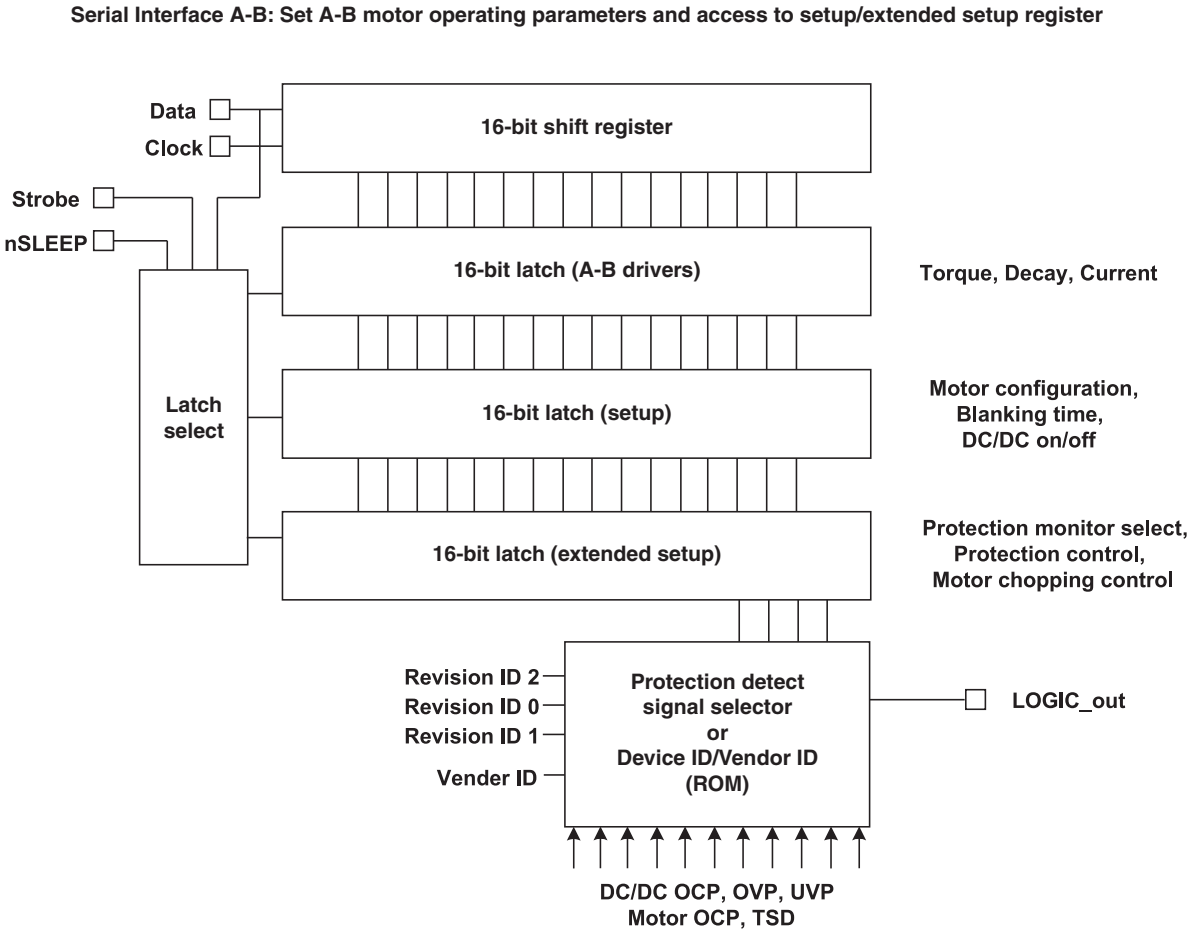
Figure 3. Serial Interface

Setup Mode/Power-Down Mode

The motor output mode is configured through serial interface (DATA AB, CLK AB and STROBEAB) when nSLEEP = L. After setup, the nSLEEP pin must be pulled high for normal motor drive control. The condition that the device requires for setup (initialization) is after the nORT (Reset) output goes to high from the low level (power on, recovery from V_M < 7 V). While nSLEEP is low, all the motor drive functions are shut down and their outputs are high-impedance state. Also the stepper parameters in the register are all reset to 0. This device forces motor driver functions to shut down for the power-down mode, and it is not damaged even if nSLEEP is asserted during motor driving. At the Strobe pulse rising edge, the DATA signal level must be low for normal setup mode (see *Extended Setup Mode* for another option).

Extended Setup Mode

While nSLEEP = L, if the DATA signal level is set high when the Strobe pulse is set, the serial interface recognizes the input data to set the extended setup mode. This extended setup register enables monitoring and controlling the fault condition of this chip. One of the internal protection control signals is selected and provided to LOGIC OUT pin. Also, this enables the application to ignore the protection control and/or suppress the reset signal generation. This device has device ID (3-bit ROM) and vendor ID (1-bit ROM), which can be read out from LOGIC OUT. Four bits are assigned to select the LOGIC OUT signal, including the ID ROM bit readout.



A. A-B register at EXT-setup mode has device/vendor ID ROM. The ID must be read out at LOGIC OUT pin.

Figure 4. Serial Interface A-B

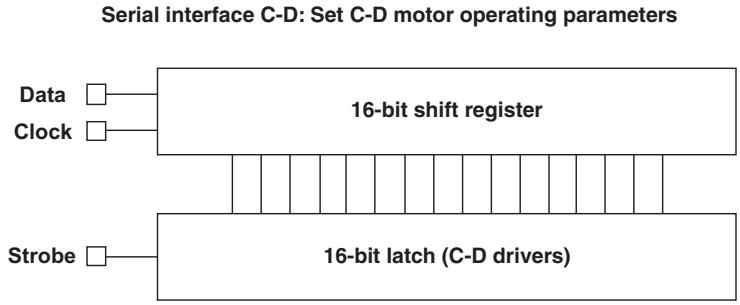


Figure 5. Serial Interface C-D

Serial Interface Timing

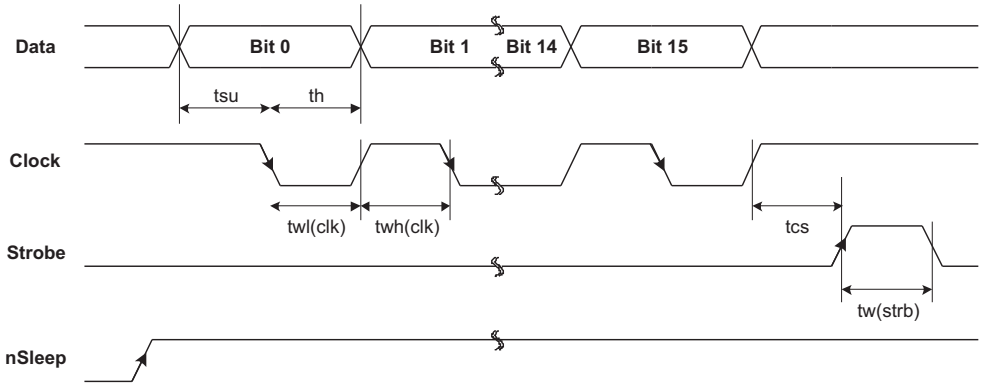


Figure 6. nSLEEP = H: Set Stepper Motor Operating Parameters

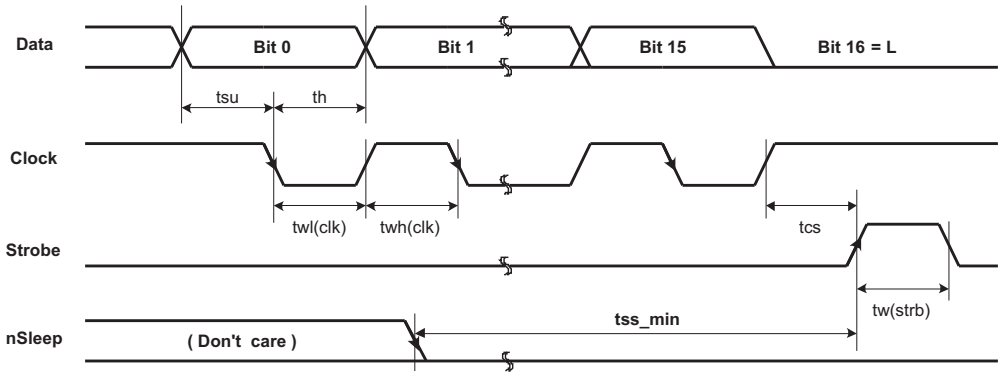
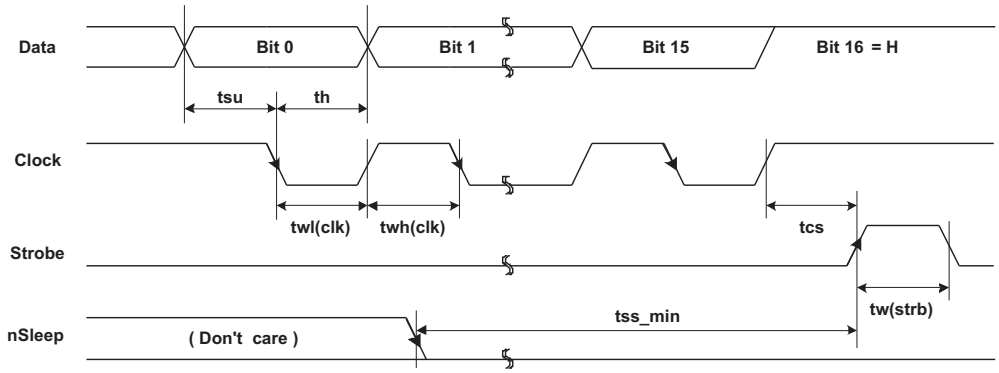


Figure 7. nSLEEP = L (Bit 16 = L): Setup Mode



A. For initial setup, nSLEEP state can be don't care before the tss_min timing prior to the strobe.

Figure 8. nSLEEP = L (Bit 16 = H): Extended Setup Mode

Setup Register Bit Assignment

Setup register bits are assigned for motor configuration, blanking time, gain, and DC-DC switches. This register can be accessed only in Setup mode (nSLEEP = L and bit 16 data = L) .

Table 2. Setup Register

BIT NO.	NAME	DEFAULT	DESCRIPTION
0	Motor select 0	0	Motor configuration, < 2,1,0 > (0,0,0): Stepper × 2 (default) (0,0,1): Stepper + LDC, (0,1,0): Stepper + 2 × sDCs (0,1,1): DCL + 2 × sDC, (1,0,0): DCL × 2 (1,0,1): 4 × sDC (1,1,0): Large stepper (1,1,1): Ultra-large DC
1	Motor select 1	0	
2	Motor select 2	0	
3	TBLNK AB0	0	Tblank for DC motor driving, Tblank is inserted at any phase change and beginning of each chopping cycle. AB1 AB0: Blanking time for A/B side drivers, CD1 CD0: Blanking time for C/D side drivers, 00: $(1 \div f_{CHOP}) \div 8 \times 5$ (= 6.25 µs) (default) 01: $(1 \div f_{CHOP}) \div 8 \times 6$ (= 7.50 µs) 10: $(1 \div f_{CHOP}) \div 8 \times 3$ (= 3.75 µs) 11: $(1 \div f_{CHOP}) \div 8 \times 4$ (= 5.00 µs) For stepper motor driving, only the fixed blanking time is applied.
4	TBLNK AB1	0	
5	TBLNK CD0	0	
6	TBLNK CD1	0	
7	DC/DC_A SW	0	DC-DC ODA control, 0: ON (default), 1: OFF
8	DC/DC_B SW	0	DC-DC ODB control, 0: ON (default), 1: OFF
9	DC/DC_C SW	0	DC-DC ODC control, 0: ON (default), 1: OFF This bit is ignored when DCDC_MODE = H or open
10	Motor_AB gain	0	0: 1/10 (default), 1: 0
11	Motor_CD gain	0	0: 1/10 (default), 1: 0
12	OSCD frequency 0	0	<1,0> = (0,0) 100 kHz (default) (0,1) 50 kHz (1,0) 200 kHz (1,1) 132.5 kHz These setup bits can be changed when the DC-DC regulators are in operation.
13	OSCD frequency 1	0	
14	OSCM frequency 0	0	<1,0> = (0,0) 800 kHz (default) (0,1) 400 kHz (1,0) 1.06 MHz (1,1) 1.6 MHz
15	OSCM frequency 1	0	

The device can be configured to one out of eight different motor control combination modes. When the device is powered on or is recovering from reset, the mode can be selected by writing to the setup register through the serial interface AB, during Setup mode (nSLEEP = L).

Table 3. DC and Stepper Motor Configuration

SETUP REGISTER			H-BRIDGE AND MOTOR CONFIGURATION			
BIT 2	BIT 1	BIT 0	OUTA+, OUTA–	OUTB+, OUTB–	OUTC+, OUTC–	OUTD+, OUTD–
0	0	0	Stepper motor drive		Stepper motor drive	
0	0	1	Stepper motor drive		Large DC motor drive	
0	1	0	Stepper motor drive		DC motor drive	DC motor drive
0	1	1	Large DC motor drive		DC motor drive	DC motor drive
1	0	0	Large DC motor drive		Large DC motor drive	
1	0	1	DC motor drive	DC motor drive	DC motor drive	DC motor drive
1	1	0	Large stepper motor drive: A + B for first winding, C + D for second winding			
1	1	1	Ultra-large DC motor drive			
Default setting is (M0, M1, M2) = (0, 0, 0)						

Extended setup (EX-setup) register bits are assigned for protection control, pre TSD, and multiplexer test mode selection. This register can be accessed only in Setup mode (nSLEEP = L and bit 16 data = H).

Table 4. Extended Setup Register (EX-setup) Bit Assignment

BIT NO.	NAME	DEFAULT	DESCRIPTION
0	Signal select 0	0	Signal selector monitored on LOGIC_OUT DC-DC OCP detection, DC-DC voltage supervisor (OVP or UVP), Motor overcurrent (four H-bridges), TSD, etc. [shutdown (protection) signals must be latched]
1	Signal select 1	0	
2	Signal select 2	0	
3	Signal select 3	0	
4	Ignore SD 0	0	0 = Normal operation, 1 = Ignore DC-DC OCP
5	Ignore SD 1	0	0 = Normal operation, 1 = Ignore DC-DC voltage supervisor
6	Ignore SD 2	0	0 = Normal operation, 1 = Ignore motor OCP
7	Ignore SD 3	0	0 = Normal operation, 1 = Ignore thermal shutdown
8	Disable nORT 0 (selective shutdown for DC-DC Ch-C)	0	0 = Normal operation 1 = Disable nORT assertion but shut down DC-DC Ch-C, in case of DC-DC Ch-C fault condition Ch-C shutdown is released by nSLEEP rise edge. If fault condition is on the other channels (with bit = 0), assert nORT and shut down all three DC-DC channels. This bit is ignored when DCDC_MODE = H or open
9	Disable nORT 1 (Selective shutdown for DC-DC Ch-B)	0	0 = Normal operation 1 = Disable nORT assertion but shut down DC-DC channel B, in case of DC-DC Ch-B fault condition Ch-B shutdown is released by nSLEEP rise edge. If fault condition on the other channels (with bit = 0), assert nORT and shut down all three DC-DC channels.
10	Disable nORT 2 (Selective shutdown for DC-DC Ch-A)	0	0 = Normal operation, 1 = Disable nORT assertion but shutdown the DC-DC Ch-A, in case of DC-DC Ch-A fault condition. Ch-A shutdown is released by nSLEEP rise edge. If fault condition on the other channels (with bit is 0), assert nORT and shut down all three DC-DC channels .
11	Pre TSD 0	0	0 = Ttsd0 = Ttsd - 20°C, 1 = Ttsd1= Ttsd - 30°C
12	Pre TSD 1	0	0 = Pre-TSD (logic) output, 1 = TH_OUT Analog output
13	Test mux 0	0	Test mode selection, < 2,1,0 > = (0,0,0) Normal operation (0,0,1) TSD control – 1, (0,1,0) TSD control – 2, (0,1,1) OSC monitor enable,
14	Test mux 1	0	
15	Test mux 2	0	

Table 5. LOGIC OUT Selection

NO.	EX-setup REGISTER (BITS 3–0)	SIGNAL SELECTION MONITORED ON LOGIC OUT (LISTED SIGNALS TO BE MUXED BY OR)			SIGNAL POINT
0	0000 (default)	DC-DC OCP_A	DC-DC OVP_A	DC-DC UVP_A	Latched out
1	0001	DC-DC OCP_B	DC-DC OVP_B	DC-DC UVP_B	Latched out
2	0010	DC-DC OCP_C	DC-DC OVP_C	DC-DC UVP_C	Latched out
		This bit is ignored when DCDC_MODE pin = H or open.			
3	0011	DC-DC OCP_A	DC-DC OCP_B	DC-DC OCP_C	Latched out
4	0100	DC-DC OVP_A	DC-DC OVP_B	DC-DC OVP_C	Latched out
5	0101	DC-DC UVP_A	DC-DC UVP_B	DC-DC UVP_C	Latched out
6	0110	Motor OCP			Latched out
7	0111	TSD			Latched out
8	1000	Revision <0> = 1: For this device <2,1,0> = (1,0,1) = 5			ROM
9	1001	Revision <1> = 0: For this device			ROM
10	1010	Revision <2> = 1: For this device			ROM
11	1011	Vendor <0> = 0: For TI <1,0> = TI (0,0), NG (1,0)			ROM
12	1100	Vendor <1> = 0: For TI <1,0> = Reserve (0,1), (1,1)			ROM
13	1101	Internal oscillator clock (as divided by 32 = 200 kHz)			
14	1110	Fixed value as 1 (open-drain output buffer off)			
15	1111	Fixed value as 1 (open-drain output buffer off)			

Table 6. Test Mux Selection

NO.	BITS 15, 14, 13	DESCRIPTION	
0	0, 0, 0	Normal operation	
1	0, 0, 1	TSD control 1	At TSD event, shut down only motor driver part, DC-DC keep ON, keep setup register values, motor shutdown released by nSLEEP = L, no nORT assertion
2	0, 1, 0	TSD control 2	At TSD event, shut down only motor driver part, DC-DC keep ON, keep setup register values, motor shutdown released by nSLEEP = L, nORT assertion: 40-ms single pulse
3	0, 1, 1	OSC monitor enable	Provide clock to OSCD_mon and OSCM_mon pins

The serial interfaces communicate to the stepper parameter registers during nSLEEP = H . When nSLEEP = L, all register values are cleared.(1) (2)

Table 7. Register Settings for Stepper Motor Driving Parameter

BIT NO.	NAME	DEFAULT VALUE	DESCRIPTION
0	Torque 0	0	Torque control, b1 b0 00 equates to 50% 01 equates to 70 % 10 equates to 85% 11 equates to 100% Specified by design
1	Torque 1	0	
2	Decay B(D)0	0	Decay mode control(1) B(D)1, B(D)0: 00 equates to 12.5 % (do not use) 01 equates to 37.5 % (do not use) 10 equates to 75% 11 equates to fast decay Specified by design
3	Decay B(D)1	0	

(1) This device has issues with stepper motor current setting accuracy.
(2) Decay mode should be 75% or fast decay (do not use mode 00 and 01) in this device.
(1) Decay mode should be 75% or fast decay (do not use mode 00 and 01) in this device.

Table 7. Register Settings for Stepper Motor Driving Parameter (continued)

BIT NO.	NAME	DEFAULT VALUE	DESCRIPTION
4	Current B(D)0	0	Phase B(D) current level setting(1)
5	Current B(D)1	0	
6	Current B(D)2	0	
7	Current B(D)3	0	
8	Phase B(D)	0	Control direction of current flow through winding B(D). A logic 1 allows conventional current flow from OUTB(D)+ to OUTB(D)–.
9	Decay A(C)0	0	Decay mode control(1) A(C)1, A(C)0: 00 equates to 12.5 % (do not use) 01 equates to 37.5 % (do not use) 10 equates to 75% 11 equates to fast decay
10	Decay A(C)1	0	
11	Current A(C)0	0	Phase A current level setting(1)
12	Current A(C)1	0	
13	Current A(C)2	0	
14	Current A(C)3	0	
15	Phase A(C)	0	Control direction of current flow through winding A(C). A logic 1 allows conventional current flow from OUTA(C)+ to OUTA(C)–.

Table 8. Torque Control Bit

VREF INPUT CONTROL MOTOR TORQUE	
BIT VALUE	**ROUGH OUTPUT CURRENT SETTING**
Torque 0, 1 = 0, 0	50% high power consumption, I(max) = VREF * gain/RSense
Torque 0, 1 = 0, 1	70% power
Torque 0, 1 = 1, 0	85% power
Torque 0, 1 = 1, 1	100% power

Table 9. Decay Mode Control Bit

BIT VALUE	DECAY MODE SETTING
Decay x0, x1 = 0, 0	12.5% decay mode (do not use)
Decay x0, x1 = 0, 1	37.5% decay mode (do not use)
Decay x0, x1 = 1, 0	75% decay mode
Decay x0, x1 = 1, 1	100% fast decay mode

Table 10. Current Flow Direction Bit

BIT VALUE	CURRENT DIRECTION
Phase X = 0	OUTx+ = L, OUTx– = H
Phase X = 1	OUTx+ = H, OUTx– = L

Table 11. Revision Code/Vendor Code ROM Readout at LOGIC OUT

NO.	EX-setup REGISTER (BITS 3–0)	SIGNAL SELECTION MONITORED ON LOGIC OUT
8	1000	Revision <0> = 1: For this device * <2,1,0> = (1,0,1) = 5
9	1001	Revision <1> = 0: For this device
10	1010	Revision <2> = 1: For this device
11	1011	Vendor <0> = 0: For TI <1,0> = TI (0,0), NG(1,0)
12	1100	Vendor <1> = 0: For TI <1,0> = Reserve (0,1), (1,1)

Table 12. Different Motor Drive Configuration Pinouts (Selected By Setup Register Bits 0 to 3)

<setup>		0 (0,0,0)	1 (0,0,1)	2 (0,1,0)	3 (0,1,1)	4 (1,0,0)	5 (1,0,1)	6 (1,1,0)	7 (1,1,1)
	SETUP	STEPPER MTR ×2	STEPPER MTR AND DC (LARGE)	STEPPER MTR AND DC (SMALL) ×2	DC (LARGE) AND DC (SMALL) ×2	DC (LARGE) ×2	DC (SMALL) ×4	LARGE STEPPER	ULTRA-LARGE DC
1	Test-LGND								
2	MGND								
3	OUTA–	OUTA–	OUTA–	OUTA–	OUTLAB–	OUTLAB–	OUTSA–	OUTLAB–	OUTULABCD–
4	RSA1	RSA1	RSA1	RSA1	RSLAB1	RSLAB1	RSA1	RSLAB1	RSULABCD1
5	RSA2	RSA2	RSA2	RSA2	RSLAB2	RSLAB2	RSA2	RSLAB2	RSULABCD1
6	OUTA+	OUTA+	OUTA+	OUTA+	OUTLAB+	OUTLAB+	OUTSA+	OUTLAB+	OUTULABCD+
7	MGND								
8	MGND								
9	OUTB+	OUTB+	OUTB+	OUTB+	OUTLAB+	OUTLAB+	OUTSB+	OUTLAB+	OUTULABCD+
10	RSB2	RSB2	RSB2	RSB2	RSLAB2	RSLAB2	RSB2	RSLAB2	RSULABCD1
11	RSB1	RSB1	RSB1	RSB1	RSLAB1	RSLAB1	RSB1	RSLAB1	RSULABCD1
12	OUTB–	OUTB–	OUTB–	OUTB–	OUTLAB–	OUTLAB–	OUTSB–	OUTLAB–	OUTULABCD–
13	MGND								
14	LGND								
15	DCDC_MODE								
16	FBC								
17	OD_C								
18	OD_C								
19	OD_B								
20	OD_B								
21	FBB								
22	VCP								
23	OSCD_mon								
24	CP2								
25	CP1								
26	VDIN								
27	VDIN								
28	VDIN								
29	VM								
30	VREF_AB								
31	VREF_CD								
32	FBA								
33	ODA								
34	ODA								
35	LGND								
36	MGND								
37	OUTC–	OUTC–	OUTLCD–	OUTSC–	OUTSC–	OUTLCD–	OUTSC–	OUTLCD–	OUTULABCD–
38	RSC1	RSC1	RSLCD1	RSC1	RSC1	RSLCD1	RSC1	RSLCD1	RSULABCD1
39	RSC2	RSC2	RSLCD2	RSC2	RSC2	RSLCD2	RSC2	RSLCD2	RSULABCD1
40	OUTC+	OUTC+	OUTLCD+	OUTSC+	OUTSC+	OUTLCD+	OUTSC+	OUTLCD+	OUTLABCD+
41	MGND								
42	MGND								
43	OUTD+	OUTD+	OUTLCD+	OUTSD+	OUTSD+	OUTLCD+	OUTSD+	OUTSD+	OUTULABCD+
44	RSD2	RSD2	RSLCD2	RSD2	RSD2	RSLCD2	RSD2	RSD2	RSULABCD1
45	RSD1	RSD1	RSLCD1	RSD1	RSD1	RSLCD1	RSD1	RSD1	RSULABCD1
46	OUTD–	OUTD–	OUTLCD–	OUTSD–	OUTSD–	OUTLCD–	OUTSD–	OUTSD–	OUTULABCD–
47	MGND								
48	GND								
49	C_SELECT								

Table 12. Different Motor Drive Configuration Pinouts (Selected By Setup Register Bits 0 to 3) (continued)

<setup>		0 (0,0,0)	1 (0,0,1)	2 (0,1,0)	3 (0,1,1)	4 (1,0,0)	5 (1,0,1)	6 (1,1,0)	7 (1,1,1)
SETUP		STEPPER MTR ×2	STEPPER MTR AND DC (LARGE)	STEPPER MTR AND DC (SMALL) ×2	DC (LARGE) AND DC (SMALL) ×2	DC (LARGE) ×2	DC (SMALL) ×4	LARGE STEPPER	ULTRA-LARGE DC
50	-	-	-	ENABLE_SD	ENABLE_SD	-	ENABLE_SD	-	
51	STROBE_CD	STROBE_CD	ENABLE_LCD	ENABLE_SC	ENABLE_SC	ENABLE_ LCD	ENABLE_SC	ENABLE_ LCD	
52	TH_OUT								
53	LOGIC OUT								
54	-	-	-	-	-	-	ENABLE_SB	-	
55	STROBE AB	STROBE AB	STROBE AB	STROBE AB	ENABLE_LAB	ENABLE_ LAB	ENABLE_SA	ENABLE_ LAB	ENABLE_ ABCD
56	nORT								
57	LGND								
58	OSCM_mon								
59	DATA_CD	DATA_CD	-	PHASE SD	PHASE SD	-	PHASE SD	-	
60	CLK_CD	CLK_CD	PHASE_LCD	PHASE SC	PHASE SC	PHASE_LCD	PHASE SC	PHASE_LCD	
61	DATA_AB	DATA_AB	DATA_AB	DATA_AB	-	-	PHASE SB	-	
62	CLK_AB	CLK_AB	CLK_AB	CLK_AB	PHASE_LAB	PHASE_LAB	PHASE SA	PHASE_LAB	PHASE_ABCD
63	nSLEEP=L	nSLEEP=H							
64	In-Reset								

Motor Driver Configuration

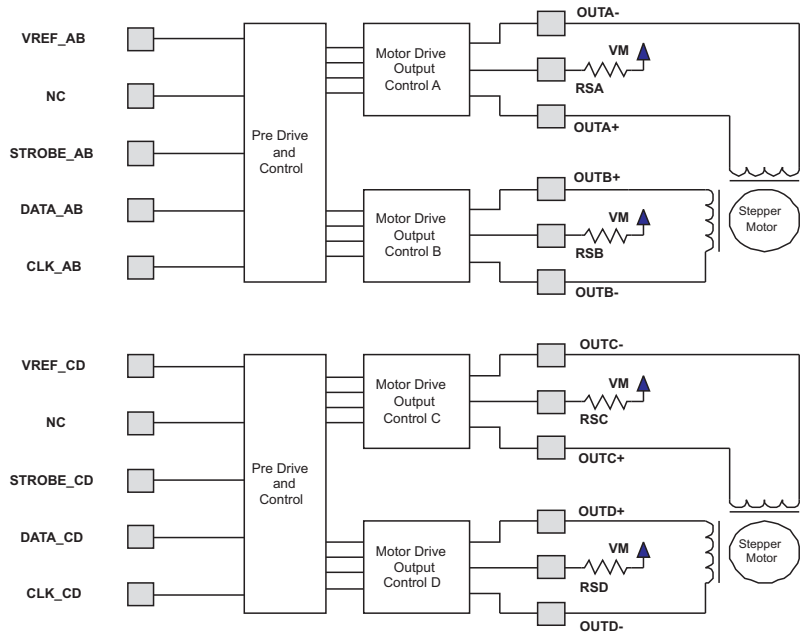


Figure 9. Motor Configuration 0, Two Stepper

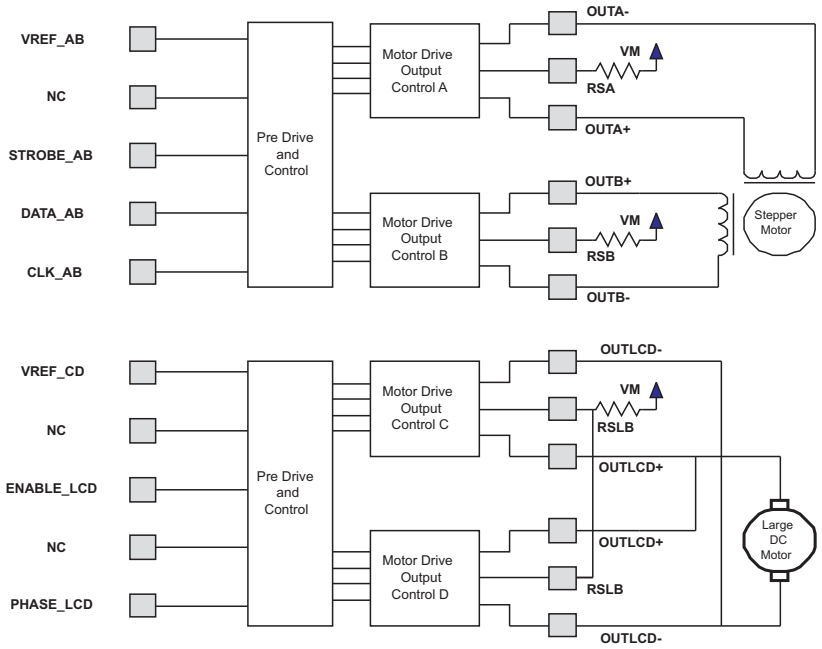


Figure 10. Motor Configuration 1, One Stepper and One Large DC

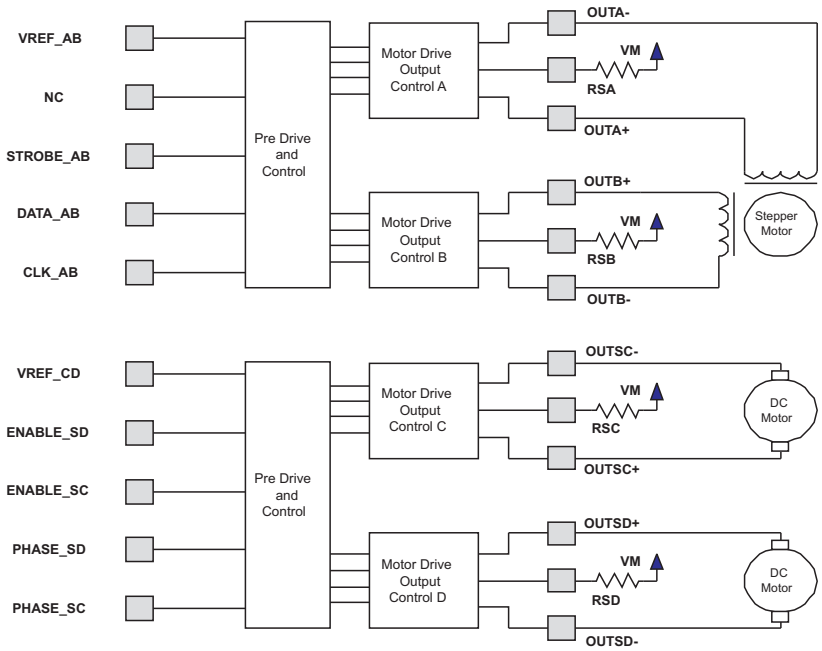


Figure 11. Motor Configuration 2, One Stepper and Two Small DCs

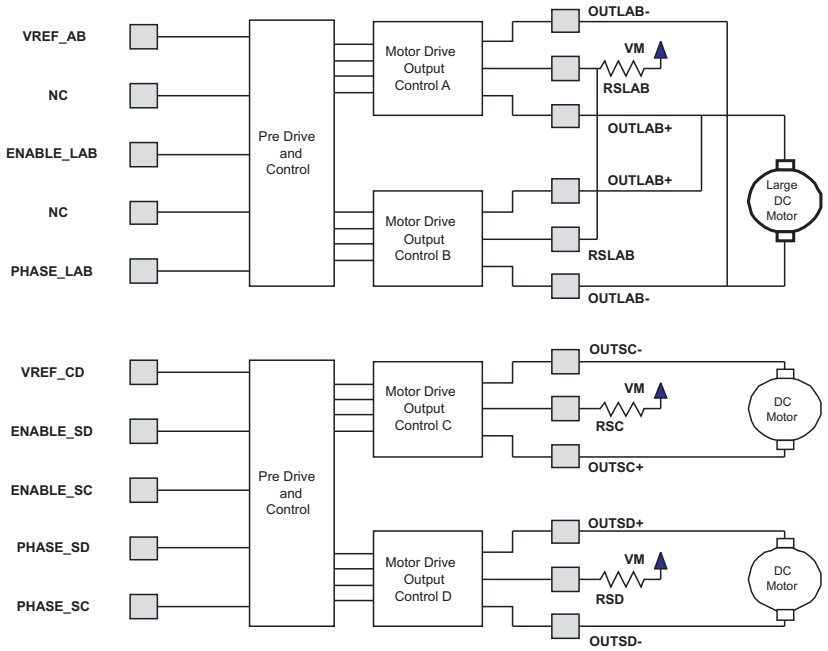


Figure 12. Motor Configuration 3, One Large DC and Two Small DCs

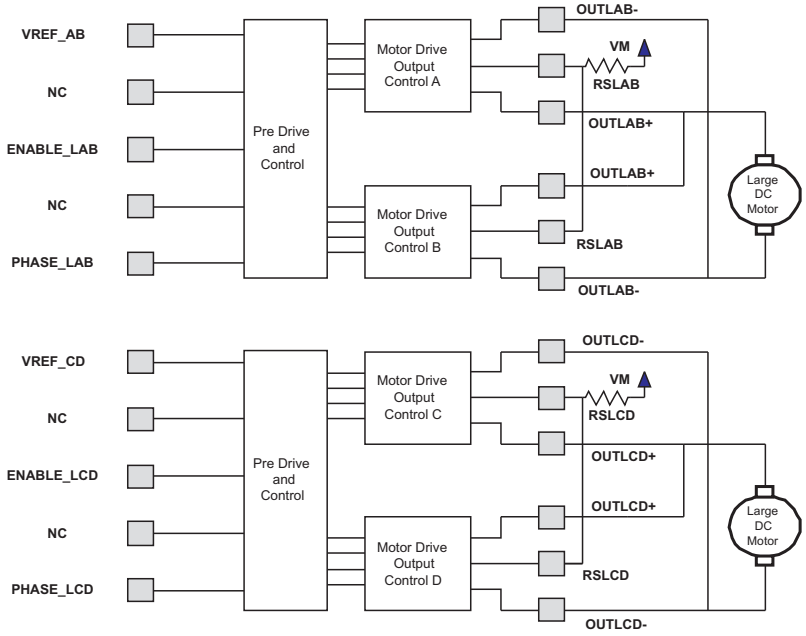


Figure 13. Motor Configuration 4, Two Large DCs

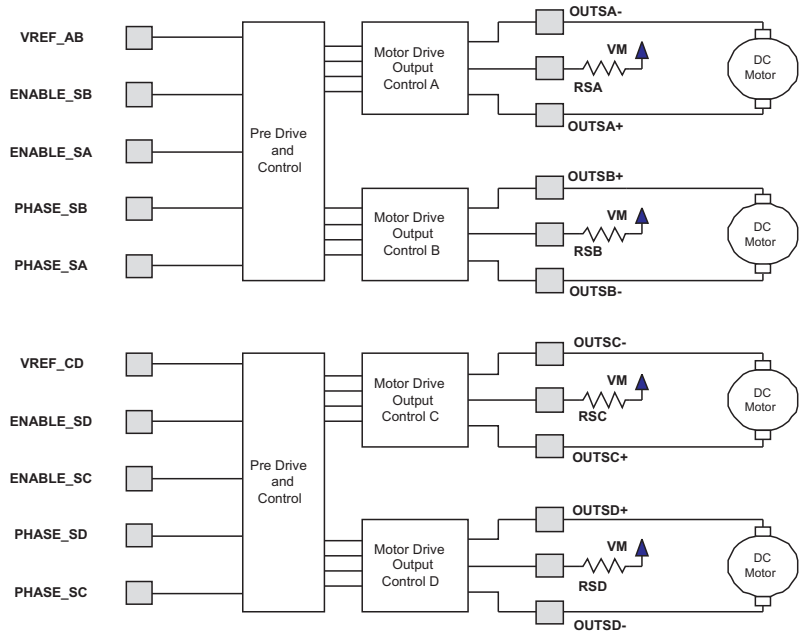


Figure 14. Motor Configuration 5, Four Small DCs

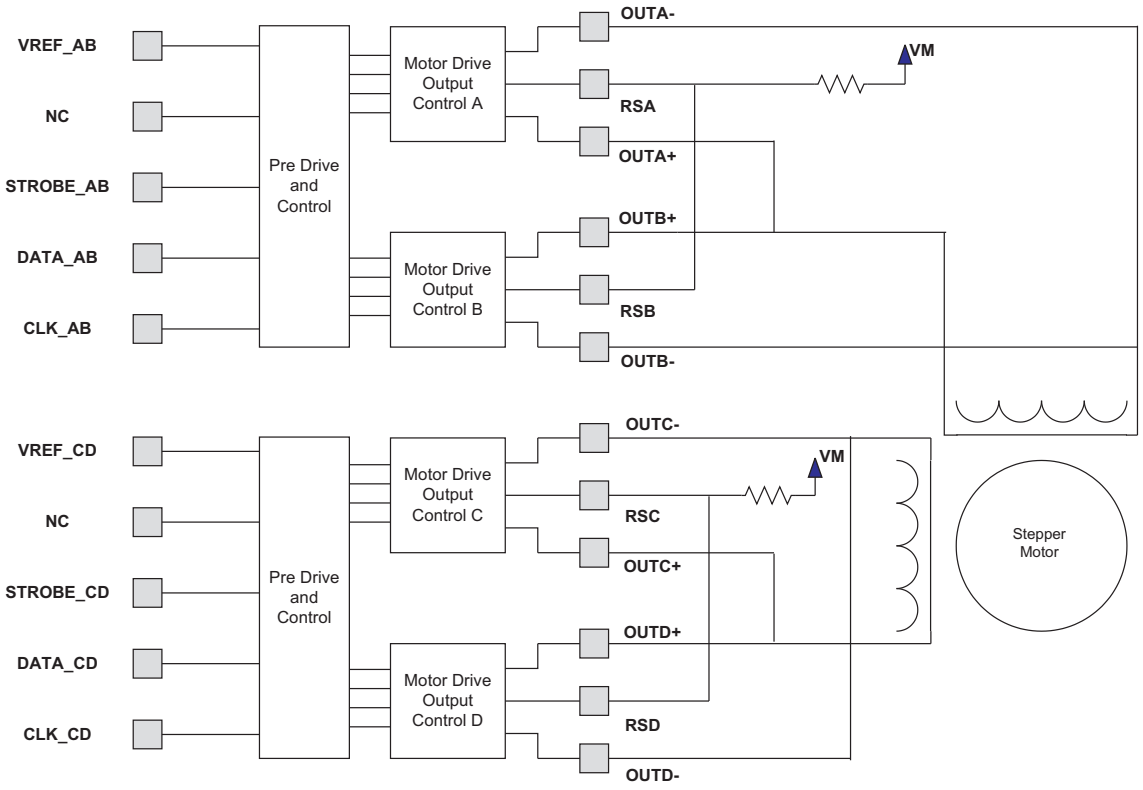


Figure 15. Motor Configuration 6, Single Large Stepper Motor

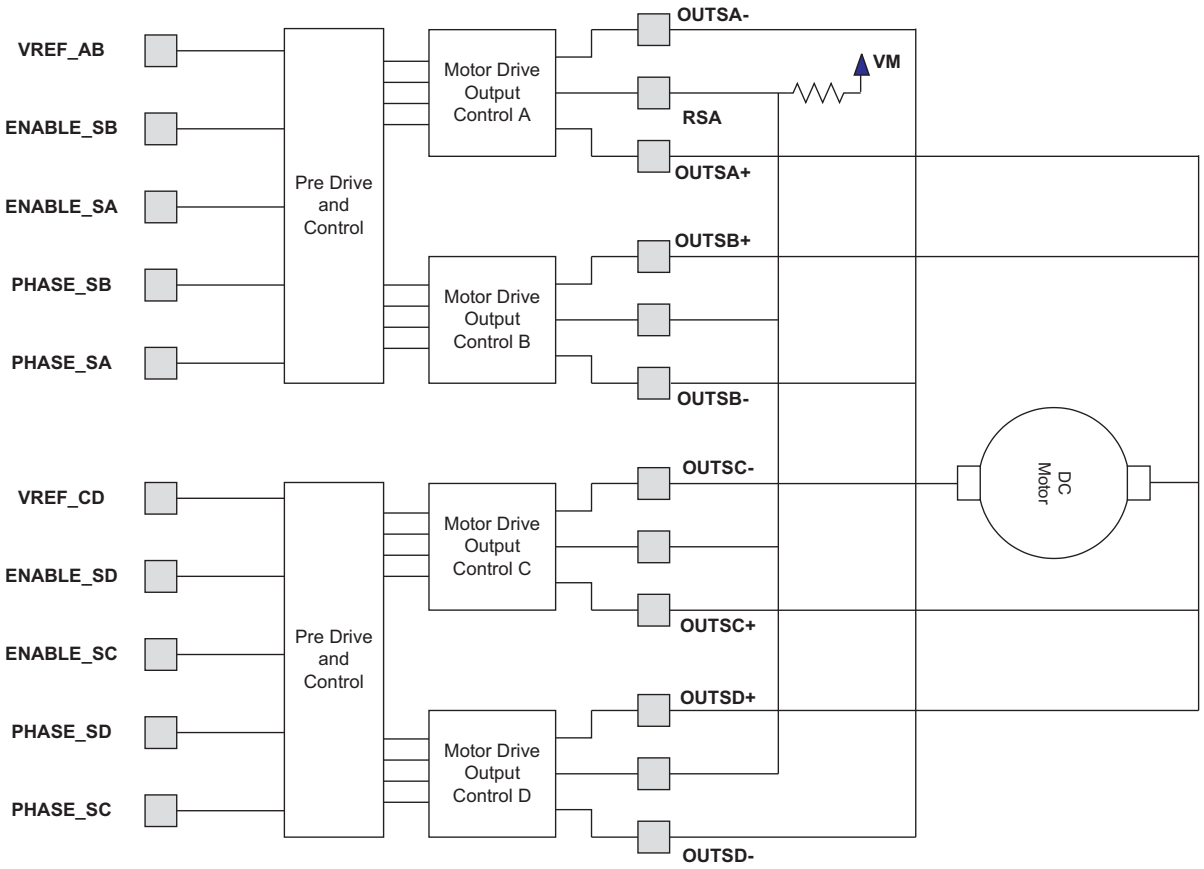


Figure 16. Motor Configuration 7, Ultra-Large DC

Bipolar Current Regulated Stepper Motor Drive

The following functionality is common to all the H-bridge drives. A crossover delay is inherent to the control circuitry to prevent cross conduction of the upper and lower switches on the same side of the H-bridge. A blanking (deglitch) time is incorporated to prevent false triggering due to initial current spikes at turnon with a discharged capacitive load.

The stepper motor current can be programmed to 16 different current levels using a 4-bit register. The average current level for a particular angular rotation is shown in Table 14.

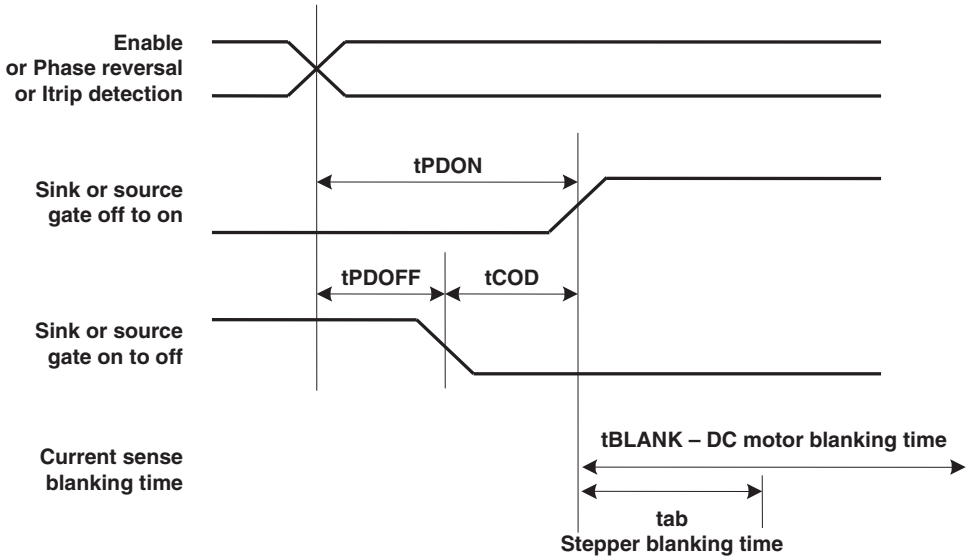


Figure 17. Crossover and Blanking Timing for H-Bridge

For stepper motor configured H-bridges, only tab (stepper blanking time) is set for current sensing. For DC motor-configured H-bridges, tBLANK is included to ignore huge current spike due to rush current to varistor capacitance.

Short/Open for Motor Outputs

When a short/open situation happens, the protection circuit prevents device damage under certain conditions (short at start up, etc).

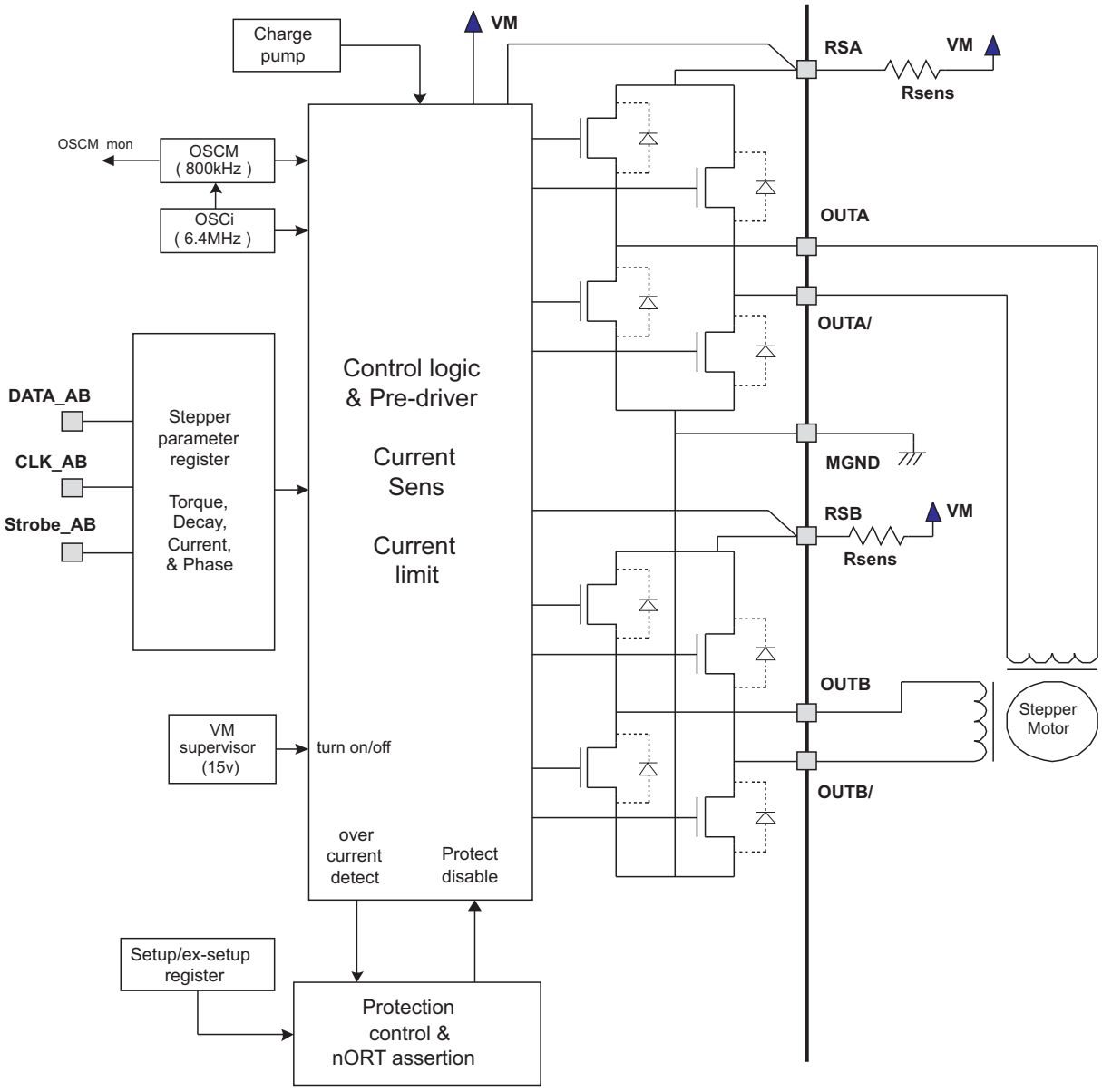
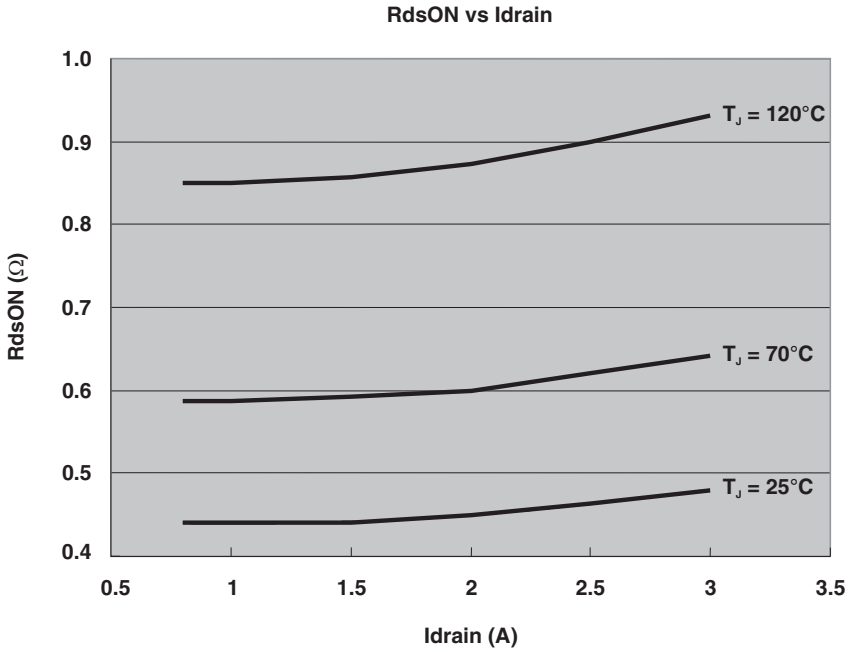


Figure 18. Stepper Motor Driver

Table 13. Angular Rotation Setting for Stepping Motor Driver (Parameter Bit in Stepper Register)

STEP	SET ANGLE (deg)	BIT 14	BIT 13	BIT 12	BIT 11	BIT 7	BIT 6	BIT 5	BIT 4
		CURRENT A (C) 3	CURRENT A (C) 2	CURRENT A (C) 1	CURRENT A (C) 0	CURRENT B (D) 3	CURRENT B (D) 2	CURRENT B (D) 1	CURRENT B (D) 0
16	90	H	H	H	H	L	L	L	L
15	84.4	H	H	H	H	L	L	L	H
14	78.8	H	H	H	L	L	L	H	L
13	73.1	H	H	L	H	L	L	H	H
12	67.5	H	H	L	L	L	H	L	L
11	61.2	H	L	H	H	L	H	L	H
10	56.3	H	L	H	L	L	H	H	L
9	50.6	H	L	L	H	L	H	H	H
8	45	H	L	L	L	H	L	L	L
7	39.4	L	H	H	H	H	L	L	H
6	33.8	L	H	H	L	H	L	H	L
5	28.1	L	H	L	H	H	L	H	H
4	22.5	L	H	L	L	H	H	L	L
3	16.9	L	L	H	H	H	H	L	H
2	11.3	L	L	H	L	H	H	H	L
1	5.6	L	L	L	H	H	H	H	H
0	0	L	L	L	L	H	H	H	H



A. This plot includes both actual device characterization data and extrapolated data.

B. Actual device has self-heating effect to increase the junction temperature, with continuous loading current more than 1 A.

C. The device temperature is set to 70°C for the $R_{ds(ON)}$ test.

Figure 19. Typical $R_{ds(ON)}$ Value vs Drain Current (DMOS FET in H-Bridge)

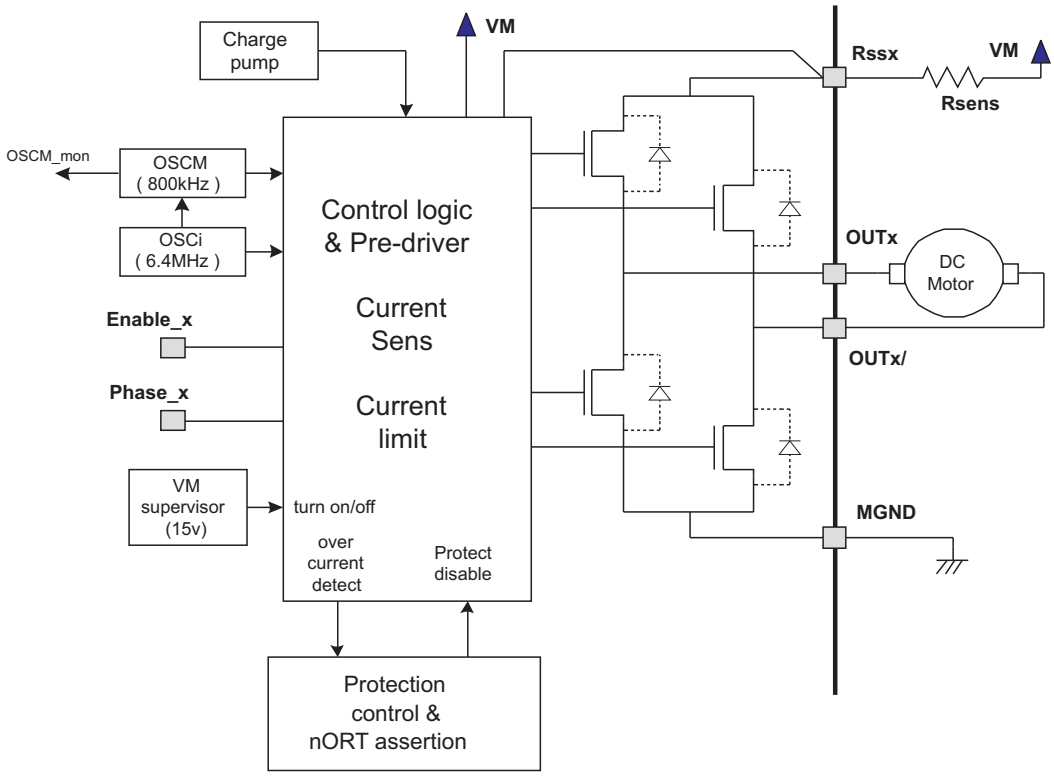


Figure 20. DC Motor Drive

The motor configuration setup bits in the setup register can select three types of DC motor driving: utilizing a single H-bridge, utilizing two (A and B, or C and D) H-bridges in parallel, or utilizing four H-bridges in parallel.

For the setup register value (bit 2,1,0) = (1,0,1), the device configuration is 4× DC motor, which enables each H-bridge to drive a DC motor independently. The ENABLEx and PHASEx input terminals are reassigned from the serial interface pins and some reserved pins, after nSLEEP pin is set to H.

For the setup register value (bit 2,1,0) = (0,1,1), the device configuration is 1× large DC + 2× DC motor mode. The large DC driving utilizes two H-bridges in parallel and controlled by ENABLE_AB and PHASE_AB pins. Two Rsens pins should be connected together.

The VREF inputs are used for the Rsense comparator reference voltage. VREF_AB provides the voltage to both H-bridge A and B, and VREF_CD provides the voltage for H-bridge C and D.

Table 14. DC Motor Drive Truth Table

FAULT CONDITION	nSLEEP	ENABLEX	PHASEX	+ HIGH SIDE	+ LOW SIDE	- HIGH SIDE	- LOW SIDE
0	0	X	X	OFF	OFF	OFF	OFF
0	1	0	X	OFF	OFF	OFF	OFF
0	1	1	0	OFF	ON	ON	OFF
0	1	1	1	ON	OFF	OFF	ON
Motor OCP	1	X	X	OFF	OFF	OFF	OFF
TSD	X	X	X	OFF	OFF	OFF	OFF

Charge Pump

The charge-pump voltage-generator circuit utilizes external storage and bucket capacitors. It provides the necessary voltage to drive the high-side switches for both DC-DC regulators and motor drivers. The charge-pump circuit is driven at a frequency of 1.6 MHz (nom). Recommended bucket capacitance is 10 nF, 16 V (min), and storage capacitance is 0.1 µF, 60 V (min). The charge-pump storage capacitor, Cstage, should be connected from the VCP output, pin 22, to V_M.

For power-saving purposes in sleep mode, the charge pump is stopped when n_sleep = L and all three regulators are turned OFF. When the part is powered up, the charge pump is started first after the C_select capture, and 10 ms after the CP startup, the first regulator is started up.

Table 15. Charge Pump

FAULT CONDITION	DC-DC Ch-A	DC-DC Ch-B	DC-DC Ch-C	nSLEEP	CHARGE PUMP
0	OFF	OFF	OFF	0	OFF
0	ON	X	X	X	ON
0	X	ON	X	X	ON
0	X	X	ON	X	ON
0	X	X	X	1	ON
Motor OCP	X	X	X	1	ON
TSD	X	X	X	X	OFF

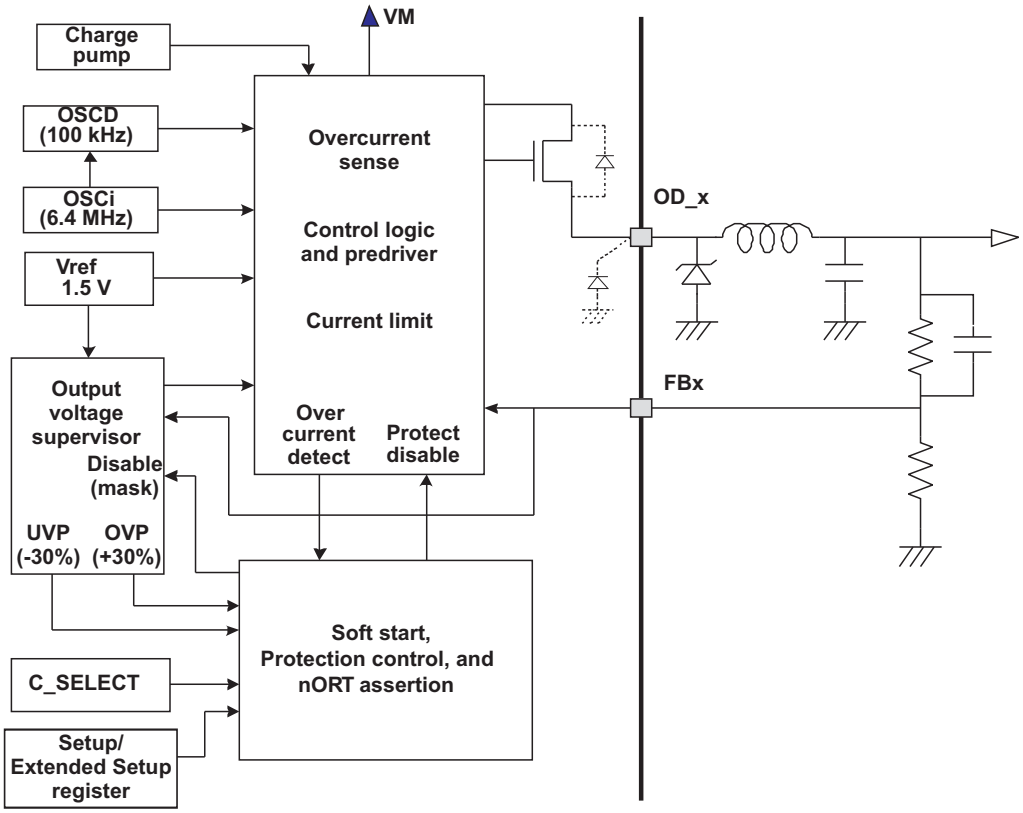


Figure 21. DC-DC Converter

This is a switch-mode regulator with integrated switches, to provide a programmed output set by the feedback terminal. The DC-DC converter has a fixed frequency variable duty cycle topology with a switching frequency of 100 kHz (nom). External filtering (inductor and capacitor) and external catch diode are required. The output voltage is short-circuit protected. If the system has a high input voltage and a very light load on the output, the converter may not provide energy to the inductor (skip) until the load line or the minimum voltage threshold is reached.

The regulator has a soft-start function to limit the rush current during start up. It is achieved by using VFB ramp during soft start.

For unused DC-DC converter channels, the external components can be removed if the channel is set to inactive by the C_SELECT pin and register bits. Also, the VFB pin can be left open or connected to ground.

DCDC_MODE selector can operate channel B and C in parallel mode to handle 2× output driving capability. VFB_B pin is active for feedback, and VFB_C pin must be pulled down internally.

DCDC_MODE for Parallel-Mode Control

The DCDC_MODE pin selects the DC-DC converter parallel driving for Ch-B and Ch-C. The input is pulled up to internal 3.3 V by a 200-kΩ resistor. When the pin is H or left open, Ch-B and Ch-C are driven in parallel.

Table 16. C_SELECT for Start-Up

C_SELECT	PIN VOLTAGE	DC-DC Vout1, ODA	DC-DC Vout2, ODB	DC-DC Vout3, ODC
Gnd	0 V to 0.3 V	OFF	OFF	OFF
Pull Down (by external 200 kW)	1.3 V to 2 V	See Table 17		
OPEN	3 V to 3.3 V	ON	ON	ON

DCDC_MODE and C_SELECT Timing Delay and Start-Up Order

DCDC_MODE and C_SELECT play a role in the order of regulator enablement, as well as the time when the first regulator is enabled to when the second is enabled. Regulators B and C are always enabled together, whether they are working in parallel mode or not.

Table 17. DCDC_MODE and C_SELECT Timing Delay (DRV8809)

DCDC_MODE	C_SELECT	TIMING DELAY	DESCRIPTION
L	GND	None	No regulator is enabled.
L	Pull down	None	No regulator is enabled.
L	3 V to 3.3 V	1.6 ms	Ch-A followed by Ch-B and Ch-C
H	GND	None	No regulator is enabled.
H	Pull down	1.6 ms	Ch-B and Ch-C followed by Ch-A
H	3 V to 3.3 V	1.6 ms	Ch-A followed by Ch-B and Ch-C

Table 18. DCDC_MODE and C_SELECT Timing Delay (DRV8810)

DCDC_MODE	C_SELECT	TIMING DELAY	DESCRIPTION
L	GND	None	No regulator is enabled.
L	Pull down	None	No regulator is enabled.
L	3 V to 3.3 V	1.6 ms	Ch-A followed by Ch-B and Ch-C
H	GND	None	No regulator is enabled.
H	Pull down	20 ms to 40 ms	Ch-B and Ch-C followed by Ch-A
H	3 V to 3.3 V	20 ms to 40 ms	Ch-A followed by Ch-B and Ch-C

In-Reset: Input for System Reset

In-Reset pin assertion stops all the DC-DC converters and H-bridges. It also reset all the register contents to default value. After deassertion of the input, the device follows the initial start-up sequence. The C_SELECT state is captured after the In-Reset deassertion. The input is pulled up to internal 3.3 V by 200-kΩ resistor. When the pin = H or left open, reset function is asserted. Also it has deglitch filter of 2.5 µs to 7.5 µs.

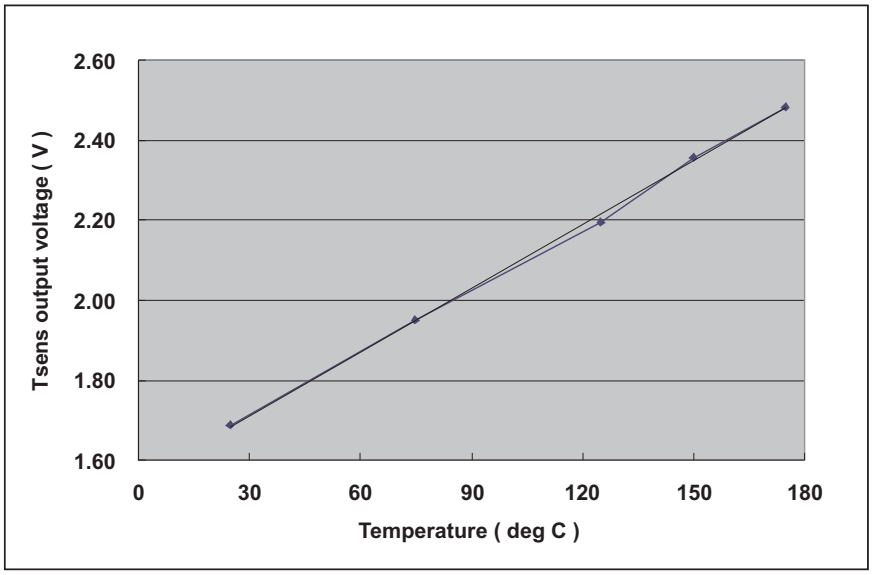
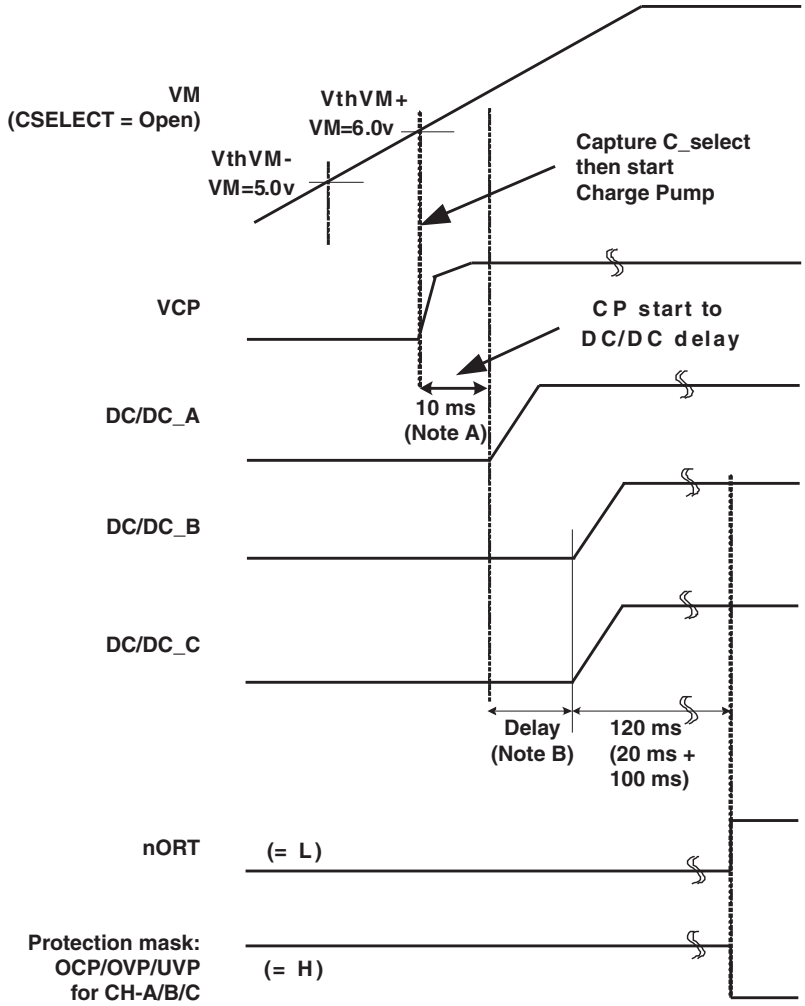


Figure 22. Tsens (Analog Out) Temperature Coefficient: Voltage Plot Example (Typical)



A. Charge-pump wake-up delay, from 10 ms to 20 ms, due to asynchronous event capture

B. For the DRV8809, delay is 1.6 ms for both DC_MODE high and low. For the DRV8810, delay is 20 ms to 40 ms for DC_MODE high and 1.6 ms for DC_MODE low.

Figure 23. Power-Up Timing (Power Up With DC-DC Turn-On By C_SELECT)

NOTE

When V_M crosses $VthV_{M+}$ (about 6 V), the C_select state is captured. If C_SELECT is open (pulled up to internal 3.3 V), all DC-DC regulator channels (A, B, and C) are turned on. The time of channels B and C to be turned on, with regards to channel A, depends on the state of DC_MODE.

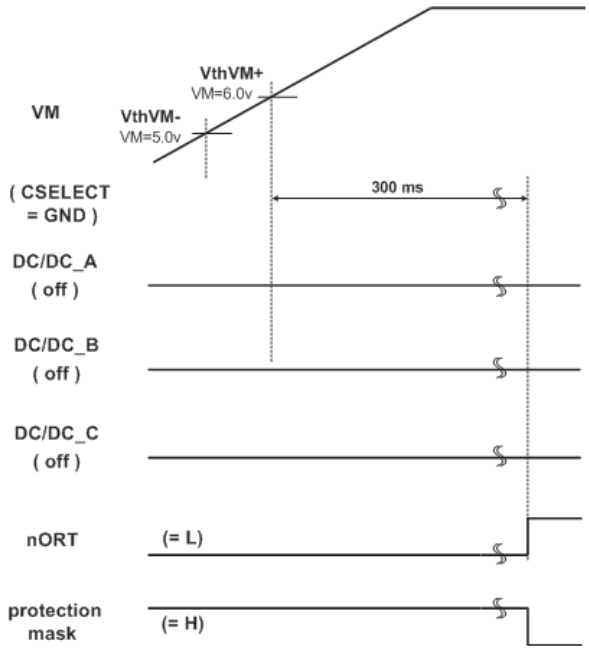
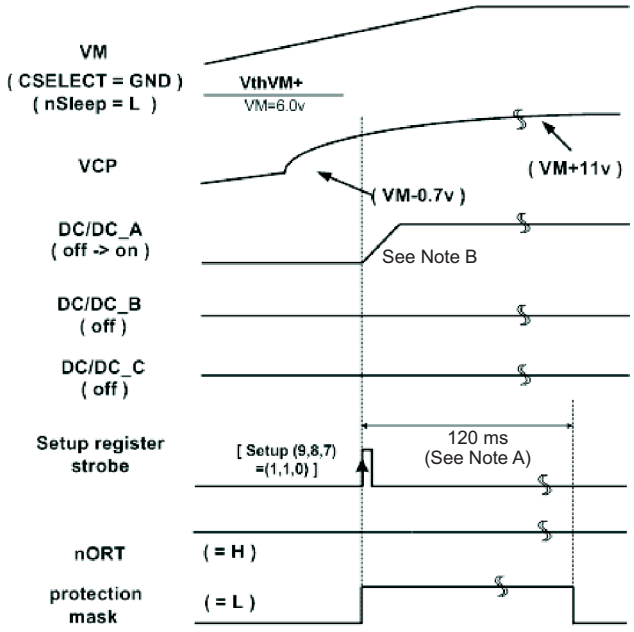


Figure 24. Power-Up Timing (Power Up Without DC-DC Turn-On: C_SELECT = GND)

NOTE

When V_M crosses $VthV_{M+}$ (about 6 V) with C_SELECT = GND, none of the three regulators are turned on. The nORT output is released to H after 300 ms from the $VthV_{M+}$ crossing.



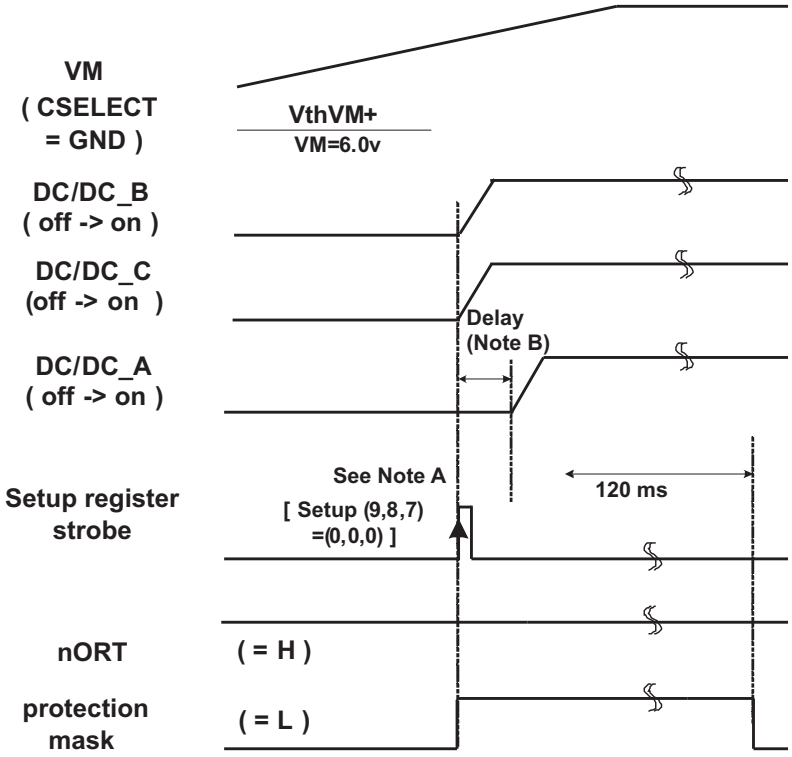
A. 120 ms to 140 ms due to asynchronous event capture

B. After VM power up, DC-DC starts at the setup register strobe.

Figure 25. Power-Up Timing (DC-DC Regulator Wake Up by Setup Register)

NOTE

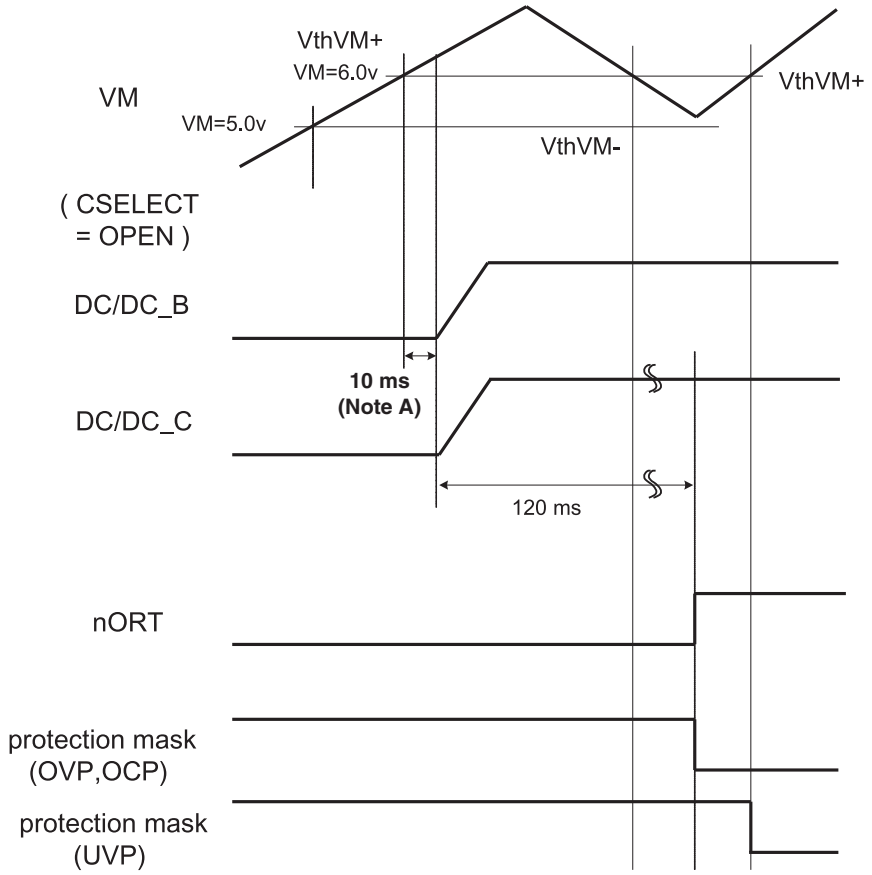
The regulator is started from the strobe input, same as charge pump. There is no 10-ms waiting period, because VCP pin already reached V_M – 0.7 V.



A. After VM power up, DC-DC starts at the setup register strobe.

B. For the DRV8809, delay is 1.6 ms for both DC_MODE high and low. For the DRV8810, delay is 20 ms to 40 ms for DC_MODE high and 1.6 ms for DC_MODE low.

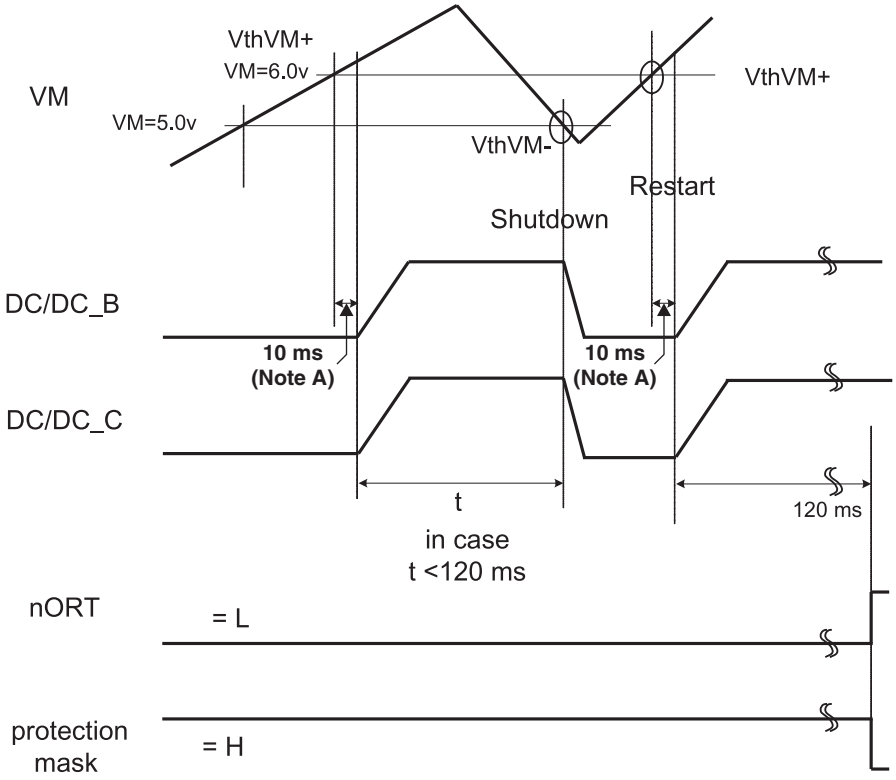
Figure 26. Power-Up Timing (DC-DC Regulator Wake Up by Setup Register, All Three Channels On)



A. Charge-pump wake-up delay, from 10 ms to 20 ms, due to asynchronous event capture

B. Start-up with V_M glitch (not below VthV_). Only channels B and C are shown. Same applies to Channel A.

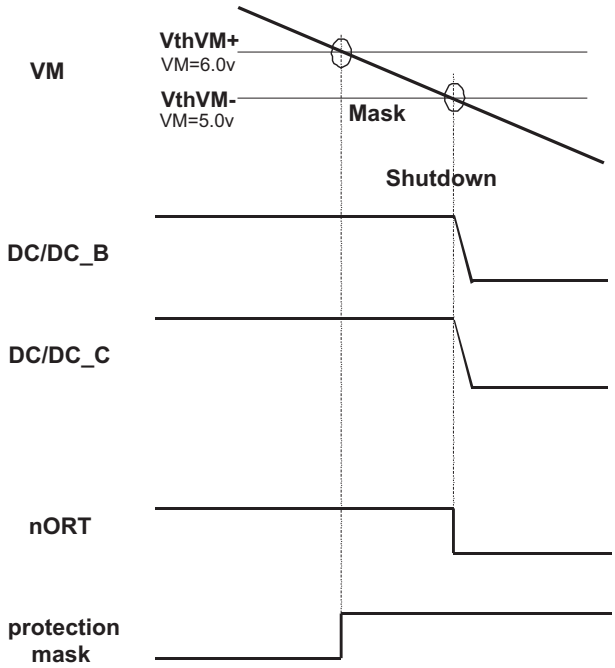
Figure 27. V_M Start-Up/Power-Down and Glitch Condition



A. Charge-pump wake-up delay, from 10 ms to 20 ms, due to asynchronous event capture

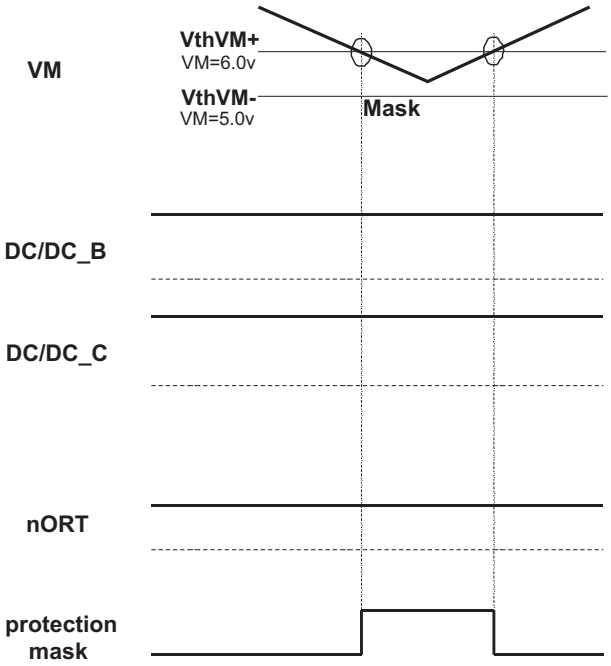
B. Start-up with V_M glitch (below VthV_). Only channels B and C are shown. Same applies to Channel A.

Figure 28. V_M Startup/Power-Down and Glitch Condition



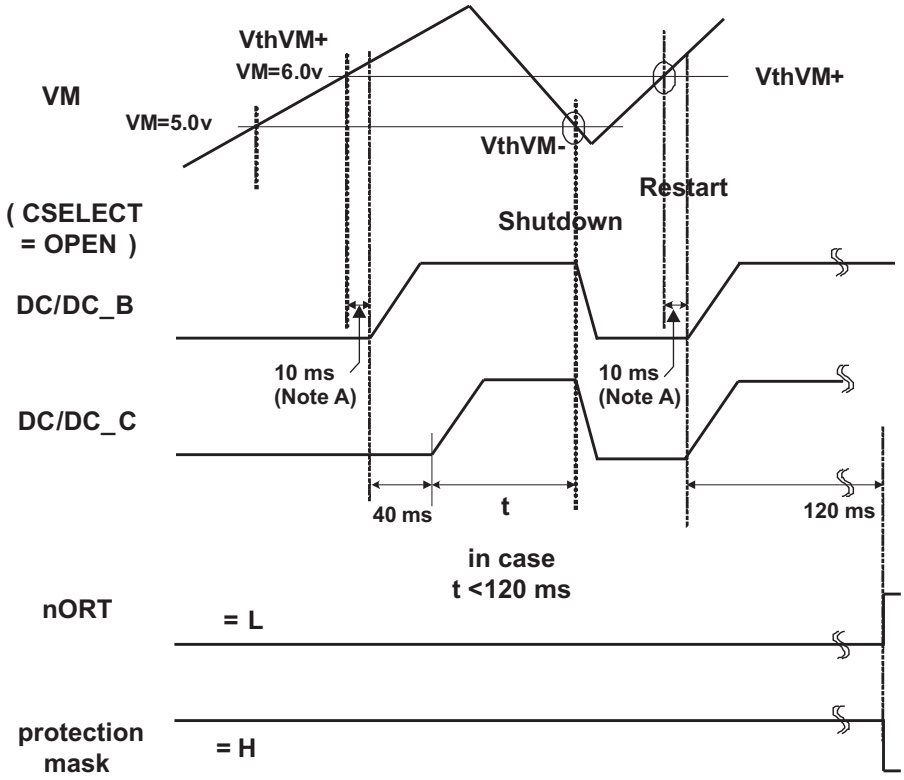
A. Only channels B and C are shown. Same applies to Channel A.

Figure 29. Power Down (Normal)



A. Only channels B and C are shown. Same applies to Channel A.

Figure 30. Power Down (Glitch on V_M)



A. Charge-pump wake-up delay, from 10 ms to 20 ms, due to asynchronous event capture

B. Only channels B and C are shown. Same applies to Channel A.

Figure 31. Power Down (Glitch on V_M Below VthV_)

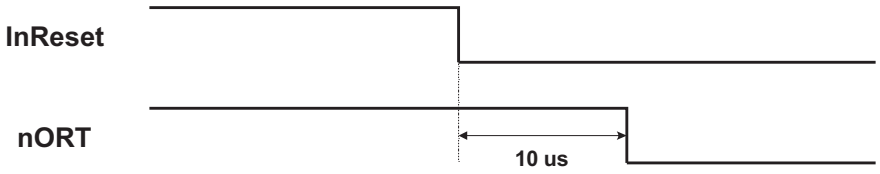


Figure 32. Shutdown by In-Reset

Blanking Time Insertion Timing for DC Motor Driving

For the DC motor driving H-bridge, tBlank is inserted at each phase reversal and also following each chopping cycle (once every eight OSCM clocks).

For a large n number (5 or 6) tBlank setup may decrease the itrip detect window. The user must be careful to optimize in the system.

Case A: Phase duty = 25%

Case A*1 for setup bit = (1,0)

Case A*2 for setup bit = (0,1)

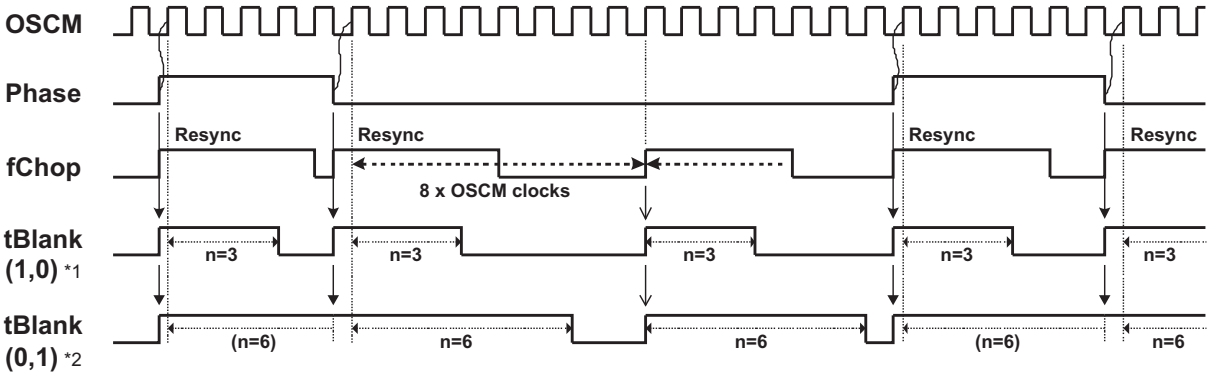
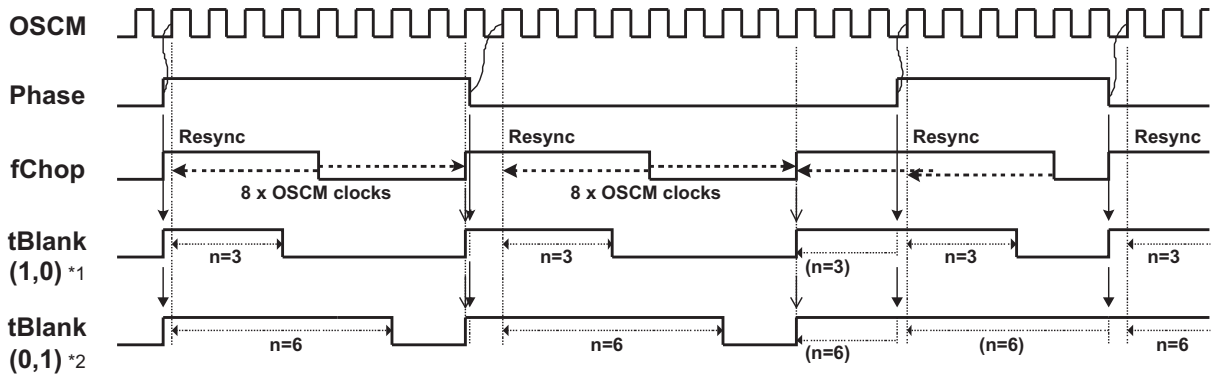


Figure 33. Blanking Time Insertion Timing, Case A

Case B: Phase duty = 40%

Case B*1 for setup bit =(1,0)

Case B*2 for setup bit =(0,1)



*1 : Setup register bit <4,3> = (1,0) : tBlank = OSCM clock x 3 (or bit <5,6> for H-bridge C,D channel)
*2 : Setup register bit <4,3> = (0,1) : tBlank = OSCM clock x 6 (or bit <5,6> for H-bridge C,D channel)

Figure 34. Blanking Time Insertion Timing, Case B

Table 19. Function Table nORT, Power Down, V_M < 4.5 V Conditions

DEVICE STATUS	CHARGE PUMP	OSCD	OSCM	nORT (RESET) OUTPUT	MODE SETTING
nSLEEP	Active	Active	Active	Inactive	Available
nORT	Inactive	Active	Active	Active	Depend on power down
V_M < 6 V during power down	Active	Active	Active	See timing chart	Depend on power down
4.5 V < V_M	Inactive	Inactive	Inactive	Active	Unavailable

Table 20. Shutdown Functions

CASE OF SUPPLY SHUTDOWN	DC-DC Vout1	DC-DC Vout2	DC-DC Vout3	MOTOR	nORT (RESET)
DC-DC Vout1 OCP, OVP	Shut down	Shut down	Shut down	Shut down	Reset ON (L out)
DC-DC Vout2 OCP, OVP	Shut down	Shut down	Shut down	Shut down	Reset ON (L out)
DC-DC Vout3 OCP, OVP	Shut down	Shut down	Shut down	Shut down	Reset ON (L out)
Motor OCP	NA	NA	NA	OFF	Reset one pulse (t_{low} = 40 ms)
TSD	Shut down	Shut down	Shut down	Shut down	Reset ON (L out)

- Shutdown of DC-DCs is released at V_M > $VthV_{M+}$ when V_M is increasing. In case V_M decreases, DC-DCs are shut down when V_M <VthV_. When V_M decreases and $VthV_{M+}$ > V_M > VthV_, the DC-DC output voltage supervisor is ignored.
- Motor shutdown is released by V_M < 4.5 V or nSLEEP rising edge.
- nORT (reset) ON/OFF time is 40 ms.
- The data in Table 21 is valid if the protection control bits in the EX-setup register are all 0.

Table 21. Modes of Operation(1) (2)

POR	M OFF	ISD				OVP			TSD	EXTERNAL PIN		IC	BLOCK FUNCTIONS				
VM	VM	Vout1	Vout2	Vout3	MOTOR	Vout1	Vout2	Vout3	MOTOR	nSLEEP	CSEL		MOTOR	Vout1	Vout2	Vout3	nORT
0	0	0	0	0	0	0	0	0	0	H		N	On	On	On	On	H
1	X	X	X	X	X	X	X	X	X	X	X	Off	Off	Off	Off	Off	L
0	1	X	X	X	X	X	X	X	X	X	X	O	On	Off	On/Off	On/Off	H
	0	1	X	X	X	X	X	X	X	X	X	p	S/D	S/D	S/D	S/D	L
		0	1	X	X	X	X	X	X	X	X	e	S/D	S/D	S/D	S/D	L
			0	1	X	X	X	X	X	X	X	r	S/D	S/D	S/D	S/D	L
				0	1	X	X	X	X	X	X	a	Off	On	On	On	L/P
					0	1	X	X	X	X	X	t	S/D	S/D	S/D	S/D	L
						0	1	X	X	X	X	l	S/D	S/D	S/D	S/D	L
							0	1	X	X	X	o	S/D	S/D	S/D	S/D	L
								0	1	X	X	n	S/D	S/D	S/D	S/D	L
									0	Low	X	S	Off	On	On	On	H
										High	All off		X	Off	Off	Off	L
											200 k		X	On	On	Off	H
											Open		X	Off	On	On	H

(1) Valid only if the protection control bits (in EX-setup register) are all 0.
(2) N = Normal operation, S = Sleep mode, 0 = Off, 1 = On, X = Don't care, S/D = Shutdown, P = Pulse after fault occurs (retry), OFF = Must toggle sleep terminal or power-on reset (nORT), S/D = Must do a power-on reset (nORT)

APPLICATION INFORMATION

Application Schematic

For one stepper and two DC motor configuration:

- DC-DC Ch-A = 5 V (12 V)
- DC-DC Ch-B = 1.5 V
- DC-DC Ch-C = 3.3 V

If start-up from Ch-B (1.5 V) ≥ Ch-A (5 V), Ch-C 3.3 V should be turned on by the setup register (200 kΩ between C_SELECT pin and GND).

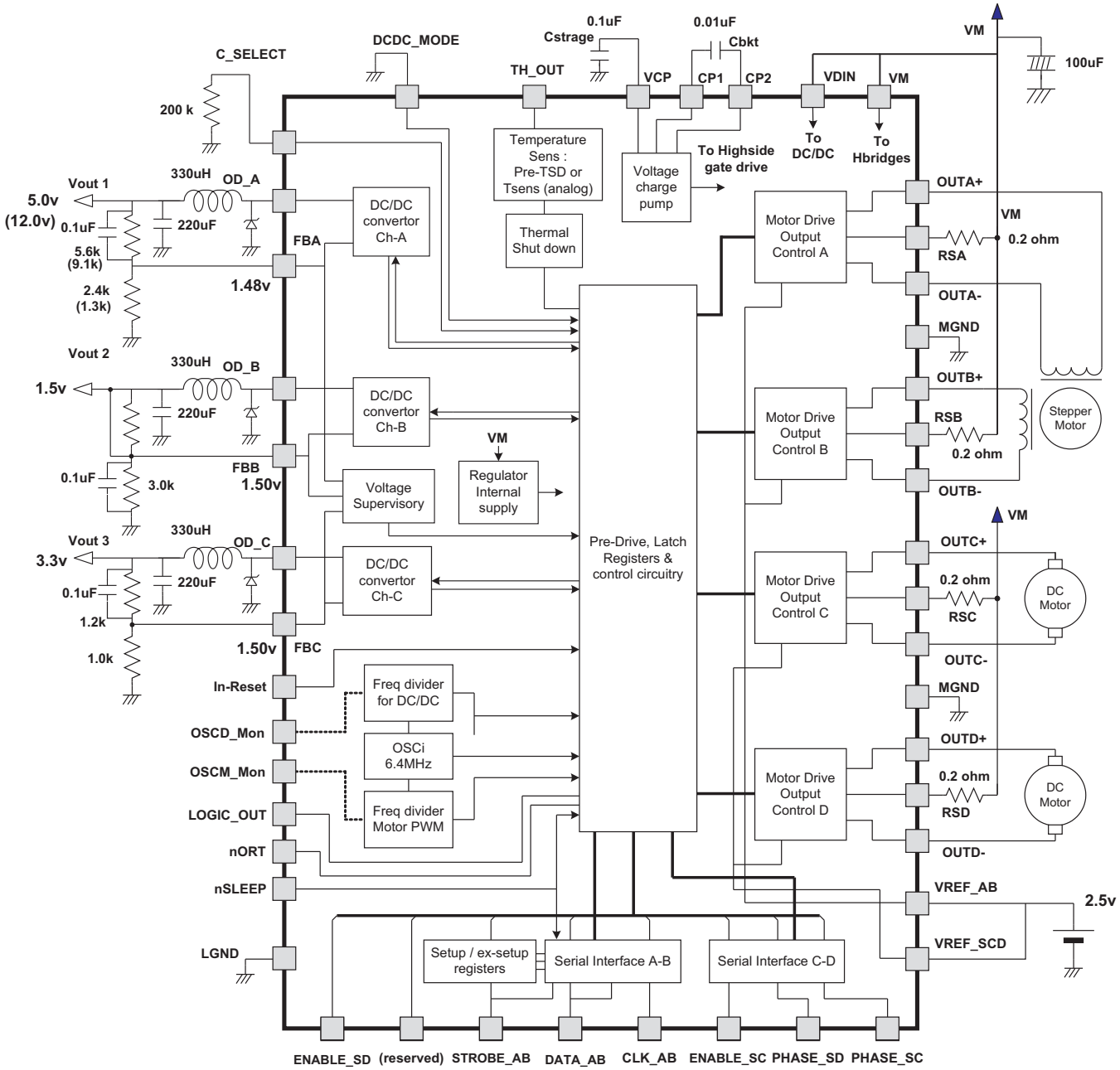


Figure 35.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8809PAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 50	DRV8809 1	Samples
DRV8810PAP	ACTIVE	HTQFP	PAP	64	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-10 to 64	DRV8810 1	Samples

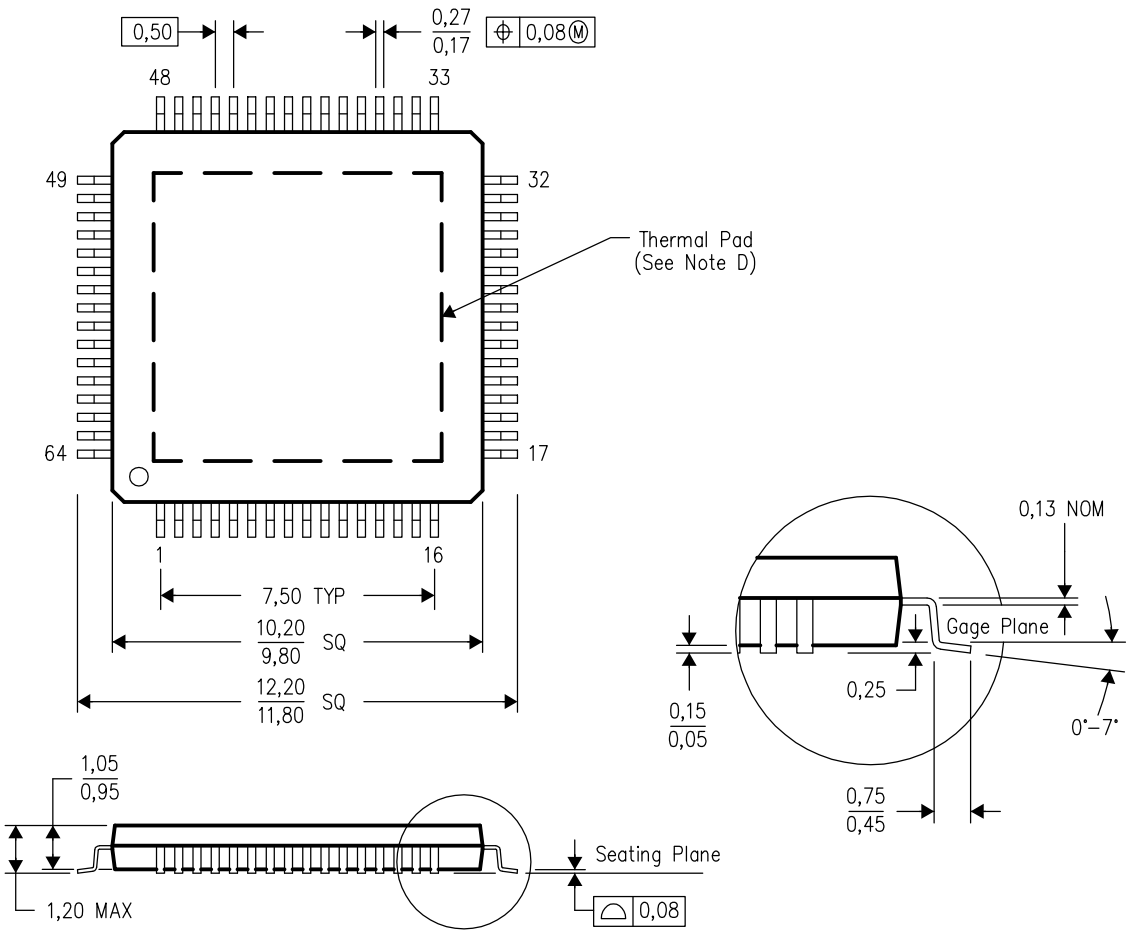
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

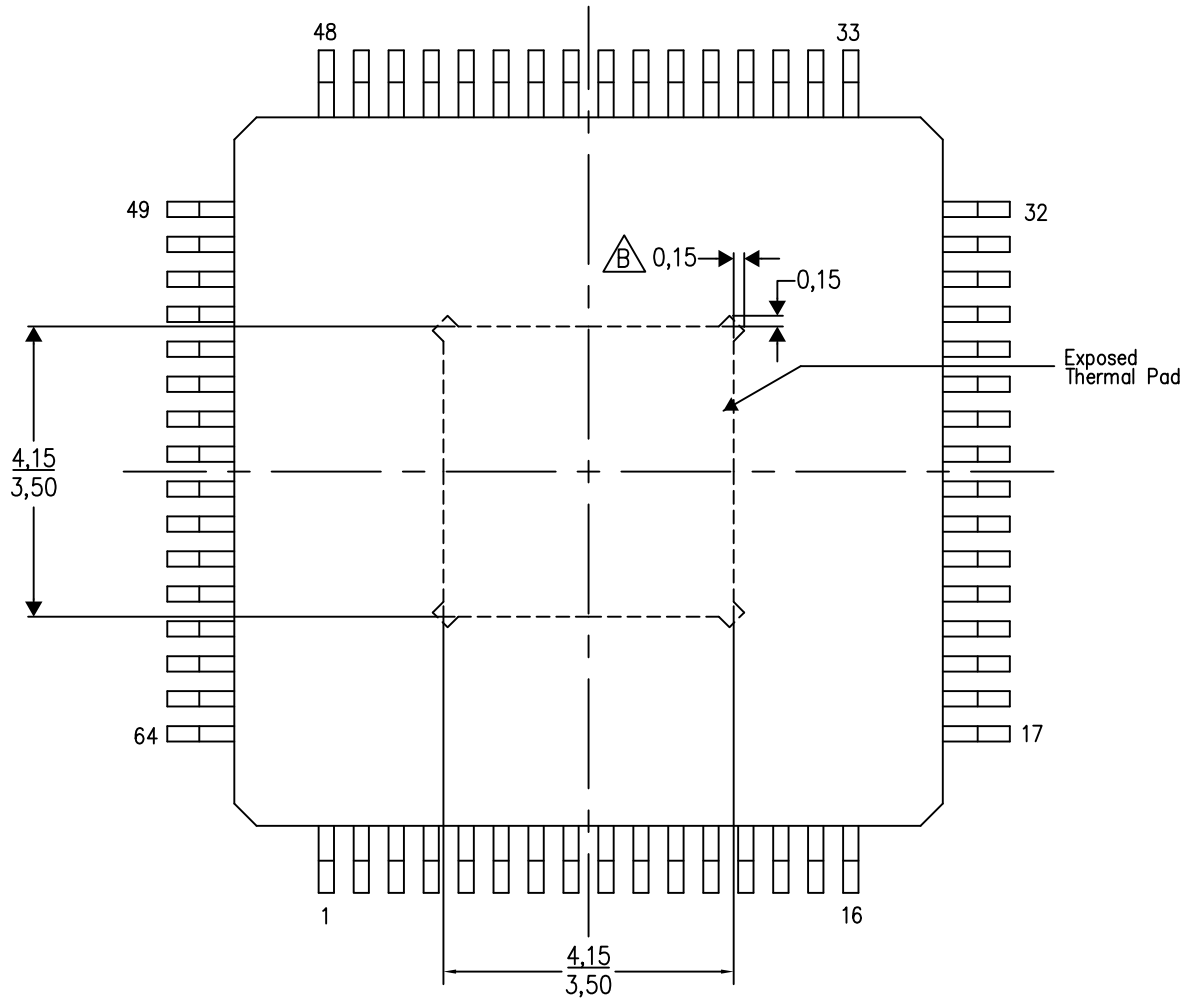
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–2/N 02/13

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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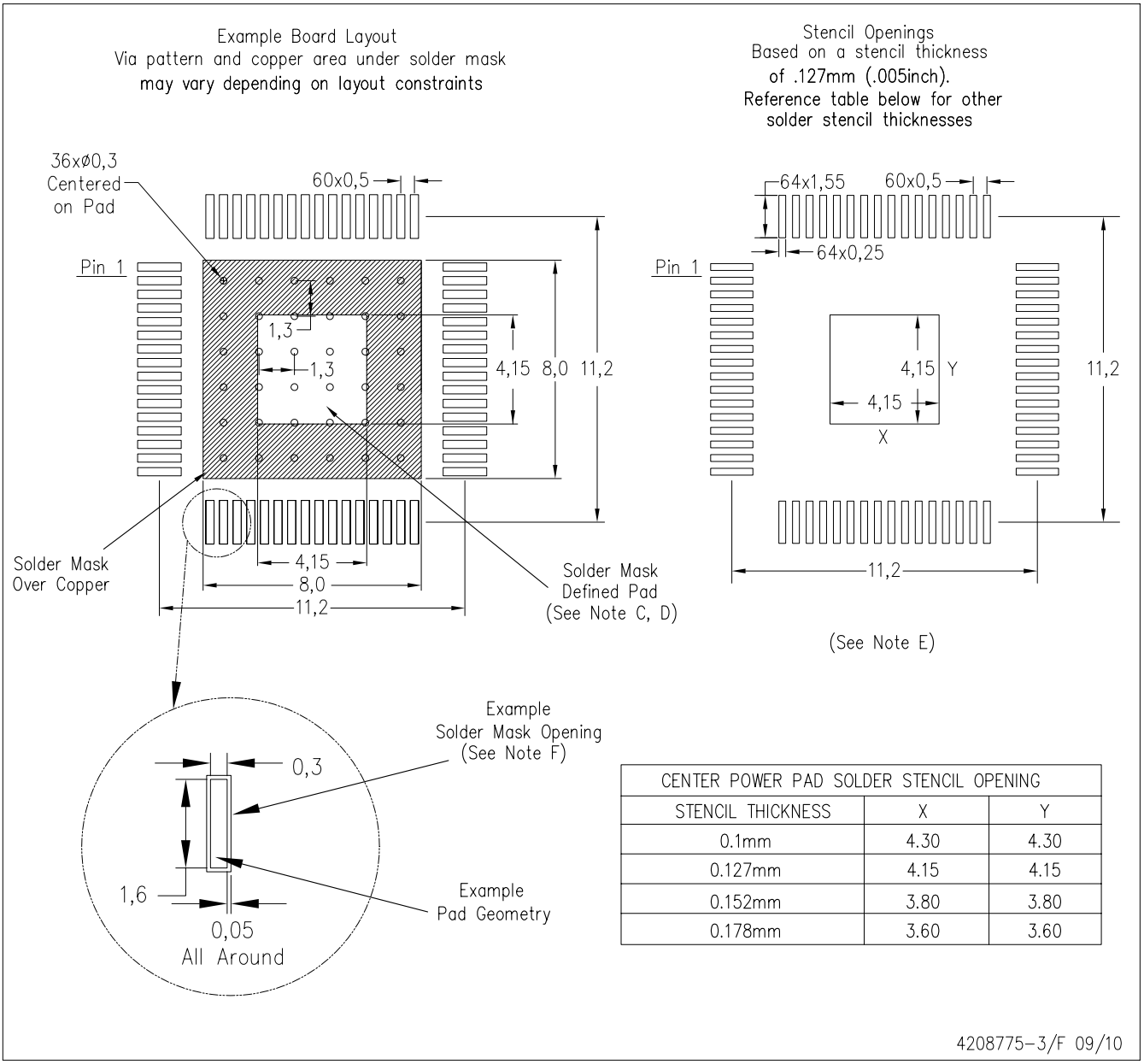
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.30	4.30
0.127mm	4.15	4.15
0.152mm	3.80	3.80
0.178mm	3.60	3.60

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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