# Chip Card & Security

# SLE 4406SP
# SLE 4406SPE

Intelligent 112–Bit EEPROM Counter
for > 20000 Units with Security Logic

Short Product Information

October 2008

| SLE 4406SP/06SPE Short Product Information | | Ref.: SPI_SLE4406SP_1008.doc |
|---|---|---|
| **Revision History:** | **Current Version 2008-10-14** | |
| Previous Releases: | 2005-06-29 | |
| Page | Subjects (changes since last revision) | |
| | Editorial update | |

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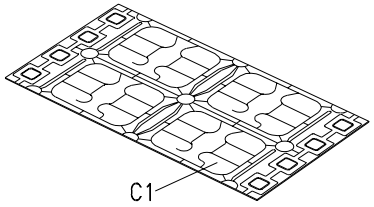
# Intelligent 112–Bit EEPROM Counter for > 20000 Units with Security Logic

## Features




**M3**

- **100% functional compatibility to 4406S/06SE**
- **112 bit EEPROM and 16 bit ROM**

  104 bit user memory fully compatible with SLE 4406/06E
  – 64 bit Identification Area 1 consisting of
    • 16 bit Manufacturer code
    • SLE 4406SP:
      8 bit Manufacturer data, card issuer dependent
      40 bit for personalization data of card issuer
    • SLE 4406SPE:
      48 bit for personalization data of card issuer
  – 40 bit Counter Area including 1 bit for personalization (PROM/EEPROM)

  24 bit additional memory for advanced features configurable during personalization
  – either 24 bit Identification Area 2 for personalization data of card issuer
  – or 24 bit Data Area for free user access
- **Counter with up to 33352 count units**
  – Five stage abacus counter
  – Due to testing purposes a maximum of 21064 count units is guaranteed
- **Transport Code protection for delivery**
- **Contact configuration and Answer-to-Reset (synchronous transmission) in accordance to standard ISO/IEC 7816**
- **Sophisticated electrical characteristics**
  – Ambient temperature $T_A$ –40 … +80°C for chip
  – Supply voltage 5 V ± 10 %
  – Supply current < 1 mA
  – EEPROM programming time 5 ms
  – ESD protection minimum 2,000 V, typical 4,000 V
  – Endurance minimum 100,000 write/erase cycles / bit[1)]
  – Data retention for minimum of 30 years[1)]
- **Advanced 1.2 µm CMOS-technology optimised for security layout**
  – EEPROM-cells protected by shield
  – Secure wiring for all security relevant signals
  – Shielding of deeper layers via metal
  – Sensory and logical security functions
  – No isolation on backside necessary

1) Values are temperature dependent

**Table 1 Ordering Information**

| Type | Package[1)] | Remark | Access of 3rd byte |
|---|---|---|---|
| SLE 4406SP C | Die (on Wafer) | unsawn | Data of 3rd byte are programmed by Infineon exclusively |
| SLE 4406SP D | Die (on Wafer) | sawn | |
| SLE 4406SP M3 | T-M3.2-6 | | |
| SLE 4406SP MFC3 | S-MFC3.1-6-1 | FCoS™ [2)] | |
| SLE 4406SPE C | Die (on Wafer) | unsawn | Data of 3rd byte are programmed by the card manufacturer at personalisation |
| SLE 4406SPE D | Die (on Wafer) | sawn | |
| SLE 4406SPE M3 | T-M3.2-6 | | |
| SLE 4406SPE MFC3 | S-MFC3.1-6-1 | FCoS™ [2)] | |

## Pin Description

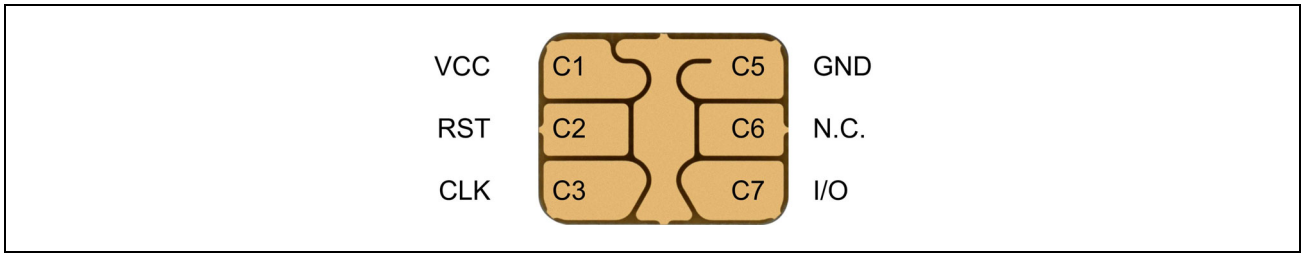



**Figure 1 Pin Configuration Wire-bonded Module M3.2 (top view)**

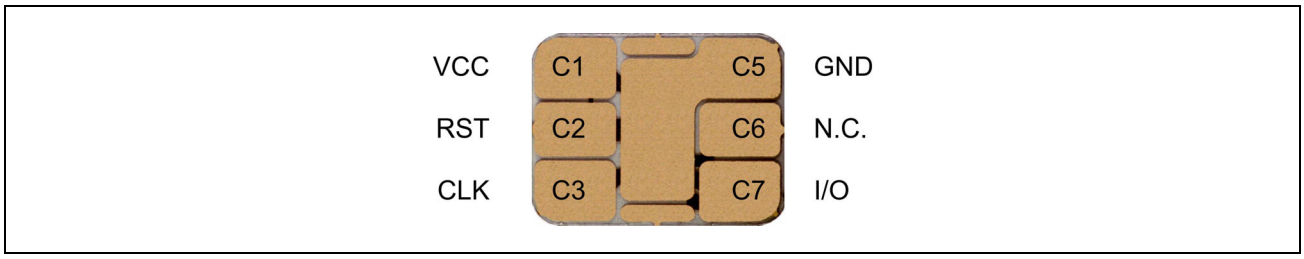



**Figure 2 Pin Configuration Flip Chip Module MFC3.1 (top view)**

1) Available as a Flip Chip Module (MFC3), wire-bonded module (M3) for embedding in plastic cards or as a die on unsawn (C) / sawn wafer (D) for customer packaging

2) FCoS™ Flip Chip on Substrate

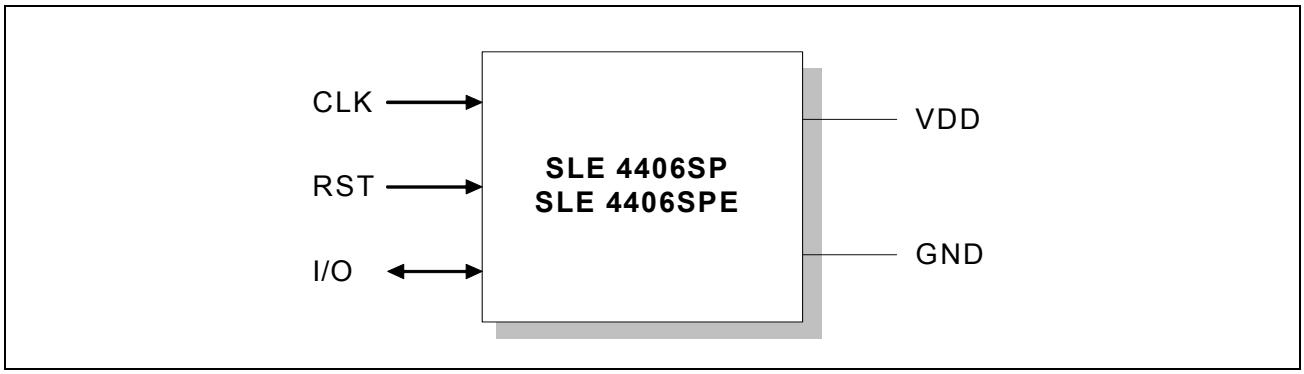



**Figure 3 Pad Configuration Die**

**Table 2 Pin Definitions and Functions**

| Card Contact | Symbol | Function |
|---|---|---|
| C1 | VCC | Supply voltage |
| C2 | RST | Control input (Reset Signal) |
| C3 | CLK | Clock input |
| C5 | GND | Ground |
| C6 | N.C. | Not connected |
| C7 | I/O | Bi-directional data line (open drain) |

## General Description

SLE 4406SP/06SPE is designed for applications in prepaid telephone cards. The chip consists of an EEPROM memory of 112 bit, a ROM of 16 bits and a control/security unit.

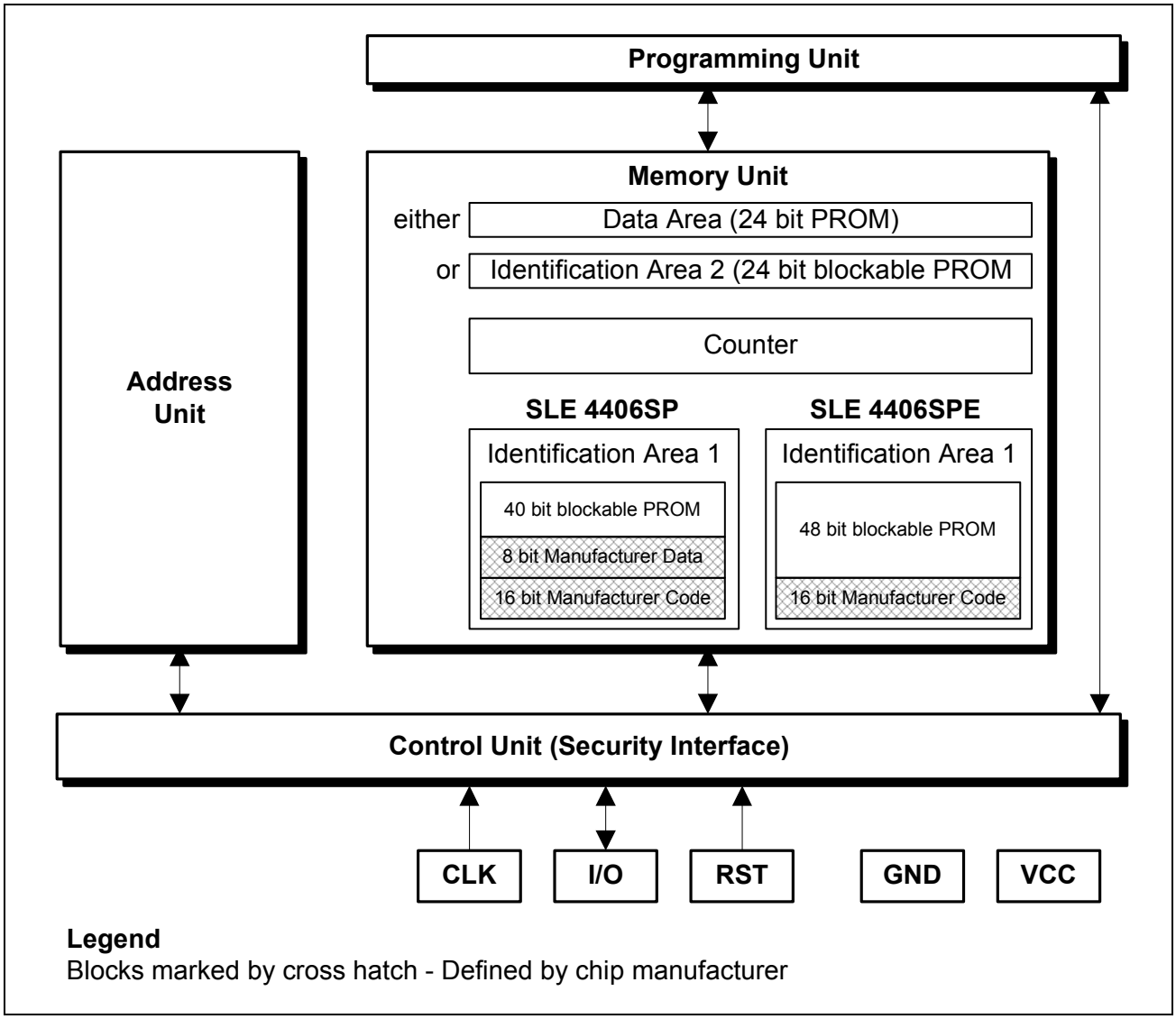



**Figure 4 Block Diagram**

- **Memory Unit**
  Counter, Identification Data (e.g. serial number, expiry date) and Data Area.
- **Address Unit**
  Setting of the address counter is synchronously with the CLK.
- **Programming Unit**
  The programming voltage for the EEPROM/PROM is generated internally.
- **Security Interface**
  Ensures a minimum and a maximum frequency and proper logical voltage levels.