

User Guide

IF310 DVK

Version 0.1

Revision History

Version	Date	Notes	Contributors	Approver
0.1	6 Feb 2026	Preliminary Release	Jacky Kuo	Jonathan Kaye

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1 Overview

The Vela™ IF310 development kit provides a platform for rapid developing and testing all variations of the Vela™ IF310 modules. This document describes the development board hardware, highlighting the setup and interfaces available to maximize user flexibility in developing their applications.

2 Vela™ IF310 Development Kit Part Number

Table 1: Available Development Kits

Part Number	Product Description
453-00390-K1	Development Kit, Module, Vela IF310, Integrated Antenna
453-00391-K1	Development Kit, Module, Vela IF310, MHF4

Table 2: Applicable to the following Vela™ IF310 Module part numbers:

Part	Product Description
453-00390R	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), Integrated Antenna, Tape / Reel
453-00391R	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), MHF4, Tape and Reel
453-00392R	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), Trace Pin, Tape and Reel
453-00390C	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), Integrated Antenna, Cut Tape
453-00391C	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), MHF4, Cut Tape
453-00392C	Vela IF310, Bluetooth / Bluetooth LE Audio Module, (Infineon CYW55310), Trace Pin, Cut Tape

3 Vela™ IF310 Development Platform

The **Vela IF310 development platform** provides a complete set of test interfaces and connections. On-board headers and jumpers provide a convenient method of isolating power and signal nets for debugging and power measurements during hardware and software development. The platform also offers two power-level options for its test interfaces, giving users greater flexibility to accommodate different voltage requirements.

In addition, the platform supports **two power input methods: DC 12V and USB Type-C**, allowing customers to choose the option that best fits their power supply needs. For audio applications, the platform provides **two sets of TDM signal interfaces**, enabling users to configure a variety of audio use cases.

Software access and firmware download to the Vela IF310 module can be done through the **Type-C** connector provided on the platform or external FTDI cable.

3.1 Key Features

The Vela™ IF310 Development Kit (453-00390-K1 and 453-00391-K1) has the following features:

- Vela IF310 series module soldered onto the development board
 - Integrated chip antenna variant or
 - MHF4 connector variant
- Vela IF310 HCI UART can be interfaced to:
 - Type-C using the RP2040 USB-UART bridge.
 - External UART Source (using J16 pin 1~6 comply with FTDI cable (USB to TTL 232))
- Vela IF310 module Supported an external 16Mbit NOR flash and an external 64Mbit PSRAM
- On-board 3.3V and 1.8V supplied from either Type-C (J3, 5V) or external DC JACK (CON1, 12V).
- Main module power can be isolated and provided externally for power requirement measurements.
- Two tricolors with white LEDs for user interaction, one connected to the Vela IF310 and the other to the RP2040
- Two LED indicators for indicating the 3.3V and 1.8V power rails.
- Single or Dual row 2.54 mm pitch pin headers which bring out all Vela IF310 module interfaces:
 - GPIOs
 - Wakeup signals
 - TDM signals
 - I²S for Ezurio's SMARC board
 - BT_REG_ON signal
 - HCI UART
 - DMIC
 - MICP
 - I²C
 - Coexistence signals
- One user button connected to the module
- One reset button for the module, one reset button for RP2040
- One recovery button for the module to enter download mode
- 16Mbit QSPI Flash with BOOTSEL button for the RP2040 firmware storage

3.2 Vela IF310 Development Kit Specifications

Characteristic	Specifications
Configuration Mode	UART
Host Interface	USB
Power Supply	DC 12V or Type-C 5V
Antenna Gain	<ul style="list-style-type: none">• 3.2 dBi peak gain by PCB printed antenna variant• 2.4 dBi peak gain via external antenna variant
Dimension	110 mm x 90 mm x 16.6 mm

4 Development Kit Contents

Table 3: 453-00390-K1 and 453-00391-K1 Development Kit Contents

Development Board	453-00390-K1, Development Kit, Module, Vela IF310, Integrated Antenna
	453-00391-K1, Development Kit, Module, Vela IF310, MHF4
Antennas	<ul style="list-style-type: none"> 1pcs i-Flex PIFA Antenna (PN#EFG2401A3S-10MH4L) for 453-00391-K1 development kit variant only
Cables	<ul style="list-style-type: none"> 1pcs USB-C cable 6pcs Fly lead jumper cable
Jumper	<ul style="list-style-type: none"> 5pcs jumper caps
Stand-Off	<ul style="list-style-type: none"> 4pcs stand-offs and nuts

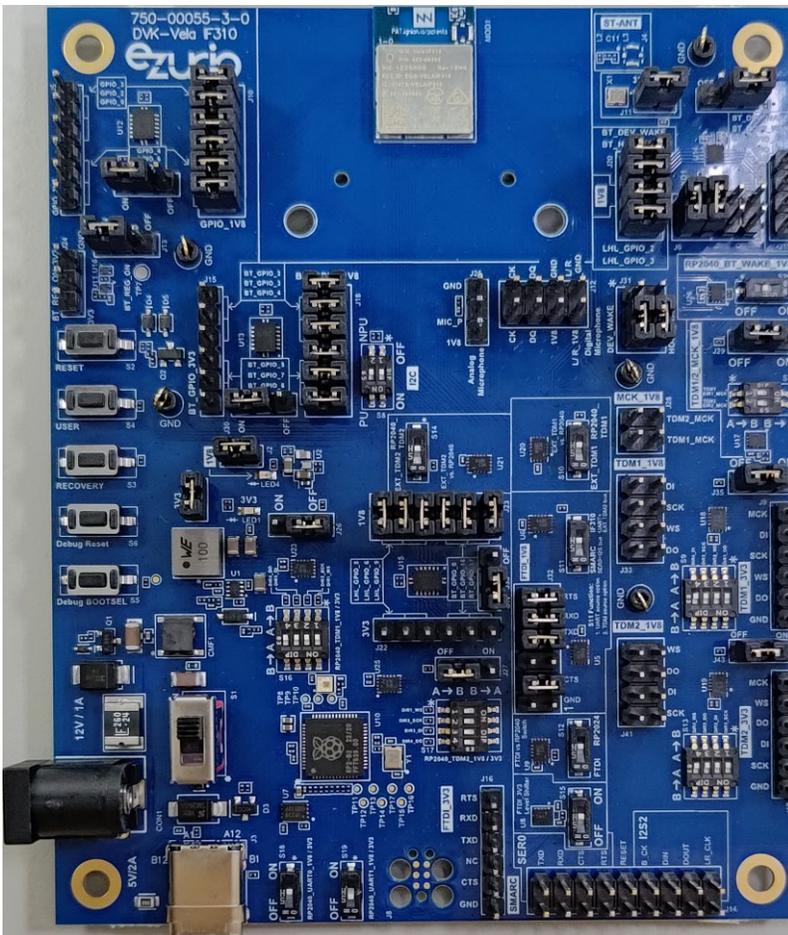


Figure 1: 453-00390-K1 Development kit (453-00390 Module)

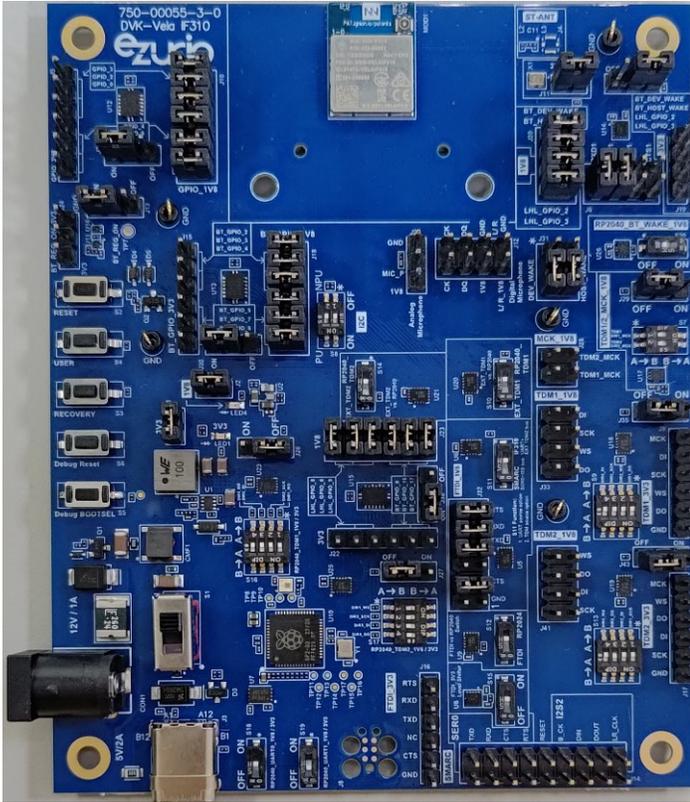


Figure 2: 453-00391-K1 Development kit (453-00391 Module)



Figure 3: i-Flex PIFA Antenna for 453-00391-K1 development board and 453-00391 module

5 Hardware Overview

5.1 Block Diagram

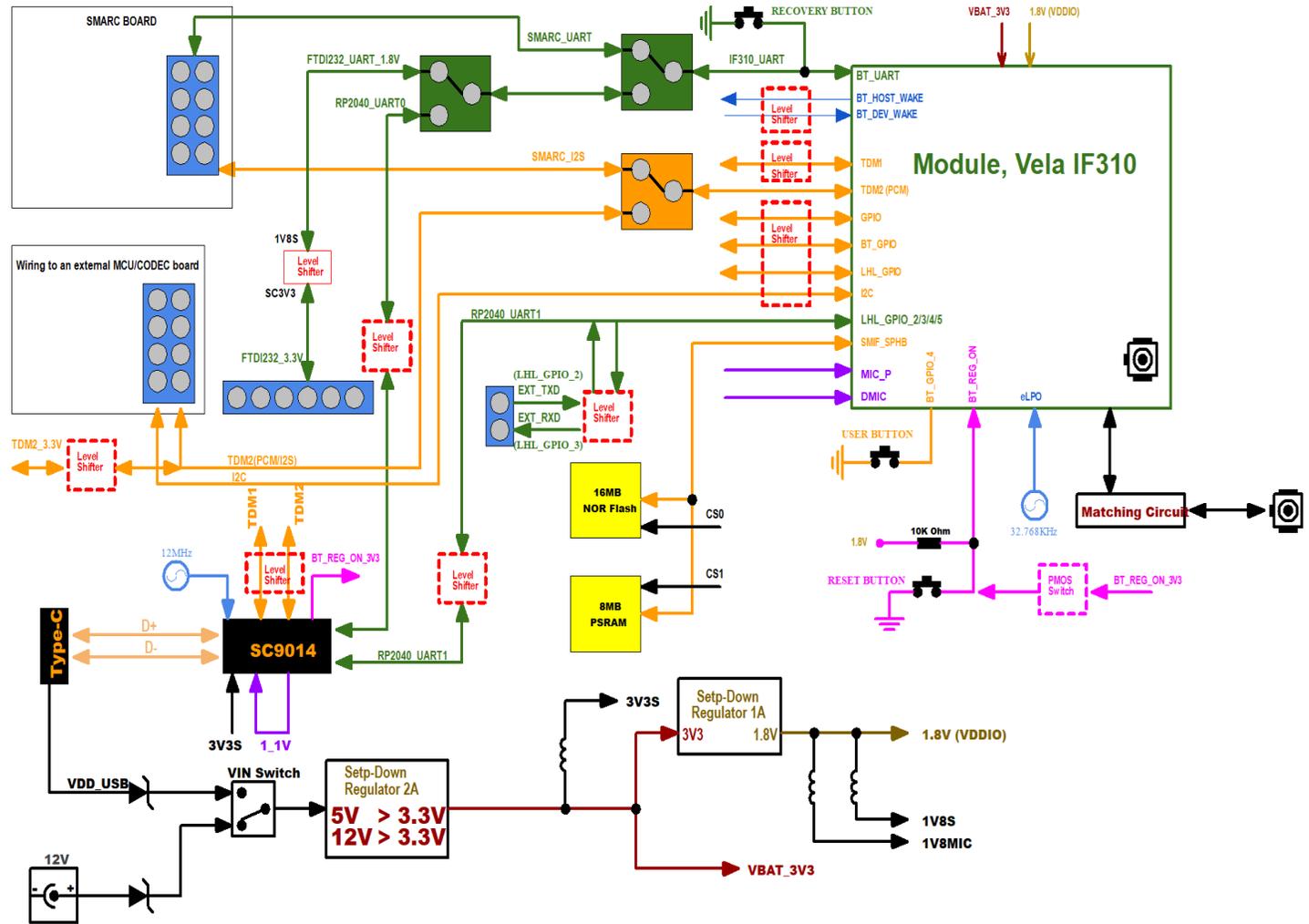


Figure 4: Vela IF310 development board block diagram

5.3 Connectors, Switches, Push buttons, and Headers

Table 1: Configuration switches and jumpers

Connector / Switch / Push button / Header	Descriptions
CON1	External DC 12V/1A input port, with a 2.1 mm PHY diameter.
J3	<ul style="list-style-type: none"> DC 5V input via the Type-C port. RP2040 and Vela IF310 module Communication Interface. Programming RP2040 port.
S1	The board power supply options- DC 12V(CON1) or Type-C 5V(J3).
J1	Current measurement header for Vela IF310 module (3.3V).
J2	Current measurement header for Vela IF310 module (1.8V).
S18	On/Off Control Switch for the RP2040 UART0 bus Level Translator(3.3V < >1.8V).
S19	On/Off Control Switch for the RP2040 UART1 bus Level Translator(3.3V < >1.8V).
J26	On/Off Control for RP2040 TDM1 bus level translator(3.3V < >1.8V).
S16	Controlling the RP2040 TDM1 signals direction (WS, SCK, DI, DO).
J27	On/Off Control for RP2040 TDM2 bus level translator(3.3V < >1.8V).
S17	Controlling the RP2040 TDM2 signals direction (WS, SCK, DI, DO).
J9	External TDM1 bus input header (pitch 2.54 mm), operating at a 3.3V voltage level (WS, SCK, DI, DO, MCK).
J35	On/Off Control for External TDM1 bus level translator(3.3V < >1.8V) (WS, SCK, DI, DO).
S9	Controlling the external TDM1 signals direction (WS, SCK, DI, DO).
J33	External TDM1 bus input header (pitch 2.54 mm), operating at a 1.8V level (WS, SCK, DI, DO).
J17	External TDM2 bus input header (pitch 2.54 mm), operating at a 3.3V level (WS, SCK, DI, DO, MCK).
J43	On/Off Control for External TDM2 bus level translator(3.3V < >1.8V) (WS, SCK, DI, DO).
S13	Controlling the external TDM2 signals direction (WS, SCK, DI, DO).
J41	External TDM2 bus input header (pitch 2.54 mm), operating at a 1.8V level (WS, SCK, DI, DO).
J29	On/Off Control for External TDM1_MCK and TDM2_MCK signals level translator(3.3V < >1.8V).
S7	Controlling the external TDM1_MCK and TDM2_MCK signals direction.
J28	External TDM1_MCK and TDM2_MCK signals input header (pitch 2.54 mm), operating at a 1.8V level.
S10	TDM1 signal source selection- External TDM (J9 or J33) or RP2040.
S14	TDM2 signal source selection- External TDM (J17 or J41) or RP2040.
J14	Ezurio's SMARC board UART bus and I ² S bus header.
J16	External FTDI cable header (3.3V).
S15	On/Off Control Switch for external FTDI bus level translator(3.3V < >1.8V).
J32	External FTDI cable header (1.8V).
S12	Select the UART bus source for controlling the IF310 module - external FTDI cable or RP2040.

Connector / Switch / Push button / Header	Descriptions
S11	I ² S signal and UART controlling source- <ul style="list-style-type: none"> From Ezurio's SMARC board- UART and I²S. From DVK-IF310 board- UART (Determined by the S12) and external TDM2 signal (J17 or J41).
J24	BT_REG_ON signal input from an external source.
J13	On/Off control for the level translator (3.3V < > 1.8V) of external BT_REG_ON signal (J24).
S2	Reset button for Vela IF310 module.
S4	Button for user interaction with Vela IF310 module.
S3	Recovery button, ensure user can program the Vela IF310 module over the HCI UART.
S6	Debug reset button for the RP2040.
S5	Debug BOOTSEL button for firmware programming to the RP2040.
J8	TAG connector (TC2030) for programming the RP2040, default not fitted.
J19	<ul style="list-style-type: none"> External WAKEUP signals In/Out header (pitch 2.54 mm), operating at a 3.3V voltage level (BT_DEV_WAKE and BT_HOST_WAKE). LHL_GPIO_2 and LHL_GPIO_3 signals In/Out header (pitch 2.54 mm), operating at a 3.3V voltage level.
J21	On/Off Control for all BT_DEV_WAKE, BT_HOST_WAKE, LHL_GPIO_2, and LHL_GPIO_3 signals level translator(3.3V < > 1.8V).
J20	External signals header, operating at a 1.8V voltage level (BT_DEV_WAKE, BT_HOST_WAKE, LHL_GPIO_2, and LHL_GPIO_3).
J6	RP2040 UART1 bus header (pitch 2.54 mm)
S20	On/Off Control Switch for the Level Translator (3.3V < > 1.8V) of the RP2040's BT_DEV_WAKE and BT_HOST_WAKE Signals.
J31	Select the BT_DEV_WAKE and BT_HOST_WAKE source- External (J19) or RP2040.
J5	GPIO_0, 2~6 header (pitch 2.54 mm), operating at a 3.3V voltage level.
J7	On/Off control for the level translator (3.3V < > 1.8V) of GPIO_0, 2~6.
J10	GPIO_0, 2~6 header (pitch 2.54 mm), operating at a 1.8V voltage level.
J15	BT_GPIO_2~7 header (pitch 2.54 mm), operating at a 3.3V voltage level.
J30	On/Off control for the level translator (3.3V < > 1.8V) of BT_GPIO_2~7.
J18	GPIO_2~7 header (pitch 2.54 mm), operating at a 1.8V voltage level.
S8	I ² C bus pull-up resistor to enable switch (When BT_GPIO_6 and BT_GPIO_7 are used as the I ² C bus, each of these two signals must have a pull-up resistor, operating at the 1.8V level.
J22	BT_GPIO_0, 16~17 and LHL_GPIO_6, 8~9 header (pitch 2.54 mm), operating at a 3.3V voltage level.
J38	On/Off control for the level translator (3.3V < > 1.8V) of BT_GPIO_0, 16~17 and LHL_GPIO_6, 8~9.
J23	BT_GPIO_0, 16~17 and LHL_GPIO_6, 8~9 header (pitch 2.54 mm), operating at a 1.8V voltage level.
J25	Analog Microphone input header (pitch 2.54 mm).
J12	Digital Microphone input header (pitch 2.54 mm).
J11	Enable/Disable the external 32.768 KHz signal header.

5.4 Hardware Settings

The main purpose of this chapter is to inform the user of the development board's factory default hardware settings, pre-operation considerations, and various configuration methods.

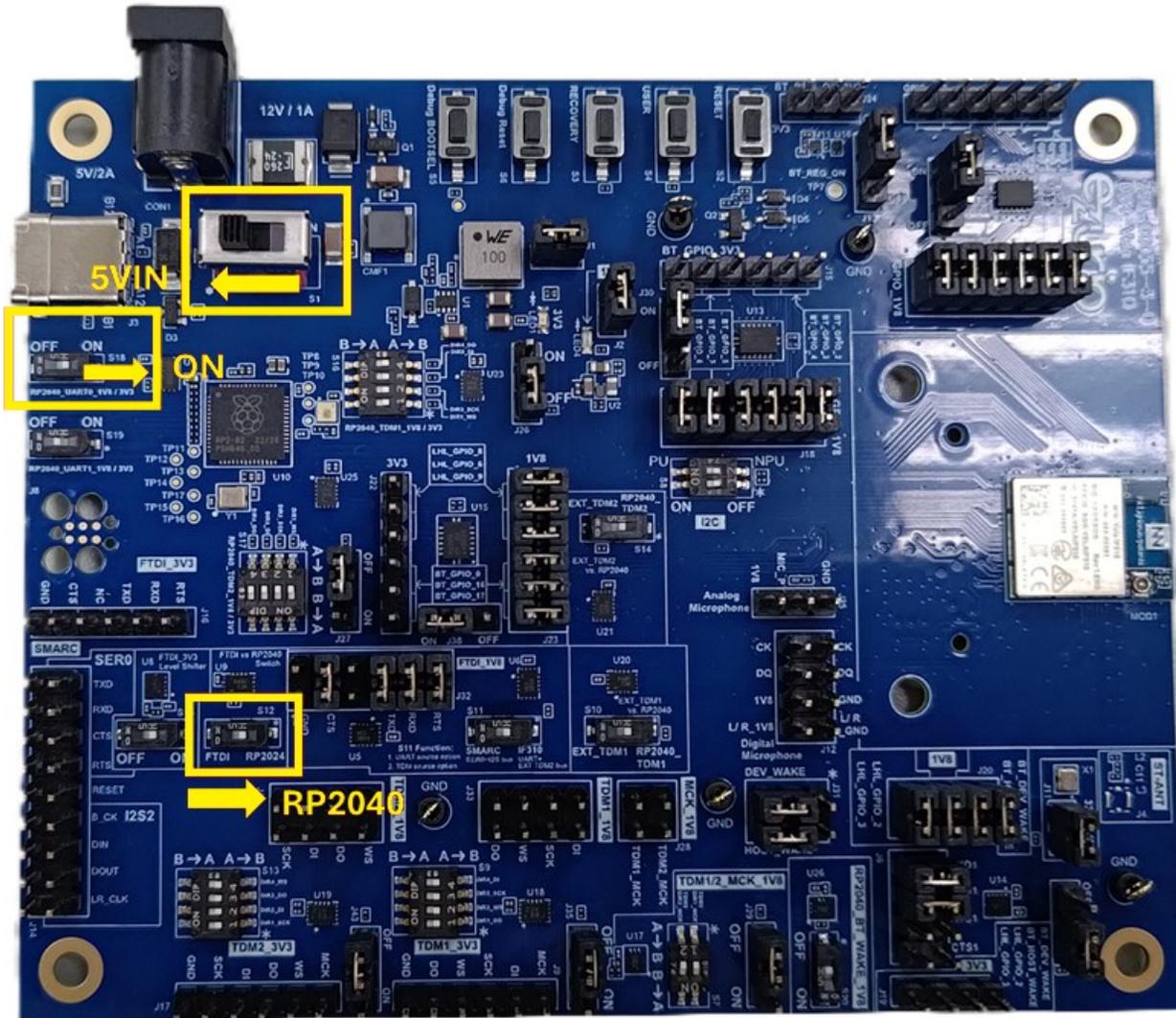


Figure 7: Default hardware settings

5.4.1 Power Supply and board control

The Vela IF310 development board supports two DC power supply methods: one via the DC power jack (CON1) and the other via the Type-C connector (J3). The user selects the DC power source using the on-board switch (S1). The selected input voltage is then converted by high-performance, high-output-current regulators into 3.3 V and 1.8 V supplies for the Vela IF310 module and other peripheral circuits, as shown in Figure 8.

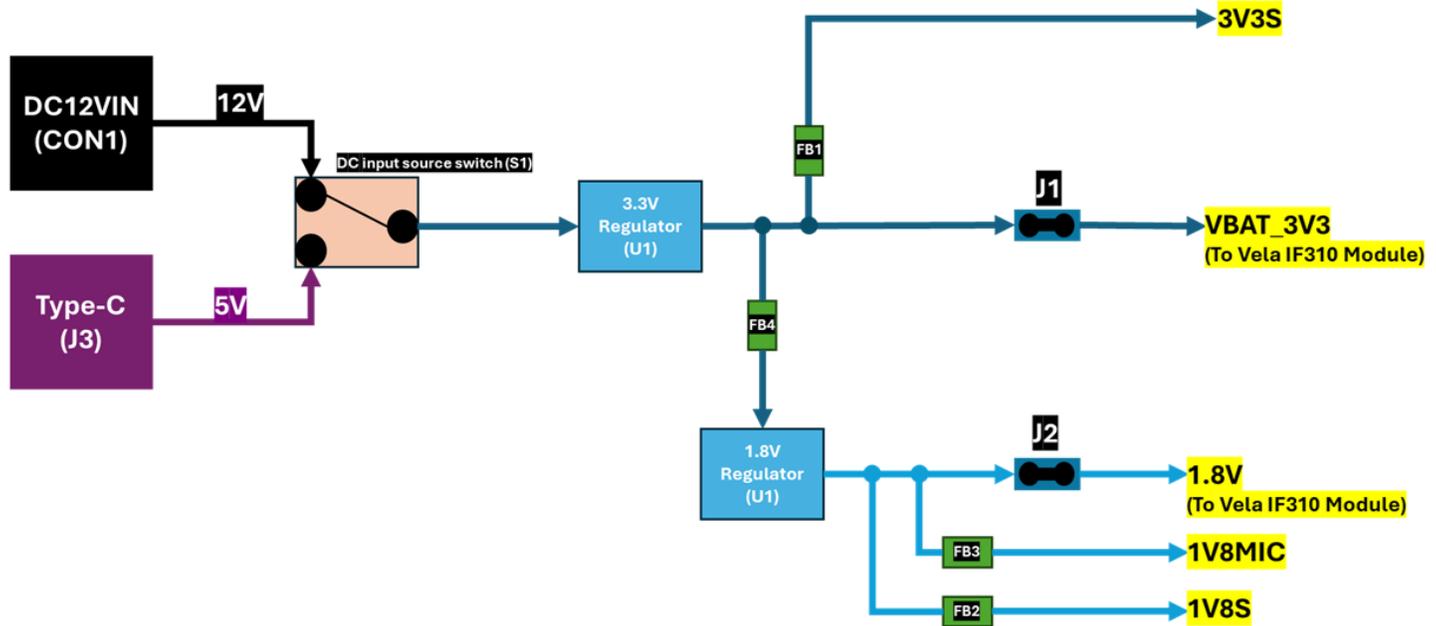


Figure 8: DC Power Supply Topology of the Vela IF310 Development Board

Access to and control of the Vela IF310 module can be achieved via the on-board Type-C connector (J3) or an external FTDI cable, with the control port source selected through a level translator and a double-pole double-throw (DPDT) switch. Another control source is the UART bus (SER0) provided on Ezurio’s SMARC board, which can directly access the Vela IF310 module through a DPDT switch, as shown below. Table 2 provides the configurations for DC power source selection and control port selection.

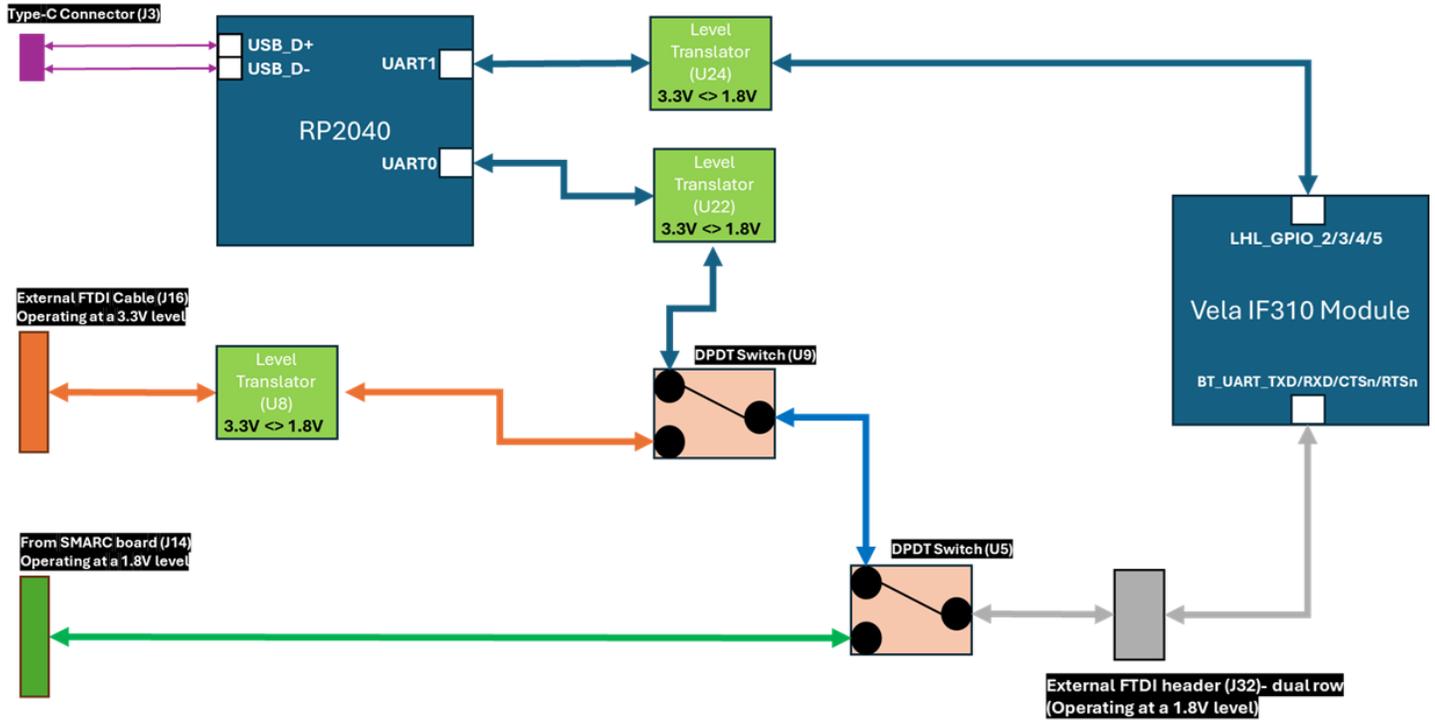


Figure 9: Control Port Topology of the Vela IF310 Development Board

Table 2: Power Supply and board Controls

DC Supply	Connector/Switch	Control Port	Descriptions
12VIN	<ul style="list-style-type: none"> Apply a 12V DC power source to the CON1 Set S1 to the "12VIN" position Set S18 to the "On" position Keep S12 at the "RP2040" position 	J3	<ul style="list-style-type: none"> Programming the RP2040 Programming the Vela IF310 Access/control the Vela IF310 module Access/control the RP2040 function
5VIN	<ul style="list-style-type: none"> Apply a Type-C cable to the J3 Set S1 to the "5VIN" position Set S18 to the "On" position Keep S12 at the "RP2040" position 	J3	
12VIN	<ul style="list-style-type: none"> Apply a 12V DC power source to the CON1 Set S1 to the "12VIN" position Ignored the S18 position Set S12 to the "FTDI" position 	<ul style="list-style-type: none"> J16^{Note 1} J32^{Note 2} 	<ul style="list-style-type: none"> Programming the Vela IF310 module Access/control the Vela IF310 module

5.4.2 External TDM1 and TDM2 bus configurations

The Vela IF310 development board provides two TDM bus interfaces, allowing users to connect to other CODEC boards. Both sets of TDM signals can have different voltage levels and signal directions selected using switches and jumpers on the development board. Please refer to [Table 2](#) for the power supply and control methods. The RP2040 itself also supports the TDM1 and TDM2 buses, and users can easily select the source of the TDM signal via the switch on the development board, as shown in [Figure 10](#).

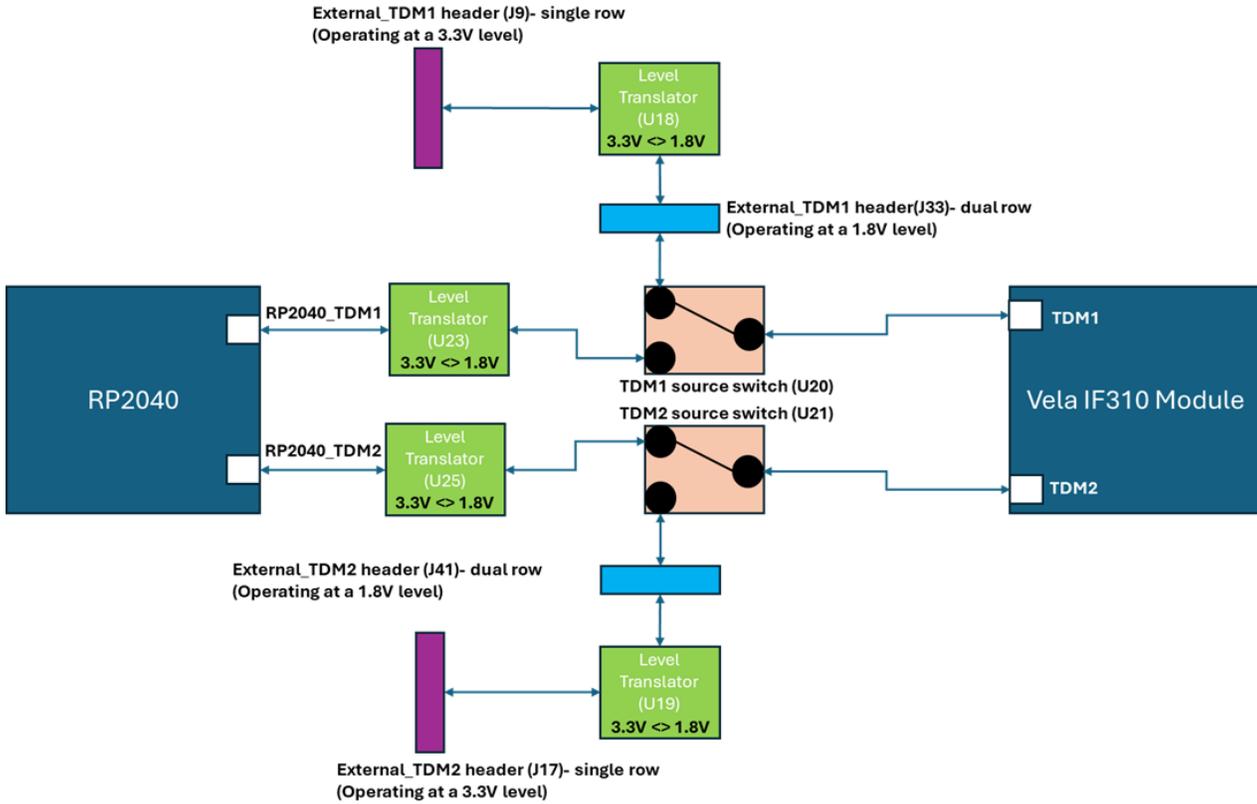


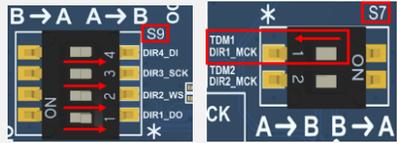
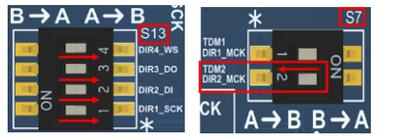
Figure 9: TDM buses options- RP2040 and External sources

Table 3 shows both TDM1 and TDM2 buses configuration through the switches and pin headers, operating at a 3.3V voltage level.

Table 4 shows both TDM1 and TDM2 buses configuration through the switches and pin headers, operating at a 1.8V voltage level.

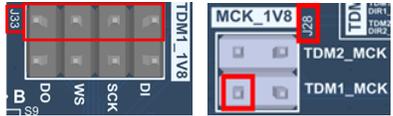
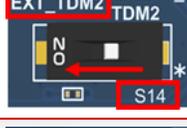
Table 3: TDM1 and TDM1 switch and pin header mapping table (Operating at a 3.3V voltage level)

Audio Bus	Signal Port	Control Port	Switch and Pin header configuration	
		J3 (Type-C)	S12- Set to the "RP2040" position.	
		J16 (External FTDI cable Note 3)	S12- Set to the "FTDI" position.	
TDM1	J9		S11- Set to the "IF310 UART+EXT TDM2 bus" position.	
		Refer to the J3 or J16 configuration	S10- Set to the "EXT_TDM1" position.	
			J35- Install the jumper cap in the "On" position. J29- Install the jumper cap in the "On" position. (For the TDM1_MCK signal)	

Audio Bus	Signal Port	Control Port	Switch and Pin header configuration
			<p>S9- When the Vela IF310 is used as a slave, the positions of WS, SCK, DI, and DO are as follows: TDM1_WS- OFF, TDM1_SCK- OFF, TDM1_DI- OFF, TDM1_DO- ON</p> <p>S7- When the Vela IF310 is used as a slave, the positions of TDM1_MCK are as follows: TDM1_MCK- OFF</p> 
			<p>J33- Install all jumper caps on the header. J28- Install a jumper cap on the "TDM1_MCK" header.</p> 
	J3 (Type-C)		<p>S12- Set to the "RP2040" position.</p> 
	J16 (External FTDI cable Note 3)		<p>S12- Set to the "FTDI" position.</p> 
TDM2	J17		<p>S11- Set to the "IF310 UART+EXT TDM2 bus" position.</p> 
	Refer to the J3 or J16 configuration		<p>S14- Set to the "TDM2" position.</p> 
			<p>J43- Install the jumper cap in the "On" position. J29- Install the jumper cap in the "On" position. (For the TDM2_MCK signal)</p> 
			<p>S13- When the Vela IF310 is used as a slave, the positions of WS, SCK, DI, and DO are as follows: TDM2_WS- OFF, TDM2_SCK- OFF, TDM2_DI- OFF, TDM2_DO- ON</p> <p>S7- When the Vela IF310 is used as a slave, the positions of TDM1_MCK are as follows: TDM2_MCK- OFF</p> 
			<p>J41- Install all jumper caps on the header. J28- Install a jumper cap on the "TDM2_MCK" header.</p> 

The Vela IF310 provides additional pin headers for TDM1 and TDM2 buses that operate at 1.8 V, eliminating the need to use the level shifters on the development board. The detailed configuration is shown in [Table 4](#).

Table 4: TDM1 and TDM2 switch and pin header mapping table (Operating at a 1.8V voltage level)

Audio Bus	Signal I/O Port	Control Port	Switch and Pin header configuration
TDM1	J33	J3 (Type-C)	<p>S12- Set to the "RP2040" position.</p> 
		J16 (External FTDI cable ^{Note 3})	<p>S12- Set to the "FTDI" position.</p> 
		Refer to the J3 or J16 configuration	<p>S11- Set to the "IF310 UART+EXT TDM2 bus" position.</p> 
			<p>S10- Set to the "EXT_TDM1" position.</p> 
<p>J33- The external TDM1 bus connection includes TDM1_DI, TDM1_SCK, TDM1_WS, and TDM1_DO.</p> <p>J28- The external TDM1_MCK signal connection.</p> 			
TDM2	J41	J3 (Type-C)	<p>S12- Set to the "RP2040" position.</p> 
		J16 (External FTDI cable ^{Note 3})	<p>S12- Set to the "FTDI" position.</p> 
		Refer to the J3 or J16 configuration	<p>S11- Set to the "IF310 UART+EXT TDM2 bus" position.</p> 
			<p>S14- Set to the "EXT_TDM2" position.</p> 
<p>J41- The external TDM2 bus connection includes TDM2_DI, TDM2_SCK, TDM2_WS, and TDM2_DO.</p> <p>J28- External TDM2_MCK signal connection.</p> 			

5.4.3 RP2040 TDM1 and TDM2 bus configuration

As shown in Figure 10, the RP2040 on the Vela IF310 development board also provides two sets of TDM buses, allowing users to select the source of audio signals. The TDM buses from RP2040 pass through level translators to ensure that the RP2040 and the Vela IF310 operate at the same voltage level. Table 5 lists the direction DIP switches and level translator ON/OFF pin headers for the RP2040 TDM1 and TDM2 bus signals. This table allows users to easily understand and control the direction and switching of these two buses originating from the RP2040 chip. Table 6 lists the corresponding configuration options.

Table 5: Direction Control and Level Translator ON/OFF for RP2040 TDM1 and TDM2 Buses

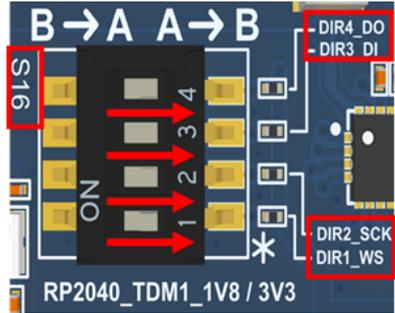
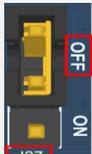
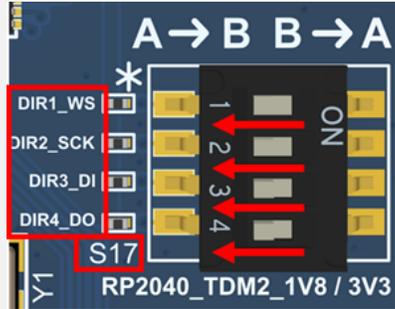
Audio Bus	Level Translator	Pin Header	Direction Switch
RP2040_TDM1	U23	<p>J26- OFF (Default mode) The level translator is disabled.</p>  <p>J26- ON The level translator is working.</p> 	<p>S16- OFF (Default mode) WS, SCK, DI and DO are all driven by the RP2040.</p> 
RP2040_TDM2	U25	<p>J27- OFF (Default mode) The level translator is disabled.</p>  <p>J27- ON The level translator is working.</p> 	<p>S17- OFF (Default mode) WS, SCK, DI and DO are all driven by the RP2040.</p> 

Table 6: From RP2040 TDM buses configuration

Audio Bus	Control Port	Switch configuration
RP2040_TDM1	J3 (Type-C)	<p>S12- Set to the "RP2040" position.</p> 
		<p>S11- Set to the "IF310 UART+EXT TDM2 bus" position.</p> 

Audio Bus	Control Port	Switch configuration
		S10- Set to the "RP2040_TDM1" position.
RP2040_TDM2	J3 (Type-C)	S12- Set to the "RP2040" position.
		S11- Set to the "IF310 UART+EXT TDM2 bus" position.
		S14- Set to the "RP2040_TDM2" position.

5.4.4 SMARC board

Ezurio offers a variety of SOM boards along with a dedicated SMARC carrier board. This carrier board includes a built-in CODEC circuit and brings the I²S bus out to a pin header, allowing users to connect it to the reserved SMARC interface on the Vela IF310 development board via jumper wires. In addition, the SMARC interface on the Vela IF310 development board also provides a UART bus for communication with the SMARC modules.

Please contact Ezurio's sales and FAE to further discuss which SMARC SOM best meets your requirements. [Figure 10](#)[figure 11](#) shows the connection between the audio signals from the SMARC board and the TDM2 signals of the Vela IF310 module and [Table 7](#) details the configuration of the switches and pin header for the SMARC board when utilized with the Vela IF310 development board.

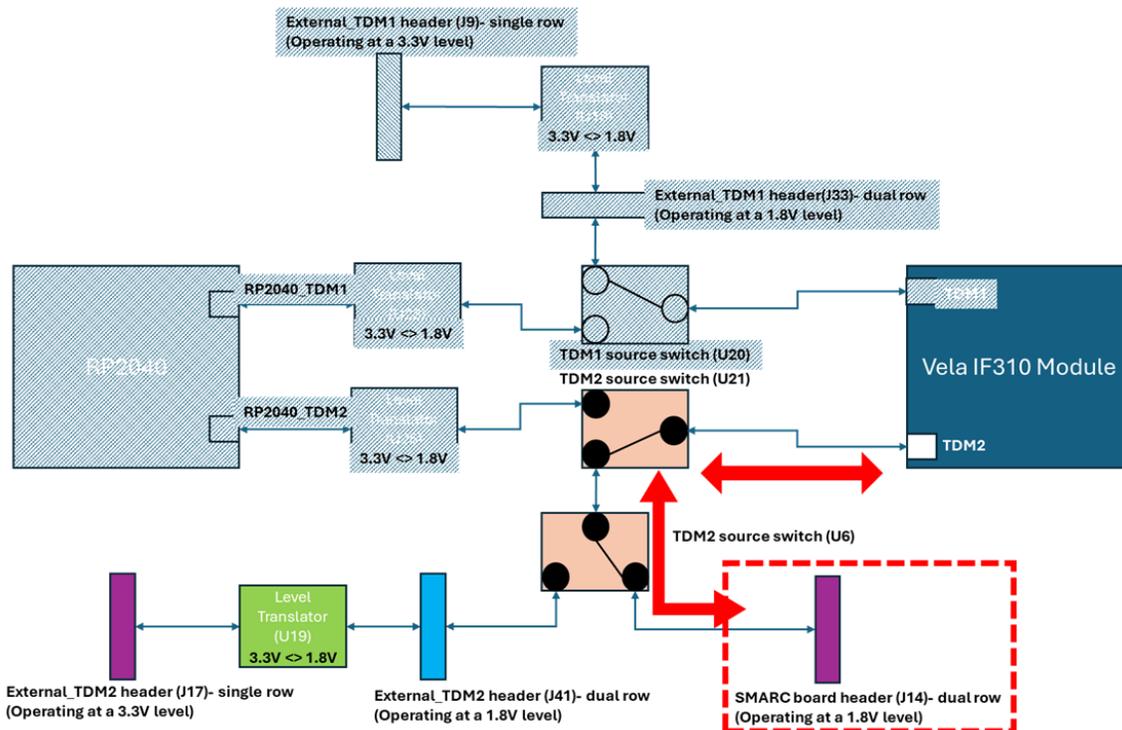


Figure 101: The audio signals come from the SMARC board

Table 7: Vela IF310 development board configuration matches that of the SMARC board used

Audio Bus	Control Port	Switch and Pin header configuration
I ² S	J14 (Pin Header)	<p>J14-</p> <p>SER0: Controls the Vela IF310 module.</p> <p>I²S2: The audio signal is transmitted through this port.</p> <p>Reset: Reset the Vela IF310 module.</p>
		<p>S11- Set to the "SMARC SER0+I2S bus bus" position.</p>
		<p>S14- Set to the "EXT_TDM2" position.</p>

5.4.5 GPIO configurations

The Vela IF310 development board provides ample GPIO ports. Each set of GPIO ports features **2.54 mm-pitch headers**, allowing users to easily connect to other application boards. In addition, each set of GPIO ports includes headers for both **3.3V and 1.8V logic levels**, with level translators integrated into each GPIO circuit. **Figure 12** illustrates the placement of all GPIO circuits on the development board and **Table 7** details the configuration of these pin headers.

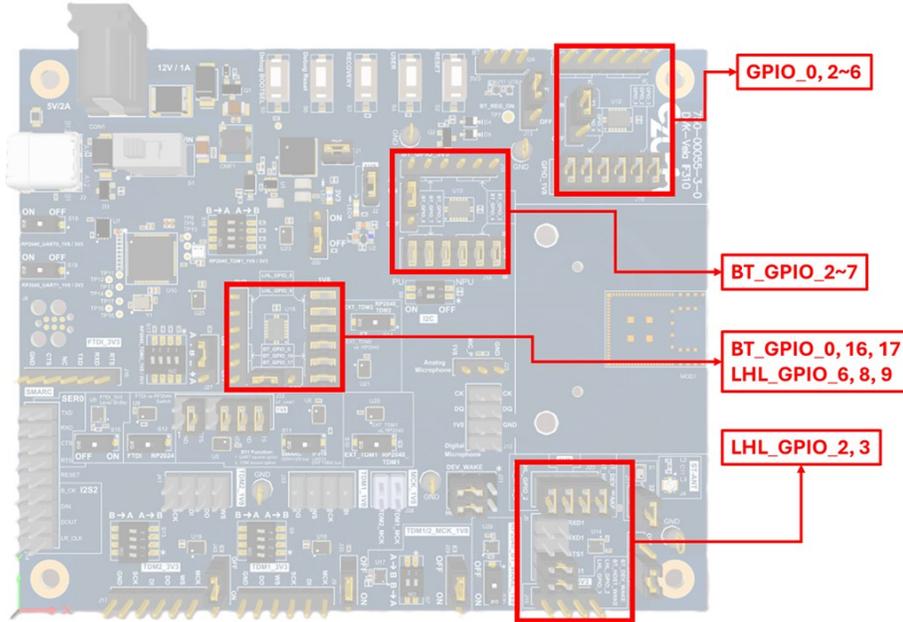
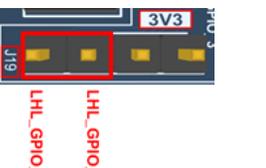
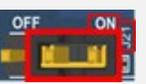


Figure 11: The position of each set of GPIO ports on the Vela IF310 development board

Table 8: Each GPIO ports configuration

GPIO Port	GPIO_0	BT_GPIO_2	BT_GPIO_0	LHL_GPIO_2
	GPIO_2	BT_GPIO_3	BT_GPIO_16	LHL_GPIO_3
	GPIO_3	BT_GPIO_4	BT_GPIO_17	
	GPIO_4	BT_GPIO_5	LHL_GPIO_6	
	GPIO_5	BT_GPIO_6	LHL_GPIO_8	
	GPIO_6	BT_GPIO_7	LHL_GPIO_9	
Operating at 3.3V	Pin Header: J5 	Pin Header: J15 	Pin Header: J22 	Pin Header: J19 
Level Translator	Default State: ON  Disable the U12: OFF 	Default State: ON  Disable the U13: OFF 	Default State: ON  Disable the U15: OFF 	Default State: ON  Disable the U14: OFF 

GPIO Port	GPIO_0	BT_GPIO_2	BT_GPIO_0	LHL_GPIO_2
	GPIO_2	BT_GPIO_3	BT_GPIO_16	LHL_GPIO_3
	GPIO_3	BT_GPIO_4	BT_GPIO_17	
	GPIO_4	BT_GPIO_5	LHL_GPIO_6	
	GPIO_5	BT_GPIO_6	LHL_GPIO_8	
	GPIO_6	BT_GPIO_7	LHL_GPIO_9	

Operating at 1.8V

Pin Header: J10
All jumper caps have been installed in the default state.



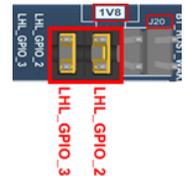
Pin Header: J18
All jumper caps have been installed in the default state.



Pin Header: J23
All jumper caps have been installed in the default state.



Pin Header: J20
All jumper caps have been installed in the default state.



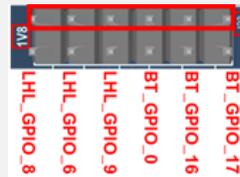
Pin Header J10:
The GPIO signals operate at a 1.8V level can be connected via the pin header shown below (red box).



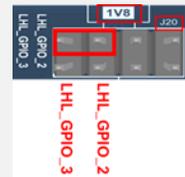
Pin Header: J18
The GPIO signals operate at a 1.8V level can be connected via the pin header shown below (red box).



Pin Header: J23
The GPIO signals operate at a 1.8V level can be connected via the pin header shown below (red box).



Pin Header: J20
The GPIO signals operate at a 1.8V level can be connected via the pin header shown below (red box).



Options

- BT_GPIO_2 to 4 can be used for the coexistence^{Note 4} function.
 - BT_GPIO_2 = BT_ACTIVE
 - BT_GPIO_3 = BT_PRIORITY
 - BT_GPIO_4 = WLAN_ACTIVE
- BT_GPIO_6 and BT_GPIO_7 can be used for I²C^{Note 4} bus, "S8" must be set to "ON" position.



- BT_GPIO_6 = I2C_SDA
- BT_GPIO_7 = I2C_CLK

- When both pins are configured as GPIO, all jumper caps on J6 must be removed. (They are installed by default.)



5.4.6 Microphone Input

The Vela IF310 development board provides digital and analog microphone ^{Note 4} input ports (2.54 mm pitch pin headers). Table 7 lists the circuits and pin header definitions for these two types of microphones on the development board.

Table 9: Microphone signal input configuration

Type	Circuit on the board	Pin Header (Refer to Figure 6)	Descriptions
Analog Microphone			The output of the analog microphone element is connected to pin 2 (MIC_P) of J25.
Digital Microphone			J12 supports dual microphones.

5.4.7 Wake-Up Signals

The Vela IF310 development board provides two wake-up signal interfaces: one from the RP2040 and the other via an external pin header, as shown in Figure 13. Both interfaces utilize level translators to convert the wake-up signals to 1.8V. Table 8 describes the selection methods for the wake-up signal source.

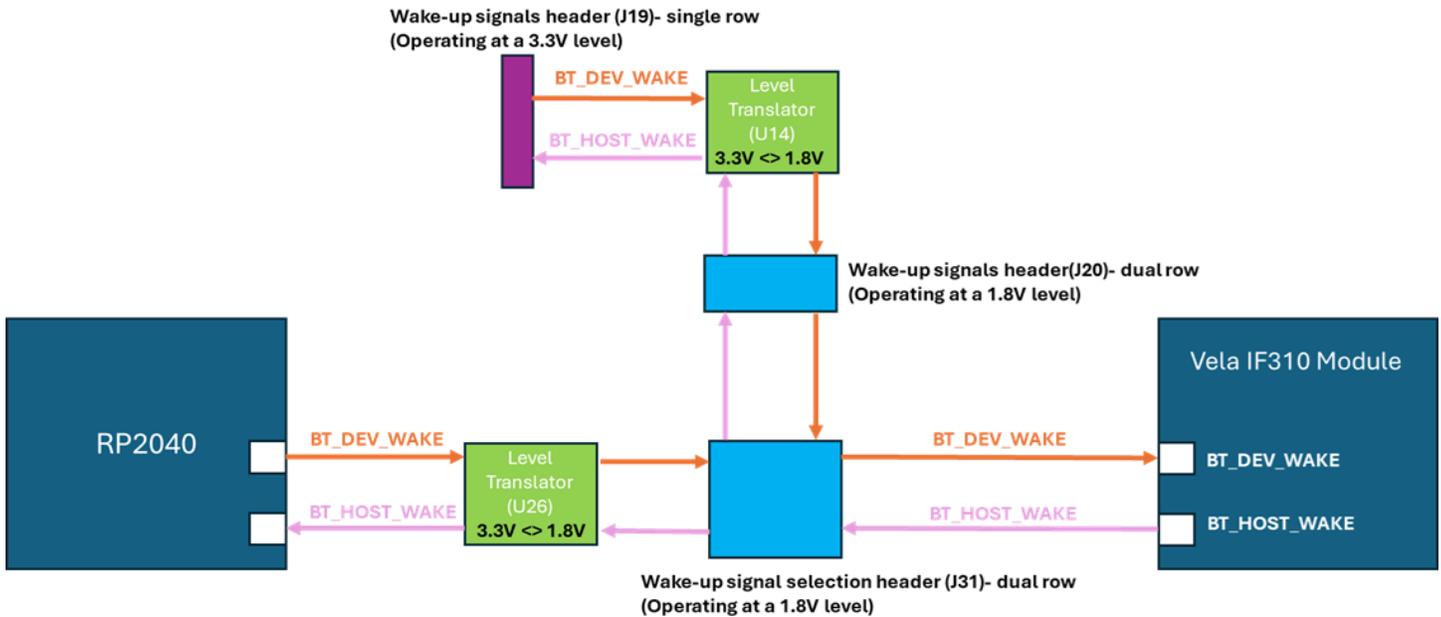
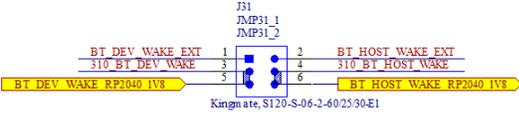
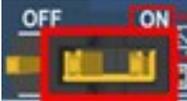
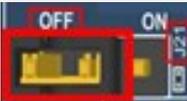
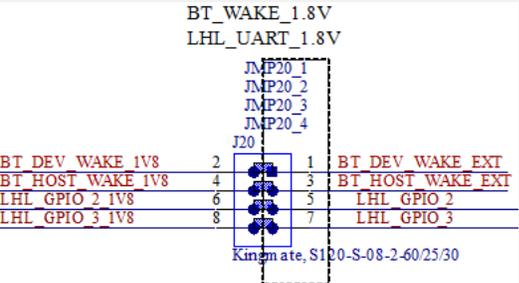
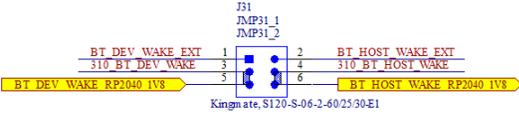


Figure 12: The Vela IF310 development board Wake-up signals source

Table 10: Wake-up signals selection configurations

Wake-up signal source	Level Translator (U26) ON/OFF	Circuit on the board	Pin Header
RP2040	<p>Default State- OFF</p>  <p>Enable the U26- ON</p> 		<p>J31-</p> <p>Pin3, 5 for the BT_DEV_WAKE</p> <p>Pin 4, 6 for the BT_HOST_WAKE</p> 
J19 (Operating at a 3.3V level)	<p>Default State- ON</p>  <p>Disable the U14: OFF</p> 	<p>BT_WAKE_1.8V</p> <p>LHL_UART_1.8V</p> 	<p>J20- Both jumper caps have been installed in the default state.</p>  <p>J20- Both wake-up signals operate at a 1.8V level can be connected via the pin header shown below (red box).</p> 
			<p>J31-</p> <p>Pin 1, 3 for the BT_DEV_WAKE</p> <p>Pin 2, 4 for the BT_HOST_WAKE</p>

Wake-up signal source	Level Translator (U26) ON/OFF	Circuit on the board	Pin Header
			

5.4.8 BT_REG_ON Signal

The control signal, BT_REG_ON, is used to power-up the Vela IF310 module and take the section out of reset. On the Vela IF310 development board, there are four sources that can control the BT_REG_ON signal, including an external trigger switch (S2), the RP2040 (GPIO13), an external pin header (J24), and the reset signal from the SMARC board (J14). **Figure 14** shows the block diagram of the above BT_REG_ON signal control.

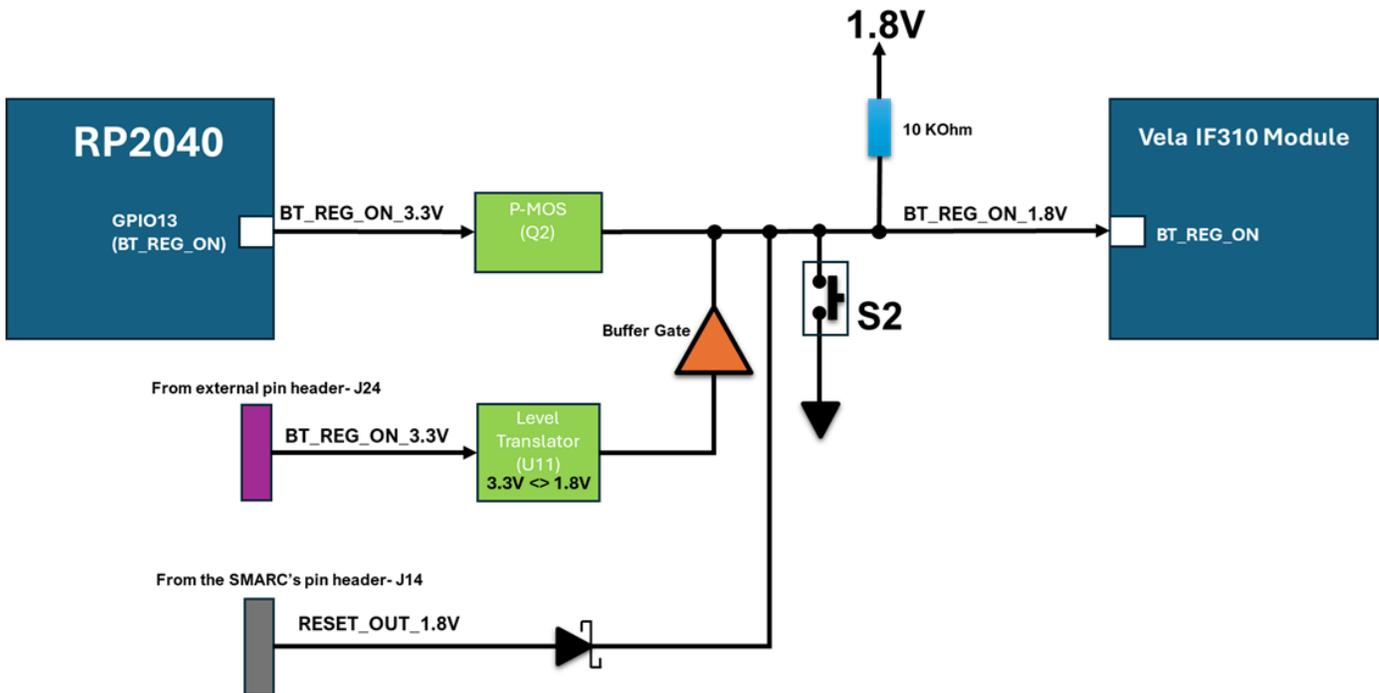
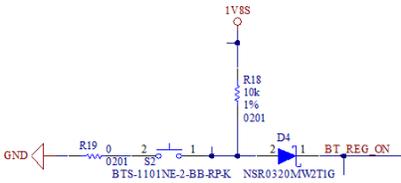
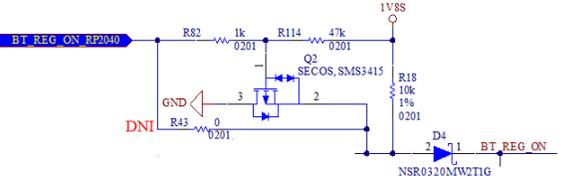
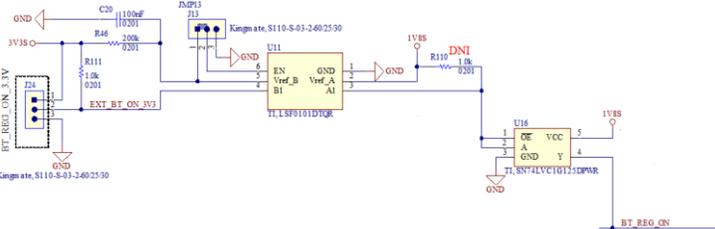
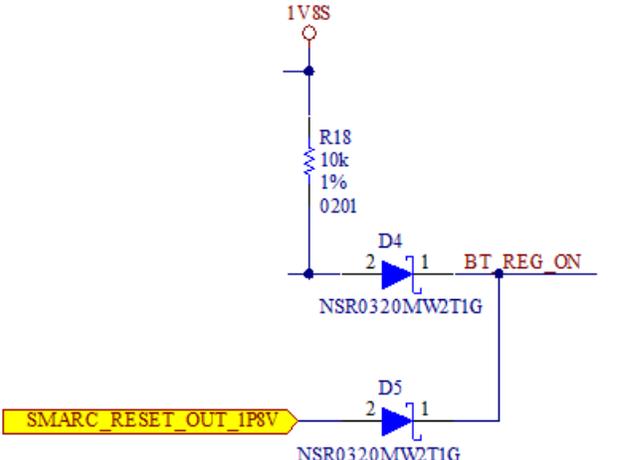


Figure 13: The BT_REG_ON sources diagram

The circuits and descriptions corresponding to these four methods of controlling the BT_REG_ON signal are listed in **Table 11**.

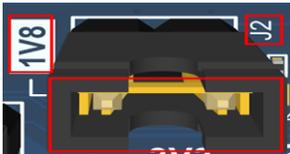
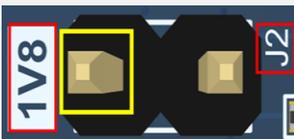
Table 11: The BT_REG_ON control sources explain

BT_REG_ON Control Sources	Circuit on the Development board	Descriptions
<p>From the toggle switch (S2)</p>		<p>S2- Open by default.</p> 
<p>From RP2040's GPIO13</p>		<p>Q2- The control signal "BT_REG_ON_RP2040" switches Q2 to reset the Vela IF310 module.</p>
<p>External control through the J24 pin header</p>		<p>J24- An external control signal can be connected to this pin header. J13- It must be kept in the ON position; otherwise, the BT_REG_ON signal cannot be controlled.</p> 
<p>From the SMARC board through the J14 pin header</p>		<p>The control signal "SMARC_RESET_OUT_1V8" come from the J14 pin header.</p> 

5.4.9 Current Measurement

The Vela IF310 module requires 3.3 V and 1.8 V power inputs. On the Vela IF310 development board, there are external pin headers providing these two power supplies, allowing the user to supply power externally and simultaneously measure the current of the Vela IF310 module. [Table 12](#) shows the locations and descriptions of these two power supplies.

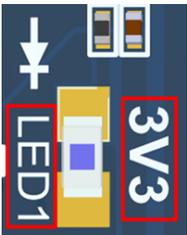
Table 12: Locations and descriptions of the 3.3 V and 1.8 V power rails

Power Rail	Locations	Descriptions
3.3V	<p>J1- The jumper cap is installed in the default mode.</p> 	The 3.3V power comes from the development board.
	<p>J1- Removed the jumper cap for an external source.</p> 	The 3.3V power comes from an external source, as shown in the yellow box in the left figure.
1.8V	<p>J2- The jumper cap is installed in the default mode.</p> 	The 1.8V power comes from the development board.
	<p>J2- Removed the jumper cap for an external source.</p> 	The 1.8V power comes from an external source, as shown in the yellow box in the left figure.

5.4.10 Indicators

To help users easily identify whether the board's power supplies are active, the Vela IF310 development board has two indicator LEDs, which show the status of the 3.3 V and 1.8 V power rails. [Table 13](#) describes the locations and functions of these two LEDs.

Table 13: Locations and functions of indicators

Power Rail	Indicators	Descriptions
3.3V	<p>LED1 (Blue color)-</p> 	When the development board provides a stable 3.3V power supply, the LED1 indicator will be solidly lit.

Power Rail	Indicators	Descriptions
1.8V	LED4 (Orange color)- 	When the development board provides a stable 1.8V power supply, the LED1 indicator will be solidly lit.

- Note 1:** An external 3.3V FTDI cable is necessary, refer to the “TTL-232R-3V3” specification.
- Note 2:** An external 1.8V FTDI cable is necessary, refer to the “TTL-232RG-VREG1V8-WE” specification.
- Note 3:** If you are using an external FTDI cable with a 1.8 V voltage level through the J32 pin header, you can ignore the position of S12.
- Note 4:** The appropriate firmware is required and is available with the ifx_flasher utility at https://github.com/Ezurio/ifx_flasher. Please contact Ezurio sales or FAE for assistance.

5.5 Miscellaneous

5.5.1 User Button

One push button is reserved for user interaction with the Vela IF310 module. It is connected to one of the Vela IF310, which maps to "BT_GPIO_4" of the CYW55310 chipset. Pressing this button pulls the pin to ground. **Figure 14** shows the location of this button on the development board.



Figure 14: The "USER" button (S4) on the development board

5.5.2 UART1

There is a second UART bus provided by the RP2040 and can also be used to access a second UART on the Vela IF310 module. This UART can be used when developing a ModusToolbox application for the IF310 module.

Table 14 lists the configuration of DVK to use the UART1 interface.

Table 14: EZ-Serial interface configurations

Circuit on the board	Configuration
<p>The diagram shows the RP2040 chip with pins A1-A4 connected to the level translator (U24). Pin OE is connected to ground through a 100k resistor (R132). A dip switch (S19) is connected between pin 1 and ground, with a 100k resistor (R132) to 1V88. The switch is labeled 'Off by default'.</p>	<p>S19- The dip switch is set to the "OFF" position by default.</p> <p>U24- The level translator is active by default.</p>
<p>The diagram shows a 4-pin header (J6) with pins 1-4 connected to LHL_GPIO_5, LHL_GPIO_4, LHL_GPIO_2, and LHL_GPIO_3 respectively. Pins 2-4 are also connected to LHL_GPIO_4 UART CTSN, LHL_GPIO_5 UART RTSN, and LHL_GPIO_2 UART TXD.</p>	<p>J6- All jumper caps need to be installed.</p>
<p>The diagram shows a 4-pin header (J20) with pins 2-4 connected to LHL_GPIO_2 1V8 and LHL_GPIO_3 1V8. Pins 6-8 are connected to LHL_GPIO_2 and LHL_GPIO_3. Jumper caps are shown being removed from pins 5-6 and 7-8.</p>	<p>J20- Jumper caps on pins 5-6 and 7-8 must be removed from the J20 pin header.</p>

5.5.3 32.768 KHz Signal

This clock signal is provided for use by the Vela IF310 module and must not be interrupted or removed; otherwise, the Vela IF310 module will stop operating. Figure 15 16 shows the location of this clock signal on the development board. "J11" supplies power to "X1"; therefore, its jumper cap must always be installed.



Figure 15: 32.768 KHz circuit

6 Firmware Update

6.1 Firmware Upgrade on the RP2040

Warning: The RP2040 on the IF310 DVK board is not meant for custom firmware development, it is the interface MCU for the development kit (USB to serial/debugger/GPIO control). Removing the existing firmware and replacing it with custom firmware is not an option, as the DVK will no longer function correctly without the intended firmware loaded to the RP2040.

6.1.1 Via Type-C connector

Firmware images for the RP2040 are available here https://github.com/Ezurio/dvk_probe

Firmware upgrade is performed over Type-C using “Debug BOOTSEL” mode, the button as shown in [Figure 17](#).



Figure 17: Debug BOOTSEL button

To enter Debug BOOTSEL mode on the RP2040 and load firmware via Type-C connector, the user needs to hold down the “Debug BOOTSEL” button and then power on the development board.

Once in “Debug BOOTSEL” mode, the user should see a USB storage device show up on their computer named “RPI-RP2”. Drag-and-drop the firmware “.uf2” file onto the storage device. The firmware will be loaded and the RP2040 will reset, as shown in [Figure 18](#).

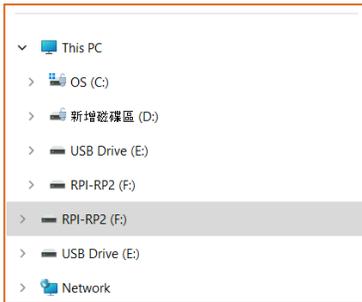


Figure 18: The “RPI-RP2” storage appears on the computer

6.1.2 Via SWD Interface

RP2040 firmware can also be upgraded via the SWD interface.

Use a Tag-Connect cable to connect to the onboard TC2030 footprint. The SWD interface can then be used to upgrade the firmware or debug the RP2040. The onboard TC2030 footprint as shown in [Figure 19](#).



Figure 19: Onboard TC2030 footprint

6.2 Firmware Download via RP2040

The Vela IF310 module requires firmware to operate properly. The firmware is in “.hcd” or “.hex” format. Users can download the firmware file into the IF310 module via the Type-C port (J3) provided on the development board. Figure 16 shows the firmware download path to the Vela IF310 module through the J3 port. The RP2040 driver is pre-programmed before shipment.

The “.hcd” firmware file is downloaded into the RAM of the main chip inside the Vela IF310 module. However, when the Vela IF310 module is power cycled, the firmware stored in RAM will be cleared, so it needs to be reloaded. In contrast, the “.hex” file is directly programmed into the external NOR Flash of the Vela IF310 module, which ensures that the firmware is not lost due to a system reset or power cycle. The choice between these two-firmware download/programming methods depends on the customer’s usage mode—Hosted or Hostless. Please refer to [Hosted Mode](#) and [Hostless Mode](#) for more details.

The ifx_flasher tool is used to download firmware over the HCI UART, and the Vela IF310 firmware is hosted within the ifx_flasher repo on Github. The tool can be obtained from here: https://github.com/Ezurio/ifx_flasher

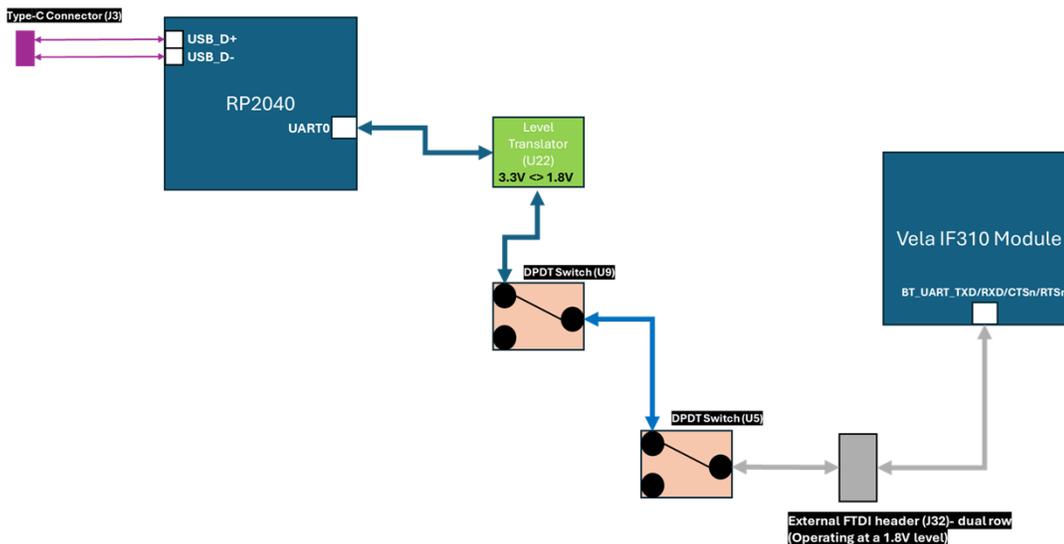


Figure 16: “.hcd” file and “.hex” file download path

Figure 17 shows the hardware configuration for downloading the “.hcd” file or “.hex” file, which is also used to access and control the Vela IF310 module through the RP2040 chip.

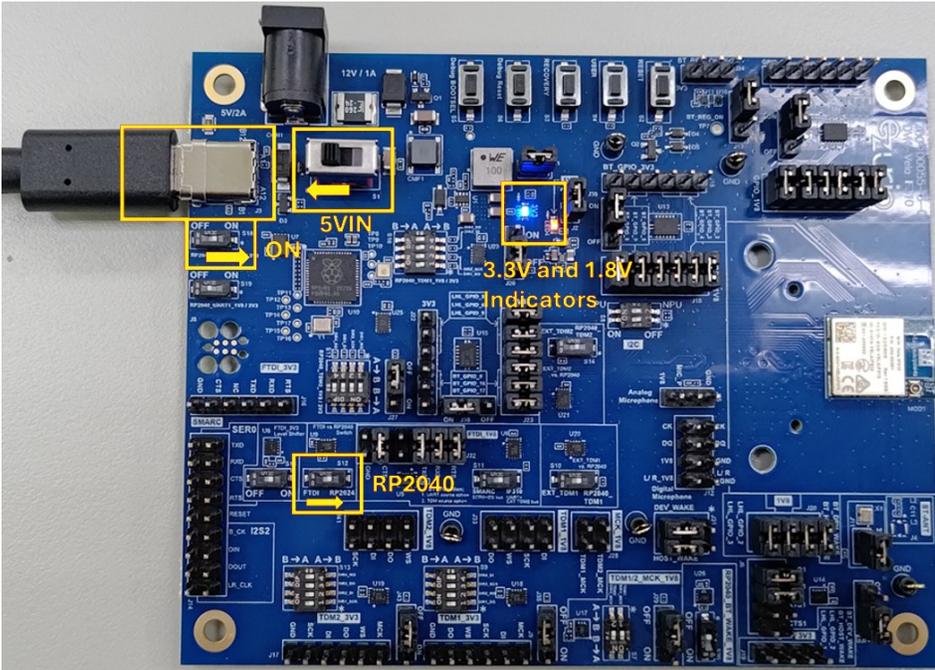


Figure 17: Hardware configuration for “.hcd” file Download and “.hex” file Program

When the DVK-IF310 board is powered via J3 (S1 position on “5VIN”), LED2 briefly flashes white (as shown in Figure 18), indicating that the RP2040 has been successfully initialized. At the same time, two virtual COM ports will appear in the Ports menu of Device Manager. The port with “MI_01” in the *Device instance path* is the valid and usable port, as shown in Figure 19.

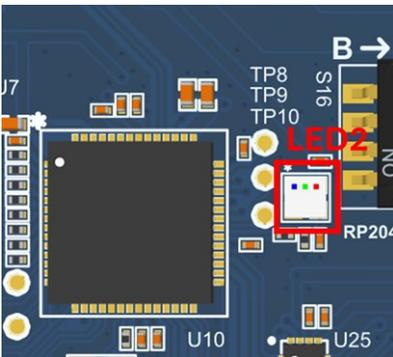


Figure 18: LED2 indicates successful RP2040 initialization



Figure 19: The virtual COM port identifies

6.2.1 HCD File Download

Place the “ifx_flasher_cli” executable, and the “.hcd” file to be programmed in the same directory, as shown in [Figure 20](#).

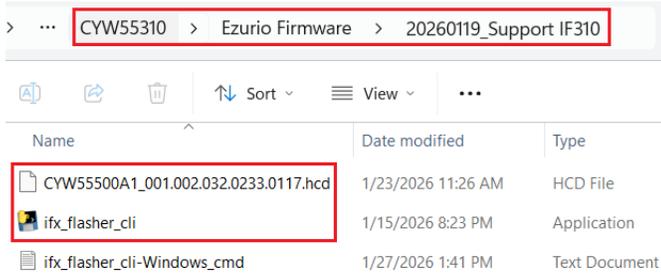


Figure 20: Place the HCD file and the programming executable in the same directory

Open a DOS window in the directory shown in [Figure 20](#), as illustrated in [Figure 21](#).

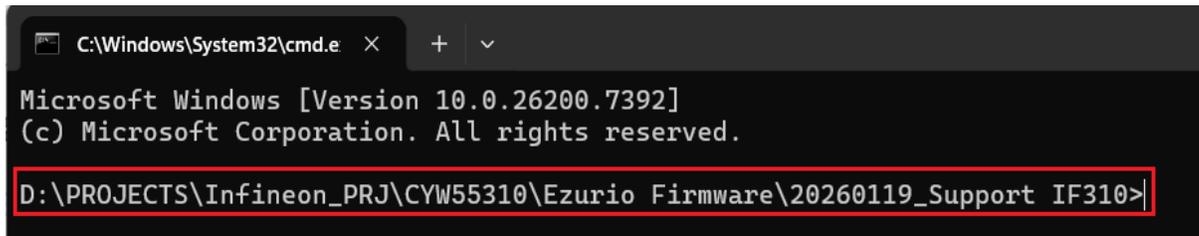


Figure 21: DOS window in the directory

Input the HCD file download script as shown in [Figure 22](#). [Figure 23](#) shows the description of the programming script.

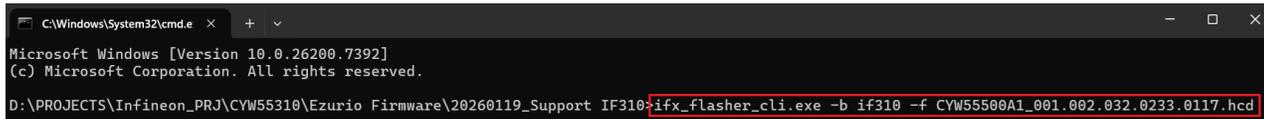


Figure 22: HCD file download script

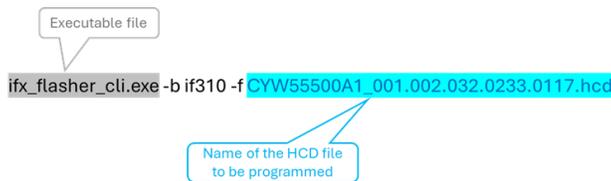


Figure 23: Description of programming script

After pressing the **Enter** key on the keyboard, the programming tool will automatically start the programming process and the system will display the “Programming HCD file...” prompt, as shown in [Figure 28](#).

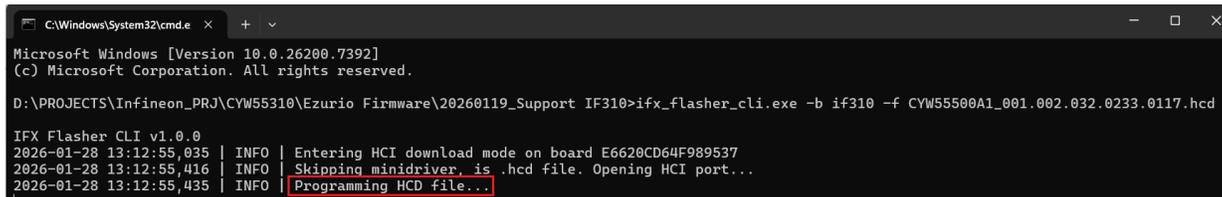


Figure 28: Programming HCD File Started

Figure 29 shows that the HCD file programming is finished.

```
C:\Windows\System32\cmd.e x + v
Microsoft Windows [Version 10.0.26200.7392]
(c) Microsoft Corporation. All rights reserved.

D:\PROJECTS\Infinion_PRJ\CYW55310\Ezurio Firmware\20260119_Support IF310>ifx_flasher_cli.exe -b if310 -f CYW55500A1_001.002.032.0233.0117.hcd

IFX Flasher CLI v1.0.0
2026-01-28 13:12:55,035 | INFO | Entering HCI download mode on board E6620CD64F989537
2026-01-28 13:12:55,416 | INFO | Skipping minidriver, is .hcd file. Opening HCI port...
2026-01-28 13:12:55,435 | INFO | Programming HCD file...
2026-01-28 13:13:14,725 | INFO | Finished programming!
```

Figure 29: HCD File Programmed

6.2.1.1 If COM Port is Not Detected

In some cases, COM port detection with the IFX_Flasher tool may fail. If **Error / No boards found** response is received after using the IFX Flasher utility to flash the firmware, you may need to manually specify the COM port in the command.

```
rikki@rikki-Precision-M4700:~/ifx_flasher$ python3 ifx_flasher_cli.py -b if310 -f
CYW55500A1_001.002.032.0233.0117.hcd
IFX Flasher CLI v1.0.0
2026-01-26 16:21:01,171 | ERROR | No boards found
```

Use the following command, where the -c parameter is used to manually specify the COM port:

ifx_flasher\$ python ifx_flasher_cli.py -b if310 -c /dev/ttyACM0 -f [FilePath/Name]

```
rikki@rikki-Precision-M4700:~/ifx_flasher$ python ifx_flasher_cli.py -b if310 -c /dev/ttyACM0 -f
CYW55500A1_001.002.032.0233.0117.hcd
IFX Flasher CLI v1.0.0
Ensure the board is in HCI download mode and press enter to continue...
```

If prompted to “Ensure the board is in HCI download mode”, then hold down the “Module Reset” and “Module RECOVERY” buttons at the same time. Then release the “Module Reset” button so the device boots, while still holding down Module RECOVERY button. After one second release the “Module RECOVERY” button. The device will now be in HCI download mode, press Enter in the command window to continue the installation process.

The Module Reset and Module Recovery buttons are on the edge of the board as highlighted below.



```
rikki@rikki-Precision-M4700:~/ifx_flasher$ python ifx_flasher_cli.py -b if310 -c /dev/ttyACM0 -f
CYW55500A1_001.002.032.0233.0117.hcd
IFX Flasher CLI v1.0.0
Ensure the board is in HCI download mode and press enter to continue...
2026-01-27 10:40:04,895 | INFO | Skipping minidriver, is .hcd file. Opening HCI port...
2026-01-27 10:40:04,900 | INFO | Programming HCD file...
2026-01-27 10:40:20,101 | INFO | Finished programming!
```

6.2.2 HEX File Program

Place the “ifx_flasher_cli” executable, and firmware file (“.hex” format) to be programmed in the same directory, as shown in **Figure 30**.

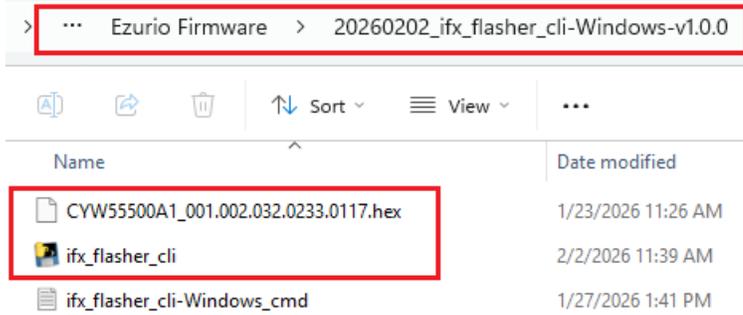


Figure 30: Place the Firmware(.hex format) and the programming executable in the same directory

Open a DOS window in the directory shown in **Figure 30**, as illustrated in **Figure 31**.

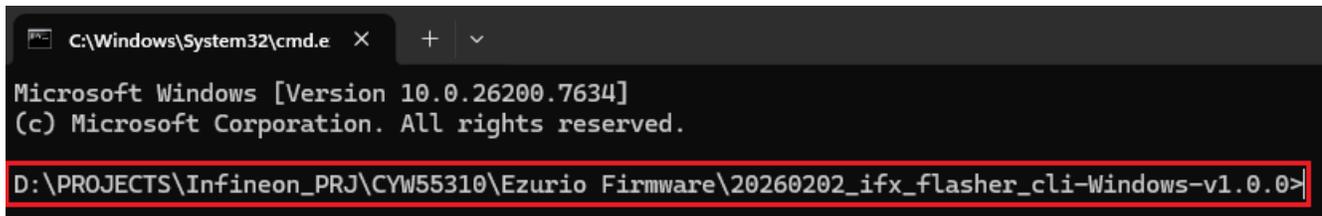


Figure 31: DOS window in the directory

Input the Firmware file(“.hex” format) download script and press the “Enter” key to start the programming, as shown in **Figure 32**. **Figure 33** shows the description of the programming script.

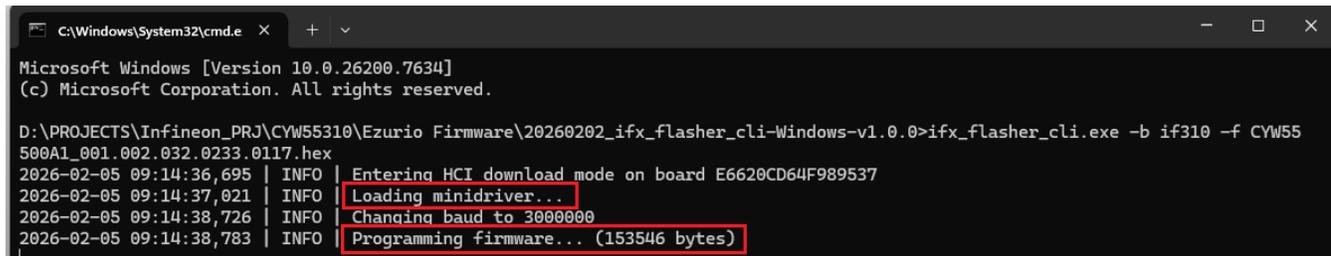


Figure 32: HEX file program script

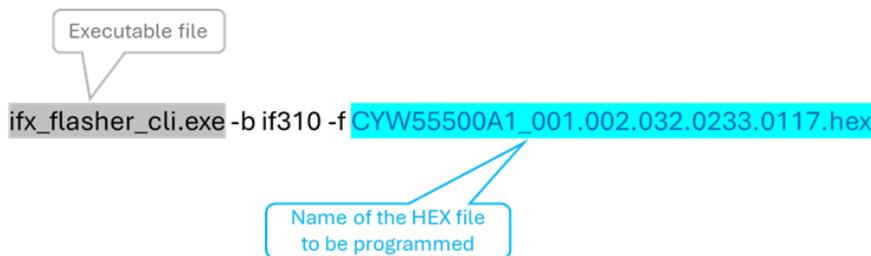


Figure 33: Description of programming script

Figure 34 shows that the HCD file programming is finished.

```

C:\Windows\System32\cmd.e  x  +  v
Microsoft Windows [Version 10.0.26200.7634]
(c) Microsoft Corporation. All rights reserved.

D:\PROJECTS\Infineon_PRJ\CYW55310\Ezurio Firmware\20260202_ifx_flasher_cli-Windows-v1.0.0>ifx_flasher_cli.exe -b if310 -f CYW55
500A1_001.002.032.0233.0117.hex
2026-02-05 09:14:36,695 | INFO | Entering HCI download mode on board E6620CD64F989537
2026-02-05 09:14:37,021 | INFO | Loading minidriver...
2026-02-05 09:14:38,726 | INFO | Changing baud to 3000000
2026-02-05 09:14:38,783 | INFO | Programming firmware... (153546 bytes)
2026-02-05 09:14:47,865 | INFO | Finished programming!
  
```

Figure 34: HEX File Programmed

Important: Please power-cycle the board before executing any commands.

7 Hosted Mode and Hostless Mode

The Vela IF310 module provides an “SMIF_SPHB” interface that allows users to connect an external NOR Flash as a storage device, since the Vela IF310 module does not have built-in storage. Therefore, the Vela IF310 module can be used in two operating modes- Hosted mode and Hostless mode.

7.1 Hosted Mode

Referring to an architecture in which the device operates under the control of an external host MPU / MCU. In this mode, the Vela IF310 firmware is stored in an external Flash connected to the MPU / MCU. Therefore, upon system power-up (or after power cycle), the firmware is loaded into the Vela IF310 module via the UART bus connecting it to the MPU / MCU.

Figure 35 illustrates a Hosted mode architecture, where the MCU acts as the host and stores the Bluetooth stack, application, and controller firmware image in external Flash. The Vela IF310 module operates as a Bluetooth controller and communicates with the host MCU via a UART (HCI) interface.

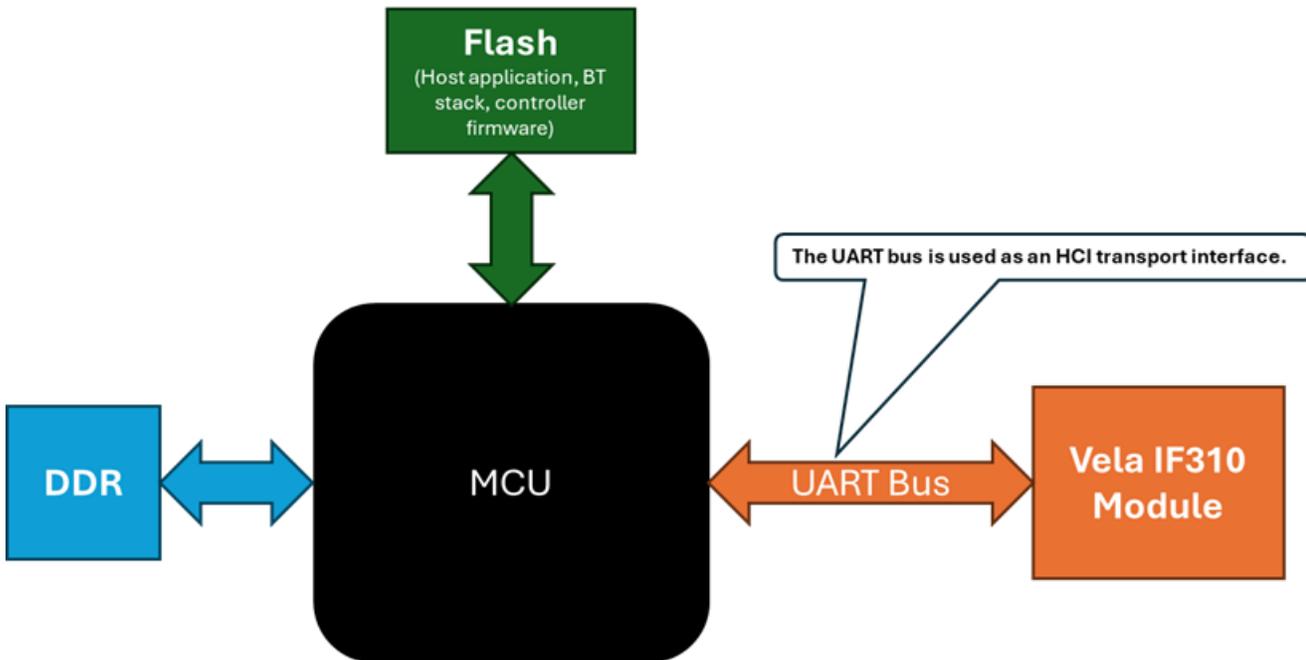


Figure 35: Vela IF310 module in Hosted mode architecture

7.2 Hostless Mode (Standalone Mode)

Referring to an operating mode in which the module functions independently without an external host processor. In this mode, an external NOR Flash is typically used as storage to hold firmware or configuration data. Hostless mode simplifies system architecture, reduces dependency on an external host, and is suitable for standalone applications. In this mode, as the firmware is programmed into the external NOR Flash, the Vela IF310 module will automatically load firmware and initialize upon every power cycle.

Figure 36 illustrates the **Hostless mode** architecture, where the Vela IF310 module operates independently, fetching the application and BT stack from the external NOR Flash via the SMIF_SPHB bus.



Figure 36: Vela IF310 module in Hostless mode architecture

8 Vela IF310 Development Board Schematic

When designing with the Vela IF310 module, customers can refer to these schematics, which include the power supply design, module peripherals, RP2040 schematics, control port switching, and level translator circuits, as shown below.

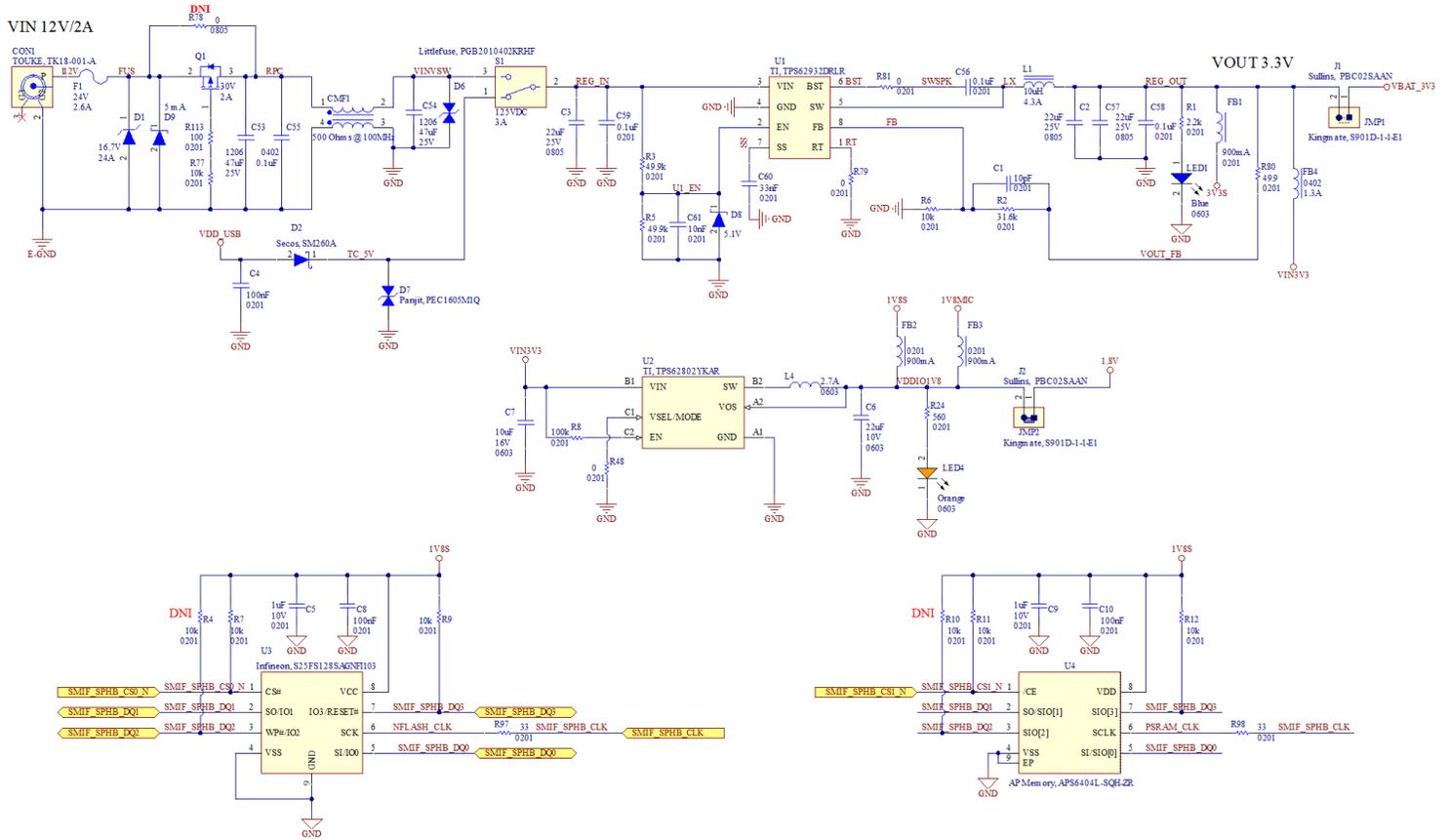


Figure 32: PMU, External NOR Flash, and External PSRAM schematic

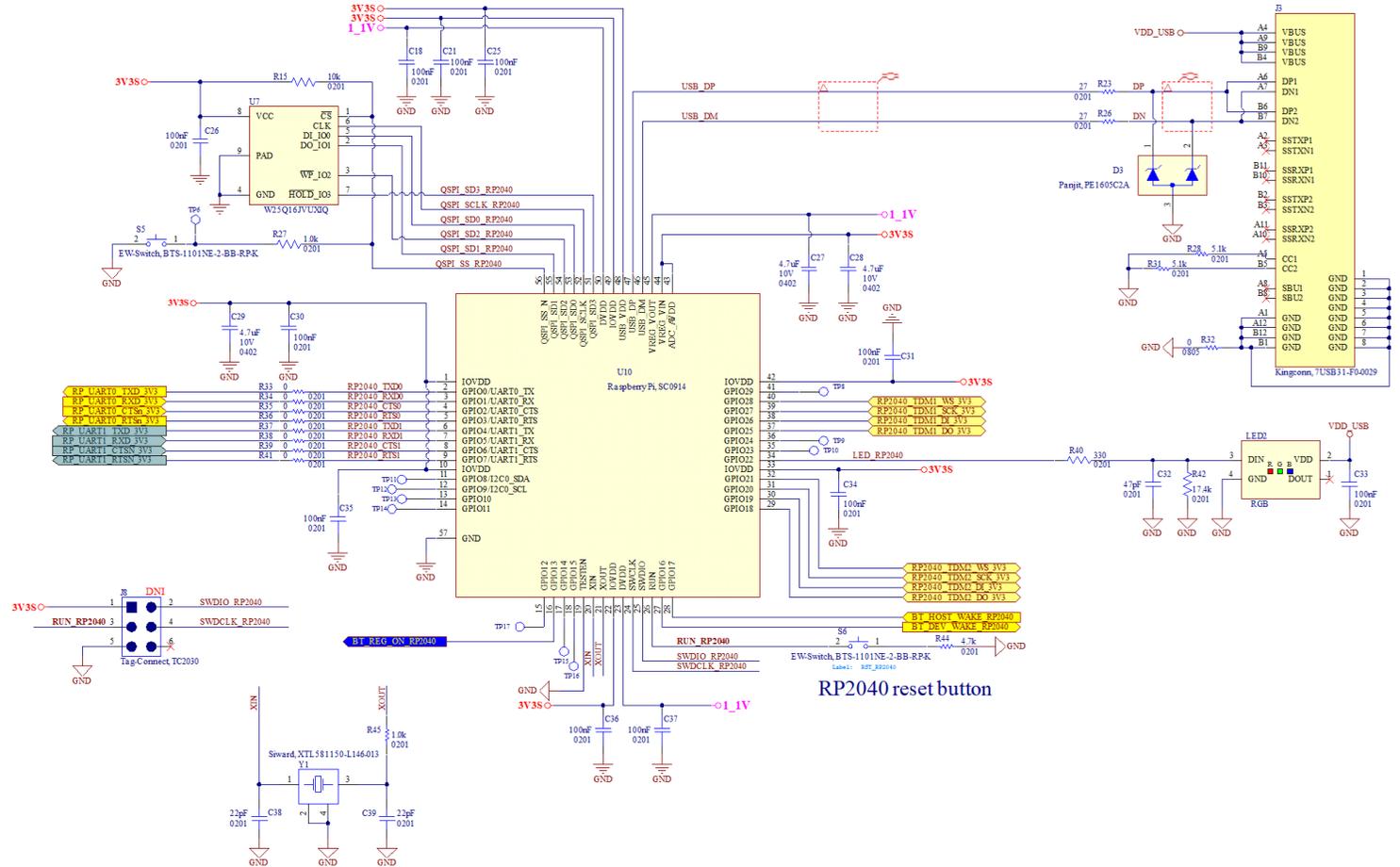


Figure 33: Type-C and RP2040 schematic

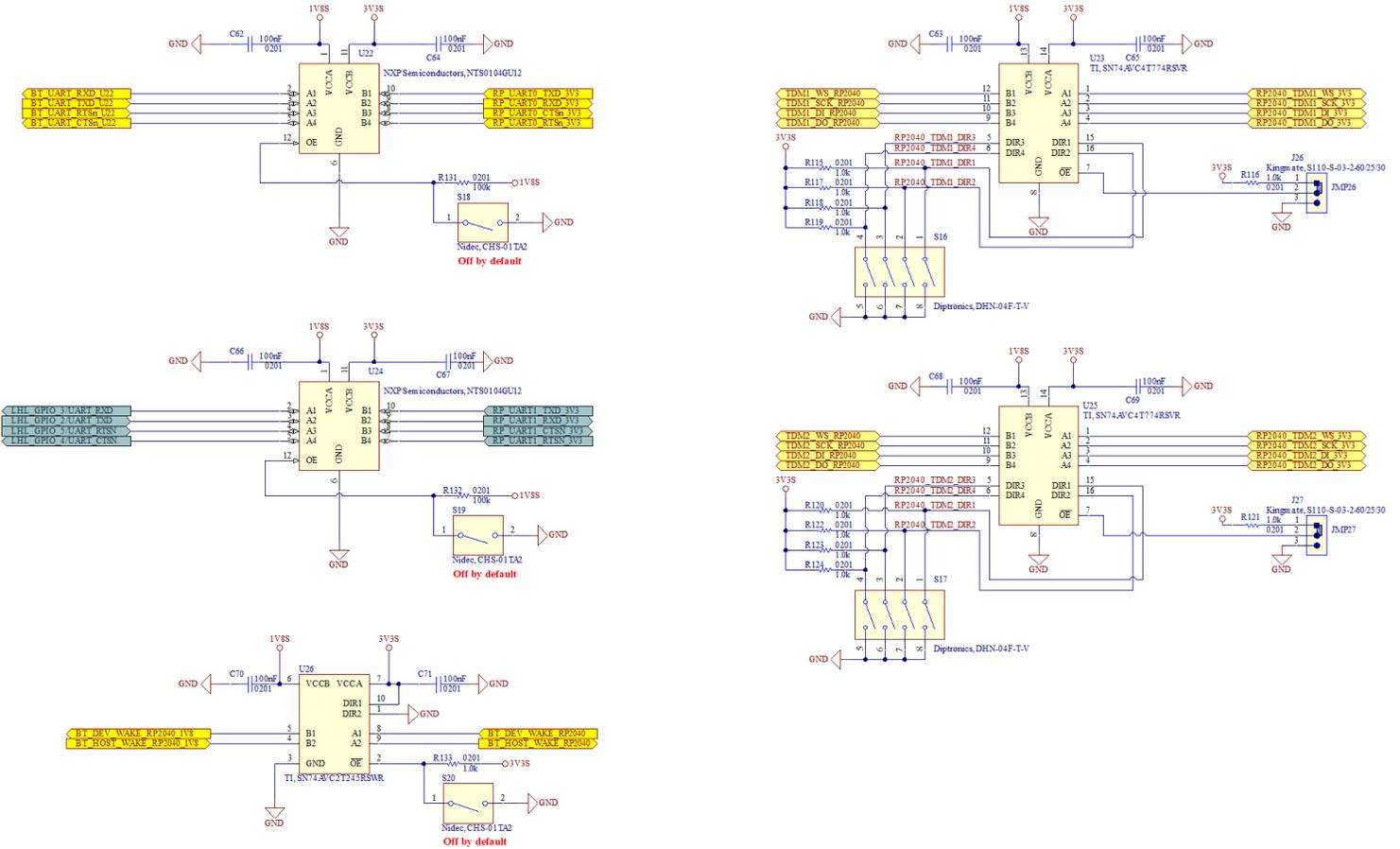


Figure 34: Level translator schematic for the RP2040

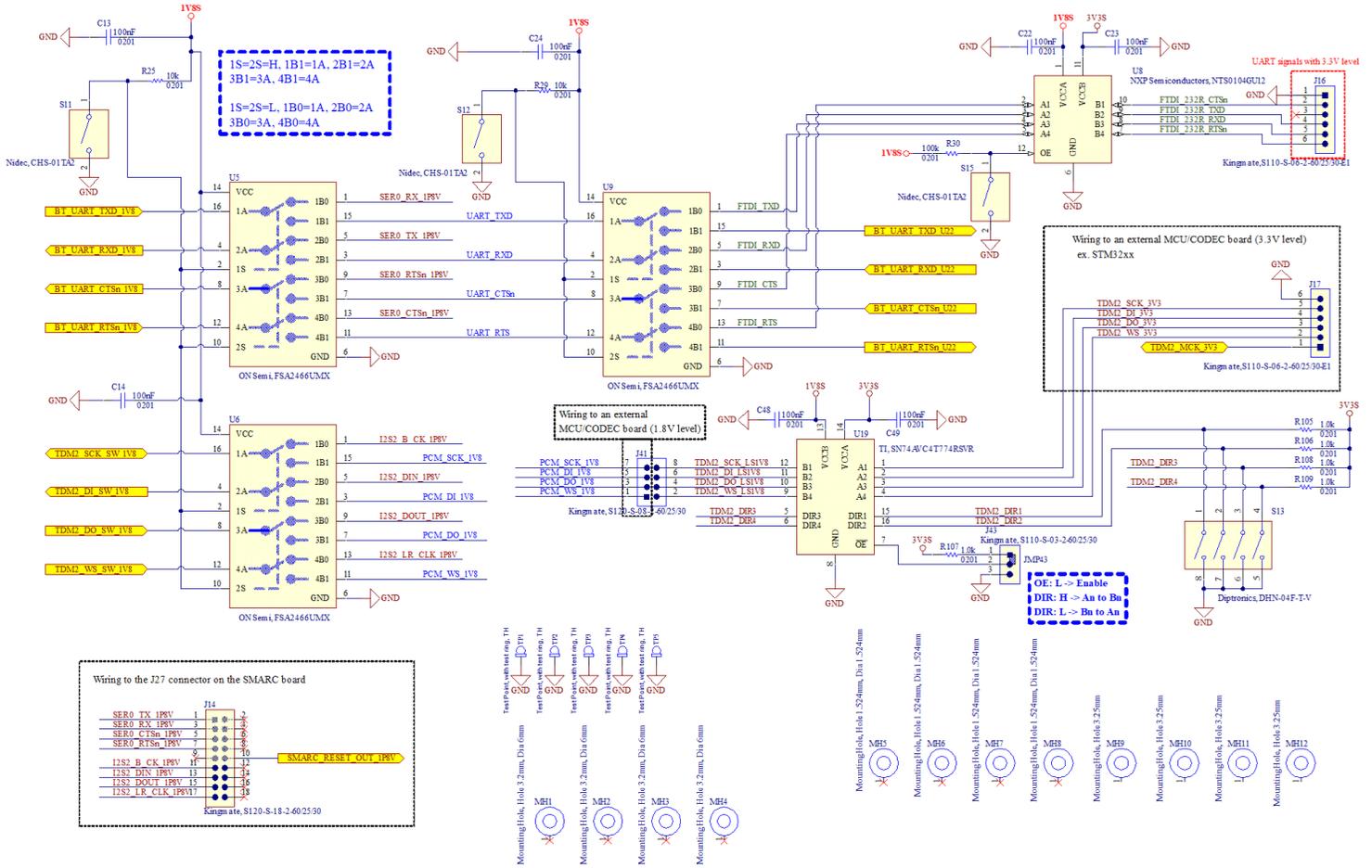


Figure 35: DPDT switches for UART and TDM buses

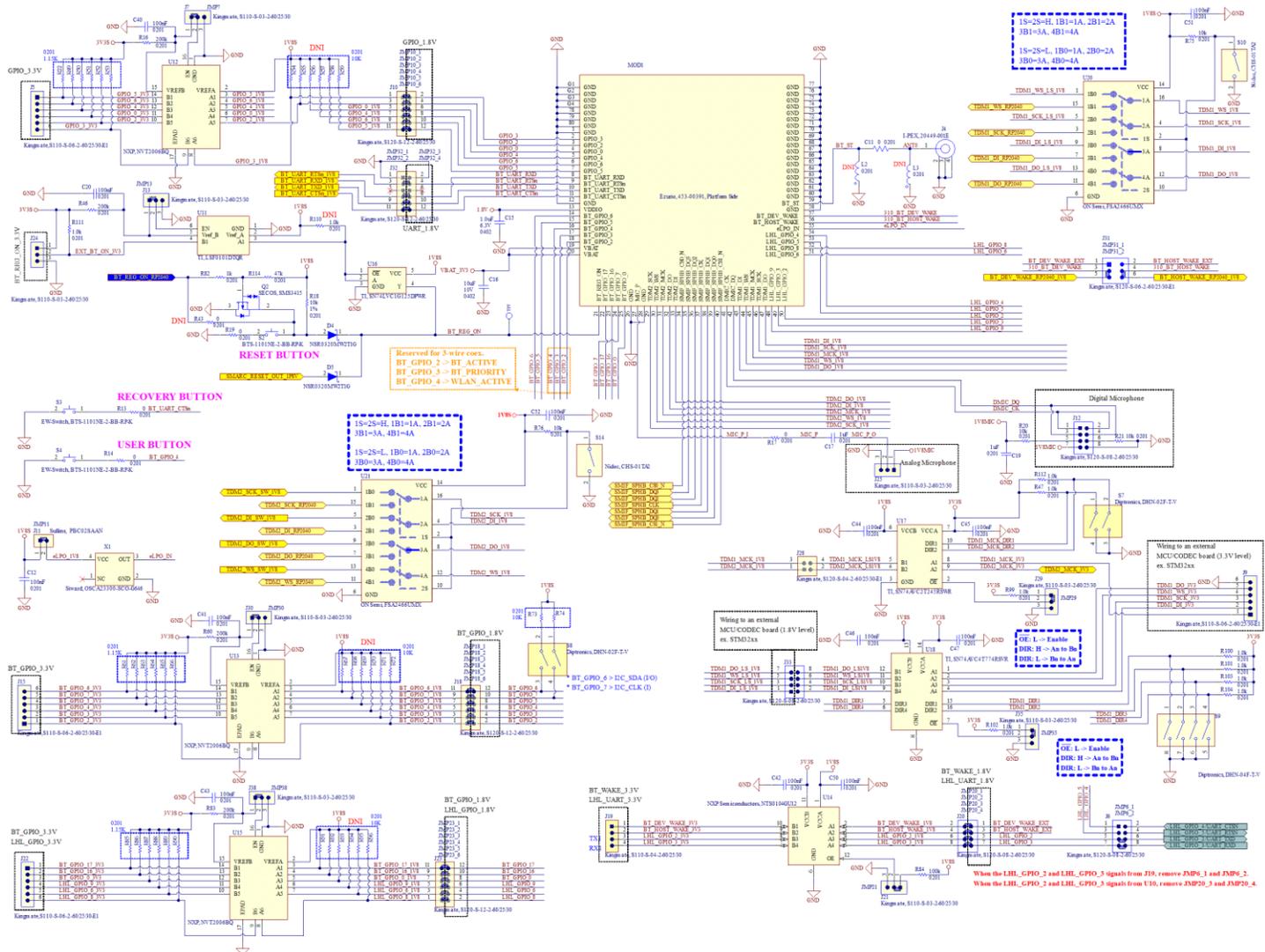


Figure 36: Vela IF310 module, GPIOs, BT_GPIOs, LHL_GPIOs, TDM buses, and Wake-up schematic

9 Additional Information

Please contact your local sales representative or our support team for further assistance:

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