Agilex™ 5 FPGAs and SoCs Device Data Sheet

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Contents

Agilex™ 5 FPGAs and SoCs Device Data Sheet

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing.

Until the data sheet status for a device reaches Final, the specifications are subject to change at any time and at Altera's discretion.

Table 1. Data Sheet Status for Agilex™ 5 FPGAs and SoCs

Devices[1]	Specification	Package	Status
A5E 008, A5E 013	A, C	All	Final
A5E 008, A5E 013 (with CS in optional suffix)	B, D, E	All	Final
All other devices	All	All	Preliminary

The following descriptors designate the status level currently applicable to the relevant variant:

- Advance: These are target specifications based on simulation.
- Preliminary: These specifications are based on simulation, early validation, and/or early characterization data.
- Final: These are production specifications based on silicon validation and/or characterization.

(1) Refer to *Agilex™ 5 FPGAs and SoCs Device Overview* for details on device ordering part numbers.

Table 2. Device Grades, Core Speed Grades, and Power Options Supported

For specification status, see the *Data Sheet Status* table

Series	Device Group	Temperature Grade	Speed Grade and Power Option Supported
D	A	Extended / Industrial	–1V (fastest)
			–2V
			–3V
E	A	Extended / Industrial	–1V (fastest)
			–2V
			–2E
			–3V
	B	Extended / Industrial	–4S (fastest)
			–5S
			–6S
			–6X

The suffix after the speed grade denotes the power options offered.

- V—standard power (VID)
- E—low power (VID)
- S—standard power (fixed voltage)
- X—low power (fixed voltage)

Related Information

Agilex™ 5 FPGAs and SoCs Device Overview

Electrical Characteristics

Operating Conditions

The devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. D-Series FPGAs Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage supply	—	–0.5	1.21	V
V_{CCP}	Periphery supply voltage for the I/O banks	—	–0.5	1.21	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	—	–0.5	1.332	V
V_{CCPT}	Power supply for I/O, DTS, SDM, and system PLL	—	–0.5	2.08	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	–0.5	1.64	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCBAT} (2)	Battery back-up power supply (for design security volatile key register)	—	–0.5	2.08	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O supply voltage sense of bank 3A	1.2 V	–0.5	1.6	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	—	–0.5	1.21	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	—	–0.5	1.21	V
V_{CCL_SDM}	SDM digital power supply	—	–0.5	1.07	V
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	—	–0.5	1.07	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	–0.5	1.07	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	—	–0.5	1.21	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS A55 cores power rail	—	–0.5	1.21	V

continued...

(2) Power up V_{CCBAT} with a non-volatile battery power source when using the device security AES BBRAM key. When not using the AES BBRAM key, tie this pin to ground.

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCL\_HPS\_CORE2}$	HPS A76 core power rail	—	–0.5	1.21	V
$V_{CCL\_HPS\_CORE3}$	HPS A76 core power rail	—	–0.5	1.21	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply	—	–0.5	1.21	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply	—	–0.5	1.21	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	—	–0.5	2.08	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
$V_{CCEHT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA, TX PLL, transceiver reference clock, and global reference clock high-voltage analog power supply	—	–0.5	2.08	V
$V_{CCERT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA, transceiver reference clock, and global reference clock low-voltage analog power supply	—	–0.5	1.34	V
V_{CCIO_PIO}	HSIO bank power supply	V_{CCIO_PIO} = 1.0 V	–0.5	1.365	V
		V_{CCIO_PIO} = 1.05 V	–0.5	1.43	V
		V_{CCIO_PIO} = 1.1 V	–0.5	1.5	V
		V_{CCIO_PIO} = 1.2 V	–0.5	1.64	V
		V_{CCIO_PIO} = 1.3 V	–0.5	1.74	V
V_{CCIO_HVIO}	HVIO bank power supply	V_{CCIO_HVIO} = 3.3 V	–0.5	3.74	V
		V_{CCIO_HVIO} = 2.5 V	–0.5	2.83	V
		V_{CCIO_HVIO} = 1.8 V	–0.5	2.04	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	–0.5	2.04	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.0 V (3) (4)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.05 V (3) (4)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.1 V (3) (4)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.2 V (3) (4)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.3 V (3) (4)	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3	$V_{CCIO\_SDM(MAX)}$ + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	$V_{CCIO\_HPS(MAX)}$ + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3	$V_{CCIO\_HVIO(MAX)}$ + 0.3	V
I_{OUT} (5) (6)	DC output current per pin	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V (7) (8)	–7.5	7.5	mA
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (9)	–20	20	mA

continued...

(3) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

(4) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to $V_{CCIO\_PIO(MAX)}$ + 0.3 V.

(5) Total current per I/O bank must not exceed 100 mA.

(6) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(7) The maximum current allowed through any HSIO pin during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage. While this device is not turned on, the I/O pin should be tri-stated or not driven with any external voltages.

(8) The DC output current per pin may exceed 7.5 mA with a duration limit. For more details, refer to the related information.

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 12 mA[10] [11]	–8	8	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 9 mA[10] [11]	–6	6	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 6 mA[10] [11]	–4	4	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 3 mA[10] [11]	–2	2	mA
T_J [12]	Absolute junction temperature	—	–40	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

(9) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

(10) The maximum current allowed through any HVIO pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HVIO} supply rail of the bank where the I/O pin resides in.

(11) The DC output current per pin may exceed specified values with a duration limit. For more details, refer to *General Purpose I/O User Guide*.

(12) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

Table 4. E-Series FPGAs Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.07	V
		Without Transceiver: –4S	–0.5	1.07	V
		Without Transceiver: –5S,	–0.5	1.043	V
		Without Transceiver: –6S, –6X	–0.5	1.004	V
		With Transceiver	–0.5	1.332	V
V_{CCPT}	Power supply for I/O, DTS, SDM, and system PLL	—	–0.5	2.08	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	–0.5	1.64	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCBAT} (13)	Battery back-up power supply (for design security volatile key register)	—	–0.5	2.08	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O supply voltage sense of bank 3A	1.2 V	–0.5	1.6	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
V_{CCL_SDM}	SDM digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.07	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –5S, –6S, –6X	–0.5	1.004	V
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.07	V

continued...

(13) Power up V_{CCBAT} with a non-volatile battery power source when using the device security AES BBRAM key. When not using the AES BBRAM key, tie this pin to ground.

Symbol	Description	Condition	Minimum	Maximum	Unit
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.07	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS A55 cores power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE2}$	HPS A76 core power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCL\_HPS\_CORE3}$	HPS A76 core power rail	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply	SmartVID: –1V, –2V, –2E, –3V	–0.5	1.21	V
		Fixed voltage: –4S	–0.5	1.07	V
		Fixed voltage: –5S	–0.5	1.043	V
		Fixed voltage: –6S, –6X	–0.5	1.004	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	—	–0.5	2.08	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
$V_{CCEHT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA, TX PLL, transceiver reference clock, and global reference clock high-voltage analog power supply	—	–0.5	2.08	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCERT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA, transceiver reference clock, and global reference clock low-voltage analog power supply	—	–0.5	1.34	V
V_{CCIO_PIO}	HSIO bank power supply	V_{CCIO_PIO} = 1.0 V	–0.5	1.365	V
		V_{CCIO_PIO} = 1.05 V	–0.5	1.43	V
		V_{CCIO_PIO} = 1.1 V	–0.5	1.5	V
		V_{CCIO_PIO} = 1.2 V	–0.5	1.64	V
		V_{CCIO_PIO} = 1.3 V	–0.5	1.74	V
V_{CCIO_HVIO}	HVIO bank power supply	V_{CCIO_HVIO} = 3.3 V	–0.5	3.74	V
		V_{CCIO_HVIO} = 2.5 V	–0.5	2.83	V
		V_{CCIO_HVIO} = 1.8 V	–0.5	2.04	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	–0.5	2.04	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.0 V[14] [15]	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.05 V[14] [15]	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.1 V[14] [15]	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.2 V[14] [15]	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_PIO} = 1.3 V[14] [15]	–0.3	$V_{CCIO\_PIO(MAX)}$ + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3	$V_{CCIO\_SDM(MAX)}$ + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	$V_{CCIO\_HPS(MAX)}$ + 0.3	V

continued...

(14) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

(15) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to $V_{CCIO\_PIO(MAX)}$ + 0.3 V.

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3	$V_{CCIO\_HVIO(MAX)}$ + 0.3	V
I_{OUT} (16) (17)	DC output current per pin	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V (18) (19)	–7.5	7.5	mA
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (20)	–20	20	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 12 mA(21) (22)	–8	8	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 9 mA(21) (22)	–6	6	mA
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 6 mA(21) (22)	–4	4	mA

continued...

(16) Total current per I/O bank must not exceed 100 mA.

(17) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(18) The maximum current allowed through any HSIO pin during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage. While this device is not turned on, the I/O pin should be tri-stated or not driven with any external voltages.

(19) The DC output current per pin may exceed 7.5 mA with a duration limit. For more details, refer to the related information.

(20) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

(21) The maximum current allowed through any HVIO pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HVIO} supply rail of the bank where the I/O pin resides in.

(22) The DC output current per pin may exceed specified values with a duration limit. For more details, refer to *General Purpose I/O User Guide*.

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V Current Strength Setting = 3 mA(21) (22)	–2	2	mA
T_J (23)	Absolute junction temperature	—	–40	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

Related Information

- Recommended Operating Conditions on page 22
- I/O Standard Specifications on page 45
- General-Purpose I/O User Guide: Agilex™ 5 FPGAs and SoCs

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, the toggling input data or clock signals may overshoot to the voltage listed in the following tables and undershoot to the following limits for input currents less than 100 mA and periods shorter than 20 ns.

- Undershoot limit of –1.1 V when using V_{CCIO_HPS} or V_{CCIO_SDM} of 1.8 V.
- Undershoot limit of –0.3 V when using V_{CCIO_PIO} of 1.3 V, 1.2 V, 1.1 V, 1.05 V, and 1.0 V.

No overshooting beyond 1.65 V and undershooting below 0.273 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.3 V.

No overshooting beyond 1.177 V and undershooting below 0.573 V is allowed when using True Differential Signaling I/O standard at V_{CCIO_PIO} = 1.2 V, 1.1 V, and 1.05 V.

The maximum allowed overshoot duration is specified as a percentage of high time (calculated as ([delta T]/T) × 100) over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

(23) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

Table 5. Maximum Allowed Overshoot During Transitions for 1.0 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[24]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 6. Maximum Allowed Overshoot During Transitions for 1.05 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[25]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(24) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(25) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 7. Maximum Allowed Overshoot During Transitions for 1.1 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[26]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 8. Maximum Allowed Overshoot During Transitions for 1.2 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[27]	30	%
		V_{CCIO_PIO} + 0.35	4	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

(26) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

(27) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Table 9. Maximum Allowed Overshoot During Transitions for 1.3 V I/O in HSIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.25	100	%
		V_{CCIO_PIO} + 0.30[28]	65	%
		V_{CCIO_PIO} + 0.35	7	%
		> V_{CCIO_PIO} + 0.40	No overshoot allowed	%

Table 10. Maximum Allowed Overshoot During Transitions for 1.8 V I/O in HPS and SDM I/O Banks

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_SDM} + 0.30, V_{CCIO_HPS} + 0.30	100	%
		V_{CCIO_SDM} + 0.35, V_{CCIO_HPS} + 0.35	60	%
		V_{CCIO_SDM} + 0.40, V_{CCIO_HPS} + 0.40	30	%
		V_{CCIO_SDM} + 0.45, V_{CCIO_HPS} + 0.45	20	%

continued...

(28) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the V_i (AC) for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V at an overshoot duration of 100%.

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
		V_{CCIO_SDM} + 0.50, V_{CCIO_HPS} + 0.50	10	%
		V_{CCIO_SDM} + 0.55, V_{CCIO_HPS} + 0.55	6	%
		> V_{CCIO_SDM} + 0.55, > V_{CCIO_HPS} + 0.55	No overshoot allowed	%

Table 11. Maximum Allowed Overshoot During Transitions for 1.8 V, 2.5 V, and 3.3 V in HVIO Bank

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

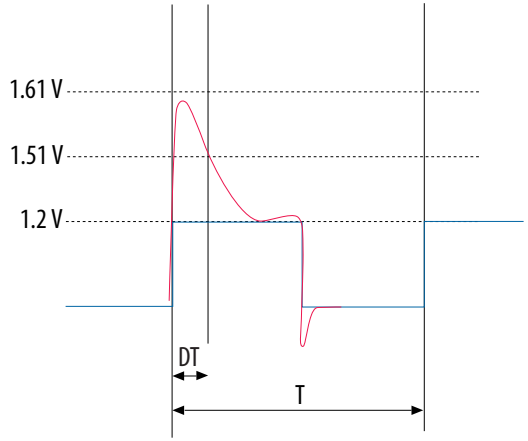
For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC) (29)	AC input voltage	V_{CCIO_HVIO} + 0.30	100	%
		V_{CCIO_HVIO} + 0.35	42	%
		V_{CCIO_HVIO} + 0.40	18	%
		V_{CCIO_HVIO} + 0.45	9	%
		V_{CCIO_HVIO} + 0.50	4	%
		> V_{CCIO_HVIO} + 0.55	No overshoot allow	%

For example, when using 1.2 V I/O standard with 1.26 V V_{CCIO_PIO}, a signal that overshoots to 1.61 V can only be at 1.61 V for ~4% over the lifetime of the device. For an overshoot of 1.51 V, the percentage of high time for the overshoot can be as high as 100% over the lifetime of the device.

(29) This value applies to both input and output configuration.

Figure 1. Overshoot Duration Example (for 1.2 V HSIO Bank at V_{CCIO_PIO} = 1.26 V)



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters.

Recommended Operating Conditions

Table 12. D-Series FPGAs Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum(30)	Typical	Maximum(30)	Unit
V_{CC}	Core voltage supply	SmartVID(31) : –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90(32)	(Typical) + 3%	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID(31): –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90(32)	(Typical) + 3%	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	—	0.975	1	1.025	V
V_{CCPT} (33)	Power supply for I/O, DTS, SDM, and system PLL	—	1.746	1.8	1.854	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	1.14	1.2	1.26	V

continued...

(30) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(31) The use of Power Management Bus (PMBus*) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

(32) The typical value is based on the SmartVID programmed value.

(33) Must use a tolerance of ±3% when sharing with V_{CCIO_HVIO}. A tolerance of ±5% is only allowed when V_{CCPT} is not shared with other rails.

Symbol	Description	Condition	Minimum[30]	Typical	Maximum[30]	Unit
V_{CCBAT} [34]	Battery back-up power supply (for design security volatile key register)	—	1	1 – 1.80	1.8	V
I_{BAT}	Battery back-up power supply (for design security volatile key register)	V_{CCBAT} = 1.2 V	—	—	200	nA
$V_{CCIO\_PIO\_SDM}$ [35]	SDM block I/O supply voltage sense of bank 3A	1.2 V	1.164	1.2	1.236	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID[31]: –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[32]	(Typical) + 3%	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	SmartVID[31]: –1V, –2V, –3V	(Typical) – 3%	0.70 – 0.90[32]	(Typical) + 3%	V
V_{CCL_SDM}	SDM digital power supply	—	0.776	0.8	0.824	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	0.776	0.8	0.824	V

continued...

(30) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(34) Power up V_{CCBAT} with a non-volatile battery power source when using the device security AES BBRAM key. When not using the AES BBRAM key, tie this pin to ground.

(35) Must be supplied at 1.2 V when using Avalon® Streaming ×16 configuration schemes. For more information, please refer to the Agilex 5 Device Family Pin Connection Guidelines.

Symbol	Description	Condition	Minimum[30]	Typical	Maximum[30]	Unit
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	1.71	1.8	1.89	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	HSIO bank power supply	1.0 V	0.95	1	1.05	V
		1.05 V[36]	1.0185	1.05	1.0815	V
		1.1 V[36]	1.067	1.1	1.133	V
		1.2 V[36]	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
V_{CCIO_HVIO}	HVIO bank power supply	3.3 V	3.201	3.3	3.399	V
		2.5 V	2.425	2.5	2.575	V
		1.8 V	1.746	1.8	1.854	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	1.746	1.8	1.854	V
V_I [37]	DC input voltage	V_{CCIO_PIO} = 1.0 V[38]	–0.3000	—	V_{CCIO_PIO} + 0.25	V

continued...

(30) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(36) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes:
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(37) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

Symbol	Description	Condition	Minimum[30]	Typical	Maximum[30]	Unit
		V_{CCIO_PIO} = 1.05 V[39] [38]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.1 V[39] [38]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.2 V[39] [38]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.3 V[39] [38]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3000	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3000	—	V_{CCIO_HPS} + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3000	—	V_{CCIO_HVIO} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	0	—	V_{CCIO_HVIO}	V

continued...

(30) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(38) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

(39) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

Symbol	Description	Condition	Minimum[30]	Typical	Maximum[30]	Unit
T_J	Operating junction temperature	Extended	0	—	100[40]	°C
		Industrial	–40	—	100[40]	°C
t_{RAMP} [41] [42]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

Table 13. E-Series FPGAs Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum[43]	Typical	Maximum[43]	Unit
V_{CC}	Core voltage supply	SmartVID[44] : –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[45]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V

continued...

(30) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(40) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

(41) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. The ramp time applies to both the ramp-up and ramp-down of the power rails.

(42) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(44) The use of Power Management Bus (PMBus) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

(45) The typical value is based on the SmartVID programmed value.

Symbol	Description	Condition	Minimum[43]	Typical	Maximum[43]	Unit
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCP}	Periphery supply voltage for the I/O banks	SmartVID[44]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[45]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCH_SDM}	SDM block transceiver supply voltage sense	SmartVID[44]: –1V, –2V, –2E, –3V	0.776	0.8	0.824	V
		Without transceiver: –4S	0.776	0.8	0.824	V
		Without transceiver: –5S	0.756	0.78	0.803	V
		Without transceiver: –6S, –6X	0.7275	0.75	0.7725	V
		With transceiver	0.975	1	1.025	V
V_{CCPT} [46]	Power supply for I/O, DTS, SDM, and system PLL	—	1.746	1.8	1.854	V
$V_{CCRCORE}$	Power supply for programmable power technology	—	1.14	1.2	1.26	V

continued...

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(46) Must use a tolerance of ±3% when sharing with V_{CCIO_HVIO}. A tolerance of ±5% is only allowed when V_{CCPT} is not shared with other rails.

Symbol	Description	Condition	Minimum[43]	Typical	Maximum[43]	Unit
V_{CCBAT} [47]	Battery back-up power supply (for design security volatile key register)	—	1	1 – 1.80	1.8	V
I_{BAT}	Battery back-up power supply (For design security volatile key register)	V_{CCBAT} = 1.2 V	—	—	200	nA
$V_{CCIO\_PIO\_SDM}$ [48]	SDM block I/O supply voltage sense of bank 3A	1.2 V	1.164	1.2	1.236	V
$V_{CC\_IO\_SDM}$	I/O digital supply voltage sense in SDM block	SmartVID[44]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[45]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
$V_{CCL\_ADC\_SDM}$	Periphery digital supply voltage sense to ADC, senses HPS digital supply on HPS devices, core supply on non-HPS devices	SmartVID[44]: –1V, –2V, –2E, –3V	(Typical) – 3%	0.70 – 0.90[45]	(Typical) + 3%	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V

continued...

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(47) Power up V_{CCBAT} with a non-volatile battery power source when using the device security AES BBRAM key. When not using the AES BBRAM key, tie this pin to ground.

(48) Must be supplied at 1.2 V when using Avalon Streaming ×16 configuration schemes. For more information, please refer to the *Agilex 5 Device Family Pin Connection Guidelines*.

Symbol	Description	Condition	Minimum[43]	Typical	Maximum[43]	Unit
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCL_SDM}	SDM digital power supply	SmartVID[44]: –1V, –2V, –2E, –3V	0.776	0.8	0.824	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	SmartVID[44]: –1V, –2V, –2E, –3V	0.776	0.8	0.824	V
		Fixed voltage: –4S	0.776	0.8	0.824	V
		Fixed voltage: –5S	0.756	0.78	0.803	V
		Fixed voltage: –6S, –6X	0.7275	0.75	0.7725	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	1.71	1.8	1.89	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	HSIO bank power supply	1.0 V	0.95	1	1.05	V
		1.05 V[49]	1.0185	1.05	1.0815	V

continued...

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

Symbol	Description	Condition	Minimum(43)	Typical	Maximum(43)	Unit
		1.1 V(49)	1.067	1.1	1.133	V
		1.2 V(49)	1.164	1.2	1.236	V
		1.3 V	1.261	1.3	1.339	V
V_{CCIO_HVIO}	HVIO bank power supply	3.3 V	3.201	3.3	3.399	V
		2.5 V	2.425	2.5	2.575	V
		1.8 V	1.746	1.8	1.854	V
V_{CCPT_HVIO}	Supply voltage for 1.8 V I/O	—	1.746	1.8	1.854	V
V_I (50)	DC input voltage	V_{CCIO_PIO} = 1.0 V(51)	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.05 V(52) (51)	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.1 V(52) (51)	–0.3000	—	V_{CCIO_PIO} + 0.25	V

continued...

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(49) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes:
- LVDS SERDES receiver mode with the use of 1.05 V, 1.1 V, 1.2 V True Differential Signaling input standard
- PHYLITE mode
- GPIO mode

(50) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(51) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{I(DC)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

(52) Applies to LVCMOS I/O standards only. For true differential input, refer to the $V_{ICM(min)}$, $V_{ICM(max)}$, and $V_{ID(max)}$ specifications.

Symbol	Description	Condition	Minimum[43]	Typical	Maximum[43]	Unit
		V_{CCIO_PIO} = 1.2 V[52] [51]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_PIO} = 1.3 V[52] [51]	–0.3000	—	V_{CCIO_PIO} + 0.25	V
		V_{CCIO_SDM} = 1.8 V	–0.3000	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3000	—	V_{CCIO_HPS} + 0.3	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	–0.3000	—	V_{CCIO_HVIO} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.0 V, 1.05 V, 1.1 V, 1.2 V, 1.3 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
		V_{CCIO_HVIO} = 1.8 V, 2.5 V, 3.3 V	0	—	V_{CCIO_HVIO}	V
T_J	Operating junction temperature	Extended	0	—	100[53]	°C
		Industrial	–40	—	100[53]	°C
t_{RAMP} [54] [55]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

(43) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(53) When using the device at T_J = 100°C, the device can operate under the recommended operating conditions over a minimum device lifetime of 11.4 years.

(54) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. The ramp time applies to both the ramp-up and ramp-down of the power rails.

(55) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

Related Information

I/O Standard Specifications on page 45

GTS Transceiver Power Supply Operating Conditions

Table 14. D-Series FPGAs GTS Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended VR Accuracy (% of Typical DC Level)	Recommended VR Ripple (% of Typical DC Level)	Recommended AC Transient (% of Typical DC Level)	Maximum (VR Accuracy + Ripple + AC Transient) (% of Typical DC Level)(56)	Unit
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	0.8	±0.5	±2.5		±3	V
$V_{CCEHT\_GTS[L1, R4][A, B, C, D]}$ (57)	Transceiver PMA, transceiver PLL, and transceiver reference clock high voltage analog power supply	1.8	±0.5	±2.0		±2.5	V
$V_{CCERT\_GTS[L1, R4][A, B, C, D]}$	Transceiver PMA and transceiver reference clock low voltage analog power supply	1	±0.5	±2.0		±2.5	V

(56) For scope measurement, 20 MHz bandwidth is sufficient. During measurement, put the ground pin as close to the power rail pin as possible.

(57) HF noise requires AC 30 mVpp above 1 MHz.

Table 15. E-Series FPGAs GTS Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Speed Grade	Typical DC Level (V)	Recommended VR Accuracy (% of Typical DC Level)	Recommended VR Ripple (% of Typical DC level)	Recommended AC Transient (% of Typical DC level)	Maximum (VR Accuracy + Ripple + AC Transient) (% of Typical DC Level)(58)	Unit
$V_{CC\_HSSI\_[L1, R4]}$	Transceiver, system PLL, and hard IP digital power supply	–6S, –6X	0.75	±0.5	±2.5		±3	V
		–5S	0.78	±0.5	±2.5		±3	V
		–1V, –2V, –2E, –3V, –4S	0.8	±0.5	±2.5		±3	V
$V_{CCEHT\_GTS[L1,R4][A, B, C]}$ (59)	Transceiver PMA, transceiver PLL, and transceiver reference clock high voltage analog power supply	—	1.8	±0.5	±2.0		±2.5	V
$V_{CCERT\_GTS[L1, R4][A, B, C]}$	Transceiver PMA and transceiver reference clock low voltage analog power supply	—	1	±0.5	±2.0		±2.5	V

(58) For scope measurement, 20 MHz bandwidth is sufficient. During measurement, put the ground pin as close to the power rail pin as possible.

(59) HF noise requires AC 30 mVpp above 1 MHz.

HPS Power Supply Operating Conditions

Table 16. D-Series FPGAs HPS Power Supply Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with Arm*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS Cortex*-A55 core 0 and core 1 power rail	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE2}$	HPS Cortex*-A76 core 2 power rail	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE3}$	HPS Cortex*-A76 core 3 power rail	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –3V[60]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

(60) The use of Power Management Bus (PMBus) voltage regulator dedicated to the SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

Table 17. E-Series FPGAs HPS Power Supply Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with Arm-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS DSU voltage and periphery circuitry power supply	SmartVID: –1V, –2V, –2E, –3V[61]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE0\_CORE1}$	HPS Cortex*-A55 core 0 and core 1 power rail	SmartVID: –1V, –2V, –2E, –3V[61]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE2}$	HPS Cortex*-A76 core 2 power rail	SmartVID: –1V, –2V, –2E, –3V[61]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCL\_HPS\_CORE3}$	HPS Cortex*-A76 core 3 power rail	SmartVID: –1V, –2V, –2E, –3V[61]	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V

continued...

(61) The use of Power Management Bus (PMBus) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG1\_HPS}$	HPS PLL1 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –2E, –3V(61)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
$V_{CCPLLDIG2\_HPS}$	HPS PLL2 digital power supply (can be connected to V_{CCL_HPS})	SmartVID: –1V, –2V, –2E, –3V(61)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4S	(Typical) – 3%	0.8	(Typical) + 3%	V
		Fixed voltage: –5S	(Typical) – 3%	0.78	(Typical) + 3%	V
		Fixed voltage: –6S, –6X	(Typical) – 3%	0.75	(Typical) + 3%	V
V_{CCPLL1_HPS}	HPS PLL1 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCPLL2_HPS}	HPS PLL2 analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 22
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 107

DC Characteristics

Supply Current and Power Consumption

Altera offers two ways to estimate power for your design—the Power and Thermal Calculator (PTC) and the Quartus® Prime Power Analyzer feature.

Use the PTC before you start your design to estimate the supply current for your design. The PTC provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

HSIO DC Characteristics

HSIO I/O Pin Leakage Current

Table 18. HSIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA

HSIO OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 19. HSIO OCT Calibration Accuracy Specifications

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of 240 Ω ±1%.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S (62)	Internal series termination with calibration (34-Ω and 40-Ω setting)	SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	20	%
		POD11 and LVSTL11 I/O standards	20	%
		LVSTL105 I/O standard	20	%
40-Ω R_S (62)	Internal series termination with calibration (40-Ω setting)	LVSTL700 I/O standard	20	%
45-Ω R_S	Internal series termination with calibration (45-Ω setting)	DPHY I/O standard	–20 to +25	%
50-Ω and 60-Ω R_T (62)	Internal parallel termination with calibration (50-Ω and 60-Ω setting)	SSTL-12 and HSTL-12 I/O standards	20	%
40-Ω, 50-Ω, and 60-Ω R_T (62)	Internal parallel termination with calibration (40-Ω, 50-Ω, and 60-Ω setting)	POD11 and POD12 I/O standards	20	%
		LVSTL11, LVSTL105, and LVSTL700 I/O standards	20	%
100-Ω R_D	Internal differential termination with calibration (100-Ω setting)	DPHY I/O standard	–20 to +25	%

(62) This specification applies to both single-ended and pseudo-differential I/O buffers.

HSIO OCT Without Calibration Resistance Tolerance Specifications

Table 20. HSIO OCT Without Calibration Resistance Tolerance Specifications

This table lists the GPIO OCT without calibration resistance tolerance to PVT changes.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.3 V LVCMOS I/O standard	30	%
34-Ω and 40-Ω R_S (63)	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.2 V LVCMOS, SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards	25	%
		1.1 V LVCMOS, POD11, and LVSTL11 I/O standards	25	%
		1.05 V LVCMOS and LVSTL105 I/O standards	25	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	1.0 V LVCMOS I/O standard	30	%
50-Ω R_T (63)	Internal parallel termination without calibration (50-Ω setting)	SSTL-12 and HSTL-12 I/O standards	25	%
		POD11 and POD12 I/O standards	25	%
		LVSTL11 and LVSTL105 I/O standards	25	%
100-Ω R_D (64)	Internal differential termination (100-Ω setting)	True differential signaling I/O standard at V_{CCIO_PIO} = 1.05	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.1	40	%

continued...

(63) This specification applies to both single-ended and pseudo-differential I/O buffers.

(64) This specification applies to $V_{ICM(DC)} \leq 1.3V$. For $V_{ICM(DC)} > 1.3V$, a specification range of -60% to +40% applies.

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.2	40	%
		True differential signaling I/O standard at V_{CCIO_PIO} = 1.3	40	%
100-Ω R_D	Internal differential termination (100-Ω setting)	SLVS400 I/O standard	30	%

HSIO Pin Capacitance

Table 21. HSIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.6(65)	pF

HSIO Internal Weak Pull-Up Resistor

All I/O pins in GPIO bank have an option to enable weak pull-up when using 1.0 V, 1.05 V, 1.1 V, 1.2 V, and 1.3 V LVCMOS I/O standards.

Table 22. HSIO Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO_PIO} = 1.3 ±3%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.2 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.1 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.05 ±5%	3	10	30	kΩ
		V_{CCIO_PIO} = 1.0 ±5%	3	10	30	kΩ

(65) This value refers to die-level pin capacitance without the device package.

HVIO DC Characteristics

HVIO I/O Pin Leakage Current

Table 23. HVIO I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_HVIO\ (MAX)}$	-10	10	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to V_{CCIO_HVIO} (MAX)	-10	10	µA

HVIO Pin Capacitance

Table 24. HVIO Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	4(66)	pF

HVIO Internal Weak Pull-Up and Pull-Down Resistor

Only input and bidirectional pins in HVIO bank have an option to enable weak pull-up and pull-down when using LVCMOS I/O standard.

Table 25. HVIO Internal Weak Pull-Up and Pull-Down Resistor Values

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the	V_{CCIO_HVIO} = 1.8, 2.5, 3.3 ±3%	15	20	30	kΩ

(66) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	programmable pull-up or pull-down resistor option.					

HVIO Hysteresis Specifications for Schmitt Trigger Input

Table 26. HVIO Hysteresis Specifications for Schmitt Trigger Input

This device supports built-in Schmitt trigger input that always enabled on HVIO I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HVIO} = 1.8 V	—	200	—	mV
		V_{CCIO_HVIO} = 2.5 V	—	250	—	mV
		V_{CCIO_HVIO} = 3.3 V	—	250	—	mV

HPS I/O DC Characteristics

HPS I/O Pin Leakage Current

Table 27. HPS I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_HPS\ (MAX)}$	–15	15	µA
	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_HPS\ (MAX)}$	–15	15	µA

HPS I/O Pin Capacitance

Table 28. HPS I/O Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	5(67)	pF

HPS I/O Internal Weak Pull-Up Resistor

The I/O pins in HPS bank are supported with weak pull-up and weak pull-down options.

Table 29. HPS Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_HPS} = 1.8 ±5%	15	20	25	kΩ
50 kΩ R_{PU}, 50 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_HPS} = 1.8 ±5%	37.5	50	62.5	kΩ
80 kΩ R_{PU}, 80 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the	V_{CCIO_HPS} = 1.8 ±5%	57	80	105	kΩ

continued...

(67) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	programmable pull-up or pull-down resistor option.					

HPS I/O Hysteresis Specifications for Schmitt Trigger Input

Table 30. HPS I/O Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on HPS I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HPS} = 1.8 V	180	–	–	mV

SDM I/O DC Characteristics

SDM I/O Pin Leakage Current

Table 31. SDM I/O Pin Leakage Current

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_SDM\ (MAX)}$	–15	15	µA
	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_SDM\ (MAX)}$	–15	15	µA

SDM I/O Pin Capacitance

Table 32. SDM I/O Pin Capacitance

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	5(68)	pF

SDM I/O Internal Weak Pull-Up Resistor

The I/O pins in SDM bank are supported with weak pull-up and weak pull-down feature. The weak pull-up and weak pull-down feature is pre-configured according to the configuration mode.

Table 33. SDM I/O Internal Weak Pull-Up Resistor

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during configuration.	V_{CCIO_SDM} = 1.8 ±5%	15	20	25	kΩ

SDM I/O Hysteresis Specifications for Schmitt Trigger Input

Table 34. SDM I/O Hysteresis Specifications for Schmitt Trigger Input

This device supports Schmitt trigger input on SDM I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_SDM} = 1.8 V	180	–	–	mV

I/O Standard Specifications

HSIO I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

(68) This value refers to die-level pin capacitance without the device package.

You must perform timing closure analysis to determine the maximum achievable frequency for general-purpose I/O standards.

Related Information

Recommended Operating Conditions on page 22

HSIO Single-Ended I/O Standards Specifications

Table 35. HSIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)(69)	V_{OH} (V)(69)
	Min	Typ	Max	Min	Max	Min	Max(70)	Max	Min
1.3 V LVCMOS	1.261	1.3	1.339	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.1 V LVCMOS	1.045	1.1	1.155	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.05 V LVCMOS	0.9975	1.05	1.1025	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}
1.0 V LVCMOS	0.95	1	1.05	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.25	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}

(69) Applicable to test condition of I_{OH} and I_{OL} at 2 mA.

(70) For LVCMOS pin utilization of equal to or less than 25 pins within a bank, the $V_{IH(max)}$ for the LVCMOS input can go up to V_{CCIO_PIO} + 0.3 V.

HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications

Table 36. HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
HSTL-12	1.14	1.2	1.26	0.47 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.53 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
HSUL-12[71]	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.45 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.55 × V_{CCIO_PIO}
POD12 (GPIO)[72] [73]	1.164	1.2	1.236	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD12 (PHYLITE)[72] [73]	1.164	1.2	1.236	0.74 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}	0.76 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD11 (GPIO)[72] [73]	1.067	1.1	1.133	0.69 × V_{CCIO_PIO}	0.7 × V_{CCIO_PIO}	0.71 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—
POD11 (PHYLITE)[72] [73]	1.067	1.1	1.133	0.74 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}	0.76 × V_{CCIO_PIO}	—	V_{CCIO_PIO}	—

continued...

(71) Usage of on-board receiver termination is optional.

(72) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

(73) For I/O lane with mixture of GPIO and PHYLITE interfaces, the V_{REF} specification for that I/O lane follows the PHYLITE V_{REF} specifications.

I/O Standard	V_{CCIO_PIO} (V)			Internal V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVSTL11[72]	1.067	1.1	1.133	0.24 × V_{CCIO_PIO}	0.25 × V_{CCIO_PIO}	0.26 × V_{CCIO_PIO}	—	GND	—
LVSTL105[72]	1.0185	1.05	1.0815	0.24 × V_{CCIO_PIO}	0.25 × V_{CCIO_PIO}	0.26 × V_{CCIO_PIO}	—	GND	—
LVSTL700	1.0185	1.05	1.0815	0.174 × V_{CCIO_PIO}	0.184 × V_{CCIO_PIO}	0.194 × V_{CCIO_PIO}	—	GND	—

HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 37. HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Max	Min	Max	Min
SSTL-12	V_{REF} – 0.075	V_{REF} + 0.075	V_{REF} – 0.100	V_{REF} + 0.100
HSTL-12	V_{REF} – 0.080	V_{REF} + 0.080	V_{REF} – 0.150	V_{REF} + 0.150
HSUL-12	V_{REF} – 0.100	V_{REF} + 0.100	V_{REF} – 0.135	V_{REF} + 0.135
POD12	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
POD11	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For output voltage swing calculation example, refer to the *General-Purpose I/O User Guide* for this device. Differential voltage referenced I/O standard uses two single-ended outputs with second output programmed as inverted.

Note: For eye height position estimation in EMIF interfaces, refer to the *PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs*. The eye mask estimation methodology defined in the *PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs* takes precedence over specifications in *HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications* table.

Related Information

- General-Purpose I/O User Guide: Agilex™ 5 FPGAs and SoCs

- PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs
  Provides eye mask estimation for EMIF interfaces.

HSIO Single-Ended LVSTL I/O Standards Specifications

Table 38. HSIO Single-Ended LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Min	Typ	Max	Max	Min	Max	Min
LVSTL11[74]	1.067	1.1	1.133	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
LVSTL105[74]	1.0185	1.05	1.0815	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070
LVSTL700	1.0185	1.05	1.0815	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For eye height position estimation in EMIF interfaces, refer to the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs. The eye mask estimation methodology defined in the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs takes precedence over specifications in HSIO Single-Ended LVSTL I/O Standards Specifications table.

Related Information

PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs

(74) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 39. HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (V)			$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12[75]	1.14	1.2	1.26	–0.15	0.15	–0.2	0.2	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSTL-12[75]	1.14	1.2	1.26	–0.16	0.16	–0.3	0.3	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSUL-12[75]	1.14	1.2	1.26	–0.2	0.2	–0.27	0.27	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12

HSIO Differential POD I/O Standards Specifications

Table 40. HSIO Differential POD I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)[76]
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12[77]	1.164	1.2	1.236	–0.11	0.11	–0.14	0.14	25
POD11[77]	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25

(75) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.

- PHYLITE mode
- GPIO mode

(76) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

Note: For eye height position estimation in EMIF interfaces, refer to the *PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs*. The eye mask estimation methodology defined in the *PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs* takes precedence over specifications in *HSIO Differential POD I/O Standards Specifications* table.

Related Information

PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs
Provides eye mask estimation for EMIF interfaces.

HSIO Differential LVSTL I/O Standards Specifications

Table 41. HSIO Differential LVSTL I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)(78)
	Min	Typ	Max	Max	Min	Max	Min	Max
LVSTL11(79)	1.067	1.1	1.133	–0.11	0.11	–0.14	0.14	25
LVSTL105(79)	1.0185	1.05	1.0815	–0.11	0.11	–0.14	0.14	25
LVSTL700	1.0185	1.05	1.0815	–0.11	0.11	–0.14	0.14	25

(77) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

(78) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

(79) Each sub-bank can only support a single voltage tolerance. The V_{CCIO_PIO} tolerance can be extended to ±5% if the entire HSIO sub-bank is operating in any of the following modes. Else, you must supply the V_{CCIO_PIO} voltage rail with a ±3% voltage supply tolerance.
- PHYLITE mode
- GPIO mode

Note: For eye height position estimation in EMIF interfaces, refer to the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs. The eye mask estimation methodology defined in the PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs takes precedence over specifications in HSIO Differential LVSTL I/O Standards Specifications table.

Related Information

PCB Design Guidelines (HSSI, EMIF, MIPI, True Differential, PDN) User Guide: Agilex™ 5 FPGAs and SoCs

HSIO Differential I/O Standards Specifications

Table 42. HSIO Differential I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (80)			V_{OCM} (V)(80)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling -1.3 V (LVDS compatible Transmitter and	1.261	1.3	1.339	100	500	0.5	—	1.40(84)	247	—	454	0.9	1	1.1

continued...

(80) R_L range: 90 ≤ R_L ≤ 110 Ω.

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (80)			V_{OCM} (V)(80)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Receiver) (81) (82) (83)														
True Differential Signaling -1.2 V (Receiver only) (81)	1.14	1.2	1.26	100	454	0.8	—	0.95	—	—	—	—	—	—
True Differential Signaling -1.1 V (Receiver only) (81)	1.045	1.1	1.155	100	454	0.8	—	0.95	—	—	—	—	—	—

continued...

(80) R_L range: $90 \leq R_L \leq 110\ \Omega$.

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (mV) (80)			V_{OCM} (V)(80)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling -1.05 V (Receiver only) (81)	0.9975	1.05	1.1025	100	454	0.8	—	0.95	—	—	—	—	—	—
SLVS400	1.164	1.2	1.236	70	—	0.07	0.2	0.33	—	—	—	—	—	—
	1.067	1.1	1.133						—	—	—	—	—	—

Related Information

- General-Purpose I/O User Guide: Agilex™ 5 FPGAs and SoCs
- LVDS SERDES User Guide: Agilex™ 5 FPGAs and SoCs
- AN 555: True Differential Signaling Termination and Biasing for Agilex™ 7 M-Series, Agilex™ 5, and Agilex™ 3 FPGAs

(80) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(81) The True Differential Signaling input buffer is supported on 1.05 V, 1.1 V, 1.2 V, and 1.3 V V_{CCIO_PIO} banks. The maximum input voltage driven into the True Differential Signaling input buffer must not exceed $V_{ICM(max)} + V_{ID(max)}/2$.

(82) True Differential Signaling - 1.3 V standard is compatible with LVDS and capable to interface with LVDS subsets such as:
- RSDS
- Mini-LVDS
- Any I/O standards using equivalent electrical specifications

(83) For further information on True Differential Signaling - 1.3 V feature support and guidelines on interfacing True Differential Signaling -1.3V standard with LVDS and its subset compliant standards, refer to the related information.

(84) The $V_{ICM(DC)}$ voltage must not exceed 1.2 V when on-chip differential termination (R_D OCT) is disabled with the use of external on-board termination.

MIPI D-PHY I/O Standards Specifications

Table 43. D-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Note	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
DPHY	Applicable for low power when the supported High Speed data rate 150Mbps to 3.5Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	–0.05	—	0.05
	Applicable for low power when the supported High Speed data rate 150Mbps to 3.5Gbps	1.067	1.1	1.133					0.95(85)	1.1(85)	1.2(85)			

(85) Receivers compliant to D-PHY v2.1 and later supports a V_{IH} compatible with V_{OH} level regardless of the supported High-Speed data rate.

Table 44. D-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition	V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			$V_{OD(DC)}$ (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
		Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
DPHY	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	–0.04	0.46
	Data rate > 1.5 Gbps to 3.5 Gbps				0.04												
	Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
	Data rate > 1.5 Gbps to 3.5 Gbps				0.04												

Table 45. E-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Device Group	Note	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
			Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
DPHY	A	Applicable for low power when the support	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	–0.05	—	0.05

continued...

I/O Standard	Device Group	Note	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
			Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
		ed High Speed data rate 150 Mbps to 3.5 Gbps													
		Applicable for low power when the supported High Speed data rate 150 Mbps to 3.5 Gbps	1.067	1.1	1.133					0.95(86)	1.1(86)	1.2(86)			
	B	Applicable for low power when the supported High Speed data rate 150 Mbps to 2.5 Gbps	1.164	1.2	1.236	—	0.55	0.74	—	1.1	1.2	1.3	–0.05	—	0.05
		Applicable for	1.067	1.1	1.133					0.95(86)	1.1(86)	1.2(86)			

continued...

(86) Receivers compliant to D-PHY v2.1 and later supports a V_{IH} compatible with V_{OH} level regardless of the supported High-Speed data rate.

I/O Standard	Device Group	Note	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OH} (V)			V_{OL} (V)		
			Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
		low power when the supported High Speed data rate 150 Mbps to 2.5 Gbps													

Table 46. E-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			$V_{OD(DC)}$ (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
	Device Group	Data Rate	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
DPHY	A	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	–0.04	0.46
		Data rate > 1.5 Gbps to 3.5 Gbps				0.04												
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
		Data rate > 1.5				0.04												

continued...

I/O Standard	Condition		V_{CCIO_PIO} (V)			V_{ID} (V)		$V_{ICM(DC)}$ (V)			$V_{OD(DC)}$ (V)			V_{OCM} (V)			V_{ILHS} (V)	V_{IHHS} (V)
	Device Group	Data Rate	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
		Gbps to 3.5 Gbps																
	B	Data rate ≤ 1.5 Gbps	1.164	1.2	1.236	0.07	—	0.07	—	0.33	0.14	0.2	0.27	0.15	0.2	0.25	–0.04	0.46
		Data rate > 1.5 Gbps to 2.5 Gbps				0.04												
		Data rate ≤ 1.5 Gbps	1.067	1.1	1.133	0.07												
		Data rate > 1.5 Gbps to 2.5 Gbps				0.04												

HVIO I/O Standard Specifications

Related Information

Recommended Operating Conditions on page 22

HVIO Single-Ended I/O Standards Specifications

Table 47. HVIO Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HVIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)(87)	V_{OH} (V)(87)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min
1.8 V LVCMOS 1.8 V LVTTL	1.746	1.8	1.854	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45
2.5 V LVCMOS 2.5 V LVTTL	2.425	2.5	2.575	-0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2
3.3 V LVCMOS 3.3 V LVTTL	3.201	3.3	3.399	-0.3	0.8	2	V_{CCIO} + 0.3	0.4	2.4

HPS I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_HPS} values. For maximum voltage values, use the maximum V_{CCIO_HPS} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

(87) Applicable to test condition of I_{OH} and I_{OL} at 3 mA.

HPS Single-Ended I/O Standards Specifications

Table 48. HPS Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HPS}			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(88)	I_{OH} (mA)(88)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_HPS}	0.65 × V_{CCIO_HPS}	V_{CCIO_HPS} + 0.3	0.4	V_{CCIO_HPS} – 0.4	8	–8

SDM I/O Standard Specifications

Tables in this section list the supported input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards.

For minimum voltage values, use the minimum V_{CCIO_SDM} values. For maximum voltage values, use the maximum V_{CCIO_SDM} values.

SDM Single-Ended I/O Standards Specifications

Table 49. SDM Single-Ended I/O Standards Specifications

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_SDM} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(89)	I_{OH} (mA)(89)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_SDM}	0.65 × V_{CCIO_SDM}	V_{CCIO_SDM} + 0.3	0.4	V_{CCIO_SDM} – 0.4	8	–8

(88) To meet the I_{OH} and I_{OL} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

(89) To meet the I_{OH} and I_{OL} specifications, you must verify the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should verify the current strength settings used is 8 mA . Using a lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

Switching Characteristics

This section provides the performance characteristics of core and periphery blocks.

Core Performance Specifications

Clock Tree Specifications

Table 50. D-Series FPGAs Clock Tree Performance Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance		Unit
	–1V, –2V	–3V	
Programmable clock routing	1,000	780	MHz

Table 51. E-Series FPGAs Clock Tree Performance Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance					Unit
	–1V, –2V, –2E	–3V	–4S	–5S	–6S, –6X	
Programmable clock routing	1,000	780	850	710	554	MHz

I/O PLL Specifications

Table 52. D-Series FPGAs I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{IN}	Input clock frequency source from core clock input and reference clock input	–1V	10	—	1,100 (90)	MHz
		–2V	10	—	900(90)	MHz
		–3V	10	—	625(90)	MHz
	Input clock frequency source from HSIO clock input	–1V	10	—	800(90)	MHz
		–2V	10	—	717(90)	MHz
		–3V	10	—	625(90)	MHz
	Input clock frequency source from HVIO clock input	—	10	—	156.25(90)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–1V	600	—	3,200	MHz
		–2V	600	—	3,200	MHz
		–3V	600	—	2,400	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	—	0.5	—	20	MHz
f_{OUT}	Output frequency for internal clock (C counter)	–1V	—	—	1,100	MHz
		–2V	—	—	1,000	MHz
		–3V	—	—	780	MHz

continued...

(90) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OUT_EXT}	Output frequency for external clock output	–1V	—	—	800	MHz
		–2V	—	—	717	MHz
		–3V	—	—	625	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 (91)	50	55 (91)/60	%
t_{FCOMP} (92)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR} (93)	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns

continued...

(91) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES FPGA IP. Refer to the *Clocking and PLL User Guide* for the detail design guidelines.

(92) Not applicable for fabric-feeding I/O PLL.

(93) PLL phase shift accuracy is 50 ps with the assumption of f_{VCO} = 1.6 GHz.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{INCCJ}	Input clock cycle-to-cycle jitter	f_{REF} < 100 MHz (94)	—	—	±750	ps (p-p)
		f_{REF} ≥ 100 MHz (94)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms) (95)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(96) (95)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (92) (97)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (94)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (94)	—	—	175	ps (p-p)

continued...

(94) f_{REF} is f_{IN}/N, specification applies when $N = 1$.

(95) Requirement for DDR/LPDDR protocol and LVDS SERDES applications only.

(96) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: `REFCLK` phase noise at f (MHz) = `REFCLK` phase noise at 100 MHz + (20 × log10 (f/100)).

(97) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the *Clocking and PLL User Guide* for the recommended spread-spectrum clock profile.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{OUTCCJ_DC} (92) (97)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (94)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (94)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (98) (97)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (94)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (94)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (98) (97)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (94)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (94)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (92)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (94)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (94)	—	—	175	ps (p-p)
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	f_{IN} ≥ 600 MHz	30	—	70	%
		450 MHz ≤ f_{IN} < 600 MHz	35	—	65	%
		250 MHz ≤ f_{IN} < 450 MHz	40	—	60	%
		10 MHz ≤ f_{IN} < 250 MHz	45	—	55	%

(98) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output clock Jitter Specifications* table.

Table 53. E-Series FPGAs I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency source from core clock input and reference clock input	–1V, –4S	10	—	1,100 (99)	MHz
		–2V, –2E, –5S	10	—	900(99)	MHz
		–3V, –6S, –6X	10	—	625(99)	MHz
	Input clock frequency source from HSIO clock input	–1V, –4S	10	—	800(99)	MHz
		–2V, –2E, –5S	10	—	717(99)	MHz
		–3V, –6S, –6X	10	—	625(99)	MHz
	Input clock frequency source from HVIO clock input	—	10	—	156.25(99)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–1V, –4S	600	—	3,200	MHz
		–2V, –2E, –5S	600	—	3,200	MHz
		–3V, –6S, –6X	600	—	2,400	MHz
f_{CLBW}	I/O PLL closed-loop bandwidth	—	0.5	—	20	MHz
f_{OUT}	Output frequency for internal clock (C counter)	–1V,–4S	—	—	1,100	MHz
		–2V, –2E, –5S	—	—	1,000	MHz
		–3V, –6S, –6X	—	—	780	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1V, –4S	—	—	800	MHz
		–2V, –2E, –5S	—	—	717	MHz

continued...

(99) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		–3V, –6S, –6X	—	—	625	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 (100)	50	55 (100)/60	%
t_{FCOMP} (101)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR} (102)	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}	Input clock cycle-to-cycle jitter	f_{REF} < 100 MHz (103)	—	—	±750	ps (p-p)

continued...

(100) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES FPGA IP. Refer to the *Clocking and PLL User Guide* for the detail design guidelines.

(101) Not applicable for fabric-feeding I/O PLL.

(102) PLL phase shift accuracy is 50 ps with the assumption of f_{VCO} = 1.6 GHz.

(103) f_{REF} is f_{IN}/N, specification applies when N = 1.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		f_{REF} ≥ 100 MHz (103)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms) (104)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise (105) (104)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz
		10 MHz	—	—	–142	dBc/Hz
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (101) (106)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (103)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (103)	—	—	175	ps (p-p)
t_{OUTCCJ_DC} (101) (106)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (103)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (103)	—	—	175	ps (p-p)

continued...

(104) Requirement for DDR/LPDDR protocol and LVDS SERDES applications only.

(105) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: `REFCLK` phase noise at f (MHz) = `REFCLK` phase noise at 100 MHz + (20 × log10 (f/100)).

(106) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the *Clocking and PLL User Guide* for the recommended spread-spectrum clock profile.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTPJ_IO} (107) (106)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (103)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (103)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (107) (106)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (103)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (103)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (101)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (103)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (103)	—	—	175	ps (p-p)
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	f_{IN} ≥ 600 MHz	30	—	70	%
		450 MHz ≤ f_{IN} < 600 MHz	35	—	65	%
		250 MHz ≤ f_{IN} < 450 MHz	40	—	60	%
		10 MHz ≤ f_{IN} < 250 MHz	45	—	55	%

Related Information

Memory Output Clock Jitter Specifications on page 93
Provides more information about the external memory interface clock output jitter specifications.

(107) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output clock Jitter Specifications* table.

DSP Block Specifications

Table 54. D-Series FPGAs DSP Block Performance Specifications for Single DSP Block

For specification status, see the *Data Sheet Status* table

Mode	Performance			Unit
	–1V	–2V	–3V	
Fixed-point 18 × 19 multiplication mode	768	655	574	MHz
Fixed-point 27 × 27 multiplication mode	768	655	574	MHz
Fixed-point 18 × 19 multiplier adder mode	768	655	574	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	768	655	574	MHz
Fixed-point six 9 × 9 multiplier adder mode	768	655	574	MHz
FP32 floating-point multiplication mode	637	492	431	MHz
FP32 floating-point adder or subtract mode	637	492	431	MHz
FP32 floating-point multiplier adder or subtract mode	637	492	431	MHz
FP32 floating-point multiplier accumulate mode	637	492	431	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	637	492	431	MHz
Sum/sub of two FP16 multiplications with FP32 (addition/subtraction)	637	492	431	MHz

continued...

Mode	Performance			Unit
	–1V	–2V	–3V	
Sum/sub of two FP16 multiplications with accumulation (addition/ subtraction)	637	492	431	MHz
Tensor floating-point mode	637	492	431	MHz
Tensor accumulation mode: fp32	637	492	431	MHz
Tensor fixed-point mode	768	655	574	MHz
INT16 complex multiplication mode	768	655	574	MHz

Table 55. D-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks

For specification status, see the *Data Sheet Status* table

Mode	Performance			Unit
	–1V	–2V	–3V	
Fixed-point 18 x 19 complex multiplication mode	768	655	574	MHz
Fixed-point 18 × 19 FIR systolic mode	768	655	574	MHz
Fixed-point 27 × 27 multiplication mode	576	492	431	MHz
Fixed-point 9 × 9 multiplication mode	576	492	431	MHz
FP32 floating-point complex multiplication	637	492	431	MHz
FP32 floating-point vector dot product	637	492	431	MHz
FP16 floating-point complex multiplication	637	492	431	MHz

continued...

Mode	Performance			Unit
	–1V	–2V	–3V	
FP16 floating-point vector dot product	637	492	431	MHz
Tensor floating-point cascade chain	637	492	431	MHz
Tensor fixed-point cascade chain	768	655	574	MHz

Table 56. E-Series FPGAs DSP Block Performance Specifications for Single DSP Block

For specification status, see the *Data Sheet Status* table

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
Fixed-point 18 × 19 multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 27 × 27 multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 multiplier adder mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	768	655	574	558	489	408	MHz
Fixed-point six 9 × 9 multiplier adder mode	768	655	574	558	489	408	MHz
FP32 floating-point multiplication mode	637	492	431	418	367	306	MHz
FP32 floating-point adder or subtract mode	637	492	431	418	367	306	MHz

continued...

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
FP32 floating-point multiplier adder or subtract mode	637	492	431	418	367	306	MHz
FP32 floating-point multiplier accumulate mode	637	492	431	418	367	306	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	637	492	431	418	367	306	MHz
Sum/sub of two FP16 multiplications with FP32 (addition/ subtraction)	637	492	431	418	367	306	MHz
Sum/sub of two FP16 multiplications with accumulation (addition/ subtraction)	637	492	431	418	367	306	MHz
Tensor floating-point mode	637	492	431	418	367	306	MHz
Tensor accumulation mode: fp32	637	492	431	418	367	306	MHz
Tensor fixed-point mode	768	655	574	558	489	408	MHz
INT16 complex multiplication mode	768	655	574	558	489	408	MHz

Table 57. E-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks

For specification status, see the *Data Sheet Status* table

Mode	Performance						Unit
	–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
Fixed-point 18 x 19 complex multiplication mode	768	655	574	558	489	408	MHz
Fixed-point 18 × 19 FIR systolic mode	768	655	574	558	489	408	MHz
Fixed-point 27 × 27 multiplication mode	576	492	431	418	367	306	MHz
Fixed-point 9 × 9 multiplication mode	576	492	431	418	367	306	MHz
FP32 floating-point complex multiplication	637	492	431	418	367	306	MHz
FP32 floating-point vector dot product	637	492	431	418	367	306	MHz
FP16 floating-point complex multiplication	637	492	431	418	367	306	MHz
FP16 floating-point vector dot product	637	492	431	418	367	306	MHz
Tensor floating-point cascade chain	637	492	431	418	367	306	MHz
Tensor fixed-point cascade chain	768	655	574	558	489	408	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 58. D-Series FPGAs Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance			Unit
		–1V	–2V	–3V	
MLAB	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	MHz
	Simple dual-port RAM with read-during-write option set to New Data or Old Data	630	510	460	MHz
M20K block(108)	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	MHz
	Simple dual-port RAM, coherent read enabled	1,000	782	667	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800	640	560	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600	480	420	MHz
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1,000	782	667	MHz
	Dual-port ROM True dual-port RAM	600	500	420	MHz
	Simple quad-port RAM	600	500	420	MHz

(108) For the M20K block, Quartus automatically optimizes timing and power based on design requirements.

Table 59. E-Series FPGAs Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance						Unit
		–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
MLAB	Single-port RAM/ROM Simple dual-port RAM	850	750	510	600	469	400	MHz
	Simple dual-port RAM with read-during-write option set to New Data or Old Data	530	450	380	400	310	280	MHz
M20K block(109)	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	700	550	465	MHz
	Simple dual-port RAM, coherent read enabled	1,000	782	667	700	550	465	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800	640	560	560	440	370	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600	480	420	420	330	280	MHz

continued...

(109) For the M20K block, Quartus automatically optimizes timing and power based on design requirements.

Memory	Mode	Performance						Unit
		–1V	–2V, –2E	–3V	–4S	–5S	–6S, –6X	
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1,000	782	667	700	550	465	MHz
	Dual-port ROM True dual-port RAM	600	500	420	445	335	280	MHz
	Simple quad-port RAM	600	500	420	445	335	280	MHz

Local Temperature Sensor Specifications

Table 60. Local Temperature Sensor Specifications

For specification status, see the *Data Sheet Status* table

Description	Temperature Range	Accuracy	Sampling Rate(110)	Conversion Time
Local temperature sensor	–40 to 125°C(111)	±5°C	1 KSPS	< 1 ms

Related Information

Recommended Operating Conditions on page 22

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The temperature diode characteristics in this table target for three-currents temperature sensing chip implementation. The characteristics can also apply to two-currents temperature sensing chip implementation.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

(110) The read out is subject to the SDM mailbox activity status.

(111) Temperature range refers to junction temperature.

Table 61. Remote Temperature Diode Specifications (Core Fabric TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	30	—	170	µA
V_{bias}, voltage across diode	0.51	—	0.82	V
Series resistance	—	—	<5	Ω
Diode ideality factor	—	1.005(112)	—	—

Voltage Sensor Specifications

Table 62. Voltage Sensor Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Minimum	Typical	Maximum	Unit
Resolution	—	7	—	Bit
Sampling rate(113)	—	—	1	KSPS
Input capacitance	—	—	40	pF
External reference voltage	1.125	1.25	1.375	V
Voltage sensor accuracy, V_{in} range: 0 V to 1.1 V(114)(115)	—	—	±3.5	%

continued...

(112) When using lower injection current (two-currents) implementation, the ideality factor is 1.014.

(113) The read out is subject to the SDM mailbox activity status.

(114) For low voltage channels in channels 0, 1, 2, 6, and 7, the ±3.5% accuracy equals to ±43.75mV. For high voltage channels in channels 3, 4, 5, and 9, the accuracy is ±4.5%. This equals to ±56.25mV.

(115) When Voltage Tamper Detection is enabled, the voltage sensor accuracy specifications are as follows:
- For low voltage channels in channels 0, 1, 2, 6, and 7, the accuracy is ±5.5%. This equals to ±68.75mV.
- For high voltage channels in channels 3, 4, 5, and 9, the accuracy is ±6.5%. This equals to ±81.25mV.

Parameter		Minimum	Typical	Maximum	Unit
Unipolar input mode	Input signal range for Vsigp	—	—	1.35	V
	Common mode voltage on Vsign	—	—	0.25	V
	Input signal range for Vsigp – Vsign	—	—	1.1	V

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

LVDS SERDES Specifications

Table 63. D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 4 and 8.

DDR registers support SERDES factor J = 1 and 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential	Clock boost factor W = 1 to 40(116)	10	—	800	10	—	800	10	—	625	MHz

continued...

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Signaling I/O Standards											
	f_{HSCLK_in} (input clock frequency) SLVS400 I/O Standards	Clock boost factor W = 1 to 40(116)	10	—	445.5	10	—	445.5	10	—	445.5	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40(116)	10	—	625	10	—	625	10	—	525	MHz
	f_{HSCLK_OUT} (output clock frequency) True Differential Signaling I/O Standards	—	—	—	800	—	—	800	—	—	625	MHz
Transmitter	True Differential Signaling I/O	SERDES factor J = 4 and 8(118) (119)	600	—	1,600	600	—	1,600	600	—	1,250	Mbps

continued...

(116) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Standards - f_{HSDR} (data rate)(117)	SERDES factor J = 2, uses DDR registers	(120)	—	500(121)	(120)	—	500(121)	(120)	—	500(121)	Mbps
		SERDES factor J = 1, uses DDR registers	(120)	—	250(121)	(120)	—	250(121)	(120)	—	250(121)	Mbps
	t_x Jitter - True Differential Signaling I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	≤1,600 Mbps: 140 ≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			≤1,600 Mbps: 140 ≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			ps

continued...

(117) Requires package skew compensation with PCB trace length.

(118) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(119) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(120) The minimum specification depends on the following factors. The differential I/O buffer within the IOE does not have a minimum data rate.

- The clock source, such as the PLL and clock pin
- The clock and data routing resource

(121) You must perform design timing analysis in Quartus Prime to achieve timing closure and run IBIS/HSPICE simulations to ensure that the I/O buffer's electrical performance meets the interface requirements.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	t_{DUTY} (122)	TX output clock duty cycle for True Differential Signaling I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} and t_{FALL} (119) (123)	True Differential Signaling I/O Standards	—	—	160	—	—	160	—	—	200	ps
	T_{CCS} (117) (122)	True Differential Signaling I/O Standards	—	—	202	—	—	202	—	—	202	ps
Receiver	True Differential Signaling I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(118) (119)	600	—	1600(124)	600	—	1600(124)	600	—	1250(124)	Mbps
	SLVS400 I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(118) (119)	600	—	891	600	—	891	600	—	891	Mbps

continued...

(122) Not applicable for DIVCLK = 1.

(123) This applies to default pre-emphasis and V_{OD} settings only.

(124) 1.05 V, 1.1 V, and 1.2 V True Differential Signaling I/O standards on receiver supports data rate up to 1000 Mbps.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	f_{HSDR} (data rate) (without DPA)(117)	SERDES factor J = 4 and 8(118) (119)	150	—	(125)	150	—	(125)	150	—	(125)	Mbps
		SERDES factor J = 2, uses DDR registers	(120)	—	500(121)	(120)	—	500(121)	(120)	—	500(121)	Mbps
		SERDES factor J = 1, uses DDR registers	(120)	—	250(121)	(120)	—	250(121)	(120)	—	250(121)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	≤10,000	—	—	≤10,000	—	—	≤10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling window	—	—	—	330	—	—	330	—	—	330	ps

(125) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Table 64. E-Series Device Group B FPGAs LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 4 and 8.

DDR registers support SERDES factor J = 1 and 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential Signaling I/O Standards	Clock boost factor W = 1 to 40(126)	10	—	625	10	—	625	10	—	500	MHz
	f_{HSCLK_in} (input clock frequency) SLVS400 I/O Standards	Clock boost factor W = 1 to 40(126)	10	—	445.5	10	—	445.5	10	—	445.5	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40(126)	10	—	625	10	—	625	10	—	525	MHz
	f_{HSCLK_OUT} (output clock	—	—	—	625	—	—	625	—	—	500	MHz

continued...

(126) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	frequency) True Differential Signaling I/O Standards											
Transmitter	True Differential Signaling I/O Standards - f_{HSDR} (data rate)(127)	SERDES factor J = 4 and 8(128) (129)	600	—	1,250	600	—	1,250	600	—	1,000	Mbps
		SERDES factor J = 2, uses DDR registers	(130)	—	500(131)	(130)	—	500(131)	(130)	—	500(131)	Mbps
		SERDES factor J = 1, uses DDR registers	(130)	—	250(131)	(130)	—	250(131)	(130)	—	250(131)	Mbps

continued...

(127) Requires package skew compensation with PCB trace length.

(128) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(129) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(130) The minimum specification depends on the following factors. The differential I/O buffer within the IOE does not have a minimum data rate.

- The clock source, such as the PLL and clock pin
- The clock and data routing resource

(131) You must perform design timing analysis in Quartus Prime to achieve timing closure and run IBIS/HSPICE simulations to ensure that the I/O buffer's electrical performance meets the interface requirements.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	t_x Jitter - True Differential Signaling I/O Standards	Total jitter for data rate, 600 Mbps – 1.25 Gbps	≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			≤1,250 Mbps: 160 ≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			≤1,000 Mbps: 180 ≤800 Mbps: 210 600 Mbps: 240			ps
	t_{DUTY} (132)	TX output clock duty cycle for True Differential Signaling I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} and t_{FALL} (129) (133)	True Differential Signaling I/O Standards	—	—	160	—	—	160	—	—	200	ps
	T_{CCS} (127) (132)	True Differential Signaling I/O Standards	—	—	202	—	—	202	—	—	202	ps

continued...

(132) Not applicable for DIVCLK = 1.

(133) This applies to default pre-emphasis and V_{OD} settings only.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver(134)	True Differential Signaling I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(128) (129)	600	—	1250(135)	600	—	1250(135)	600	—	1000(135)	Mbps
	SLVS400 I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 and 8(128) (129)	600	—	891	600	—	891	600	—	891	Mbps
	f_{HSDR} (data rate) (without DPA)(127)	SERDES factor J = 4 and 8(128) (129)	150	—	(136)	150	—	(136)	150	—	(136)	Mbps
		SERDES factor J = 2, uses DDR registers	(130)	—	500(131)	(130)	—	500(131)	(130)	—	500(131)	Mbps
		SERDES factor J = 1, uses DDR registers	(130)	—	250(131)	(130)	—	250(131)	(130)	—	250(131)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	≤10,000	—	—	≤10,000	—	—	≤10,000	UI

continued...

(134) When operating in DPA mode, you must enable the receiver equalization feature of the input buffer.

(135) 1.05 V, 1.1 V, and 1.2 V True Differential Signaling I/O standards on receiver supports data rate up to 1000 Mbps.

(136) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Parameter	Symbol	Condition	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling window	—	—	—	330	—	—	330	—	—	330	ps

DPA Lock Time Specifications

Table 65. DPA Lock Time Specifications

The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

For specification status, see the *Data Sheet Status* table

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(137)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	768
Parallel Rapid I/O	00001111	2	128	768
	10010000	4	64	768
Miscellaneous	10101010	8	32	768
	01010101	8	32	768

(137) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

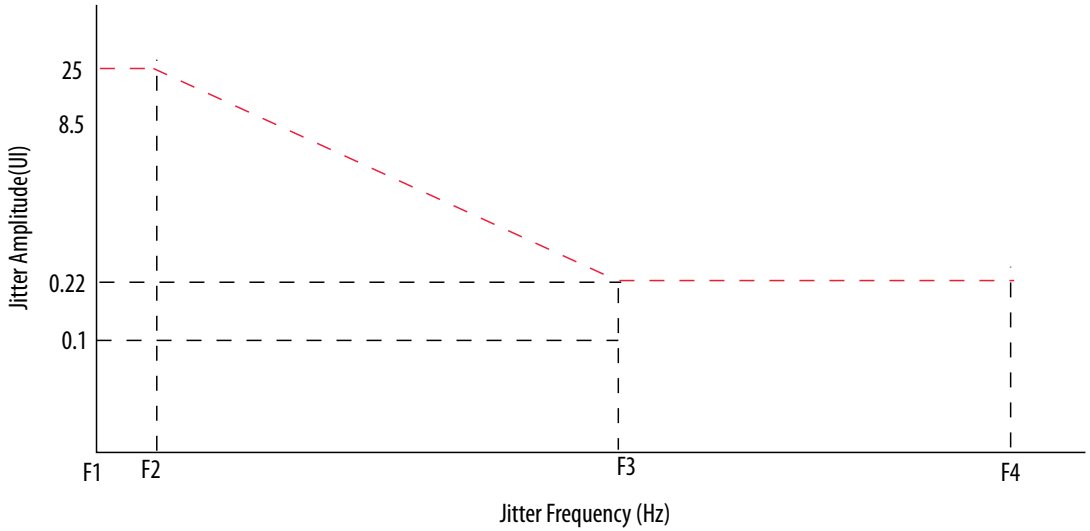
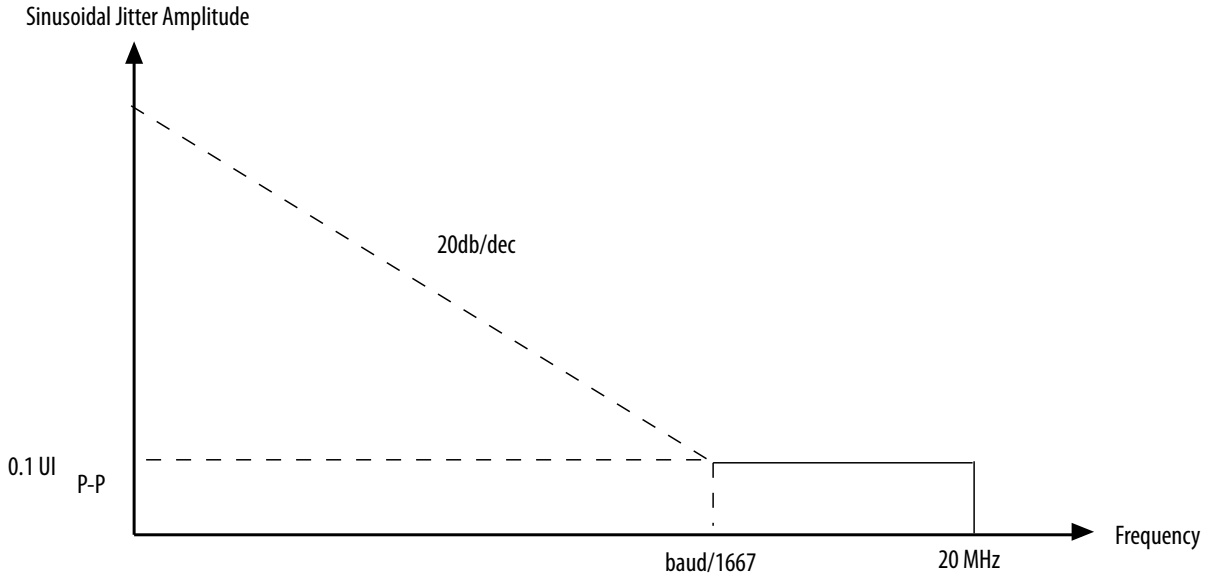


Table 66. LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

For specification status, see the *Data Sheet Status* table

Parameter	Jitter Frequency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25
F2	17,565	25
F3	1,493,000	0.22
F4	50,000,000	0.22

Figure 3. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported

Table 67. D-Series FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by D-Series FPGAs. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,600
DDR5 SDRAM	Hard memory controller	2,800
LPDDR4 SDRAM	Hard memory controller	2,133
LPDDR5 SDRAM	Hard memory controller	2,750

continued...

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	HPS hard memory controller	1,333
DDR5 SDRAM	HPS hard memory controller	2,600
LPDDR4 SDRAM	HPS hard memory controller	2,133
LPDDR5 SDRAM	HPS hard memory controller	2,600

Table 68. E-Series Device Group A FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by E-Series Device Group A. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,333
DDR5 SDRAM	Hard memory controller	1,800
LPDDR4 SDRAM	Hard memory controller	1,866
LPDDR5 SDRAM	Hard memory controller	1,866
DDR4 SDRAM	HPS hard memory controller	1,333
DDR5 SDRAM	HPS hard memory controller	1,800
LPDDR4 SDRAM	HPS hard memory controller	1,866
LPDDR5 SDRAM	HPS hard memory controller	1,866

Table 69. E-Series Device Group B FPGAs Memory Standards Supported

This table lists the overall capability of External Memory Interface supported by E-Series Device Group B. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,200
LPDDR4 SDRAM	Hard memory controller	1,333

continued...

Memory Standard	Controller Type	Maximum Frequency (MHz)
LPDDR5 SDRAM	Hard memory controller	1,066
DDR4 SDRAM	HPS hard memory controller	1,066
LPDDR4 SDRAM	HPS hard memory controller	1,333
LPDDR5 SDRAM	HPS hard memory controller	1,066

Related Information

External Memory Interface (EMIF) Spec Estimator

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Altera recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC* specifications when the phase jitter (integration bandwidth 10 kHz to 50 MHz) of the input clock is not more than 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER and 1.22 ps at $1e^{-16}$ BER.

MIPI D-PHY Performance

Table 70. D-Series FPGAs MIPI D-PHY Performance

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI D-PHY transmitter or receiver	High-speed interface, Hs	Long reference(138)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
		Short reference and standard reference(138)	150	—	3,500	150	—	3,500	150	—	3,500	Mbps
	Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz

(138) The long reference/standard reference/short reference is reference to the insertion loss condition from MIPI Alliance D-PHY specifications.

Table 71. E-Series FPGAs MIPI D-PHY Performance

For specification status, see the *Data Sheet Status* table

Parameter	Device Group	Symbol	Condition	–1, –4 Speed Grade			–2, –5 Speed Grade			–3, –6 Speed Grade			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI D-PHY transmitter or receiver	A	High-speed interface, Hs	Long reference(139)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
			Short reference and standard reference(139)	150	—	3,500	150	—	3,500	150	—	3,500	Mbps
		Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz
MIPI D-PHY transmitter or receiver	B	High-speed interface, Hs	Short reference, standard reference, or long reference (139)	150	—	2,500	150	—	2,500	150	—	2,500	Mbps
		Low-power interface, Lp	—	—	—	20	—	—	20	—	—	20	MHz

(139) The long reference/standard reference/short reference is reference to the insertion loss condition from MIPI Alliance D-PHY specifications.

GTS Transceiver Performance Specifications

GTS Transceiver Performance

Table 72. Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Transceiver Speed	Unit
Supported data rate for E-Series Device Group B (NRZ)	1 – 17.16	Gbps
Supported data rate for E-Series Device Group A (NRZ)	1 – 28.1	Gbps
Supported data rate for D-Series (NRZ)	1 – 28.1	Gbps

GTS Transceiver Reference Clock Specifications

Table 73. GTS Transceiver and System PLL Reference Clock Input Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
—	Supported I/O standards	Dedicated reference clock pin	CML, HCSL			
F_{REF}	Reference clock operating frequency	—	100(140)	—	380	MHz
$T_{REF-DUTY}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE/FALL}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
SSC	Spread-spectrum downspread	PCIe*	—	–5,000 to 0	—	ppm
$T_{REF-SINGLEEND-SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	50	ps

continued...

(140) This value is 100 MHz for down spread spectrum clocking (SSC). This value can also be 25 MHz for HDMI rate of less than 1 Gbps.

Symbol	Description	Condition	Min	Typical	Max	Unit
$Z_{REF-DIFF-DC}$	Reference clock differential input impedance – terminated mode	—	80	100	120	Ω
$V_{min-ABS}$	Absolute V_{min}	—	–0.15	—	—	V
$V_{max-ABS}$	Absolute V_{max}	—	—	—	0.85	V
$V_{REFIN-DIFF-AC}$	Input reference clock differential peak-to-peak voltage when AC-coupled on board	—	0.6	1.2	1.7	V
$V_{REFIN-IL-DC}$	Input reference clock input low voltage when DC-coupled on board	—	–0.15	0	0.15	V
$V_{REFIN-IH-DC}$	Input reference clock input high voltage when DC-coupled on board	—	0.66	0.7	0.85	V
$V_{REFIN-CM-AC}$	Input reference clock common-mode voltage when AC-coupled on board	—	Set on chip			V
$V_{REFIN-CM-DC}$	Input reference clock common-mode voltage when DC-coupled on board	—	0.255	0.35	0.5	V
PN_{REF}	Transmitter REFCLK phase noise (156.25 MHz)(141) (140)	10 kHz	—	—	–130	dBc/Hz
		100 kHz	—	—	–138	dBc/Hz
		500 kHz	—	—	–138	dBc/Hz
		3 MHz	—	—	–140	dBc/Hz

continued...

(141) To calculate the REFCLK phase noise requirement at frequencies other than 156.25 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + 20 × log(f/156.25 MHz).

Symbol	Description	Condition	Min	Typical	Max	Unit
		10 MHz	—	—	–144	dBc/Hz
		20 MHz	—	—	–146	dBc/Hz
		1 GHz	—	—	–146	dBc/Hz
$V_{REFIN-RJ-RMS}$	RMS jitter integrated from 10 kHz – 20 MHz including spurs	—	—	—	522	fs
$V_{REFIN-PPM-ERROR}$	Reference clock frequency error	—	–350 + SSC	—	+350 + SSC	ppm
R_{COMP}	External resistor for calibration	—	—	499 ± 0.1%	—	Ω

Table 74. System PLL Reference Clock (Using HVIO) Specifications

For specifications on the I/O PLL using HVIO pin, refer to *D-Series FPGAs I/O PLL Specifications* or *E-Series FPGAs I/O PLL Specifications* respectively.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF}	Clock input frequency	Powered by V_{CCIO_HVIO}	25	—	125	MHz
$T_{REF-DUTY}$	Clock input duty cycle		45	50	55	%

Table 75. GTS Transceiver Reference Clock Output Driver Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typical	Max	Unit
F_{REF_OUT}	Reference clock operating frequency	—	25	—	380	MHz
$T_{REF-DUTY\_OUT}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE\_OUT/FALL\_OUT}$	Rise and fall time (as percentage of period)	20% – 80%	—	—	0.15	T_{REF}
$T_{REF-SINGLEEND-SKEW}$	Skew between `REFCLKP` and `REFCLKN`	—	—	—	50	ps

continued...

Symbol	Description	Condition	Min	Typical	Max	Unit
$Z_{REF-DIFF-DC\_OUT}$	Reference clock differential output impedance – terminated mode	—	80	100	120	Ω
$V_{REF-DIFF-AC\_OUT}$	Output reference clock differential peak to peak voltage when AC-coupled on board	—	0.9	1	1.1	V
$V_{REF-CM-OUT}$	Output reference clock common-mode	—	0.45	0.5	0.55	V

Transmitter Specifications

Table 76. Transmitter Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Transmitter differential on-chip termination resistors	—	80	90	120	Ω
Transmitter output eye specifications	$V_{TX-DIFF-PKPK}$	Back-porch transmit amplitude	—	300	—	1,050	mV
	$V_{TX-DEEMP\_STEP}$	Transmitter tap resolution	—	—	—	2	%
	$D_{TX-PRE\_TAP\_2}$	Pre-cursor tap 2 de-emphasis	—	0	—	2.5	dB
	$D_{TX-PRE\_TAP\_1}$	Pre-cursor tap 1 de-emphasis	—	0	—	4.5	dB
	$D_{TX-POST\_TAP\_1}$	Post-cursor tap 1 de-emphasis	—	0	—	6.5	dB
	$T_{TX-SLEW}$	Rise/fall time at 20%–80%	—	10	—	20	ps

continued...

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	T_{TX-DJ}	Transmitter deterministic jitter at 25 Gbps	—	—	—	0.15	UI_{pkpk}
	T_{TX-RJ}	Transmitter total peak-peak random jitter(142)	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}
	T_{TX-TJ}	Transmitter total peak-peak jitter ($T_{TX-TJ} = T_{TX-DDJ} + T_{TX-PJ} + T_{TX-RJ}$)(142)(143)	At BER of 10^{-12}	—	—	0.28	UI_{pkpk}
Transmitter DC impedance	$Z_{TX-DIFF-DC}$	Transmitter output differential DC impedance with OCT 90 Ω mode while configured(144)	—	80	90	120	Ω
	$Z_{TX-CM-DC}$	Transmitter output common-mode DC impedance	—	20	22.5	30	Ω
Transmitter return loss	$Z_{RL-DIFF-DC}$	Transmitter differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Transmitter differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB

continued...

(142) Assume a 1st order high-pass jitter measurement filter with a cutoff of $F_{BAUD}/F_{GPLL} = N_{GPLL}$, where N_{GPLL} is the ratio of the 3 dB cutoff frequency to the data rate, with typical value of 1,667.

(143) The maximum TJ value is slightly less than the sum of DDJ + PJ + RJ to take into consideration of the worst case probability, where both deterministic and random jitter component might present at the same time.

(144) TX pins are driven to 0 V before configuration.

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	Z_{RL-CMN}	Transmitter common-mode return loss below 10 GHz	—	—	—	–6	dB
Electrical idle	$V_{TX-IDLE}$	Electrical idle output voltage	PCIe/ SATA/SAS/USB	—	—	20	mV
	$V_{CM-DELTA-SQUELCH}$	Maximum common-mode step entering/ exiting squelch mode		—	—	100	mV
	$T_{TX-IDLE-LATENCY}$	Latency entering/ exiting electrical idle		—	—	8	µs
Receiver detect	$V_{TX-RCV-DETECT}$	Receiver detect voltage change allowed during receiver detection	PCIe/ SATA/SAS/USB	—	—	600	mV
Lane-to-lane output skew	—	Lane-to-lane output skew	4 < Lane count ≤ 8	—	—	2 UI + 250 ps	ps
			Lane count ≤ 4	—	—	2 UI + 166 ps	ps

Receiver Specifications

Table 77. Receiver Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
On-chip termination	—	Receiver differential on-chip termination resistors	—	65	85	102	Ω
				80	100	120	Ω
Receiver input eye specifications	$V_{RX-DIFF-PKPK}$	Receiver input differential peak-to-peak voltage (145)	—	Closed eye (146)	—	1,200	mV

continued...

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	V_{RX-MAX}	Receiver input maximum voltage (147)	—	—	—	1	V
	V_{RX-MIN}	Receiver input minimum voltage(147)	—	–0.3	—	—	V
	$V_{RX-CM-DC}$	Receiver input DC common-mode voltage (148)	When squelch detector is not enabled	0	—	700	mV
			When squelch detector is enabled	200	—	300	mV
	T_{RX-RJ}	Receiver input random jitter	At BER of 10^{-12}	—	—	0.15	UI_{pkpk}
	T_{RX-PJ}	Receiver input periodic jitter (at high frequency)(149)	—	—	—	0.05	UI_{pkpk}
Insertion loss specification	$I_{INS-LOSS-28Gb/s\_BER10-15}$	Insertion loss at Nyquist frequency ($F_{BAUD}/2$) (150)	At BER of 10^{-15}	—	—	–27	dB
	$I_{INS-LOSS-28Gb/s\_BER10-12}$		At BER of 10^{-12}	—	—	–30	dB

continued...

(145) This is supported when the receiver is powered and configured, powered and unconfigured, or unpowered.

(146) Closed eye at the Receiver input buffer can be recovered and opened up with the GTS Receiver equalizer.

(147) V_{RX_MAX} and V_{RX_MIN} are before and after configuration.

(148) The specified common-mode range is supported when the receiver is powered and configured, powered and unconfigured, or unpowered. This specification is also supported before mode configuration. If squelch detect is used, receiver DC input common-mode voltage should be within 200 mV to 300 mV. Otherwise, use AC coupling capacitors on board.

(149) High frequency is defined as frequencies beyond the CDR loop bandwidth (typically $F_{BAUD}/1,667$).

(150) COM compliant package and channel.

Parameter	Symbol	Description	Condition	Min	Typical	Max	Unit
	$I_{INS-LOSS-17Gb/s\_BER10-12}$	Insertion loss at Nyquist frequency ($F_{BAUD}/2$) (150)	At BER of 10^{-12}	—	—	–30	dB
Receiver return loss	$Z_{RL-DIFF-DC}$	Receiver differential DC return loss	—	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Receiver differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	—	–6	dB
	Z_{RL-CM}	Receiver common-mode return loss below 10 GHz	—	—	—	–6	dB
Receiver DC impedance	$R_{DIFF-DC}$	Receiver differential DC impedance	85 Ω on-chip termination	65	85	102	Ω
			100 Ω on-chip termination	80	100	120	Ω
	R_{CM-DC}	Receiver common-mode DC impedance	—	20	25	30	Ω
Receiver signal detection (151)	$V_{IDLE-THRESH}$	Receiver signal detect input voltage threshold	—	75	120	175	mV

(151) Receiver signal detection values in this table are applicable to PCIe and similar standards, such as SATA, where a clock pattern like PCIe EIEOS 500 MHz clock pattern is used.

Electrical Compliance

Table 78. Electrical Compliance List

For specification status, see the *Data Sheet Status* table

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
XFP MSA	XFI	10.3125	10.3125
IEEE 802.3ba-2010	XLPPI	10.3125	10.3125
Serial-GMII Specification V1.7	1GE SGMII	1.25	1.25
IEEE 802.3ba	XLAUI	10.3125	10.3125
IEEE 802.3ba	CAUI-10	10.3125	10.3125
IEEE 802.3by	25GAUI-C2C/C2M	—	1x25.78125
IEEE 802.3ap 2007	10GBASE-KR	10.3125	10.3125
IEEE 802.3by 111/110	25GBASE-KR/CR	—	25.78125
IEEE 803.3ap-2007 IEEE 802.3an-2006	1000BASE-KX/CX	1.25	1.25
OIF-CEI 4.0	OIF-CEI-11G SR/MR/LR	9.95 – 11.2	9.95 – 11.2
	OIF-CEI-6G SR/LR	4.976 – 6.375	4.976 – 6.375
	OIF-CEI-28G VSR/SR/MR	—	24 – 28.1
	OIF-CEI-25G LR	—	24 – 28.1
G.709 G.sup56 G.sup43 G.sup58	OTU1	—	1.327451, 2.666
	OTU2	—	10.709, 11.049, 11.270
	OTU2e	—	11.095
	OTU2f	—	11.317, 11.846, 12.639
	OTU4 OTL4.4	—	4x27.952493
	OTU4 OTLC.4	—	4x28.076177

continued...

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
PCIe BASE 4.0 PIPE 4.4.1	PCIe 3.0 , PCIe 4.0	8, 16(152)	8, 16
SMPTE 259M	SDI SD	0.27	0.27
SMPTE 292M	SDI HD	1.485/1.483	1.485/1.483
SMPTE ST 424	SDI 3G	2.97/2.967	2.97/2.967
SMPTE ST 2081	SDI 6G	5.94/5.934	5.94/5.934
SMPTE ST 2082	SDI 12G	11.88/11.868	11.88/11.868
CPRI V7.0	CPRI	1.2288	1.2288
		2.4576	2.4576
		3.072	3.072
		4.9152	4.9152
		6.144	6.144
		8.1101	8.1101
		9.8304	9.8304
		10.1376	10.1376
		—	24.33024
JESD204B	JESD204B	up to 17.16	up to 19.66
JESD204C	JESD204C	up to 17.16	up to 28.1
DP 2.0	DisplayPort 1.4	1.62	1.62
		2.7	2.7
		5.4	5.4
		8.1	8.1

continued...

(152) PCIe 4.0 is supported for –4S (V_{CC} = 0.8 V) devices only.

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
	DisplayPort 2.0	10	10
		13.5	13.5
		—	20
FC-PI-2	Fiber Channel	1.0625	1.0625
		2.125	2.125
FC-PI-5		4.25	4.25
		8.5	8.5
10GFC		10.518	10.518
FC-PI-5		14.025	14.025
FC-PI-6		—	28.05
		—	4x28.05
Serial ATA revision 3.5a T10/BSR INCITS 519	Sata Gen 3	1.5 – 6	1.5 – 6
	SAS	1.5 – 12.0	1.5 – 22.5
G.984	GPON/EPON	—	1.244, 1.250, 2.488, 9.952, 10.313, 25
OIF-CEI-6G-SR	Interlaken	6.25	6.25
OIF-CEI-11G-SR		10.3125	10.3125
OIF-CEI-11G-SR+		12.5	12.5
OIF-28G MR (OIF-CEI 3.0)		—	25.78125
HDMI 1.4	HDMI	3.4	3.4
HDMI 2.0		6	6
HDMI 2.1		—	up to 12
SLVS-EC Specification Version 1.0	SLVS-EC RX	2.376	2.376
SLVS-EC Specification Version 2.0		5	5

continued...

Specification/Clause	Protocol	Lane Rate (Gbps)	
		E-Series Device Group B	E-Series Device Group A, D-Series
SFF-8402	SFP+	9.95 – 11.2	9.95 – 11.2
SFF-8431 4.1			
SFF-8431 Rev 4.1			
SFF-8418			
USB 3.1, USB 3.2	USB 3.1 Gen 1	5	5
	USB 3.2 Gen 2 (153)	—	10 (153)
RapidIO™ Interconnect Specification	SRIO	2 – 16	2 – 16

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing.

HPS Clock Performance

Table 79. D-Series SoC Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)(154)	Cortex-A55 Core Frequency (MHz)	Cortex-A76 Core Frequency (MHz)	DSU (DynamIQ Shared Unit) Frequency (MHz) (mpu_free_clk)	L3 Frequency (MHz) (l3_main_free_clk)	DDR4/LPDDR4/ DDR5/LPDDR5 Clock (MHz)
–1 speed grade	SmartVID	1,500	1,800	1,200	400	Refer to the *Memory Standards Supported* table.
–2 speed grade	SmartVID	1,333	1,600	1,066	400	
–3 speed grade	SmartVID	1,250	1,400	933	400	

(153) Gen 2 is supported using transceiver PMA only, with soft PIPE PCS and USB 3.2 controller in core fabric.

(154) V_{CCL_HPS} refers to $V_{CCL\_HPS\_CORE0\_CORE1}$ for HPS Cortex-A55 core 0 and core 1 power rail, $V_{CCL\_HPS\_CORE2}$ for HPS Cortex-A76 core 2 power rail, and $V_{CCL\_HPS\_CORE3}$ for HPS Cortex-A76 core 3 power rail.

Table 80. E-Series SoC Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)(155)	Cortex-A55 Core Frequency (MHz)	Cortex-A76 Core Frequency (MHz)	DSU (DynamIQ Shared Unit) Frequency (MHz) (mpu_free_clk)	L3 Frequency (MHz) (l3_main_free_clk)	DDR4/LPDDR4/ DDR5/LPDDR5 Clock (MHz)
–1 speed grade	SmartVID	1,500	1,800	1,200	400	Refer to the *Memory Standards Supported* table.
–2 speed grade	SmartVID	1,333	1,600	1,066	400	
–3 speed grade	SmartVID	1,250	1,400	933	400	
–4 speed grade	Fixed: 0.8	1,250	1,400	933	400	
–5 speed grade	Fixed: 0.78	800	800	533	400	
–6 speed grade	Fixed: 0.75	800	800	533	400	

Related Information

- HPS Power Supply Operating Conditions on page 34
- Memory Standards Supported on page 91

HPS Internal Oscillator Frequency

Table 81. HPS Internal Oscillator Frequency

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Internal oscillator frequency	150	300	400	MHz

(155) V_{CCL_HPS} refers to $V_{CCL\_HPS\_CORE0\_CORE1}$ for HPS Cortex-A55 core 0 and core 1 power rail, $V_{CCL\_HPS\_CORE2}$ for HPS Cortex-A76 core 2 power rail, and $V_{CCL\_HPS\_CORE3}$ for HPS Cortex-A76 core 3 power rail.

HPS PLL Specifications

Table 82. HPS PLL Input Requirements

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Pin Connection Guidelines* of this device for information about assigning this pin.

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	ppm
Clock input duty cycle	45	50	55	%

Table 83. HPS PLL Performance

For specification status, see the *Data Sheet Status* table

Description	Min	Max	Unit
Main PLL VCO output	—	4,000(156)	MHz
Peripheral PLL VCO output	—	4,000(156)	MHz
h2f_user0_clk(157)	—	500	MHz
h2f_user1_clk(157)	—	500	MHz

(156) For E-Series SoC, the maximum VCO output is 3,500 MHz for -5 and -6 speed grade.

(157) The HPS PLL provides this clock to the FPGA fabric.

HPS Cold Reset

Table 84. HPS Cold Reset

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
t_{RST0}	Minimum time for `HPS_COLD_nRESET` asserted(158)	3	—	ms

HPS SPI Timing Characteristics

Table 85. SPI Master Timing Requirements

You can adjust the input delay timing by programming the `rx_sample_dly` register.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
f_{clk}	SPIM_CLK clock frequency	—	—	60	MHz
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns

continued...

(158) `HPS_COLD_nRESET` may be ignored if HPS is not running or if the device is being configured.

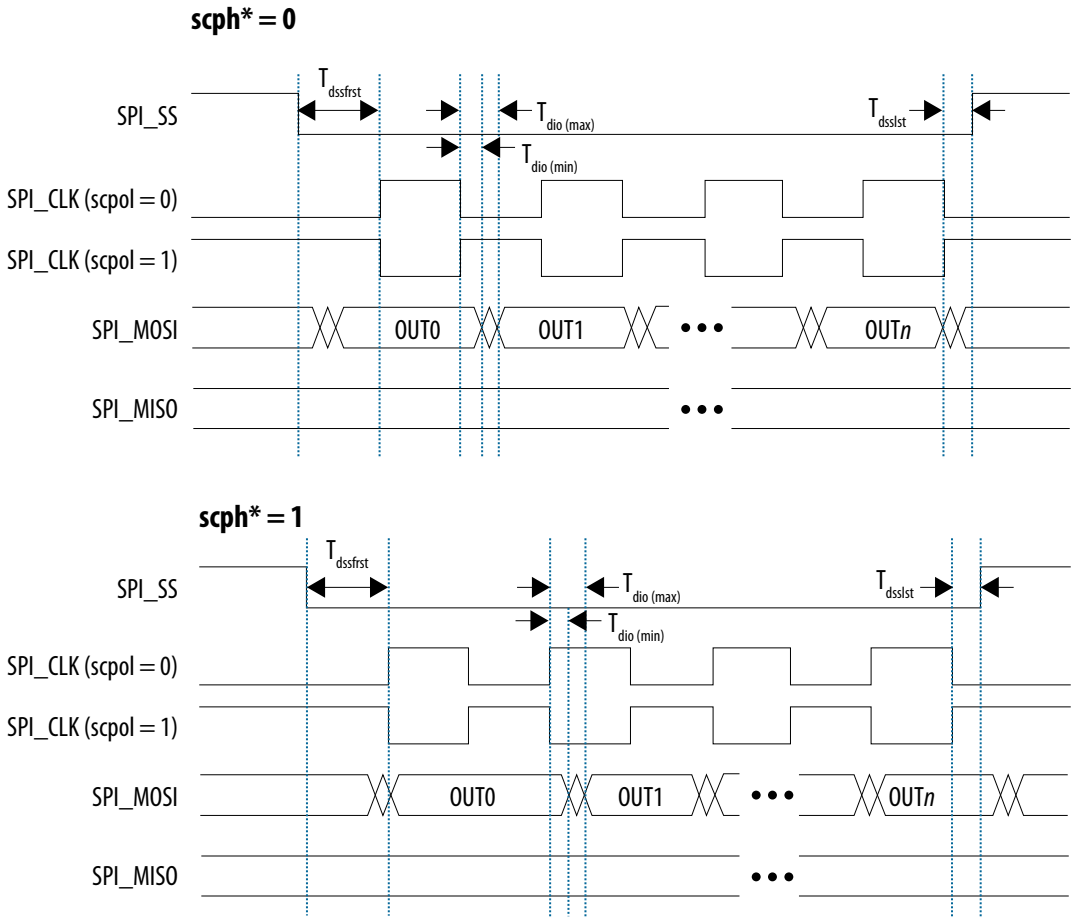
Symbol	Description	Min	Typ	Max	Unit
$T_{dssfrst}$ (159)	SPI_SS_N asserted to first SPIM_CLK edge	(1.5 × T_{clk}) – 2	—	—	ns
T_{dsslst} (159)	Last SPIM_CLK edge to SPI_SS_N deasserted	T_{clk} – 2	—	—	ns
T_{su} (160)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	5.0 – (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(161)	—	—	ns
T_h (160)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly` x $T_{spi\_ref\_clk}$)(161)	—	—	ns

(159) SPI_SS_N behavior differs depending on Motorola SPI protocols, Texas Instruments Synchronous Serial Protocols, or National Semiconductor Microwire operational mode.

(160) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for Texas Instruments Synchronous Serial Protocols, the capture edge is the falling edge; for National Semiconductor Microwire, the capture edge is the rising edge.

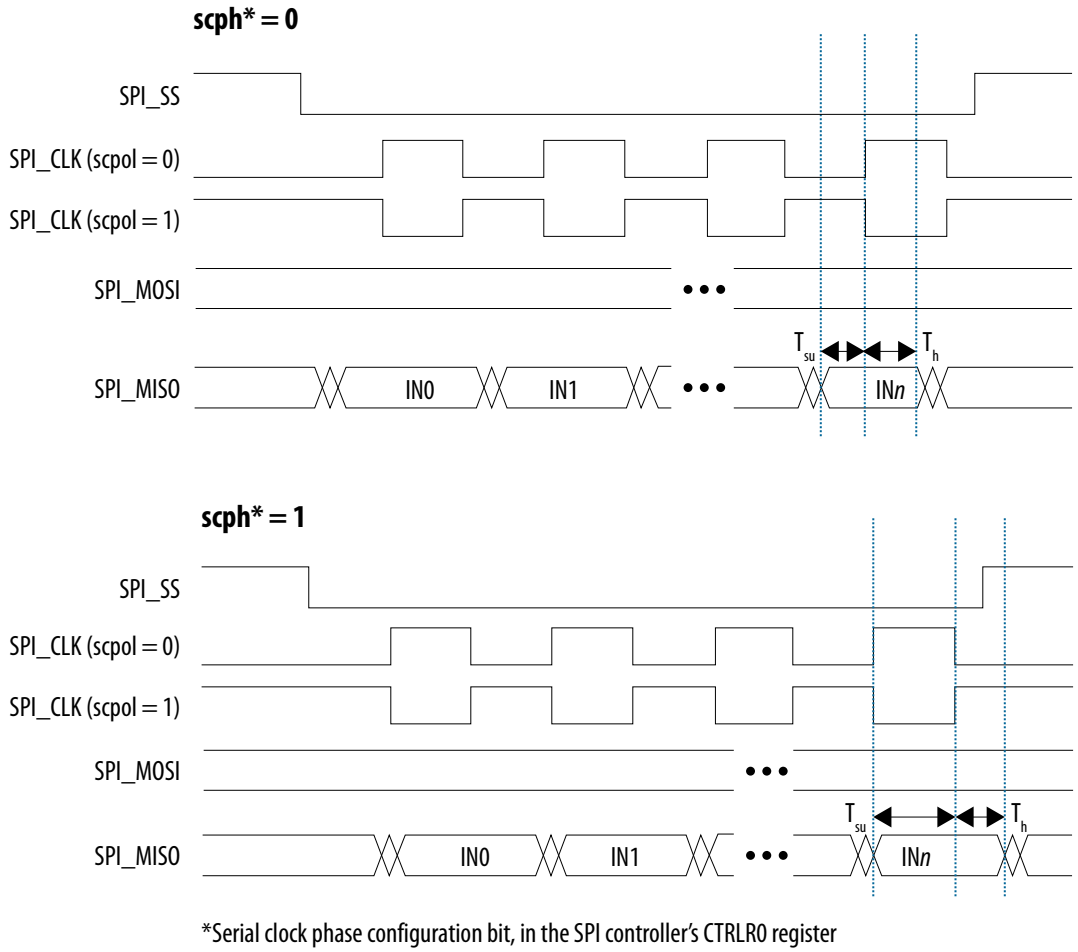
(161) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps).

Figure 4. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 5. SPI Master Input Timing Diagram



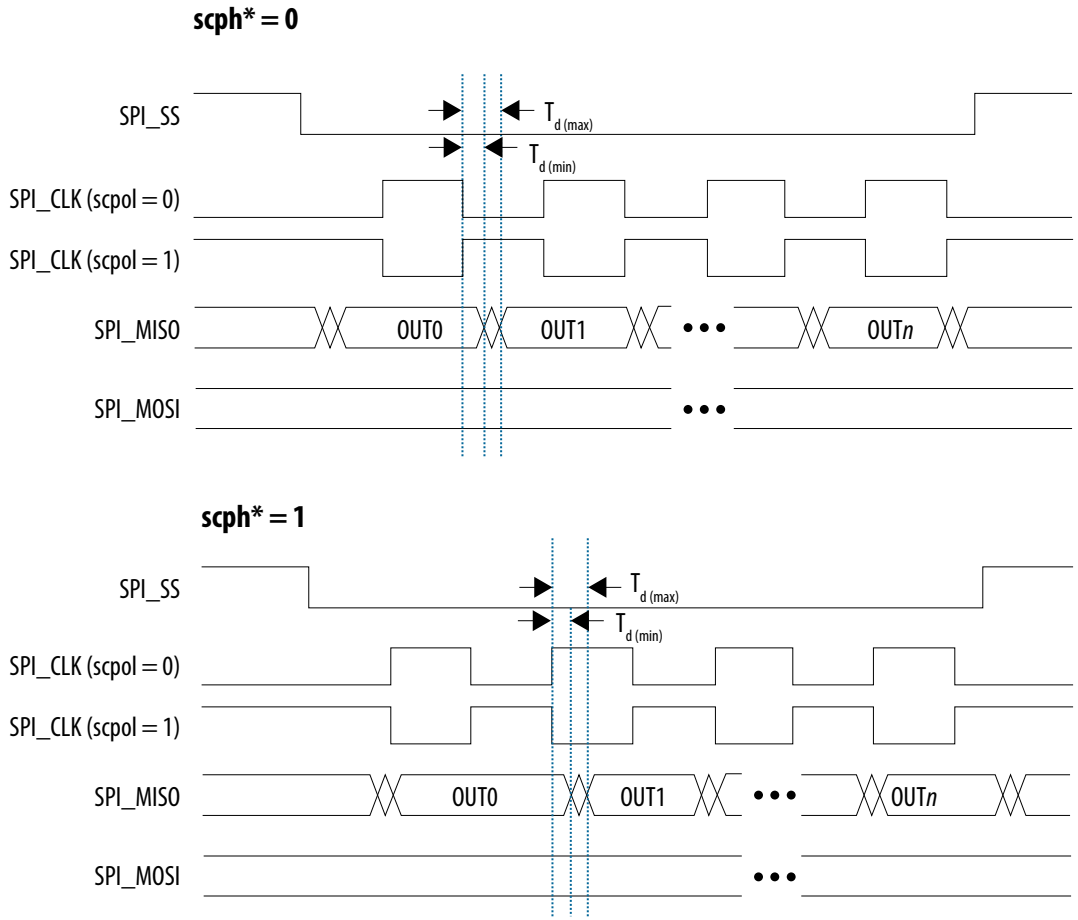
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 86. SPI Slave Timing Requirements

For specification status, see the *Data Sheet Status* table

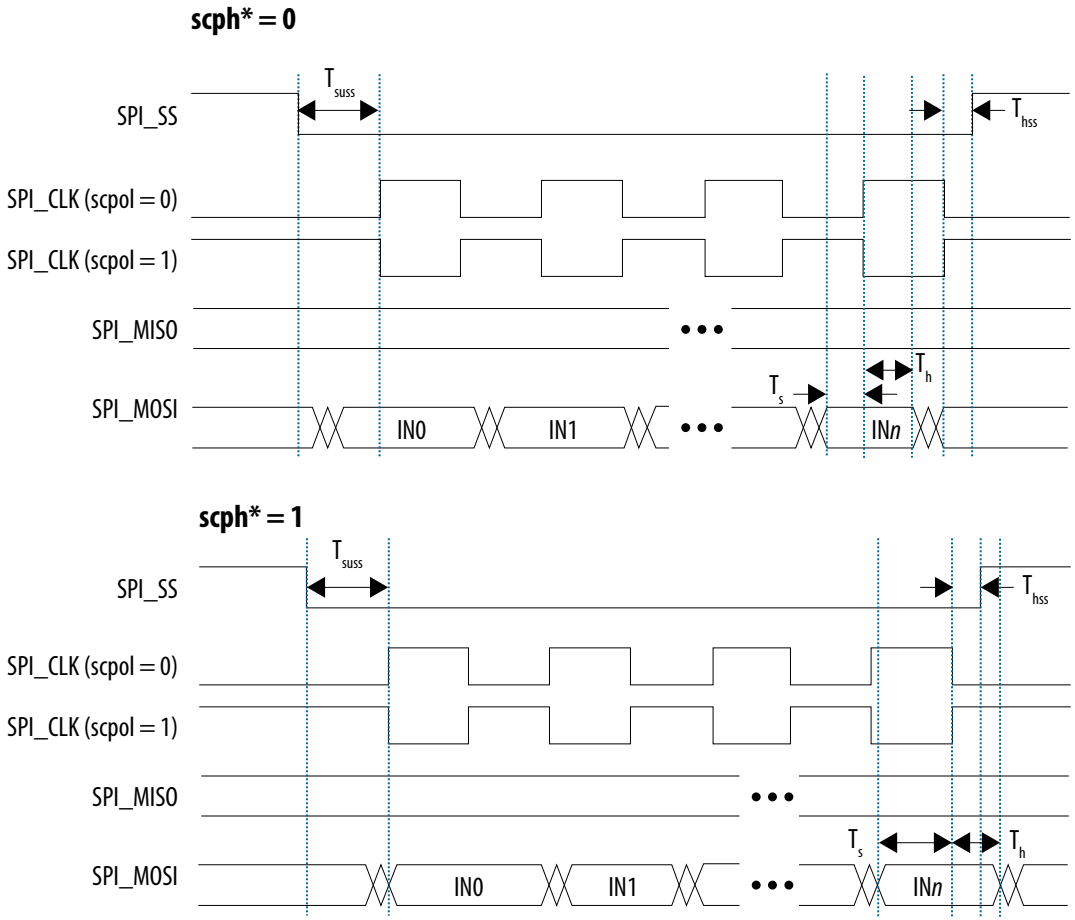
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
f_{clk}	SPIM_CLK clock frequency	—	—	33	MHz
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4.2$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4.2$	—	—	ns

Figure 6. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 7. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

HPS SD/eMMC Timing Characteristics

Table 87. HPS Secure Digital (SD)/Embedded MultiMediaCard (eMMC) Timing Requirements

Supports SD devices up to V6.1. Supports SDIO devices up to V4.1. Supports SD/eMMC devices up to V5.1.

These timings apply to SD, MMC, and eMMC cards operating at 1.8 V.

For specification status, see the *Data Sheet Status* table

Symbol	Description		Min	Typ	Max	Unit
T_{sdmmc_cclk}	SD SDMMC_CCLK clock period	Identification mode, 400 kHz	2,500	—	—	ns
		SDR12, 25 MHz	40	—	—	ns
		SDR25, 50 MHz	20	—	—	ns
		SDR50, 100 MHz	10	—	—	ns
		SDR104, <200 MHz	5	—	—	ns
		DDR50, 50 MHz	20	—	—	ns
	eMMC SDMMC_CCLK clock period	Legacy, 25MB/s, 25 MHz	40	—	—	ns
		HS_SDR, 50MB/s, 50 MHz	20	—	—	ns
		HS_DDR, 100MB/s, 50 MHz	20	—	—	ns
		HS200, SDR, 200MB/s, 200 MHz	5	—	—	ns
		HS400, DDR, 400MB/s, 200 MHz	5	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle		45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter		—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4 (200 MHz)		5	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

Table 88. SD Input Timing (SDR104, SDR50, SDR25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{is}	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR104)	1.4	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR50)	3	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR25)	6	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input setup (SDR12)	5	—	—	ns
T_{ih}	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR104)	0.8	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR50)	0.8	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR25)	2	—	—	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] input hold (SDR12)	5	—	—	ns

Figure 8. SD Input (SDR104, SDR50, SDR25, SDR12) Timing Diagram

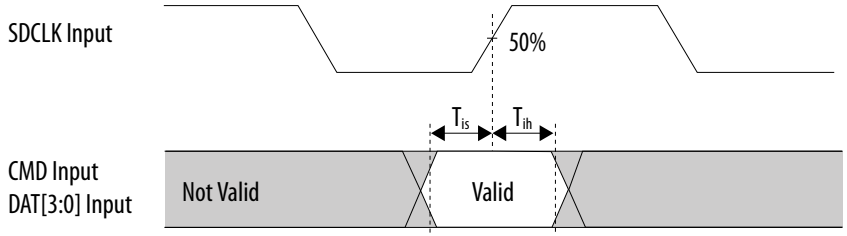


Table 89. SD Output Timing (SDR50, SDR25, SDR12)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{odly}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR50)	—	—	7.5	ns
	SDMMC_CMD/ SDMMC_DATA[7:0] output delay (SDR25, SDR12)	—	—	14	ns
T_{ohld}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 9. SD Output (SDR50, SDR25, SDR12) Timing Diagram

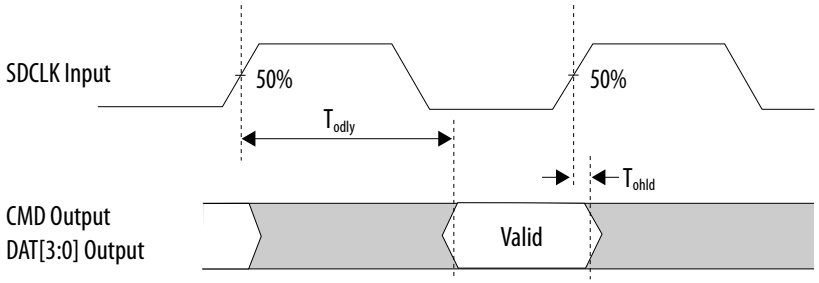


Table 90. SD Output Timing (SDR104)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{op}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{odw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 10. SD Output (SDR104) Timing Diagram

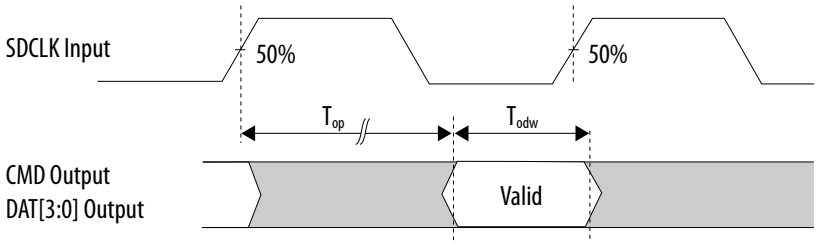


Table 91. SD Timing (DDR50)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	SDMMC_CMD input setup	6	—	—	ns
T_{ih}	SDMMC_CMD input hold	0.8	—	—	ns
T_{odly}	SDMMC_CMD output delay	—	—	13.7	ns
T_{oh}	SDMMC_CMD output hold	1.5	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
T_{isu2x}	SDMMC_DATA[7:0] input setup	3	—	—	ns
T_{ih2x}	SDMMC_DATA[7:0] input hold	0.8	—	—	ns
T_{odly2x}	SDMMC_DATA[7:0] output delay	—	—	7	ns
T_{odly2x}	SDMMC_DATA[7:0] output hold	1.5	—	—	ns

Figure 11. SD (DDR50) Timing Diagram

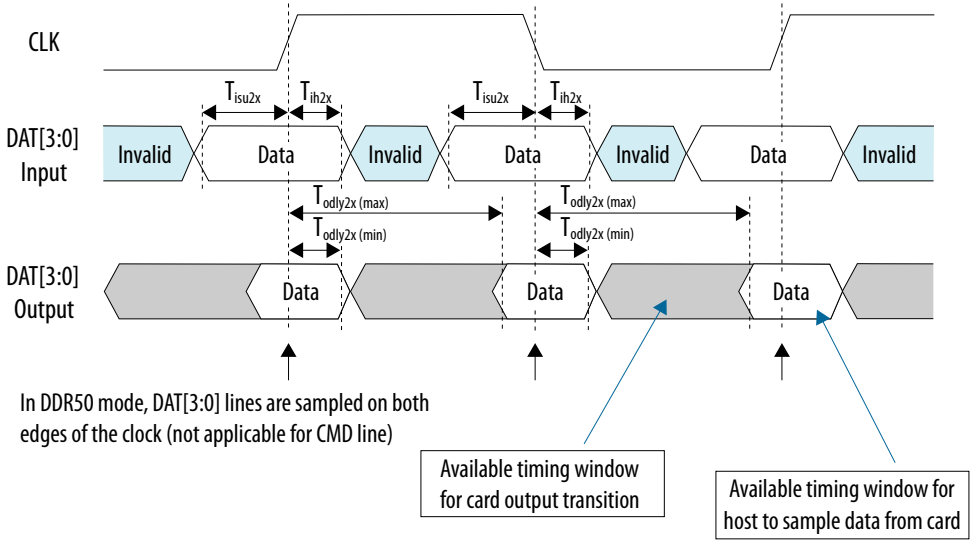
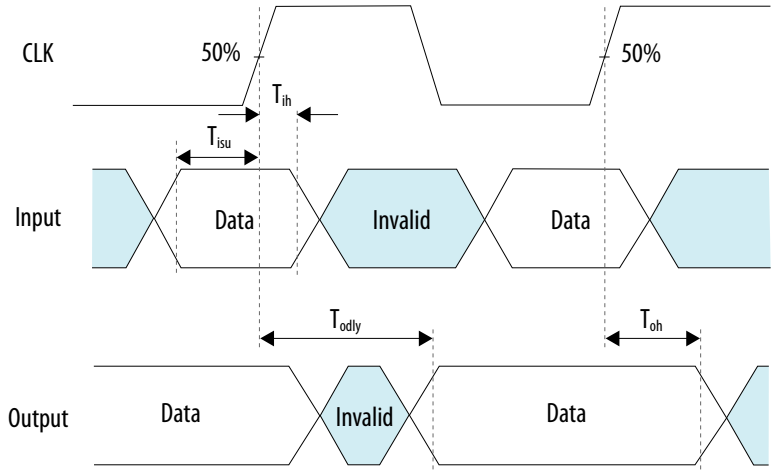


Table 92. eMMC Timing (Legacy, HS_SDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup (Legacy)	3	—	—	ns
	EMMC_CMD_DATA input setup (HS_SDR)	3	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold (Legacy)	3	—	—	ns
	EMMC_CMD DATA_input hold (HS_SDR)	3	—	—	ns
T_{odly}	EMMC_CMD_DATA output delay (Legacy)	—	—	13.7	ns
	EMMC_CMD_DATA output delay (HS_SDR)	—	—	13.7	ns
T_{oh}	EMMC_CMD_DATA output hold (Legacy)	8.3	—	—	ns
	EMMC_CMD DATA_output hold (HS_SDR)	2.5	—	—	ns

Figure 12. eMMC (Legacy, HS_SDR) Timing Diagram



Data must always be sampled on the rising edge of the clock.

Table 93. eMMC Timing (HS_DDR)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	2.5	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	2.5	—	—	ns
T_{odly_ddr}	EMMC_CMD_DATA output delay (max=delay, min=hold)	1.5	—	7	ns

Figure 13. eMMC (HS_DDR) Timing Diagram

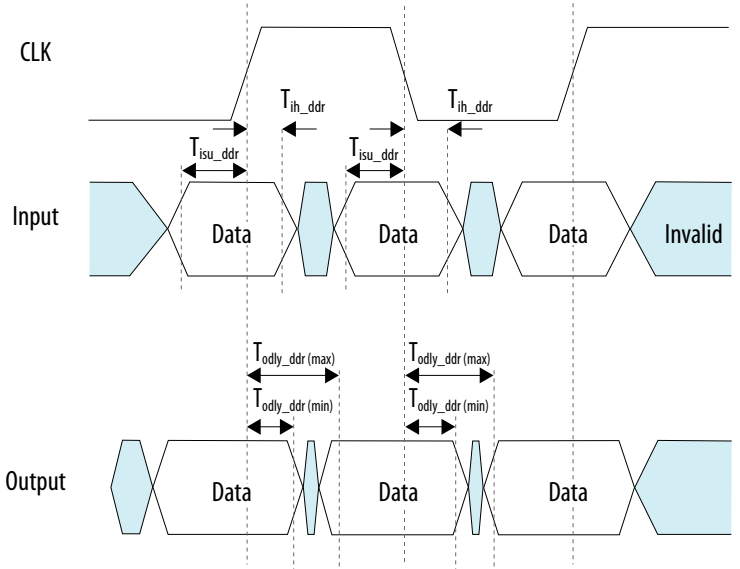


Table 94. eMMC Timing (HS200)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu}	EMMC_CMD_DATA input setup	1.4	—	—	ns
T_{ih}	EMMC_CMD DATA_input hold	0.8	—	—	ns

continued...

Symbol	Description	Min	Typ	Max	Unit
T_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{ph}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	1,550	ps
T_{vw}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	3	—	—	ns

Figure 14. eMMC Input (HS200) Timing Diagram

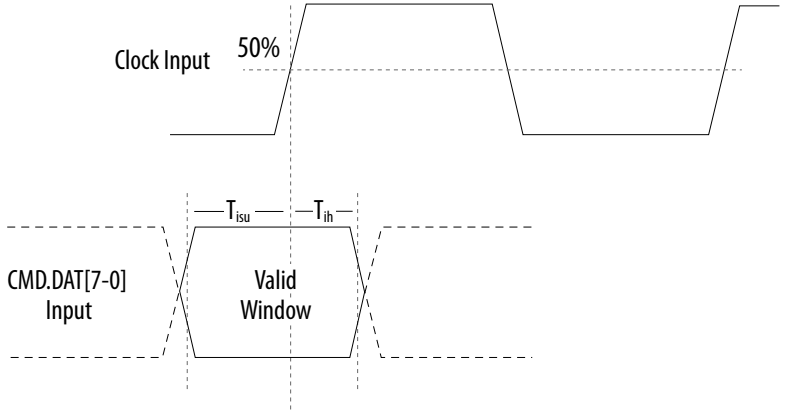


Figure 15. eMMC Output (HS200) Timing Diagram

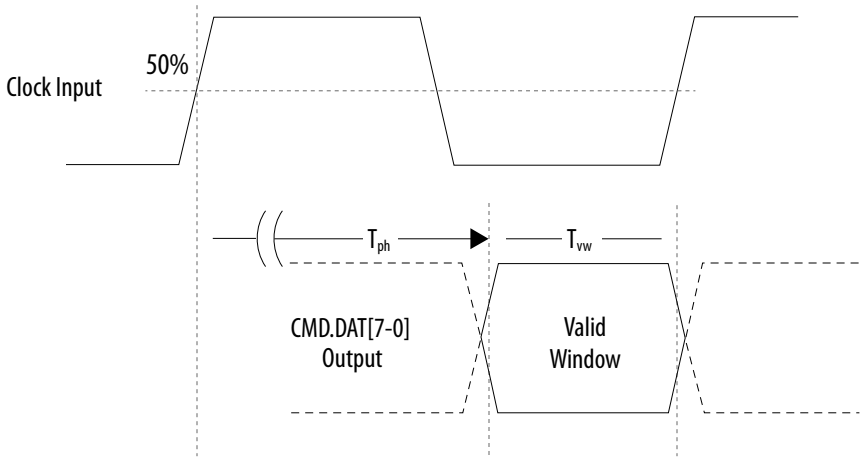


Table 95. eMMC Timing (HS400)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{isu_ddr}	EMMC_CMD_DATA input setup	0.4	—	—	ns
T_{ih_ddr}	EMMC_CMD DATA_input hold	0.4	—	—	ns
T_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output phase	0	—	10	ns
ΔT_{rq}	SDMMC_CMD/ SDMMC_DATA[7:0] output delay variation due to temperature change after tuning	–350	—	200	ps
T_{rqh}	SDMMC_CMD/ SDMMC_DATA[7:0] output hold	2	—	—	ns

Figure 16. eMMC Input (HS400) Timing Diagram

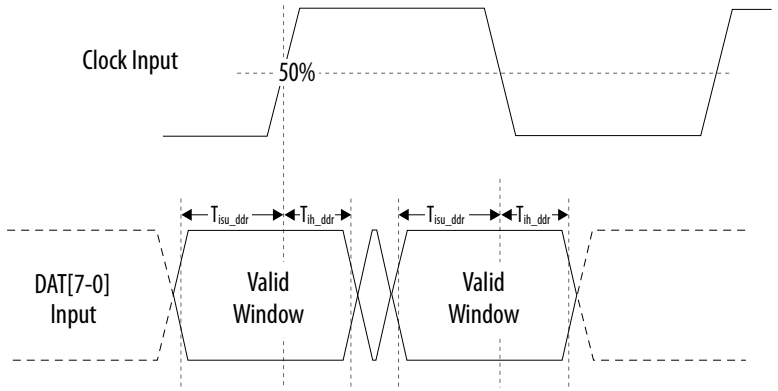
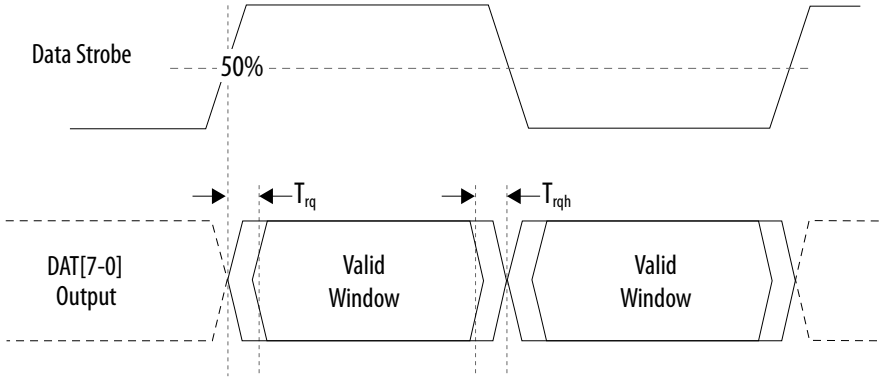


Figure 17. eMMC Output (HS400) Timing Diagram



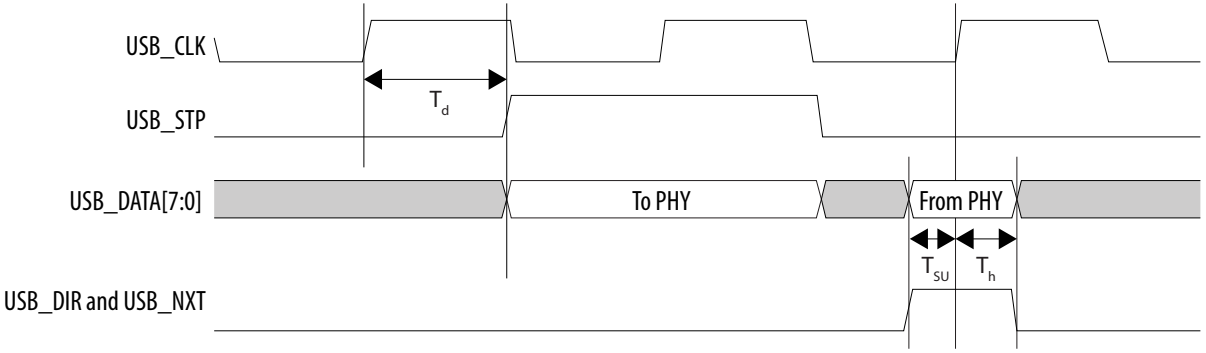
HPS USB 2.0 Timing Characteristics

Table 96. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{usb_clk}	USB_CLK clock frequency	—	60	—	MHz
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 18. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Note: If you need to adjust the timings of certain signals, you can use the HPS registers `Pin_Mux.io0_delay` through `Pin_Mux.io47_delay` to allow software to set the delay chains in each of the dedicated I/Os. For example, to add output and input delay to the USB_DATA3 signal (HPS_IOA_8), program Pin_Mux.io7_delay.output_val_en = 1, and Pin_Mux.io7_delay.output_val = 15 to add approximately 1.4 ns output delay from the HPS, and program Pin_Mux.io7_delay.input_val_en = 3, and Pin_Mux.io7_delay.input_val = 30 to add approximately 2.8 ns input delay into the HPS. See HPS Programmable I/O Timing Characteristics for more information.

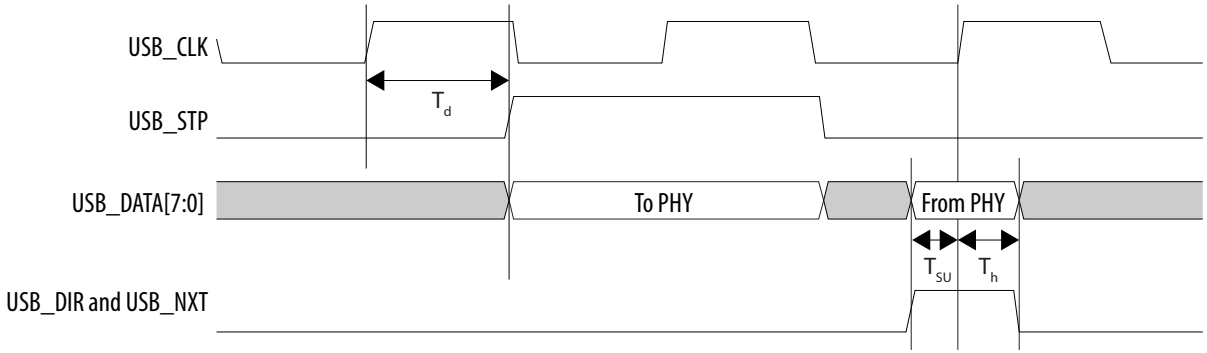
HPS USB 3.1 Timing Characteristics

Table 97. HPS USB 3.1 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{usb_clk}	USB_CLK clock frequency	—	60	—	MHz
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 19. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Note: If you need to adjust the timings of certain signals, you can use the HPS registers `Pin_Mux.io0_delay` through `Pin_Mux.io47_delay` to allow software to set the delay chains in each of the dedicated I/Os. For example, to add output and input delay to the USB_DATA3 signal (HPS_IOA_8), program Pin_Mux.io7_delay.output_val_en = 1, and Pin_Mux.io7_delay.output_val = 15 to add approximately 1.4 ns output delay from the HPS, and program Pin_Mux.io7_delay.input_val_en = 3, and Pin_Mux.io7_delay.input_val = 30 to add approximately 2.8 ns input delay into the HPS. See HPS Programmable I/O Timing Characteristics for more information.

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 98. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (1000Base-T)	TX_CLK clock period (125 MHz)	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period (25 MHz)	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period (2.5 MHz)	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (162) (163)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

(162) Rise and fall times depend on the I/O standard, drive strength, and loading. Altera recommends simulating your configuration.

(163) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5–2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1 ns data-to-clock skew requirement.

Figure 20. RGMII TX Timing Diagram

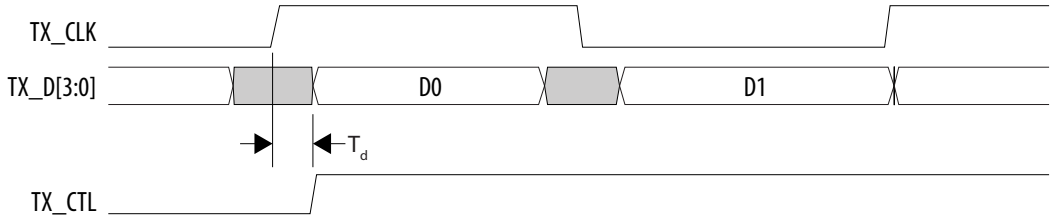


Table 99. RGMII RX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (1000Base-T)	RX_CLK clock period (125 MHz)	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period (25 MHz)	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period (2.5 MHz)	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h[(164)]	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

(164) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5–2 ns, using the HPS I/O programmable delay.

Figure 21. RGMII RX Timing Diagram

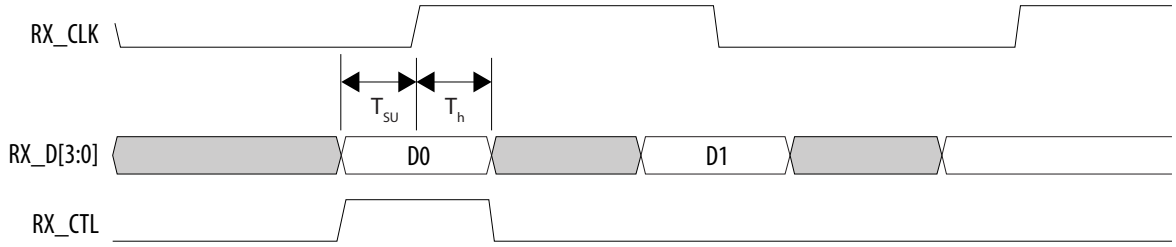
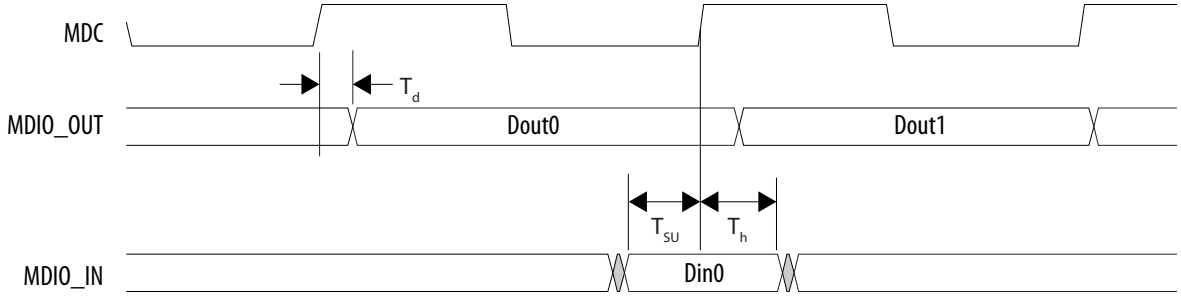


Table 100. Management Data Input/Output (MDIO) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{clk}	MDC clock frequency	—	—	2.5	MHz
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 22. MDIO Timing Diagram



SGMII Timing Requirements

SGMII operating mode is supported through FPGA fabric using SGMII PCS soft IP and LVDS SERDES FPGA IP. Refer to the *LVDS SERDES Specifications* section for timing specifications.

SGMII+ operating mode is supported through FPGA fabric using SGMII+ PCS soft IP and serial transceiver interface. Refer to the *Transceiver Performance Specifications* section for timing specifications.

Related Information

- LVDS SERDES Specifications on page 80
- GTS Transceiver Performance Specifications on page 96

HPS I²C Timing Characteristics

Table 101. HPS I²C Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{clk}	Serial clock (SCL) clock frequency	—	100	—	400	KHz
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I²C clock output jitter	—	2	—	2	%
T_{HIGH} (165)	SCL high period	4(166)	—	0.6(167)	—	µs

continued...

(165) You can adjust T_{HIGH} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(166) The recommended minimum setting for `ic_ss_scl_hcnt` is 428. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

(167) The recommended minimum setting for `ic_fs_scl_hcnt` is 75. Refer to the SCL_High_time equation in the *Hard Processor System Technical Reference Manual*.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{LOW} (168)	SCL low period	4.7(169)	—	1.3(170)	—	µs
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_{HD_DAT} (171)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
T_{VD_DAT} and T_{VD_ACK} (172)	SCL to SDA output data delay	—	3.45(173)	—	0.9(174)	µs
T_{SU_STA}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{HD_STA}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{SU_STO}	Setup time for a stop condition	4	—	0.6	—	µs

continued...

(168) You can adjust T_{LOW} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(169) The recommended minimum setting for `ic_ss_scl_lcnt` is 464. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(170) The recommended minimum setting for `ic_fs_scl_lcnt` is 163. Refer to the SCL_Low_time equation in the *Hard Processor System Technical Reference Manual*.

(171) T_{HD_DAT} is affected by the rise and fall time.

(172) T_{VD_DAT} and T_{VD_ACK} are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

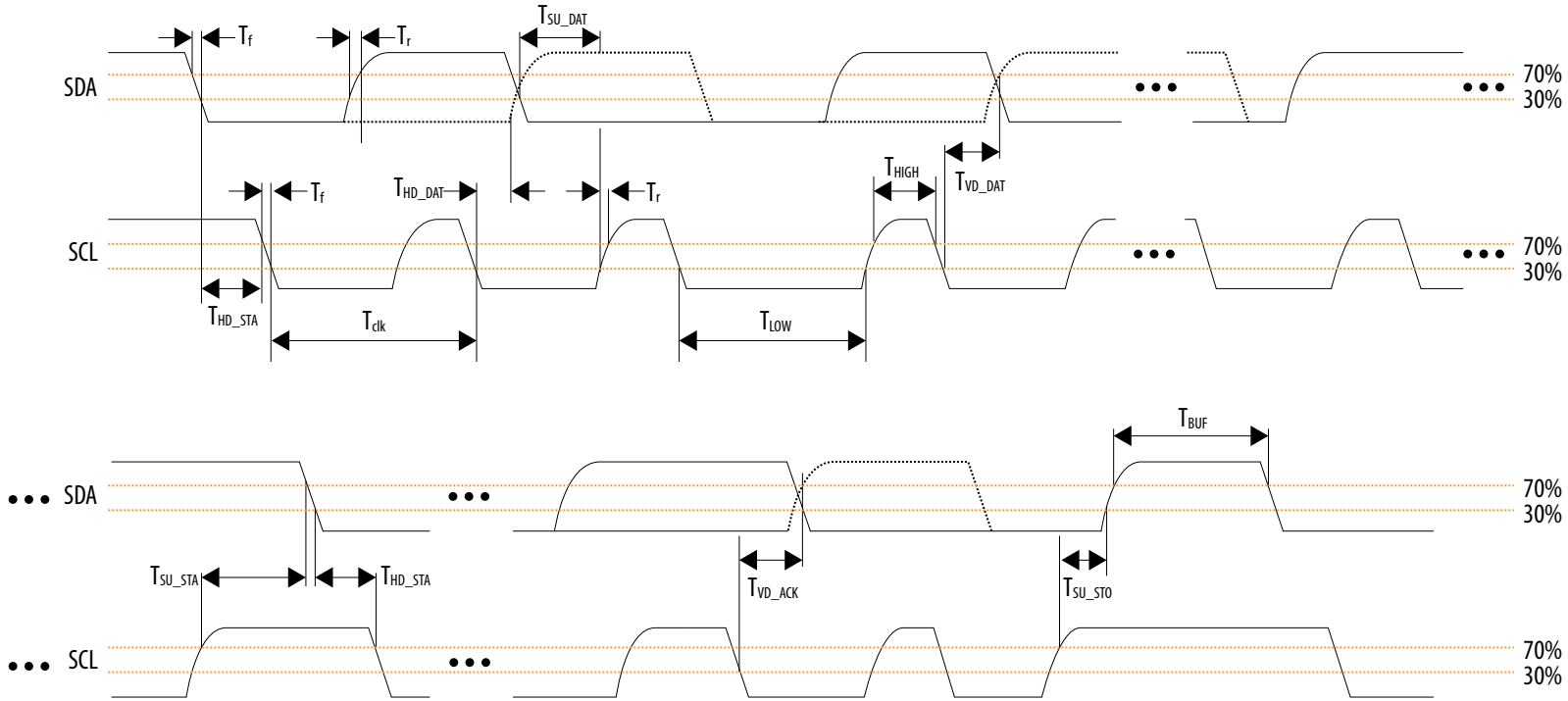
(173) Use maximum `SDA_HOLD` = 240 to be within the specification.

(174) Use maximum `SDA_HOLD` = 60 to be within the specification.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
T_{scl_r} (175)	SCL rise time	—	1,000	20	300	ns
T_{scl_f} (175)	SCL fall time	—	300	6.54	300	ns
T_{sda_r} (175)	SDA rise time	—	1,000	20	300	ns
T_{sda_f} (175)	SDA fall time	—	300	6.54	300	ns

(175) Rise and fall time parameters vary depending on external factors such as the characteristics of the I/O driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 23. I²C Timing Diagram



HPS I3C Timing Characteristics

Table 102. HPS I3C Timing Requirements When Communicating With I2C Legacy Devices

For specification status, see the *Data Sheet Status* table

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
f_{SCL}	Serial clock (SCL) clock frequency	0	0.4	0	1	MHz
T_{SCL}	SCL clock period	2.5	—	1	—	µs
T_{clk_jitter}	I3C clock output jitter	—	2	—	2	%
T_{HIGH}	SCL high period	600	—	260	—	ns
T_{DIG_H}		$T_{HIGH} + T_{scl\_r}$	—	$T_{HIGH} + T_{scl\_r}$	—	ns
T_{LOW}	SCL low period	1,300	—	500	—	ns
T_{DIG_L}		$T_{LOW} + T_{scl\_r}$	—	$T_{LOW} + T_{scl\_r}$	—	ns
T_{SU_DAT}	Setup time for serial data line (SDA) data to SCL	100	—	50	—	ns
T_{HD_DAT}	Hold time for SCL to SDA data	—	—	—	—	—
T_{SU_STA}	Setup time for a repeated start condition	600	—	260	—	ns
T_{HD_STA}	Hold time for a repeated start condition	600	—	260	—	ns
T_{SU_STO}	Setup time for a stop condition	600	—	260	—	ns
T_{BUF}	SDA high pulse duration between STOP and START	1.3	—	0.5	—	µs
T_{scl_r}	SCL rise time	20	300	—	120	ns

continued...

Symbol	Description	Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	
T_{scl_f}	SCL fall time	20 × (V_{CCIO_HPS} / 5.5 V)(176)	300	20 × (V_{CCIO_HPS} / 5.5 V)(176)	120	ns
T_{sda_r}	SDA rise time	20	300	—	120	ns
T_{sda_f}	SDA fall time	20 × (V_{CCIO_HPS} / 5.5 V)(176)	300	20 × (V_{CCIO_HPS} / 5.5 V)(176)	120	ns
T_{SPIKE}	Pulse width of spikes that the spike filter must suppress	0	50	0	50	ns

Table 103. HPS I3C Open Drain Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{HIGH}	SCL high period	—	41	ns
T_{DIG_H}		—	T_{HIGH} + T_{CF}	ns
T_{HIGH_INIT} (177)	SCL high period (for First Broadcast Address)	200	—	ns
T_{LOW_OD}	SCL low period	200	—	ns
$T_{LOW\_OD\_L}$		T_{LOW_ODmin} + T_{fDA_ODmin}	—	ns
T_{fDA_OD}	SDA signal fall time	T_{CF}	12	ns
T_{SU_OD}	Setup time for serial data line (SDA) data to SCL	3	—	ns
T_{CAS} (178)	Clock after START Condition	38.4 ns	For ENTAS0: 1 µs	—

continued...

(176) Refer to the *HPS Power Supply Operating Conditions* section for V_{CCIO_HPS} values.

(177) The controller uses this timing to send the first Broadcast Address after bus initialization, in order to disable the I2C spike filter for applicable I3C target devices.

(178) Enter Activity State (ENTAS) is a Common Command Code (CCC) supported by all I3C master and slave devices.

Symbol	Description	Min	Max	Unit
			For ENTAS1: 100 µs	—
			For ENTAS2: 2 ms	—
			For ENTAS3: 50 ms	—
T_{CBP}	Clock before STOP Condition	$T_{CASmin}/2$	—	s
$T_{MMOverlap}$	Current master to secondary master overlap time during handoff	$T_{DIG\_OD\_Lmin}$	—	ns
T_{AVAL}	Bus available condition	1	—	µs
T_{IDLE}	Bus IDLE condition	200	—	µs
T_{MMLock}	Time internal where new master not driving SDA Low	$T_{AVALmin}$	—	µs

Table 104. HPS I3C Push-Pull Timing Requirements for SDR Mode

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
f_{SCL}	Serial clock (SCL) clock frequency	0.01	12.5	12.9	MHz
T_{CLK}	SCL clock period	77.5 ns	80 ns	100 µs	—
T_{HIGH}	SCL clock high period	24	—	—	ns
T_{DIG_H}		32	—	—	ns
T_{LOW}	SCL clock low period	24	—	—	ns
T_{DIG_L}		32	—	—	ns
T_{HIGH_MIXED}	SCL clock high period for mixed bus(179)	24	—	—	ns
$T_{DIG\_H\_MIXED}$		32	—	45	ns

continued...

(179) During I3C communication on a mixed bus, to avoid I2C controllers from interpreting I3C signaling as valid I2C signaling, the T_{DIG_H} period must be constrained.

Symbol	Description	Min	Typ	Max	Unit
T_{SCO}	Clock in to data out for slave	—	—	12	ns
T_{CR}	SCL rise time	—	—	150e6 × 1/f_{SCL} (capped at 60 ns)	ns
T_{CF}	SCL fall time	—	—	150e6 × 1/f_{SCL} (capped at 60 ns)	ns
T_{HD_PP}	Hold time for SCL to SDA data (master)	T_{CR} + 3 and T_{CF} + 3	—	—	ns
	Hold time for SCL to SDA data (slave)	0	—	—	ns
T_{SU_PP}	SDA signal data setup time	3	—	—	ns
T_{CASr}	Clock after repeated START (Sr)	T_{CASmin}	—	—	ns
T_{CBSr}	Clock before repeated START (Sr)	T_{CASmin} / 2	—	—	ns
C_b	Capacitive load per bus Line (SDA/SCL)	—	—	50	pF

Figure 24. I3C Legacy Mode Timing Diagram

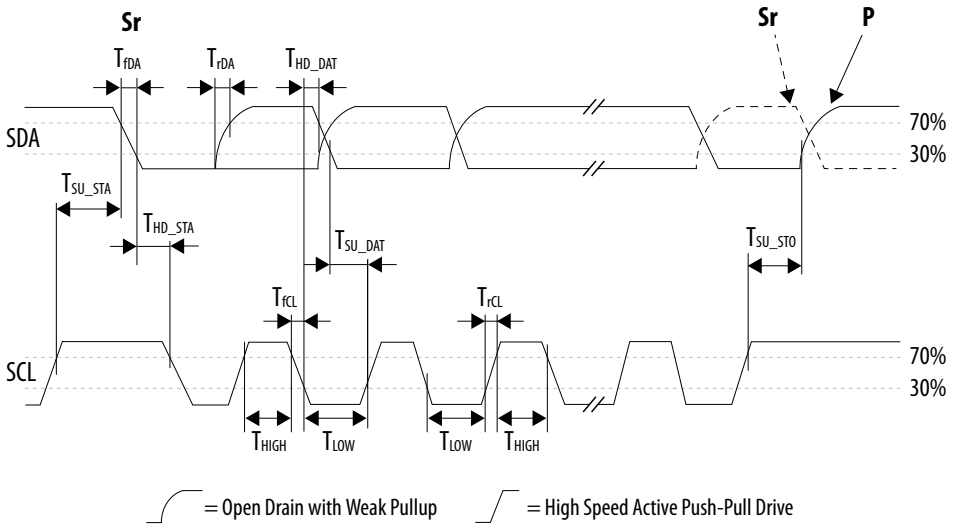


Figure 25. T_{DIG_H} and T_{DIG_L}

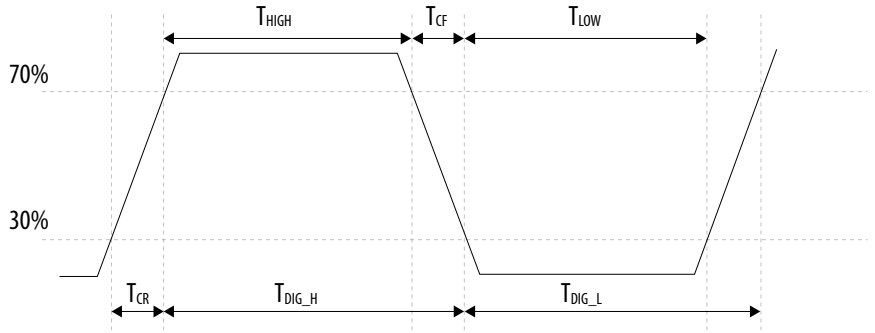


Figure 26. I3C Start Condition Timing Diagram

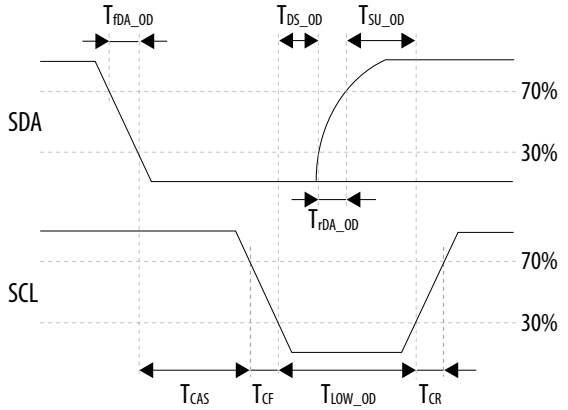


Figure 27. I3C Stop Condition Timing Diagram

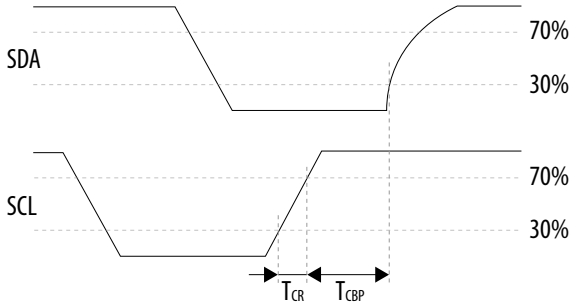


Figure 28. I3C Start Master Out Timing Diagram

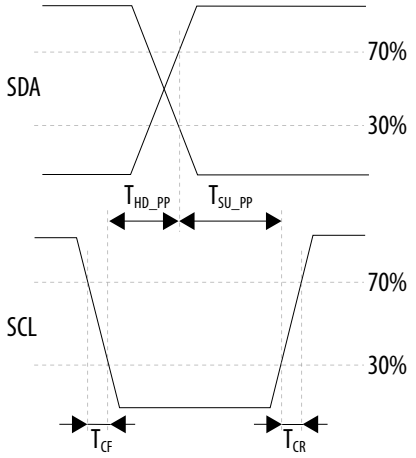


Figure 29. I3C Slave Out Timing Diagram

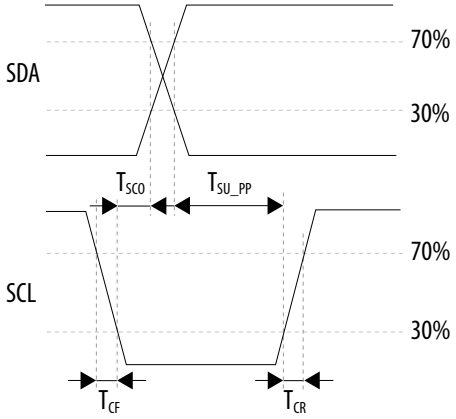
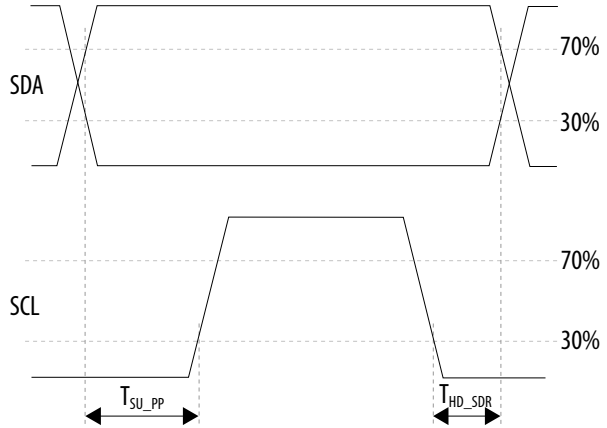


Figure 30. Master SDR Timing Diagram



Related Information

HPS Power Supply Operating Conditions on page 34

HPS NAND Timing Characteristics

Table 105. HPS NAND SDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{WP} (180)	Write enable pulse width	10	—	ns
T_{WH} (180)	Write enable hold time	7	—	ns

continued...

(180) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Symbol	Description	Min	Max	Unit
T_{RP} (180)	Read enable pulse width	10	—	ns
T_{REH} (180)	Read enable hold time	7	—	ns
T_{CLS} (180)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (180)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (180)	Chip enable to write enable setup time	15	—	ns
T_{CH} (180)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (180)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (180)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (180)	Data to write enable setup time	7	—	ns
T_{DH} (180)	Data to write enable hold time	5	—	ns
T_{WB} (180)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

Figure 31. NAND SDR Command Latch Timing Diagram

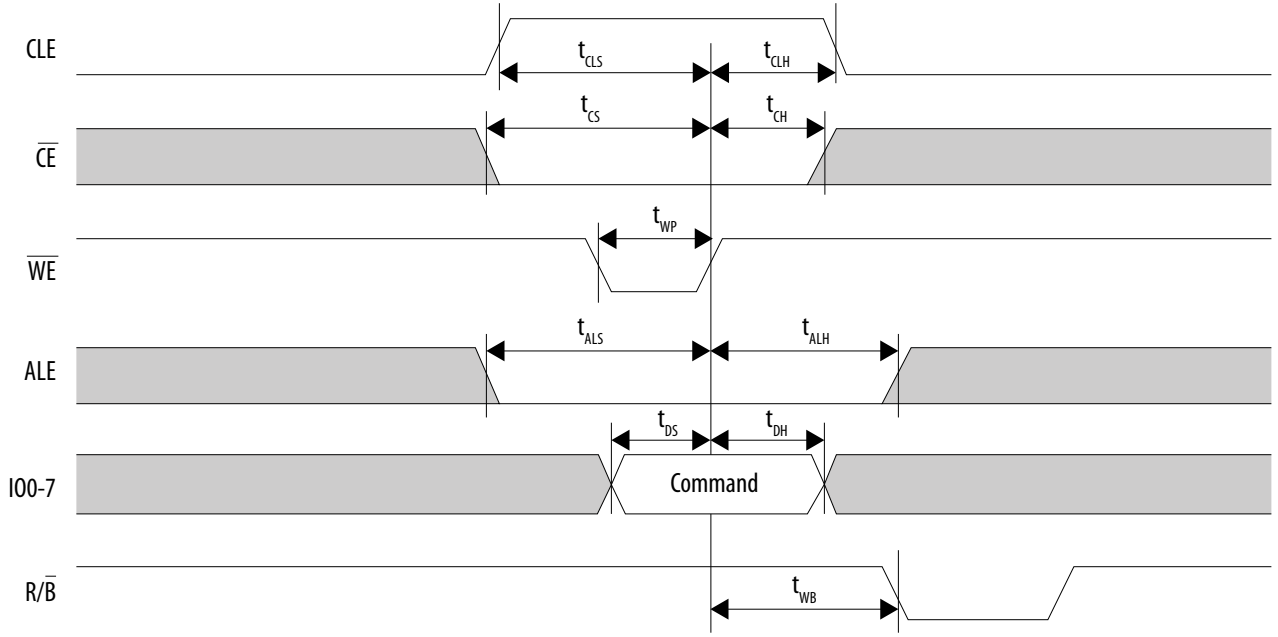


Figure 32. NAND SDR Address Latch Timing Diagram

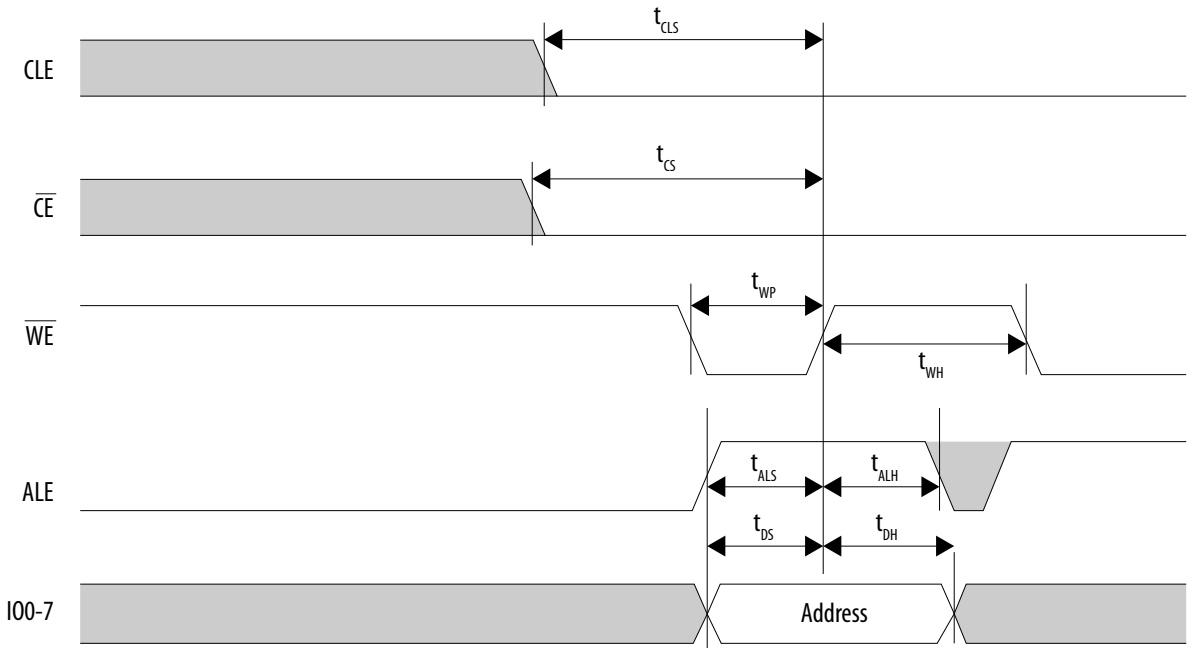


Figure 33. NAND SDR Data Output Cycle Timing Diagram

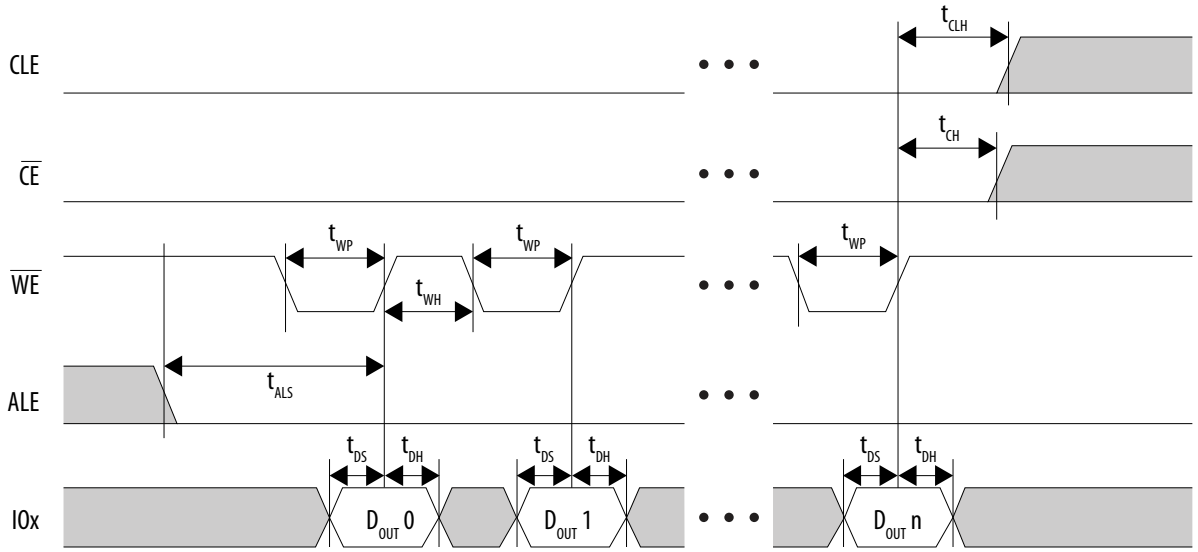


Figure 34. NAND SDR Data Input Cycle Timing Diagram

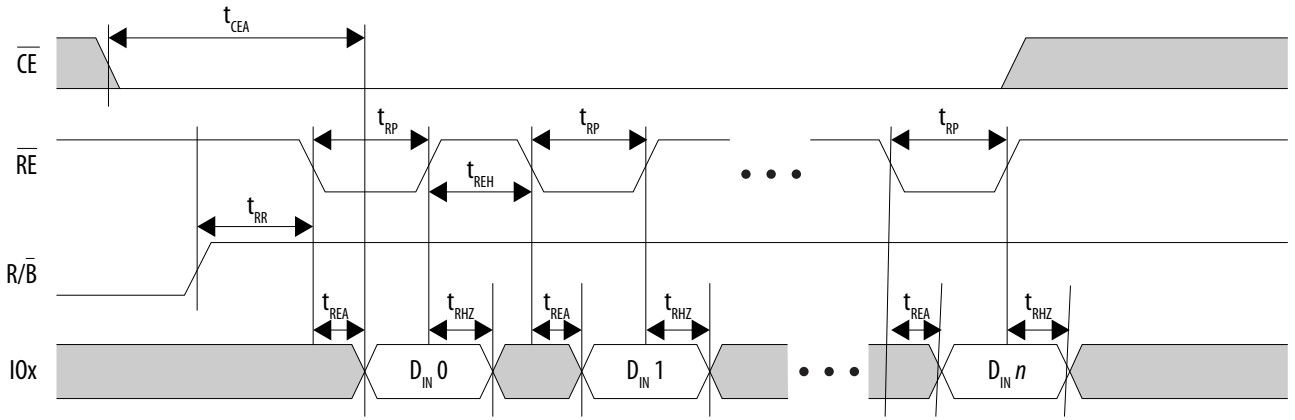


Figure 35. NAND SDR Data Input Timing Diagram for Extended Data Output (EDO) Cycle

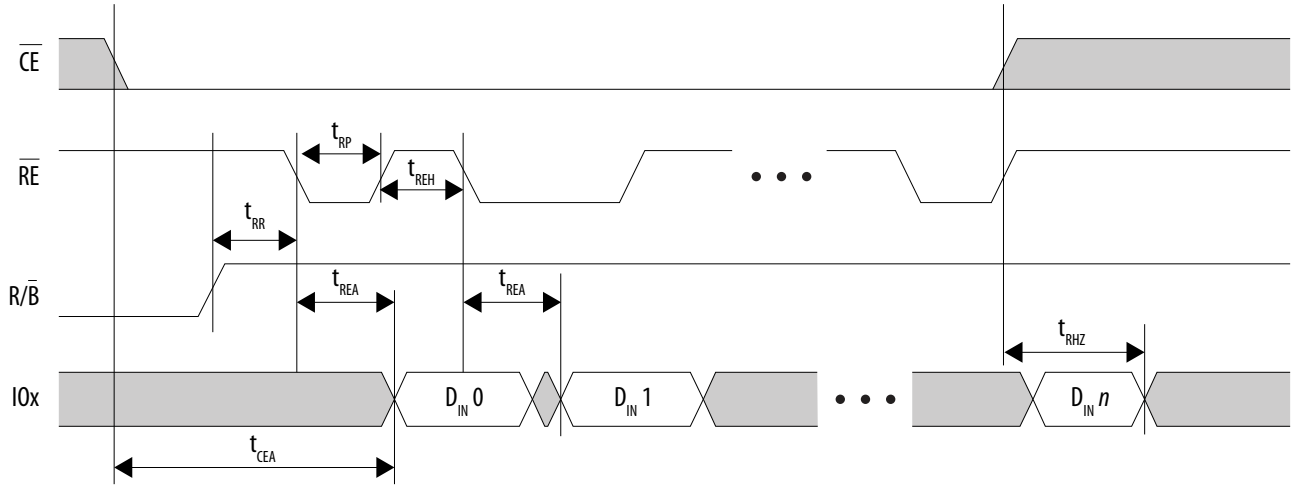


Figure 36. NAND SDR Read Status Timing Diagram

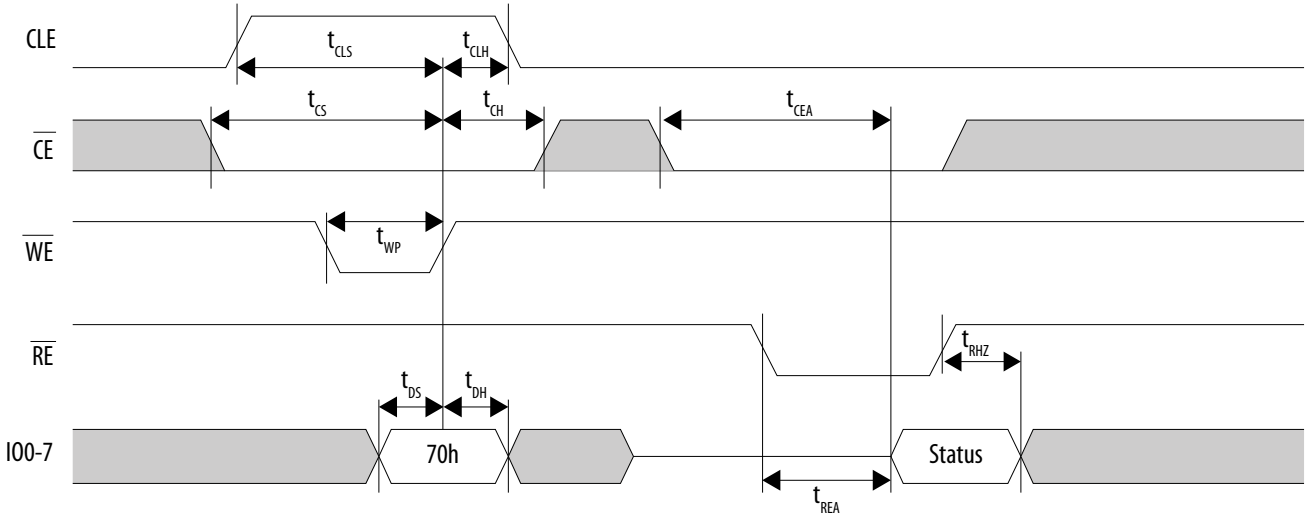


Figure 37. NAND SDR Read Status Enhanced Timing Diagram

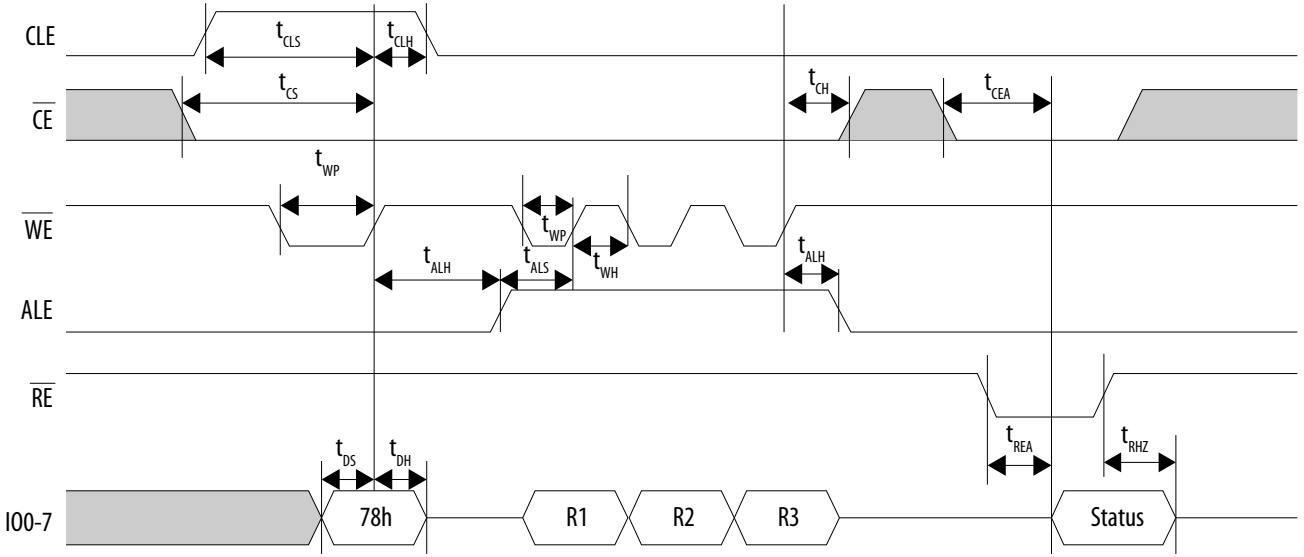


Table 106. HPS NAND DDR Timing Requirements

Compatible with the ONFI 1.x and 2.x specifications. Compatible with the Toggle 1.x and 2.x specifications. HPS I/O supports SDR, NV-DDR protocols up to 200 MT/s.

For specification status, see the *Data Sheet Status* table

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{AC}	Access window of DQ[7:0] from CLK	3	25	ns
t_{ADL}	Address cycle to data loading time	400	—	ns
t_{CADf}	Command, address, data delay (fast) (command to command, address to address, command to	25	—	ns

continued...

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
	address, address to command, command/address to start of data)			
t_{CADs}	Command, address, data delay (slow) (command to command, address to address, command to address, address to command, command/address to start of data)	45	—	ns
t_{CAH}	Command/address DQ hold time	2	—	ns
t_{CALH}	W/R_n, CLE, and ALE hold time	2	—	ns
t_{CALS}	W/R_n, CLE, and ALE setup time	2	—	ns
t_{CAS}	Command/address DQ setup time	2	—	ns
t_{CEH}	CE_n high hold time	20	—	ns
t_{CH}	CE_n hold time	2	—	ns
$t_{CK(avg)}$ or t_{CK} (181)	Average clock cycle time	10	—	ns
$t_{CK(abs)}$	Absolute clock period, measured from rising edge to the next consecutive rising edge	$t_{CK(avg)} + t_{JIT(per)\ min}$	$t_{CK(avg)} + t_{JIT(per)\ max}$	ns
$t_{CKH(abs)}$ (182)	Clock cycle high	0.43	0.57	t_{CK}
$t_{CKL(abs)}$ (182)	Clock cycle low	0.43	0.57	t_{CK}
t_{CKWR}	Data output end to W/R_n high	RoundUp{[$t_{DQSCK(max)} + t_{CK}$] / t_{CK}}	—	t_{CK}

continued...

(181) $t_{CK(avg)}$ is the average clock period over any consecutive 200 cycles window.

(182) $t_{CKH(abs)}$ and $t_{CKL(abs)}$ include static offset and duty cycle jitter.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{CS3}	CE_n setup time for data input and data output after CE_n has been high for greater than 1 µs	75	—	ns
t_{CS}	CE_n setup time	15	—	ns
t_{DH}	Data hold time	0.9	—	ns
t_{DPZ}	Data input pause setup time	1.5	—	t_{DSC}
t_{DQSCK}	Access window of DQS from CLK	3	25	ns
t_{DQSD}	W/R_n low to DQS/DQ driven by device	0	18	ns
t_{DQSH} (183)	DQS input high pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSHZ} (184)	W/R_n high to DQS/DQ tri-state by device	—	20	ns
t_{DQSL} (183)	DQS input low pulse width	0.4	0.6	t_{CK} or t_{DSC4}
t_{DQSQ}	DQS-DQ skew, DQS to last DQ valid, per access	—	0.85	ns
t_{DQSS}	Data input to first DQS latching transition	0.75	1.25	t_{CK}
t_{DS}	Data setup time	0.9	—	ns
t_{DSC}	DQS cycle time	10	—	ns
t_{DSH}	DQS falling edge to CLK rising – hold time	0.2	—	t_{CK}
t_{DSS}	DQS falling edge to CLK rising – setup time	0.2	—	t_{CK}
t_{DVW}	Output data valid window	$t_{DVW} = t_{QH} - t_{DQSQ}$		ns

continued...

(183) t_{DQSL} and t_{DQSH} are relative to t_{CK} when CLK is running. If CLK is stopped during data input, then t_{DQSL} and t_{DQSH} are relative to t_{DSC}.

(184) t_{DQSHZ} is not referenced to a specific voltage level, but specifies when the device output is no longer driving.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{FEAT}	Busy time for Set Features and Get Features	—	1	µs
t_{HP}	Half-clock period	$t_{HP} = min(t_{CKL}, t_{CKH})$		ns
t_{ITC}	Interface and Timing Mode Change time	—	1	µs
$t_{JIT(per)}$	The deviation of a given $t_{CK(abs)}$ from $t_{CK(avg)}$	–0.5	0.5	ns
t_{QH}	DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH} = t_{HP} - t_{QHS}$		ns
t_{QHS}	Data hold skew factor	—	1	ns
t_{RHW}	Data output cycle to command, address, or data input cycle	100	—	ns
t_{RR}	Ready to data output cycle (data only)	20	—	ns
t_{RST} (raw NAND)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	15/30/500	µs
t_{RST} (EZ NAND)(185)	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n	—	150/150/500	µs
t_{WB}	(WE_n high or CLK rising edge) to SR[6] low	—	100	ns
t_{WHR}	Command, address, or data input cycle to data output cycle	80	—	ns
t_{WPRE}	DQS write preamble	1.5	—	t_{CK}

continued...

(185) If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Synchronous Reset (FCh) or a Reset LUN (FAh) command then the values are as shown.

Symbol	Description	100 MHz (200 MT/s)		
		Min	Max	Unit
t_{WPST}	DQS write postamble	1.5	—	t_{CK}
t_{WRCK}	W/R_n low to data output cycle	20	—	ns
t_{WW}	WP_n transition to command cycle	100	—	ns

Figure 38. NAND DDR Command Cycle Timing Diagram

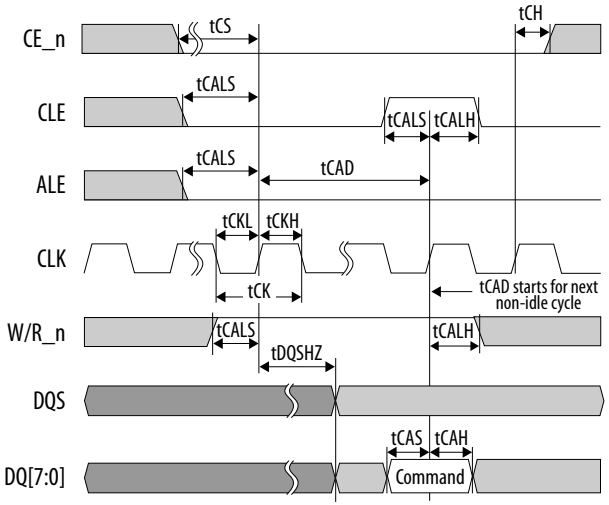


Figure 39. NAND DDR Address Cycle Timing Diagram

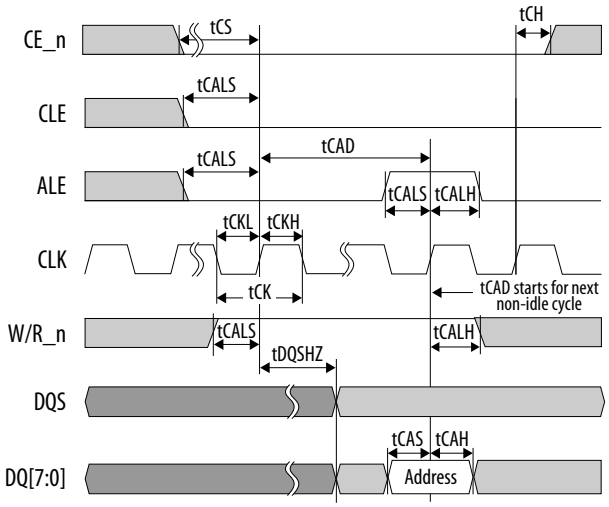


Figure 40. NAND DDR Data Input Cycle Timing Diagram

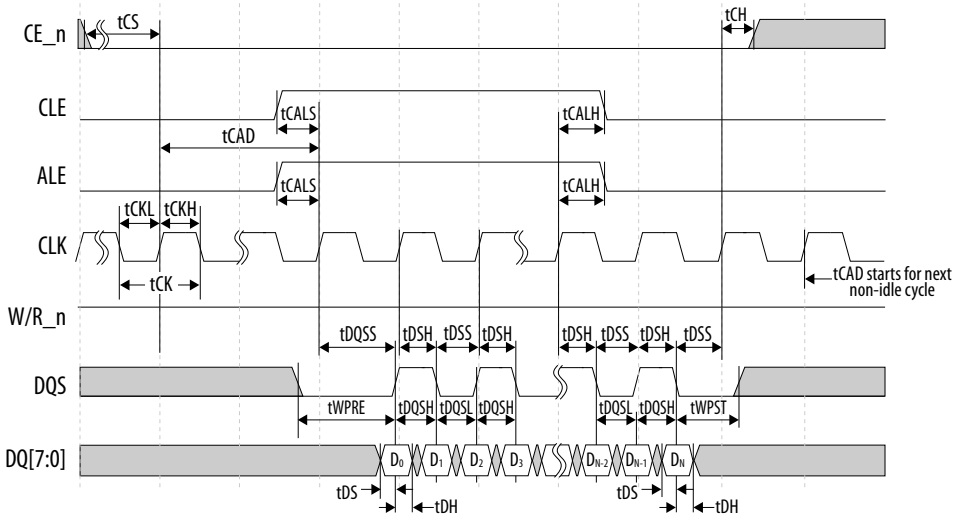


Figure 41. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped)

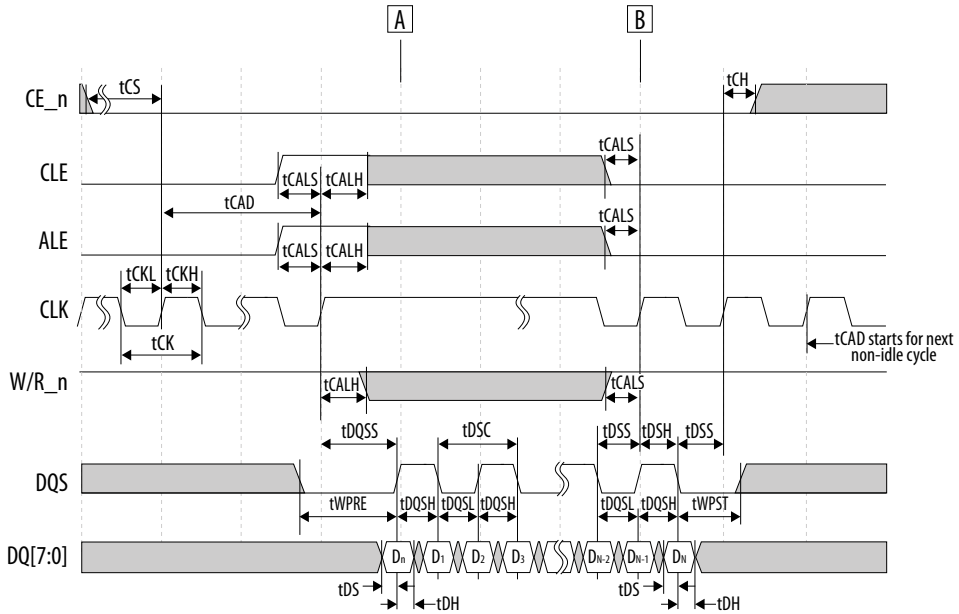


Figure 42. NAND DDR Data Input Cycle Timing Diagram (CLK Stopped with Data Pause)

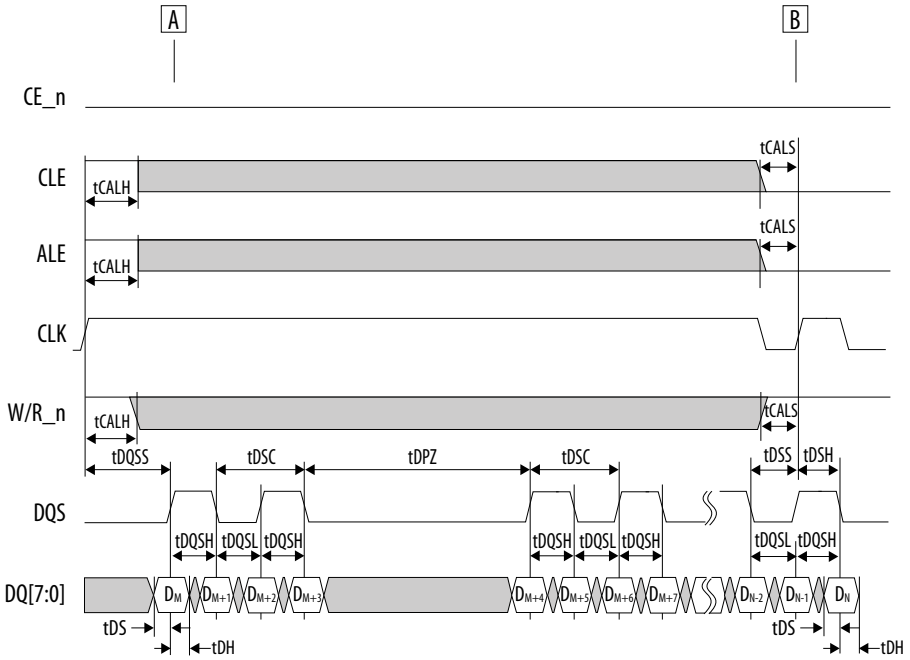


Figure 43. NAND DDR Data Output Cycle Timing Diagram

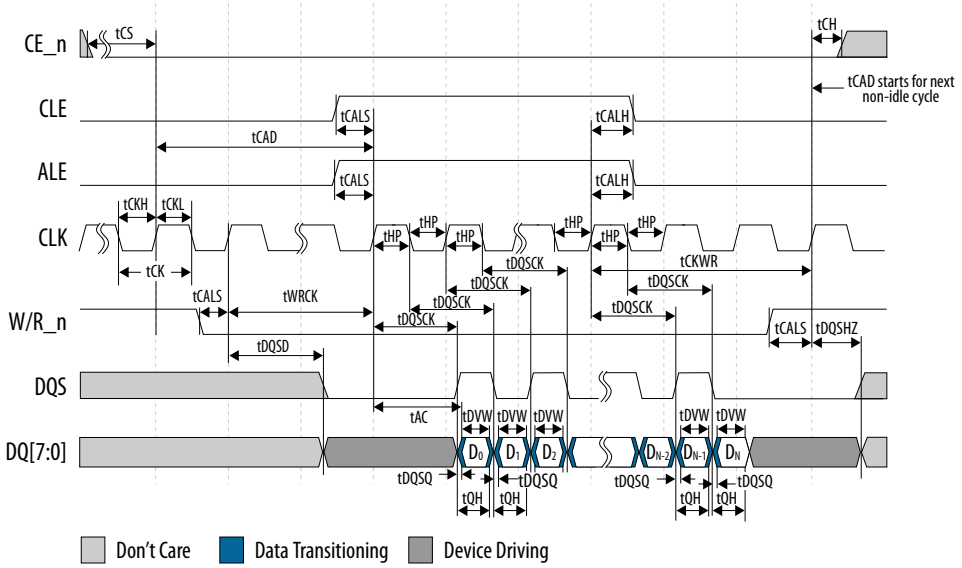


Figure 44. NAND DDR W/R_n Timing Diagram

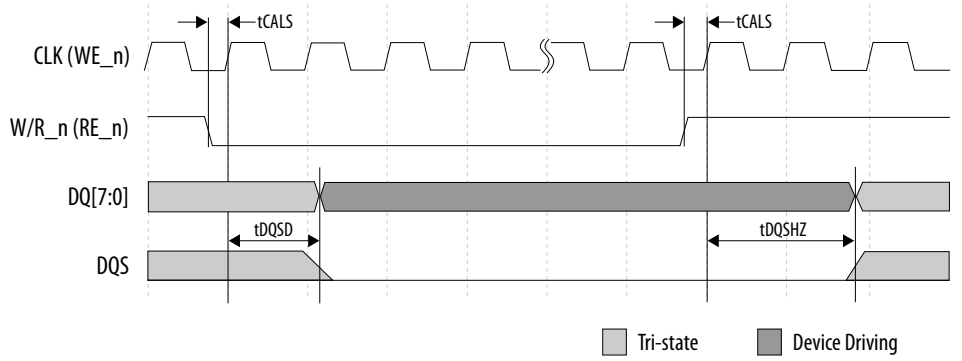
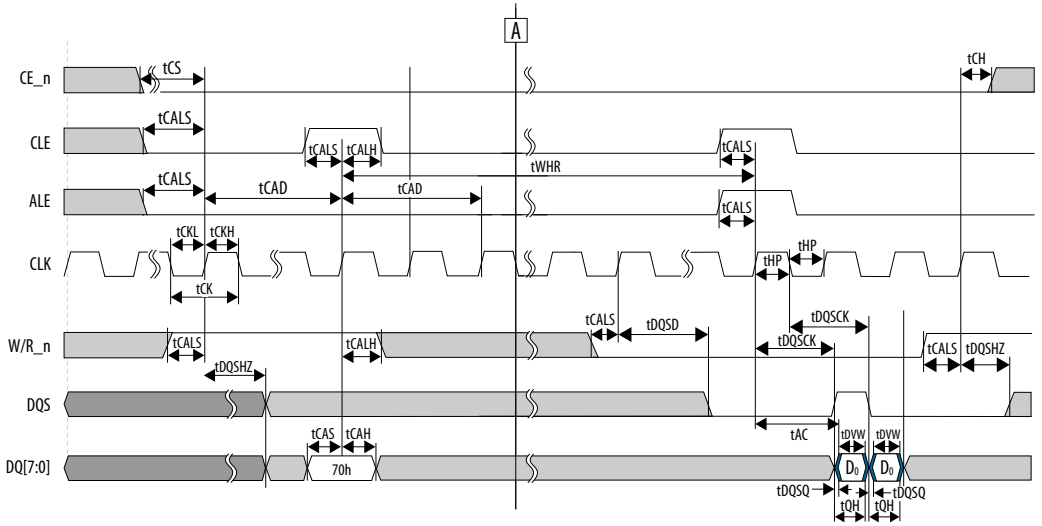


Figure 45. NAND DDR Read Status Including tWHR and tCAD Timing Diagram



HPS Trace Timing Characteristics

Table 107. Trace Timing Requirements

To increase the trace bandwidth, Altera recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

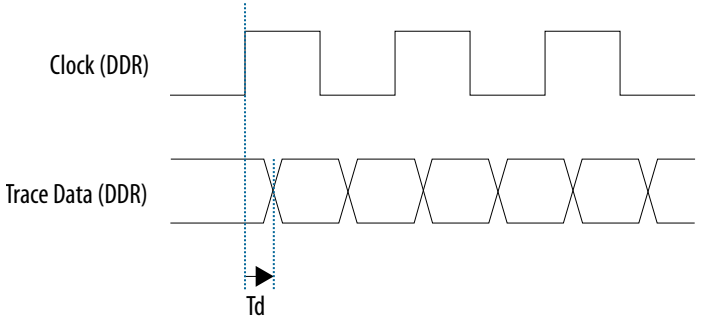
For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
F_{clk}	Trace clock frequency	—	—	200	MHz
T_{clk}	Trace clock period	5	—	—	ns

continued...

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	–0.5	—	1.3	ns

Figure 46. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

The GPIO modules provided in the HPS include optional debounce capabilities. The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock, `gpio_db_clk`.

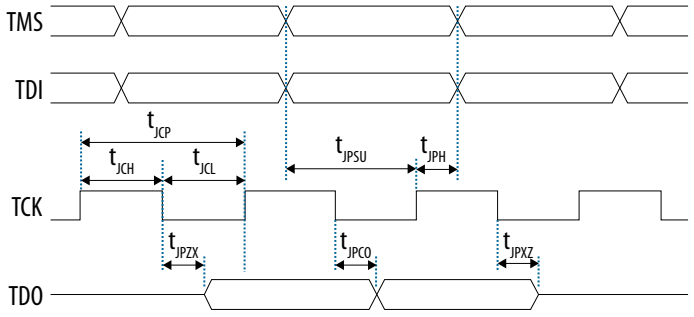
HPS JTAG Timing Characteristics

Table 108. HPS JTAG Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
F_{JCP}	TCK clock frequency	—	—	33.33	MHz
t_{JCP}	TCK clock period	30	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	5	—	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0.5	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

Figure 47. HPS JTAG Timing Diagram



HPS Programmable I/O Timing Characteristics

Table 109. HPS Programmable I/O Delay (Output Path)

For specification status, see the *Data Sheet Status* table

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	208	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	353	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	413	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	524	—	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	623	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	744	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	878	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	977	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,067	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,170	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,309	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,366	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,499	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,604	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,760	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,994	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	2,038	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	2,169	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,260	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,433	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,476	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,645	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,684	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,858	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,907	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	3,054	—	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	3,123	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	3,259	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	3,301	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	3,488	—	ps

Table 110. HPS Programmable I/O Delay (Input Path)

For specification status, see the *Data Sheet Status* table

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	208	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	353	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	413	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	524	—	ps
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	623	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	744	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	878	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	977	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,067	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,170	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,309	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,366	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,499	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,604	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,760	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,994	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	2,038	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	2,169	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,260	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,433	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,476	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,645	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,684	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,858	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,907	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	3,054	—	ps
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	3,123	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	3,259	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	3,301	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	3,488	—	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 111. General Configuration Timing Specifications

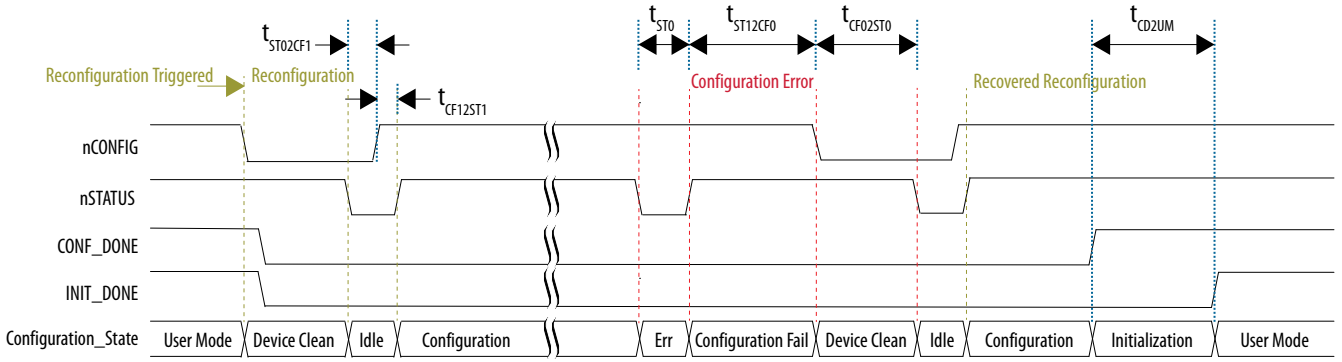
For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$ (186)	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	10	ms
t_{CD2UM} (187)	CONF_DONE high to user mode	—	5	ms
$t_{ST12CF0}$	Minimum time to drive nCONFIG from high to low after nSTATUS transitions from low to high	0	—	ms
$t_{ST02CF1}$	Minimum time to drive nCONFIG from low to high after nSTATUS transitions from high to low	0	—	ms

(186) You need to drive nCONFIG low pulse by referring to maximum value if nSTATUS cannot be monitored by host.

(187) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Figure 48. General Configuration Timing Diagram



POR Specifications

Power-on reset (POR) delay is defined as the delay between the last power rail monitored by the POR circuitry from Group 2B to reach the minimum operating condition voltage to the time your device is ready to begin configuration.

Table 112. POR Delay Specifications

For specification status, see the *Data Sheet Status* table

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16	11.5	20.2	ms
AS (Fast mode)	1.5	7.6	ms

External Configuration Clock Source Requirements

Table 113. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

For specification status, see the *Data Sheet Status* table

Description	External Clock Source	Minimum	Typical	Maximum	Unit
Clock input frequency(188)	Powered by V_{CCIO_SDM}	25/100/125			MHz
Clock input peak-to-peak period jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

JTAG Configuration Timing

Table 114. JTAG Timing Parameters and Values

For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$ (189)	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$ (189)	TMS JTAG port setup time	3	—	ns
t_{JPH} (189)	JTAG port hold time	5	—	ns

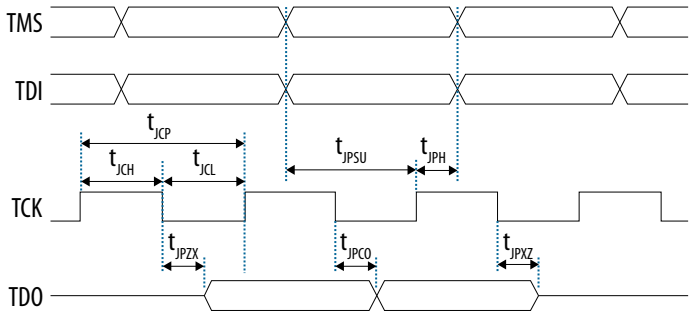
continued...

(188) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Quartus Prime software. Other frequencies in the range are not supported.

(189) For boundary-scan testing, the TMS and TDI JTAG ports minimum setup time and hold time are 7 ns.

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JPCO}	JTAG port clock to output	—	7(190)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 49. JTAG Timing Diagram



AS Configuration Timing

Table 115. AS Timing Parameters

Altera recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (191)	AS_CLK clock period	—	6.02	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%

continued...

(190) Capacitance loading at 10 pF.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	8.5(192)	—	—	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	6.8(192)	—	—	ns
T_{do} (193)	AS_DATA[3:0] output delay	–0.6	—	0.6	ns
T_{ext_delay} (194) (195) (196)	Total external propagation delay on AS signals	—	—	13.5	ns

continued...

(191) AS_CLK f_{MAX} has dependency on the maximum board loading. For AS single device configuration or AS using multiple serial flash devices configuration, use the equations in T_{do} and T_{ext_delay} notes to ensure your board has sufficient timing margin to meet flash setup/hold time specifications and AS timing specifications in this data sheet. For AS using multiple serial flash devices, refer to the *Configuration User Guide* for the recommended AS_CLK frequency and maximum board loading.

(192) AS operating at maximum clock frequency = 166 MHz. The delay is larger when operating at AS clock frequency lower than 166 MHz.

(193) Load capacitance for DCLK = 10 pF and AS_DATA = 18 pF. Altera recommends obtaining the T_{do} for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPIC simulation. To analyze flash setup time,

- $T_{su} = T_{clk}/2 - T_{do(max)} + T_{bd\_clk} - T_{bd\_data(max)}$
- $T_{ho} = T_{clk}/2 + T_{do(min)} - T_{bd\_clk} + T_{bd\_data(min)}$

(194) $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$

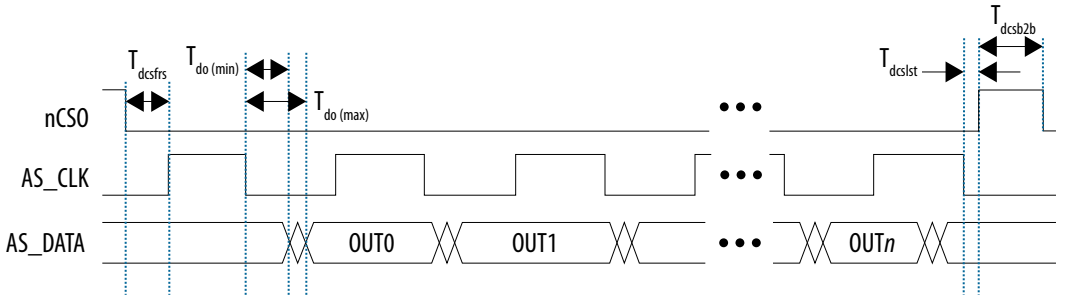
- T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.
- T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.
- T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.
- T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

(195) T_{ext_delay} specification is based on AS_CLK = 166 MHz. The value can be larger at lower AS_CLK frequency.

(196) Meeting T_{ext_delay} timing specifications indicates that the AS_DATA setup/hold timing is met.

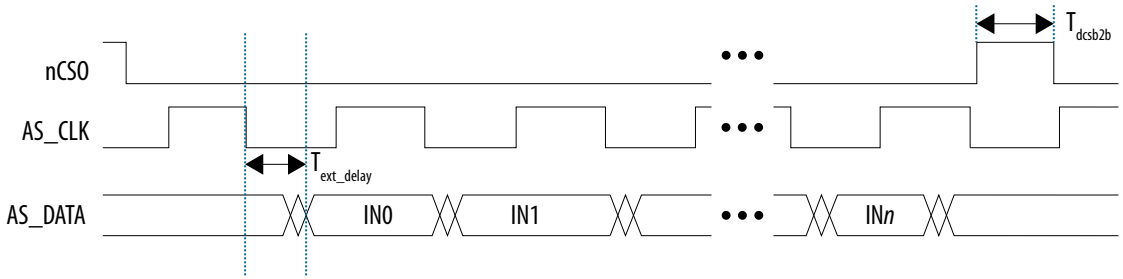
Symbol	Description	Minimum	Typical	Maximum	Unit
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	62	—	—	ns
Skew (AS_CLK – AS_nCSO)	Maximum skew tolerance between nCSO and AS_CLK	$T_{su\_ncso} - T_{dcsfrs} < Skew\ (AS\_CLK - AS\_nCSO) < AS\_CLK/2 + T_{dcslst} - T_{ho\_ncso}$ (197)			ns
Skew (AS_CLK – AS_DATA)	Maximum skew tolerance between AS_CLK and AS_DATA	$-AS\_CLK/2 + T_{do(max)} + T_{su} < Skew\ (AS\_CLK - AS\_DATA) < AS\_CLK/2 + T_{do(min)} - T_{ho}$ (197)			ns

Figure 50. AS Configuration Serial Output Timing Diagram



(197)
- T_{su} = Data setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho} = Data hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{do} = AS_DATA[3:0] output delay. Refer to the specification in this table.
- AS_CLK = AS_CLK clock period.
- T_{su_ncso} = Chip select setup time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{ho_ncso} = Chip select hold time required by the quad SPI flash. Refer to your quad SPI flash datasheet.
- T_{dcsfrs} = AS_nCSO[3:0] asserted to first AS_CLK edge. Refer to the specification in this table.
- T_{dcslst} = Last AS_CLK edge to AS_nCSO[3:0] deasserted. Refer to the specification in this table.

Figure 51. AS Configuration Serial Input Timing Diagram



Avalon Streaming Configuration Timing

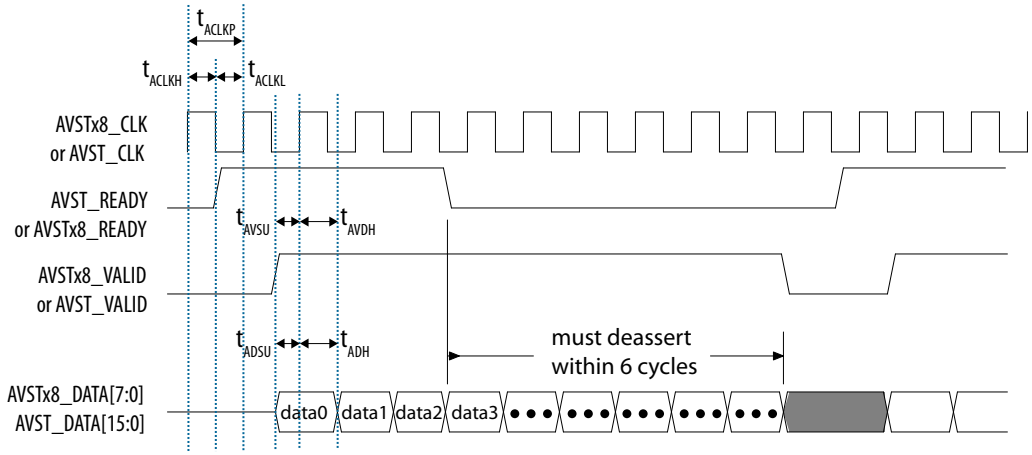
Table 116. Avalon Streaming Timing Parameters for ×8 and ×16 Configurations

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Unit
t_{ACLKH}	AVST_CLK high time	3.6	ns
t_{ACLKL}	AVST_CLK low time	3.6	ns
t_{ACLKP}	AVST_CLK period	8	ns
t_{ADSU} (198)	AVST_DATA setup time before rising edge of AVST_CLK	2.1	ns
t_{ADH} (198)	AVST_DATA hold time after rising edge of AVST_CLK	0.1	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	2.1	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

(198) Data sampled by the FPGA (sink) at the next rising clock edge.

Figure 52. Avalon Streaming Configuration Timing Diagram



Configuration Bit Stream Sizes

Table 117. Configuration Bit Stream Sizes

Configuration bit stream sizes shown in this table are based on worst-case scenarios. The sizes are typically substantially smaller because of the use of the bit stream compression. The bit stream compression efficiency has dependency on your design complexity.

128 Mb quad SPI flash size is adequate to store the periphery image.

For specification status, see the *Data Sheet Status* table

Variant	Compressed Configuration Bit Stream Size (Mbits)
A5E 005, A5E 007	38
A5E 008, A5E 013	62
A5E 043, A5E 052, A5E 065	193
A5D 051, A5D 064	255

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Programmable IOE Delay

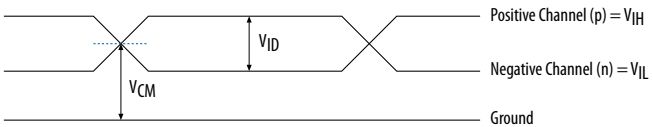
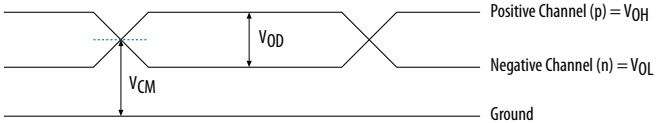
Table 118. Programmable IOE Delay Specifications

For specification status, see the *Data Sheet Status* table

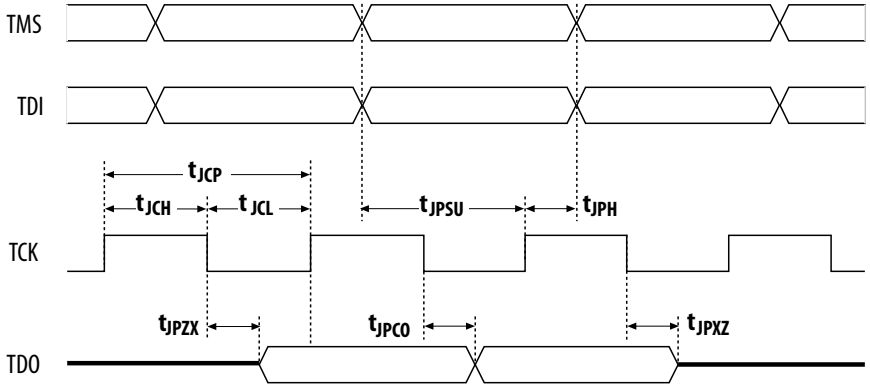
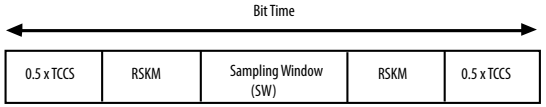
Parameter	Maximum Offset	Minimum Offset	Fast Model	Slow Model						Unit
				–E1V, –I1V	–E2V, –I2V	–E3V, –I3V	–E4S, –I4S	–E5S, –I5S	–E6S, –I6S, –E6X, –I6X	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	1.798	2.965	3.449	4.495	4.479	4.906	6.304	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.435	0.743	0.84	1.109	1.1	1.204	1.554	ns
Output Enable Delay Chain (OUTPUT_EENABLE_DELAY_CHAIN)	15	0	0.436	0.743	0.842	1.108	1.099	1.204	1.553	ns

Glossary

Table 119. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms **Single-Ended Waveform**  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.

continued...

Term	Definition
$f_{HSDRDPA}$	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications: 
R_L	Receiver differential input discrete resistor (external to the device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

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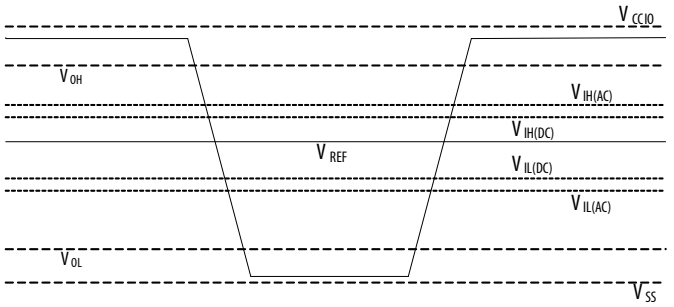
Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.

continued...

Term	Definition
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Agilex 5 FPGAs and SoCs Device Data Sheet

Document Version	Changes
2026.01.05	• Updated the maximum frequency for LPDDR5 SDRAM memory standard HPS hard memory controller in the *D-Series FPGAs Memory Standards Supported* table. • Removed the support of QDR-IV XP memory standard in the *D-Series FPGAs Memory Standards Supported* table.
2025.10.13	• Updated the status for A5E 008/013 device to Final for the B23A and B32A packages in the *Data Sheet Status for Agilex 5 FPGAs and SoCs* table. • Updated specifications in the *HPS Internal Weak Pull-Up Resistor* and *SDM I/O Internal Weak Pull-Up Resistor* tables. • Removed note about default VOD and pre-emphasis setting from the *HSIO Differential I/O Standards Specifications* table. • Updated the maximum frequency specifications for DDR4 SDRAM and DDR5 SDRAM Memory Standards in the *D-Series FPGAs Memory Standards Supported* table. • Updated the Receiver input eye specifications $V_{RX-DIFF-PKPK}$ to "closed eye" in the *Receiver Electrical Specifications* table. • Updated the description for I/O pin pull-up and pull-down resistor in the *SDM I/O Internal Weak Pull-Up Resistor* table.

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Document Version	Changes
2025.08.11	• Updated the minimum V_{IL} and maximum V_{IN} specifications for 2.5 V LVCMOS, 2.5 V LVTTL, 3.3 V LVCMOS, and 3.3 V LVTTL IO standards in the *HVIO Single-Ended I/O Standards Specifications* table. • Added description to the *System PLL Reference Clock (Using HVIO) Specifications* table. • Added Input clock or external feedback clock input duty cycle ($t_{EINDUTY}$) parameter in the *I/O PLL Specifications* table. • Updated the specifications for TCK clock frequency (F_{JCP}) and TCK clock period (t_{JCP}) in the *HPS JTAG Timing Requirements* table. • Updated the specifications in the *Programmable IOE Delay Specifications* table. • Revised the *HPS and SDM DC Characteristics* and *HPS and SDM I/O Standard Specifications*, organizing them into individual sections: ☐ *HPS I/O DC Characteristics* ☐ *SDM I/O DC Characteristics* ☐ *HPS I/O Standard Specifications* ☐ *SDM I/O Standard Specifications* • Updated the maximum specifications for Clock Frequency f_{HSCLK_in}(input clock frequency) SLVS400 I/O Standards in the *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* and *E-Series Device Group B FPGAs LVDS SERDES Specifications* tables. • Updated the conditions of Tri-stated pin to V_O in the *HVIO Pin Leakage Current* table. • Added footnote about receiver compliance to the V_{OH} in the *D-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications* and *E-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications* tables. • Added POD12 and POD11 parameters for GPIO and PHYLITE modes in the *HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications* table. • Added LVSTL700 V_{REF} specifications in the *HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications* table. • Added footnote about POD EMIF Interface to refer to eye mask estimator guidelines in the *HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications* and *HSIO Differential POD I/O Standards Specifications* tables. • Added notes to the True Differential Signaling-1.3 V (LVDS compatible Transmitter and Receiver) specifications in the *HSIO Differential I/O Standards Specifications* table. • Removed mentions of SLVS in the *HSIO OCT Calibration Accuracy Specifications*table. • Added SLVS400 I/O standard to the *HSIO OCT Without Calibration Resistance Tolerance Specifications*table. • Updated the description about overshooting values when using True Differential Signaling I/O standard at V_{CCIO_PIO} at 1.3 V in the *Maximum Allowed Overshoot and Undershoot Voltage* section. • Updated the HDMI 2.1 specifications lane rate in the *Electrical Compliance List* table. • Added OIF-CEI-28G VSR/SR/MR and OIF-CEI-25G protocols to the CEI 4.0 Specification in the *Electrical Compliance List* table. • Updated the footnotes about powering up V_{CCBAT} in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*tables.
2025.04.07	• Updated the footnote and removed LP mode (HS) label for M20K block in the *D-Series FPGAs Memory Block Performance Specifications (M20K Block)* and *E-Series FPGAs Memory Block Performance Specifications (M20K Block)* tables. • Updated the transmitter $t_{x\ Jitter}$ and T_{CCS} specifications in the *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* and *E-Series Device Group B FPGAs LVDS SERDES Specifications* tables. • Updated V_{OD}(V) to V_{OD}(DC)(V) in the *D-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications* and *E-Series FPGAs MIPI D-PHY High-Speed I/O Standards Specifications* tables. • Removed QDR-IV XP memory standard in the *D-Series FPGAs Memory Standards Supported* table.

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Document Version	Changes
	• Updated the configuration bit stream sizes for A5E005 and A5E007 variants in the *Configuration Bit Stream Sizes* table. • Updated specifications for the *HPS and SDM I/O Pin Leakage Current* table. • Removed Max and Typ specifications for the *HPS and SDM I/O Hysteresis Specifications for Schmitt Trigger Input* table. • Added notes to the *HSIO Single-Ended LVSTL I/O Standards Specifications* and *HSIO Differential LVSTL I/O Standards Specifications* tables. • Added footnote for AC input voltage V_i (AC) in the *Maximum Allowed Overshoot During Transitions for 1.8 V, 2.5V and 3.3 V in HVIO Bank* table. • Added note about voltage sensor accuracy specifications in the *Voltage Sensor Specifications* table. • Added SPIM_CLK frequency in the *SPI Master Timing Requirements* and *SPI Slave Timing Requirements* tables. • Added USB_CLK clock frequency in the following tables: ☐ *HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements* ☐ *HPS USB 3.1 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements* • Added Serial Clock (SCL) frequency in the *HPS I^2C Timing Requirements* table. • Added Trace clock frequency and updated clock period in the *Trace Timing Requirements* table. • Added TCK clock frequency in the *HPS JTAG Timing Requirements* table. • Updated specifications in the *HPS Programmable I/O Delay (Output Path)* and *HPS Programmable I/O Delay (Input Path)* tables. • Added footnote for V_{CO} in the -5 and -6 speed grade in the *HPS PLL Performance* table. • Added MDC clock frequency in the *Management Data Input/Output (MDIO) Timing Requirements* table. • Updated SCL clock period (T_{CLK}) specifications in the *HPS I^3C Push-Pull Timing Requirements for SDR mode* table. • Added SCL high period (for First Broadcast Address) specification in the *HPS I^3C Open Drain Timing Requirements* table. • Updated the description of V_{CCH_SDM} in the *Recommended Operating Conditions* and *Absolute Maximum Ratings* tables.
2025.01.23	• Updated the 9x9 and 27x27 specifications in the *D-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* and *E-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks)* tables. • Updated Internal VREF specifications for LVSTL700, LVSTL105 and LVSTL11 I/O standards in the *HSIO Single-Ended SSTL, HSTL, HSUL, POD, and LVSTL I/O Reference Voltage Specifications* table. • Updated the maximum data rate for True Differential Signaling I/O standards – f_{HSDR} (data rate) when using LVDS SERDES factor J=1 and J=2 in the *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* and *E-Series Device Group B FPGAs LVDS SERDES Specifications* tables. • Added the configuration bit stream sizes for A5D 051 and A5D 064 variants in *Configuration Bit Stream Sizes* table.
2024.11.25	• Updated the minimum value of T_{ext_delay} symbol in the *AS Timing Parameters* table. • Update the maximum data rate for LVDS SERDES Receiver specifications in the *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* and *D-Series and E-Series Device Group B FPGAs LVDS SERDES Specifications* tables. • Minor update on the description in the *HVIO Hysteresis Specifications for Schmitt Trigger Input* table. • Updated the maximum frequency of DDR4 SDRAM Memory Standards in the *D-Series FPGAs Memory Standards Supported* and *E-Series Device Group B FPGAs Memory Standards Supported* tables. • Minor update in the footnote for the *Voltage Sensor Specifications* table.

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Document Version	Changes
	• Updated the f_{HSDR} data rate (without DPA) in SERDES factor J = 4 and 8 specifications in the *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* and *D-Series and E-Series Device Group B FPGAs LVDS SERDES Specifications* tables. • Updated the clause used to IEEE 802.3by for 25GAUI-C2C/C2M in the *Electrical Compliance List* table. • Updated the Hold time for USB_DIR/USB_NXT/USB_DATA[7:0] (T_h) specifications in the *HPS USB UPLI Timing Characteristics* table.
2024.08.05	• Added note on 100 ohm for V_{CCIO_PIO} in *HSIO OCT Without Calibration Resistance Tolerance Specifications* table. • Updated the minimum timing parameters for t_{ADSU} and t_{AVSU} symbols in *Avalon Streaming Timing Parameters for x8 and x16 Configurations* table. • Updated the specifications in *HVIO I/O Pin Leakage Current* table. • Updated the specifications in *HVIO Internal Weak Pull-Up and Pull Down Resistor Value* table. • Updated the specifications in *D-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications* and *E-Series FPGAs MIPI D-PHY Low-Power I/O Standards Specifications* tables. • Updated the specifications in the -E6S, -I6S, -E6X and -I6X speed grade in *Programmable IOE Delay Specifications* table. • Updated the LPDDR5 SDRAM Memory Standard parameters in *E-Series Device Group B FPGAs Memory Standards Supported* table. • Added footnote for Receiver DPA mode with J-factor 4 and 8 for all speed grade at maximum corner data rates in the following tables: ☐ *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* ☐ *E-Series Device Group B FPGAs LVDS SERDES Specifications* • Updated the Typical values in the *HPS Programmable I/O Delay (Output Path)* and *HPS Programmable I/O Delay (Input Path)* tables. • Updated t_{INCCJ} specifications to ±750 ps in *I/O PLL Specifications* table. • Added CML and HSCL as the supported I/O standards in *GTS Transceiver and System PLL Reference Clock Input Specifications* table.
2024.04.01	Initial release.
2023.08.11	• Updated the *D-Series FPGAs Absolute Maximum Ratings* table. ☐ Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. ☐ Added V_{CCIO_PIO} specifications for V_{CCIO_PIO} = 1.0 V. ☐ Updated V_I specifications and footnote. ☐ Updated I_{OUT} specifications and added footnote. • Updated the *E-Series FPGAs Absolute Maximum Ratings* table. ☐ Updated –6L to –6X speed grade. ☐ Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. ☐ Added V_{CCIO_PIO} specifications for V_{CCIO_PIO} = 1.0 V. ☐ Updated V_I specifications and footnote. ☐ Updated I_{OUT} specifications and added footnote. • Updated the description in the *Maximum Allowed Overshoot and Undershoot Voltage* section and added the following tables: ☐ *Maximum Allowed Overshoot During Transitions for 1.0 V I/O in HSIO Bank* ☐ *Maximum Allowed Overshoot During Transitions for 1.3 V I/O in HSIO Bank*

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Document Version	Changes
	• Updated the *D-Series FPGAs Recommended Operating Conditions* table. ☐ Updated $V_{CCIO\_PIO\_SDM}$ specifications. ☐ Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. ☐ Updated V_{CCIO_PIO} specifications and footnote. ☐ Updated V_I specifications and footnote. ☐ Added V_O specifications for V_{CCIO_PIO} = 1.0 V. ☐ Updated t_{RAMP} footnote. • Updated the *E-Series FPGAs Recommended Operating Conditions* table. ☐ Updated –6L to –6X speed grade. ☐ Updated V_{CCH_SDM}, $V_{CCIO\_PIO\_SDM}$, and $V_{CC\_IO\_SDM}$ specifications. ☐ Updated the symbol from $V_{CCLHPS\_ADC\_SDM}$ to $V_{CCL\_ADC\_SDM}$ and updated description. ☐ Updated V_{CCIO_PIO} specifications and footnote. ☐ Updated V_I specifications and footnote. ☐ Added V_O specifications for V_{CCIO_PIO} = 1.0 V. ☐ Updated t_{RAMP} footnote. • Added footnote to maximum value column in the *D-Series FPGAs GTS Transceiver Power Supply Operating Conditions* table. • Updated the *E-Series FPGAs GTS Transceiver Power Supply Operating Conditions* table. ☐ Added footnote to maximum value column. ☐ Updated –6L to –6X speed grade. • Updated the *HSIO OCT Calibration Accuracy Specifications* table. ☐ Removed 50-Ω R_S specification. ☐ Added footnote to R_S and R_T. ☐ Removed DPHY11 I/O standards support. • Updated the *HSIO OCT Without Calibration Resistance Tolerance Specifications* table. ☐ Added 34-Ω and 40-Ω R_S specifications for 1.0 V LVCMOS and 1.3 V LVCMOS I/O standards. ☐ Added footnote to R_S and R_T. • Added specifications for V_{CCIO_PIO} = 1.0 ±5% and V_{CCIO_PIO} = 1.3 ±5% in the *HSIO Internal Weak Pull-Up Resistor* table. • Updated I_I and I_{OZ} specifications for V_I = 0 V to V_{CCIO_HVIO} = 2.5 V in the *HVIO I/O Pin Leakage Current* table. • Updated C_{IO} specification in the *HVIO Pin Capacitance* table. • Updated V_{HYS} specification for V_{CCIO_HVIO} = 3.3 V in the *HVIO Hysteresis Specifications for Schmitt Trigger Input* table. • Added specifications for 1.0 V LVCMOS and 1.3 V LVCMOS I/O standards in the *HSIO Single-Ended I/O Standards Specifications* table. • Updated POD11 and POD12 specifications in the *HSIO Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications* table. • Updated LVSTL11, LVSTL105, and LVSTL700 specifications in the *HSIO Single-Ended LVSTL I/O Standards Specifications* table. • Added footnote to SSTL-12, HSTL-12, and HSUL-12 in the *HSIO Differential SSTL, HSTL, and HSUL I/O Standards Specifications* table. • Updated POD11 and POD12 specifications in the *HSIO Differential POD I/O Standards Specifications* table.

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Document Version	Changes
	• Updated LVSTL11, LVSTL105, and LVSTL700 specifications in the *HSIO Differential LVSTL I/O Standards Specifications* table. • Updated f_{IN} specifications in the *D-Series FPGAs I/O PLL Specifications* table. • Updated the *E-Series FPGAs I/O PLL Specifications* table. ☐ Updated f_{IN} specifications. ☐ Updated –6L to –6X speed grade. • Updated Fixed-point complex multiplication mode to Fixed-point 18 x 19 complex multiplication mode in the *D-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* table. • Updated –6L to –6X speed grade in the *E-Series FPGAs DSP Block Performance Specifications for Single DSP Block* table. • Updated the *E-Series FPGAs DSP Block Performance Specifications for Multiple DSP Blocks* table. ☐ Updated –6L to –6X speed grade. ☐ Updated Fixed-point complex multiplication mode to Fixed-point 18 x 19 complex multiplication mode. • Updated –6L to –6X speed grade in the *E-Series FPGAs Memory Block Performance Specifications* table. • Updated the *Voltage Sensor Specifications* table. ☐ Added external reference voltage specifications. ☐ Updated footnote to voltage sensor accuracy, V_{in}. • Split the *LVDS SERDES Specifications* table into the following tables and updated specifications: ☐ *D-Series and E-Series Device Group A FPGAs LVDS SERDES Specifications* ☐ *E-Series Device Group B FPGAs LVDS SERDES Specifications* • Removed $T_{PP\text{-}JITTER\text{-}TOLERANCE}$ specifications in the *System PLL Reference Clock (Using HVIO) Specifications* table. • Updated the *Electrical Compliance List* table. ☐ Updated specification for IEEE 802.3by 111/110 and CPRI V7.0. ☐ Added footnote to PCIe BASE 4.0 / PIPE 4.4.1 specification. ☐ Updated specification/clause and protocol for USB. • Removed the following RMII content: ☐ *Reduced Media Independent Interface (RMII) Clock Timing Requirements* table ☐ *RMII TX Timing Requirements* table ☐ *RMII TX Timing Diagram* ☐ *RMII RX Timing Requirements* table ☐ *RMII RX Timing Diagram* • Removed ONFI 3.x, INFI 4.x, NV-DDR2, and NV-DDR3 in the table description of the following tables: ☐ *HPS NAND SDR Timing Requirements* ☐ *HPS NAND DDR Timing Requirements*

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Document Version	Changes
	• Updated t_{JCP}, t_{JCH}, t_{JCL}, $t_{JPSU\ (TMS)}$, t_{JPH}, t_{JPCO}, t_{JPZX}, and t_{JPXZ} specifications in the *JTAG Timing Parameters and Values* table. • Updated t_{ACLKH}, t_{ACLKL}, t_{ACLKP}, t_{ADSU}, t_{ADH}, and t_{AVSU} specifications in the *Avalon Streaming Timing Parameters for ×8 and ×16 Configurations* table. • Updated the *Programmable IOE Delay Specifications* table. ☐ Added specifications for Output Enable Delay Chain (OUTPUT_EENABLE_DELAY_CHAIN). ☐ Updated –6L to –6X speed grade.
2023.03.27	Initial release.