SIPMOS® Small-Signal-Transistor

Feature

- P-Channel
- Enhancement mode
- Logic Level
- Avalanche rated
- d*v*/d*t* rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21

AEC Qualified

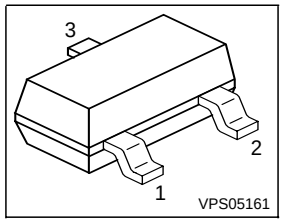
RoHS

Halogen-Free

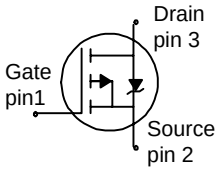
Product Summary

V_{DS}	-60	V
$R_{DS(on)}$	8	Ω
I_D	-0.17	A

PG-SOT-23



Type	Package	Tape and Reel	Marking
BSS84P	PG-SOT-23	H6327:3000pcs/r.	YBs
BSS84P	PG-SOT-23	H6433:10000pcs/r.	YBs



Maximum Ratings, at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_A=25°C T_A=70°C	I_D	 -0.17 -0.14	A
Pulsed drain current T_A=25°C	$I_{D\ puls}$	-0.68	
Avalanche energy, single pulse I_D=-0.17 A , V_{DD}=-25V, R_{GS}=25Ω	E_{AS}	2.6	mJ
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	0.036	
Reverse diode d*v*/d*t* I_S=-0.17A, V_{DS}=-48V, d*i*/d*t*=-200A/µs, T_{jmax}=150°C	d*v*/d*t*	-6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_A=25°C	P_{tot}	0.36	W
Operating and storage temperature	T_j , T_{stg}	-55... +150	°C
IEC climatic category; DIN IEC 68-1		55/150/56	
ESD Class JESD22-A114-HBM		Class 0	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - soldering point (Pin 3)	R_{thJS}	-	-	200	K/W
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	350	
@ 6 cm^2 cooling area [1)]		-	-	300	

Electrical Characteristics, at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage V_{GS}=0, I_D=-250µA	$V_{(BR)DSS}$	-60	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D=-20µA	$V_{GS(th)}$	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}				µA
V_{DS}=-60V, V_{GS}=0, T_A=25°C		-	-0.1	-1	
V_{DS}=-60V, V_{GS}=0, T_A=125°C		-	-10	-100	
Gate-source leakage current V_{GS}=-20V, V_{DS}=0	I_{GSS}	-	-10	-100	nA
Drain-source on-state resistance V_{GS}=-4.5V, I_D=-0.14A	$R_{DS(on)}$	-	8	12	Ω
Drain-source on-state resistance V_{GS}=-10V, I_D=-0.17A	$R_{DS(on)}$	-	5.8	8	

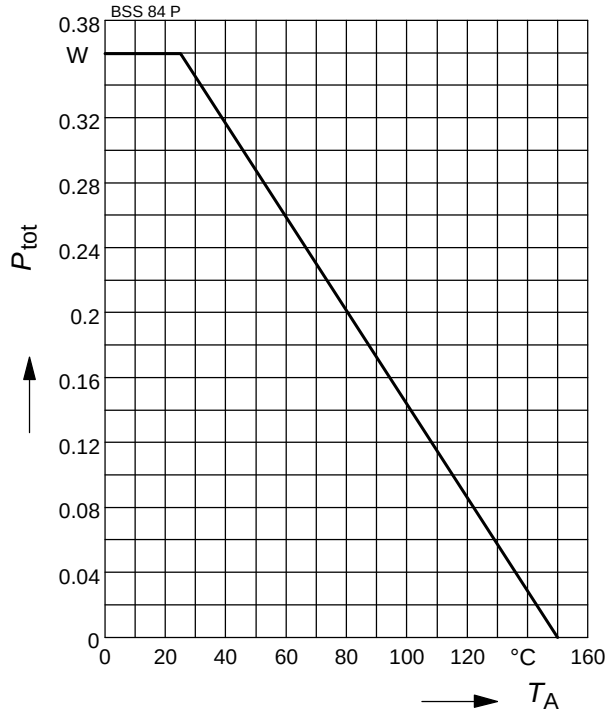
[1]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	$V_{DS}\leq 2*I_D*R_{DS(on)max}$, I_D=-0.14A	0.065	0.13	-	S
Input capacitance	C_{iss}	V_{GS}=0, V_{DS}=-25V, f=1MHz	-	15	19	pF
Output capacitance	C_{oss}		-	6	8	
Reverse transfer capacitance	C_{rss}		-	3	4	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-30V, V_{GS}=-4.5V, I_D=-0.14A, R_G=25Ω	-	6.7	10	ns
Rise time	t_r		-	16.2	24.3	
Turn-off delay time	$t_{d(off)}$		-	8.6	12.9	
Fall time	t_f		-	20.5	30.8	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=-48V, I_D=-0.17A	-	0.25	0.37	nC
Gate to drain charge	Q_{gd}		-	0.3	0.45	
Gate charge total	Q_g	V_{DD}=-48V, I_D=-0.17A, V_{GS}=0 to -10V	-	1	1.5	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=-48V, I_D=-0.17A	-	-3.42	-	V
Reverse Diode						
Inverse diode continuous forward current	I_S	T_A=25°C	-	-	-0.17	A
Inv. diode direct current, pulsed	I_{SM}		-	-	-0.68	
Inverse diode forward voltage	V_{SD}	V_{GS}=0, I_F=-0.17A	-	-0.93	-1.24	V
Reverse recovery time	t_{rr}	V_R=-30V, I_F=I_S, di_F/dt=100A/µs	-	23	34	ns
Reverse recovery charge	Q_{rr}		-	10	15	nC

1 Power dissipation

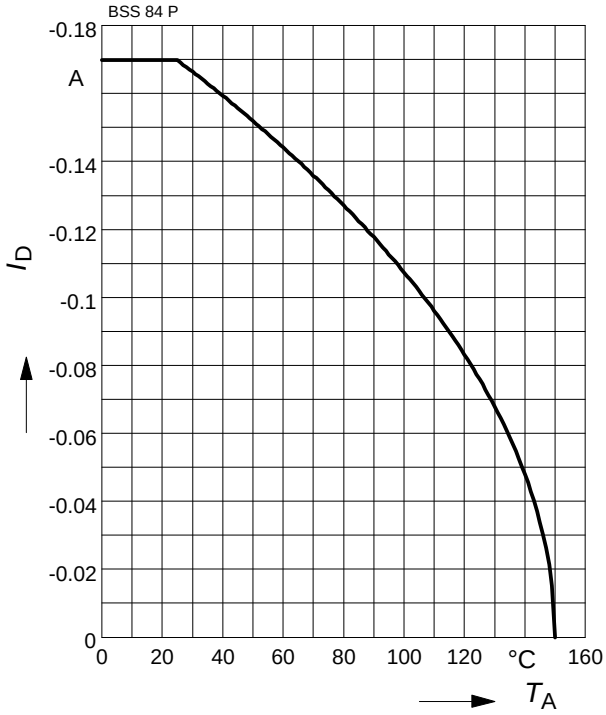
$P_{tot} = f(T_A)$



2 Drain current

$I_D = f(T_A)$

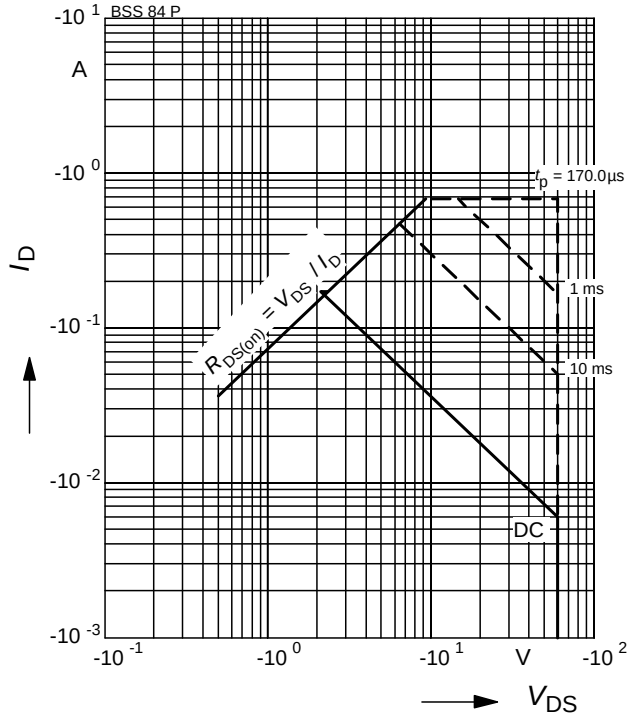
parameter: $V_{GS} \geq 10$ V



3 Safe operating area

$I_D = f(V_{DS})$

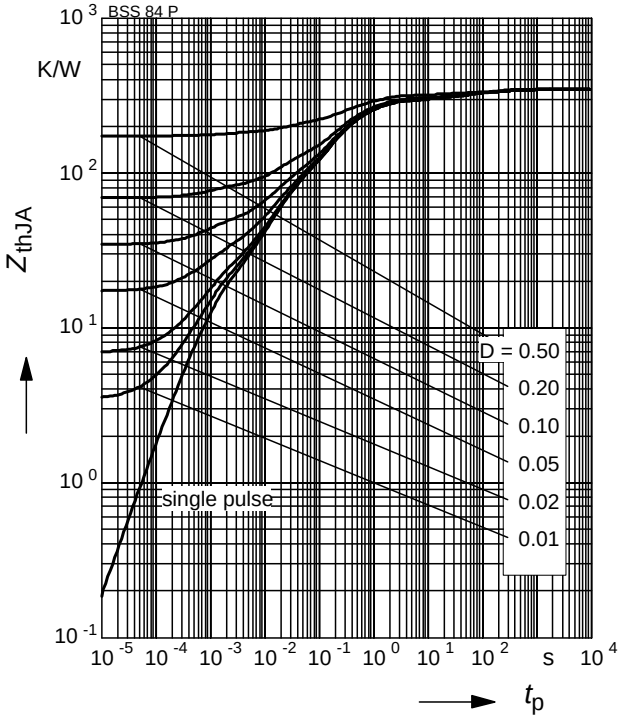
parameter : $D = 0$, $T_A = 25$ °C



4 Transient thermal impedance

$Z_{thJA} = f(t_p)$

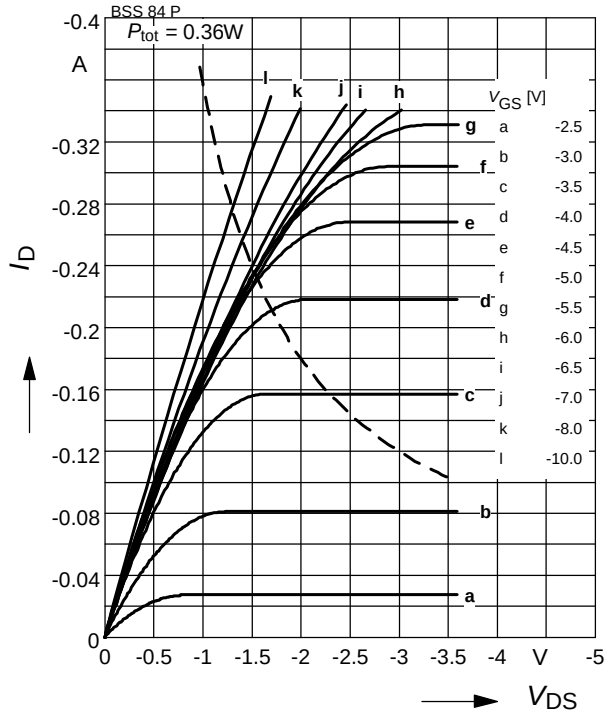
parameter : $D = t_p/T$



5 Typ. output characteristic

$I_D = f(V_{DS})$

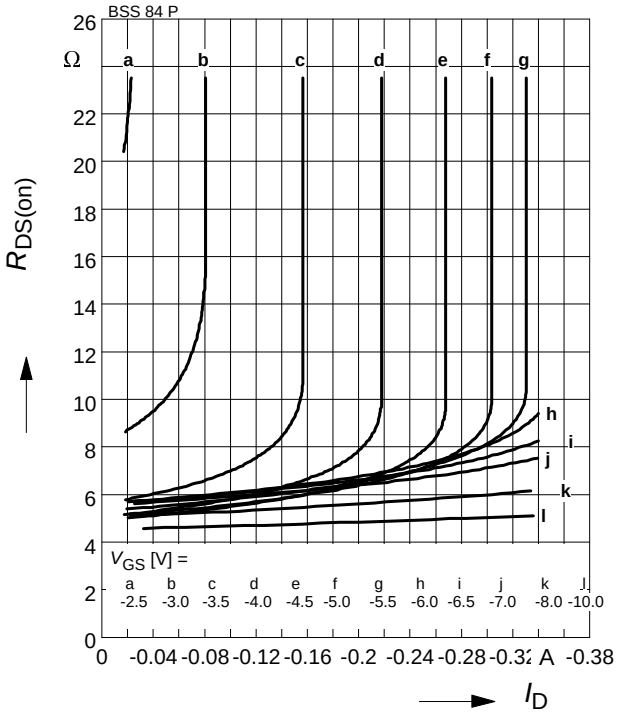
parameter: T_j = 25 °C



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$

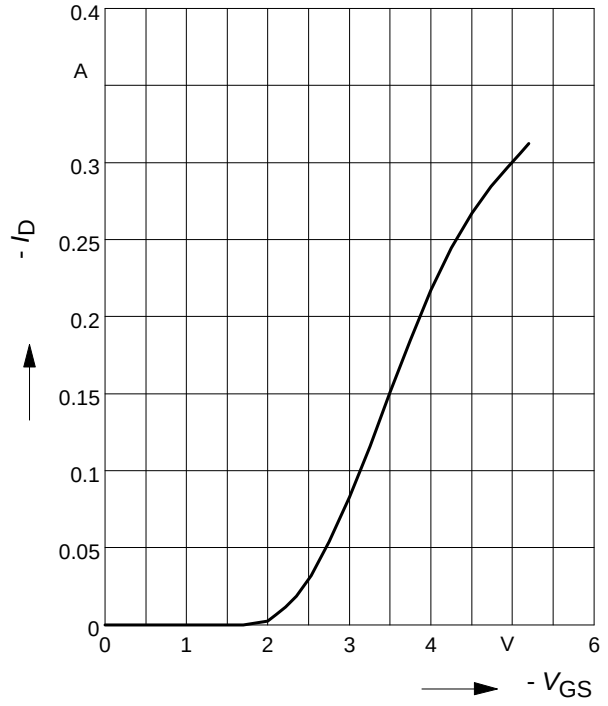
parameter: V_{GS}; T_j = 25 °C



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $|V_{DS}| \geq 2 \times |I_D| \times R_{DS(on)max}$

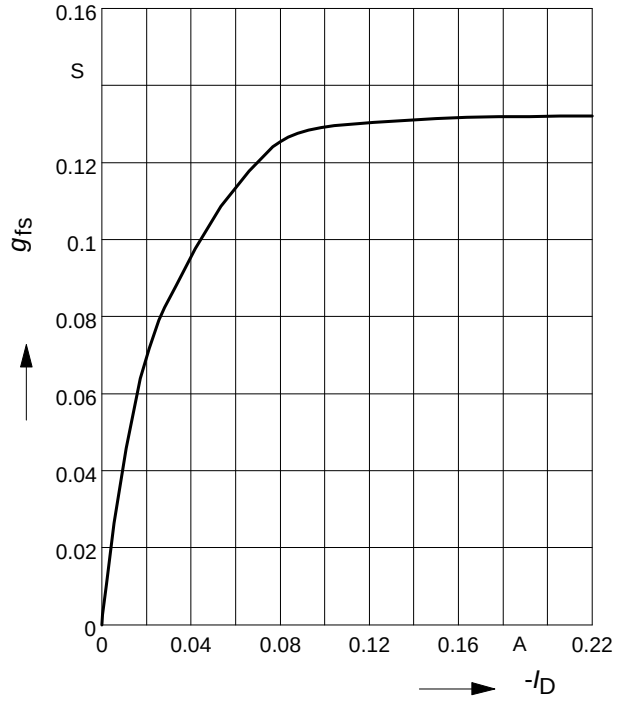
parameter: T_j = 25 °C



8 Typ. forward transconductance

$g_{fs} = f(I_D)$

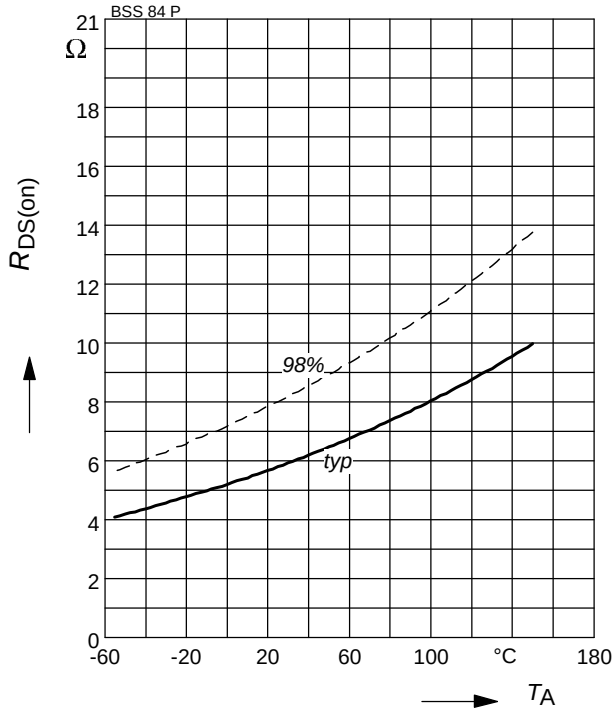
parameter: T_j = 25 °C



9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j)$

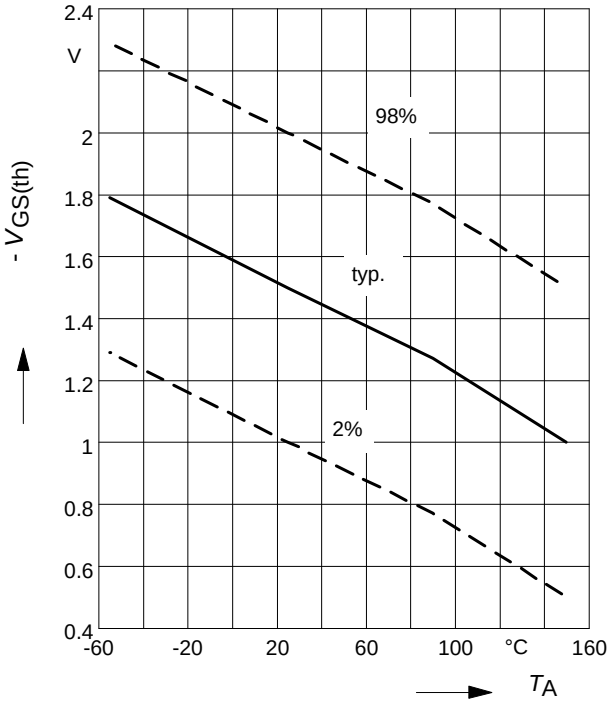
parameter : I_D = -0.17 A, V_{GS} = -10 V



10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$

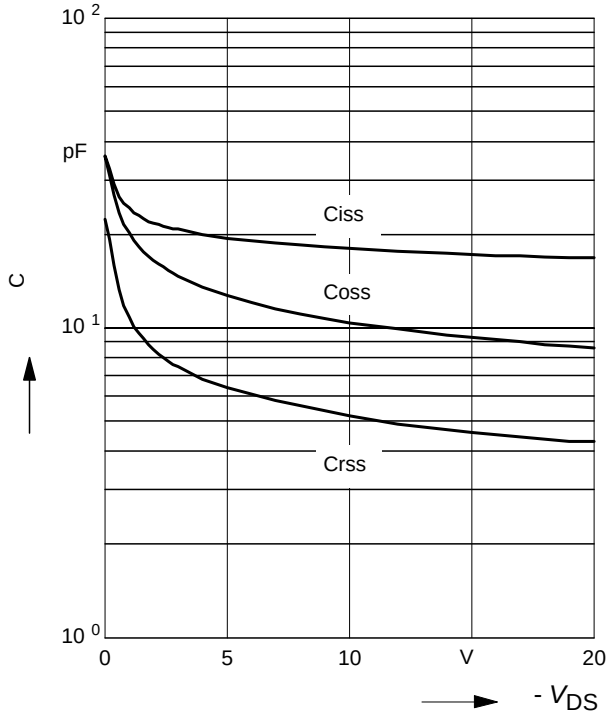
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$C = f(V_{DS})$

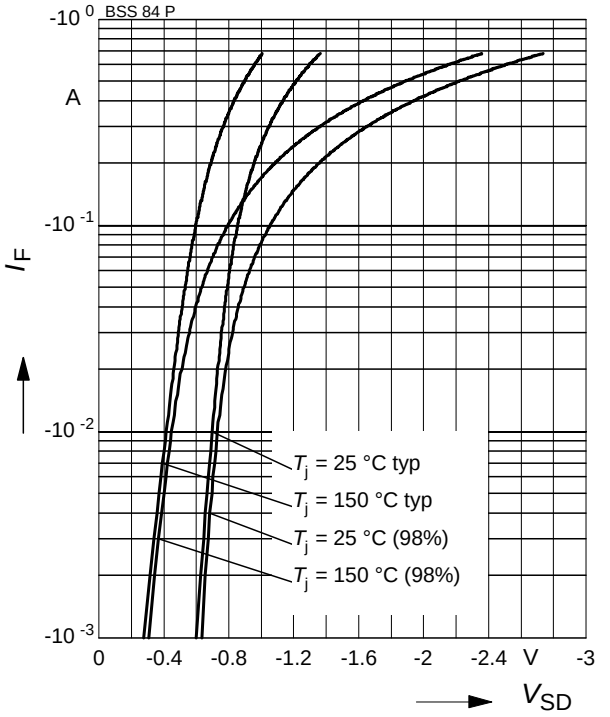
parameter: V_{GS}=0, f=1 MHz



12 Forward character. of reverse diode

$I_F = f(V_{SD})$

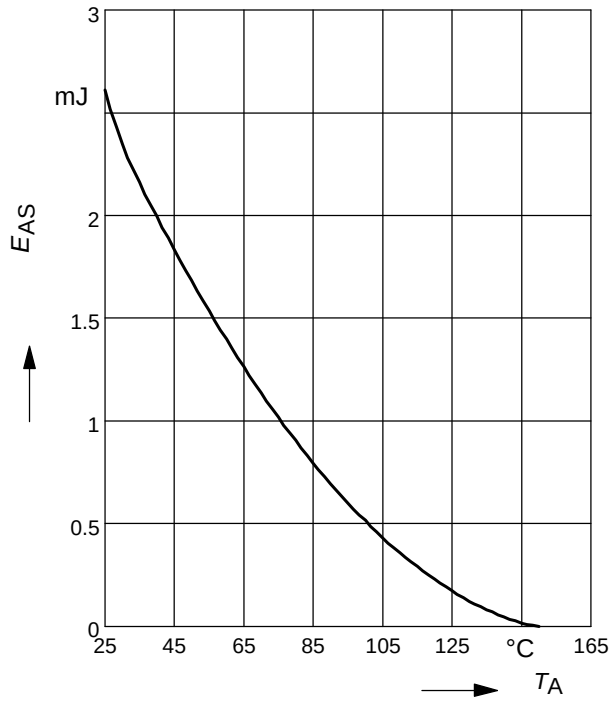
parameter: T_j , tp = 80 µs



13 Typ. avalanche energy

$E_{AS} = f(T_A)$, parameter:

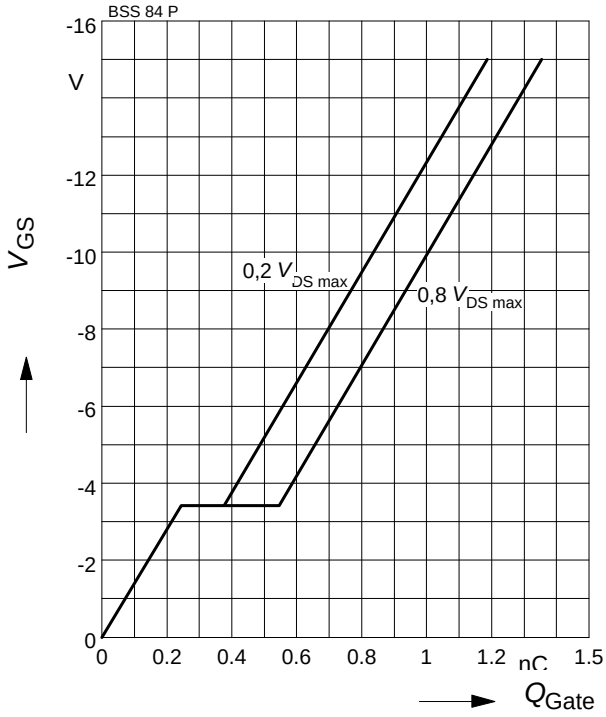
I_D = -0.17 A , V_{DD} = -25 V, R_{GS} = 25 Ω



14 Typ. gate charge

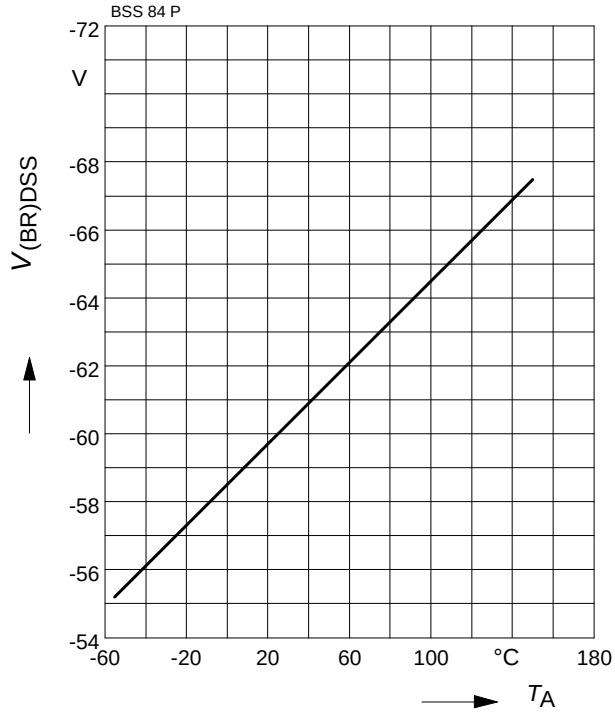
$V_{GS} = f(Q_{Gate})$

parameter: I_D = -0.17 A pulsed; T_j = 25 °C

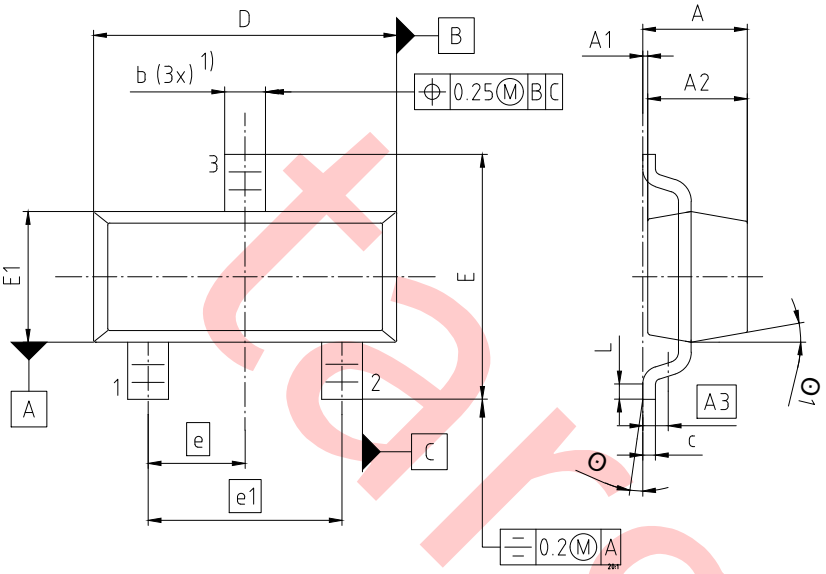


15 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_A)$



5 Package outlines



PACKAGE - GROUP NUMBER:	PG-SOT23-3-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.89	1.22
A1	---	0.10
A2	0.88	1.02
A3	0.25	
b	0.35	0.50
b1	0.10	0.25
c	0.05	0.25
D	2.80	3.00
E	2.25	2.55
E1	1.20	1.40
E2	0.15	0.25
e	0.95	
e1	1.90	
L	0.15	---
θ	0°	8°
θ1	10°	14°
N	3	

NOTES:
1) LEAD WIDTH CAN BE 0.6 MM MAX. IN DAMBAR AREA

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-SOT23-3mm

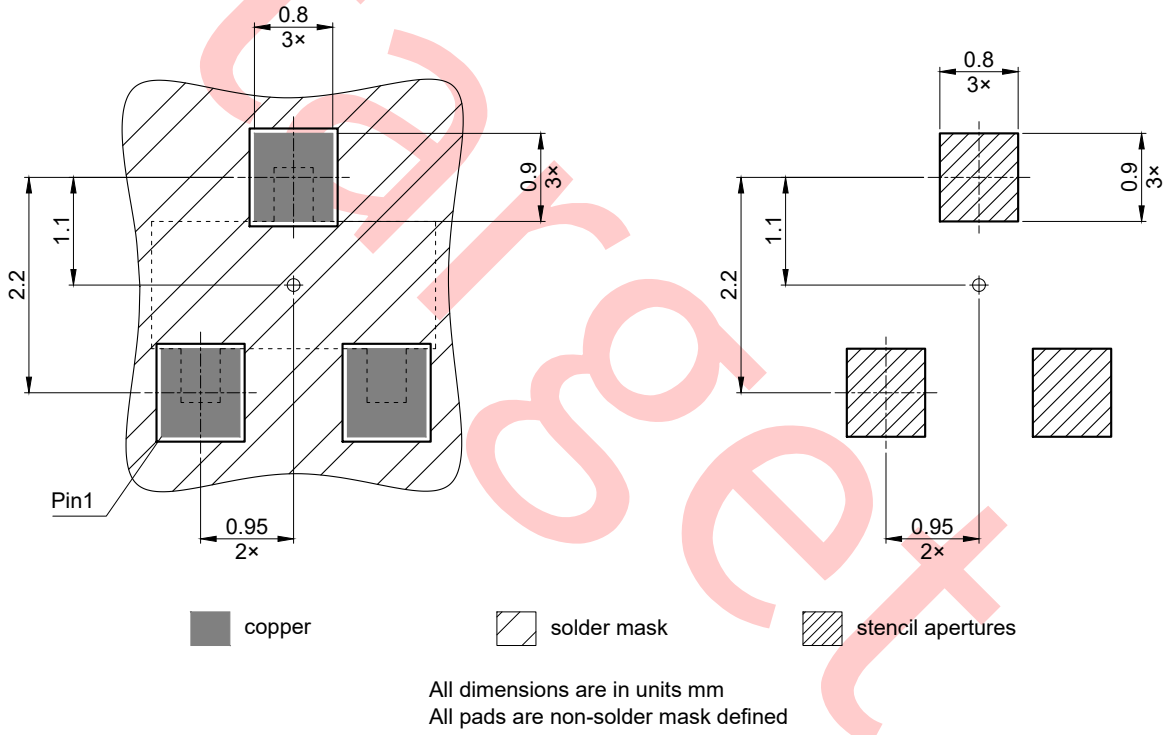


Figure 2 Footprint drawing PG-SOT23-3mm

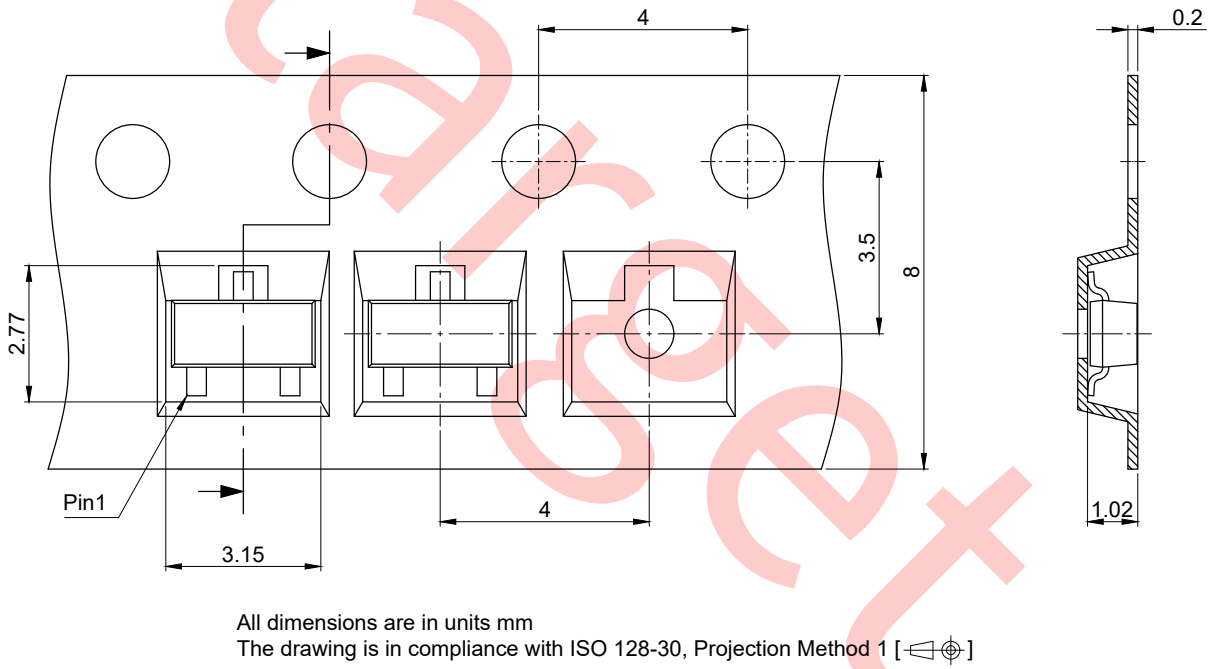


Figure 3 Packaging variant PG-SOT23-3mm

Revision history

BSS84P

Revision 2026-01-29, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-01-29	Update Crss

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