



MEDIATEK

MT6366 Power Management IC Product Brief

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The full datasheet is available with an NDA

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Version History

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Table of Contents

Version History	2
Table of Contents	3
List of Figures	3
List of Tables	3
1 Overview	4
1.1 Features	4
1.2 Applications	4
1.3 General Description	4
1.4 Ordering Information	5
1.5 Boot-up Voltage Table on Each Part	5
1.6 Pin Assignments and Description	8
2 Electrical Characteristics	14
2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range	14
2.2 Thermal Characteristics	14
2.3 Pin Voltage Range	15
2.4 Recommended Operating Range	19
2.5 Electrical Characteristics	19
3 MT6366 Packaging	20
3.1 Package Dimensions	20
Exhibit 1 Terms and Conditions	21

List of Figures

Figure 1-1. MT6366 WLCSP 192 (6.4 x 6 mm) pin assignment (top view)	8
Figure 3-1. Package dimensions	20

List of Tables

Table 1-1. Ordering options	5
Table 1-2. Boot-up voltage table	5
Table 1-3. MT6366 pin description	9
Table 2-1. Absolute maximum ratings	14
Table 2-2. Thermal characteristics	14
Table 2-3. Pin voltage range	15
Table 2-4. Operation condition	19
Table 2-5. General electrical specification	19

1 Overview

1.1 Features

- Handles IoT devices baseband power management
- Input range: 2.6V~5V
- 9 buck converters and 33 LDOs optimized for specific IoT devices subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- 32K-crystal-less RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- SPI interface
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- Storage card plug-out protection
- 192-pin MIFO WLCSP package

1.2 Applications

- MT6366 is ideal for power management of IoT devices and other portable systems.

1.3 General Description

The MT6366 is a power management system chip optimized for IoT devices. It includes 9 buck converters and 33 LDOs optimized for specific IoT devices subsystems.

Sophisticated controls are available for power-up and the RTC alarm. MT6366 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

The MT6366 adopts SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and a protocol for handshaking with baseband.

MT6366 is available in a 192-pin MIFO WLCSP package. The operating temperature ranges from -30 to +85°C.

1.4 Ordering Information

Table 1-1. Ordering options

Part Number	Package	Operational Temperature Range
MT6366W/A	192-pin MIFO WLCSP	-30~+85°C
MT6366MW/A	192-pin MIFO WLCSP	-30~+85°C
MT6366AW/A	192-pin MIFO WLCSP	-30~+85°C
MT6366NW/A	192-pin MIFO WLCSP	-30~+85°C

1.5 Boot-up Voltage Table on Each Part

Table 1-2. Boot-up voltage table

BUCK Name	Default Voltage (V)	V _{OUT} (Volt)	Voltage Step (mV)	I _{MAX} (mA)	Default ON (Y/N)	Application
VPROC11	0.800 (MT6366W) 0.750 (MT6366MW) 0.750 (MT6366AW) 0.750 (MT6366NW)	0.5~1.2	6.25	5,000	Y	Processor
VPROC12	0.800 (MT6366W) 0.750 (MT6366MW) 0.750 (MT6366AW) 0.750 (MT6366NW)	0.5~1.2	6.25	5,000	Y	Processor
VGPU	0.800 (MT6366W) 0.850 (MT6366MW) 0.750 (MT6366AW) 0.850 (MT6366NW)	0.5~1.1	6.25	5,000	Y	GPU
VCORE	0.800 (MT6366W) 0.750 (MT6366MW) 0.750 (MT6366AW) 0.750 (MT6366NW)	0.5~1.1	6.25	5,000	Y	Digital core always on
VMODEM	0.775 (MT6366W) 0.825 (MT6366MW) 0.750 (MT6366AW) 0.825 (MT6366NW)	0.5 ~ 1.1 ⁽²⁾	6.25	3,250	Y	MODEM
VDRAM1	1.125/1.225	1.06~1.3	12.5	2,300	Y	DRAM
VS1	2.0	1.86~2.2	12.5	2,000	Y	SYS LDOs power
VS2	1.35	1.25~1.5	12.5	2,000	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	1,000 ⁽¹⁾	N	3G/LTE PA

Note:

(1) Because PA application is resistance load and $R_{PA,MIN}=4.5$ ohm, VPA I_{MAX} is determined as the equation: $V_{OUT}/R_{PA,MIN}$ except I_{MAX} = 1,000 mA when V_{OUT} ≥ 3.4V.

(2) Max. V_{OUT} range is limited by platform application.
VCORE/VGPU/VMODEM V_{OUT_LIMIT}=1.1V

Type	LDO Name	Input Power Domain	Control Power Domain	Default Voltage (V)	Output Voltage (V)	I _{max} (mA)	Application
ALDO	VFE28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	50 mA	RF AFE
ALDO	VXO22	VSYS_LDO1	VSYS_LDO1	2.24	2.24	25 mA	DCXO
SLDO1	VRF18	VS1_LDO1	VSYS_SMPS	1.81	1.81	450 mA	RF
SLDO2	VRF12	VS2_LDO2	VSYS_LDO3	1.2	1.2	800 mA	RF
SLDO1	VEFUSE	VS1_LDO1	VSYS_SMPS	1.8	1.8	300 mA	E-Fuse
DLDO	VCN33	VSYS_LDO3	VSYS_LDO3	3.5	3.3/ 3.4/ 3.5/ 3.6	800 mA	Connectivity
ALDO	VCN28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	50 mA	Connectivity
SLDO1	VCN18	VS1_LDO1	VSYS_SMPS	1.8	1.8/ 1.5	300 mA	Connectivity
SLDO2	VA12	VS2_LDO2	VSYS_LDO3	1.2	1.2	300 mA	AP
ALDO	VAUX18	VSYS_LDO1	VSYS_LDO1	1.8	1.8	50 mA	AUXADC
ALDO	VAUD28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	50 mA	AUDIO
DLDO	VIO28	VSYS_LDO2	VSYS_LDO2	2.8	2.8	200 mA	I/O and sensor
SLDO1	VIO18	VS1_LDO1	VSYS_SMPS	1.8	1.8	650 mA	I/O and eMMC
SLDO2	VSRAM_PROC11	VS2_LDO3	VSYS_LDO3	0.9 (MT6366W) 0.85 (MT6366MW) 0.85 (MT6366AW) 0.85 (MT6366NW)	0.6~1.2	600 mA	SRAM
SLDO2	VSRAM_PROC12	VS2_LDO3	VSYS_LDO3	0.9 (MT6366W) 0.85 (MT6366MW) 0.85 (MT6366AW) 0.85 (MT6366NW)	0.6~1.2	600 mA	SRAM
SLDO2	VSRAM_OTHERS	VS2_LDO3	VSYS_LDO3	0.9 (MT6366W) 0.75 (MT6366MW) 0.75 (MT6366AW) 0.75 (MT6366NW)	0.55~1.2	600 mA	SRAM
SLDO2	VSRAM_GPU	VS2_LDO3	VSYS_LDO3	0.9 (MT6366W) 0.85 (MT6366MW) 0.75 (MT6366AW) 0.85 (MT6366NW)	0.65~1.2	600 mA	SRAM
SLDO2	VSRAM_CORE	VS2_LDO3	VSYS_LDO3	0.9 (MT6366W) 0.825 (MT6366MW) 0.75 (MT6366AW) 0.825 (MT6366NW)	0.65~1.2	600 mA	SRAM
SLDO1	VM18	VS1_LDO1	VSYS_SMPS	1.84	1.84	300 mA	DRAM IO
SLDO2	VMDDR	VS2_LDO1	VSYS_LDO3	0.75	0.75	600 mA	DRAM
SLDO2	VDRAM2	VS2_LDO1	VSYS_LDO3	0.6	0.6	600 mA	DRAM
					1.8	10 mA	
DLDO	VMC	VSYS_LDO2	VSYS_LDO2	3.0	1.86/ 2.9/ 3.0/ 3.3	200 mA	MSDC
DLDO	VMCH	VSYS_LDO2	VSYS_LDO2	3.0	2.9/ 3.0/ 3.3	800 mA	SD card

Type	LDO Name	Input Power Domain	Control Power Domain	Default Voltage (V)	Output Voltage (V)	I _{max} (mA)	Application
DLDO	VEMC	VSYS_LDO3	VSYS_LDO3	3.0	2.9/ 3.0/ 3.3	800 mA	eMMC and UFS
DLDO	VSIM1	VSYS_LDO1	VSYS_LDO1	1.86	1.86/ 3.0/ 3.1	200 mA	SIM1 card
DLDO	VSIM2	VSYS_LDO2	VSYS_LDO2	1.86	1.86/ 3.0/ 3.1	200 mA	SIM2 card
DLDO	VIBR	VSYS_LDO3	VSYS_LDO3	2.8	1.2/ 1.3/ 1.5/ 1.8/ 2.0/ 2.8/ 3.0/ 3.3	200 mA	Vibrator
DLDO	VUSB	VSYS_LDO1	VSYS_LDO1	3.07	3.07	200 mA	USB power and audio
ALDO	VBIF28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	50 mA	BIF
VRTC	VRTC28	VSYSYS	VSYSYS	2.8	2.8	2 mA	RTC macro
VDIG	DVDD18_DIG	VSYSSENS	VSYSSENS	1.8	1.8	10 mA	PMIC internal digital power

1.6 Pin Assignments and Description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	VS1	GND_V S1	VPA	VSYS_VPA	VSYS_VPROC11	VPROC1_1	GND_VPROC1_1	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	NC	A
B	VSYS_VS1	VS1	GND_V S1	GND_V PA	-	VSYS_VPROC11	VPROC1_1	GND_VPROC1_1	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	GND_VCORE_FB	B
C	VSYS_VS1	-	-	-	-	-	-	-	-	-	-	-	-	-	GND_VGPU_FB	VCORE_FB	C
fD	-	PWRKEY	EXT_PM IC_EN1	RESETB	VPA_FB	VPROC11_FB	GND_VPROC11_FB	GND_VPROC12_2	GND_VPROC12	GND_VPROC12_FB	VDRAM1_FB	GND_VGPU	GND_VGPU	VGPU_FB	VMODEM_FB	VS2_FB	D
E	GND_SMPS	VSYS_S MPS	VEFUSE	VS1_LD O1	EXT_P MIC_E N2	VM18	VS1_FB	PMU_T ESTIMO DE	VPROC12_FB	-	-	GND_VDRAM1_FB	-	GND_VMODEM_FB	-	-	E
F	AU_V18N	FLYN	VIO18	-	VRF18	VCN18	D_GND	D_GND	D_GND	RTC32K1V8_0	SPI_CLK	WDTRS_TB_IN	SPI_CS_N	VSYS_VMODEM	VMODEM	VMODEM	F
G	-	FLYP	-	AU_HP_R	AU_LO_LP	AU_LO_LN	D_GND	D_GND	D_GND	SPI_MISO	SPI_MOSI	RTC32K1V8_1	HOMEKEY	-	GND_VMODEM	GND_VMODEM	G
H	AVSS1_8_AU_D	AVDD1_8_AUD	-	AU_HP_L	AU_RE_FN	AU_HS_N	D_GND	D_GND	D_GND	AUD_CLK_MISO	AUD_D_AT_MISO1	-	SCP_VREQ_VA_O	-	GND_VDRAM1	-	H
J	-	-	AVDD2_8_AUD	HP_EIN_T	AVSS2_8_AUD	AU_HS_P	SRCLKEN_IN1	DVDD1_8_DIG	AUD_D_AT_MOSI0	AUD_SYNC_MISO	AUD_D_AT_MISO0	-	SD_CARD_DET_N	-	VDRAM1	VSYS_VDRAM1	J
K	AU_VI_N0_P	-	AU_VIN_2_N	AU_VIN_2_P	AU_MIBIAS0	ACCDET	-	-	-	AUD_SYNC_MOSI	-	VCDT	CHRLD_O	-	VSYS_VS2	VSYS_VS2	K
L	AU_VI_N0_N	-	AU_VIN_1_N	AU_VIN_1_P	AU_MIBIAS1	FSOURCE	SRCLKEN_IN0	DVSS18_IO	DVDD1_8_IO	AUD_D_AT_MOSI1	AUD_CLK_MOSI	BATON	BATADC	GND_VS2	VS2	VS2	L
M	-	AUXADC_VIN	AVDD1_8_AUXADC	AVSS18_AUXADC	CS_N	VAUX1_8	RTC32K2V8	VRTC28	VBIF28	VCN33	VSYSSEN_S	VREF	UVLO_VTH	VS2_LD_O4	VMDDR	-	M
N	XTAL1	AVSS22_XO_IS_O	-	XO_NFC	-	CS_P	VSIM1	VUSB	VIO28	VSYS_LDO3	VSRAM_CORE	-	GND_VREF	VS2_LD_O2	VRF12	VA12	N
P	XTAL2	AVSS22_XO	XO_WCN	XO_SOC	XO_EX_T	VXO22	VSYS_LDO1	-	VSYS_LDO2	VSIM2	VIBR	VSRAM_PROC1_1	VS2_LD_O3	VSRAM_OTHERS	VDRAM2	VRF12_S	P
R	NC	AVSS22_XOBU_E	XO_CEL	-	VAUD2_8	VCN28	VFE28	-	VMC	VMCH	VEMC	-	VSRAM_PROC1_2	VSRAM_GPU	VS2_LD_O1	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

I
O
PWR
GND
I/O
NC

Figure 1-1. MT6366 192-pin MIFO WLCSP Package (6.4 x 6 mm) pin assignment (top view)

Table 1-3. MT6366 pin description

Ball Name	Ball Location	I/O Type	Description
LDO			
VSRAM_CORE	N11	O	VSRAM_CORE output voltage
VSRAM_PROC12	R13	O	VSRAM_PROC12 output voltage
VSRAM_PROC11	P12	O	VSRAM_PROC11 output voltage
VSRAM_OTHERS	P14	O	VSRAM_OTHERS output voltage
VSRAM_GPU	R14	O	VSRAM_GPU output voltage
VUSB	N8	O	VUSB output voltage
VSIM2	P10	O	VSIM2 output voltage
VSIM1	N7	O	VSIM1 output voltage
VRF18	F5	O	VRF18 output voltage
VRF12	N15	O	VRF12 output voltage
VRF12_S	P16	I	LDO VRF12_S feedback pin
VMCH	R10	O	VMCH output voltage
VMC	R9	O	VMC output voltage
VIO28	N9	O	VIO28 output voltage
VIO18	F3	O	VIO18 output voltage
VIBR	P11	O	VIBR output voltage
VFE28	R7	O	VFE28 output voltage
VEMC	R11	O	VEMC33 output voltage
VEFUSE	E3	O	VEFUSE output voltage
VDRAM2	P15	O	VDRAM2 output voltage
VCN28	R6	O	VCN28 output voltage
VCN18	F6	O	VCN18 output voltage
VM18	E6	O	VM18 output voltage
VMDDR	M15	O	VMDDR output voltage
VCN33	M10	O	VCN33 output voltage
VBIF28	M9	O	VBIF28 output voltage
VAUX18	M6	O	VAUX18 output voltage
VAUD28	R5	O	VAUD28 output voltage
VA12	N16	O	VA12 output voltage
VXO22	P6	O	VXO22 output voltage
VRTC28	M8	O	RTC LDO output. Supply of RTC macro where a backup battery can be added.
VSYS_LDO1	P7	PWR	Power supply input of LDO group 1
VSYS_LDO2	P9	PWR	Power supply input of LDO group 2
VSYS_LDO3	N10	PWR	Power supply input of LDO group 3
VS1_LDO1	E4	PWR	2V power supply of SLDO1
VS2_LDO1	R15	PWR	1.125V power supply of SLDO1
VS2_LDO2	N14	PWR	1.35V power supply of SLDO2
VS2_LDO3	P13	PWR	1.35V power supply of SLDO3

Ball Name	Ball Location	I/O Type	Description
VS2_LDO4	M14	PWR	1.125V power supply of SLDO4
GPIO			
AUD_SYNC_MOSI	K10	I/O	Audio control interface
AUD_SYNC_MISO	J10	I/O	Audio control interface
AUD_DAT_MOSI1	L10	I/O	Audio control interface
AUD_DAT_MOSI0	J9	I/O	Audio control interface
AUD_DAT_MISO1	H11	I/O	Audio control interface
AUD_DAT_MISO0	J11	I/O	Audio control interface
AUD_CLK_MOSI	L11	I	Audio control interface
AUD_CLK_MISO	H10	O	Audio control interface
SPI_MOSI	G11	I/O	SPI control interface
SPI_MISO	G10	I/O	SPI control interface
SPI_CSN	F13	I/O	SPI control interface
SPI_CLK	F11	I	SPI control interface
BUCK			
VSYS_SMPS	E2	PWR	Power supply of buck controller
VSYS_VPROC11	A6, B6	PWR	Power supply of VPROC11
VSYS_VPROC12	A10, B10	PWR	Power supply for VPROC12
VSYS_VCORE	A15, B15	PWR	Power supply for VCORE
VSYS_VGPU	A11, B11	PWR	Power supply for VGPU
VSYS_VMODEM	F14	PWR	Power supply for VMODEM
VSYS_VDRAM1	J16	PWR	Power supply of VDRAM1
VSYS_VS1	B1, C1	PWR	Power supply of VS1
VSYS_VS2	K15, K16	PWR	Power supply of VS2
VSYS_VPA	A5	PWR	Power supply for VPA
VPROC11	A7, B7	O	Software node of VPROC11
VPROC12	A9, B9	O	Software node of VPROC12
VCORE	A14, B14	O	Software node of VCORE
VGPU	A12, B12	O	Software node of VGPU
VMODEM	F15, F16	O	Software node of VMODEM
VDRAM1	J15	O	Software node of VDRAM1
VS1	A2, B2	O	Software node of VS1
VS2	L15, L16	O	Software node of VS2
VPA	A4	O	Software node of VPA
VPROC11_FB	D6	I	BUCK VPROC11 feedback pin on V _{OUT}
VPROC12_FB	E9	I	BUCK VPROC12 feedback pin on V _{OUT}
VCORE_FB	C16	I	BUCK VCORE feedback pin on V _{OUT}
VGPU_FB	D14	I	BUCK VGPU feedback pin on V _{OUT}
VMODEM_FB	D15	I	BUCK VMODEM feedback pin on V _{OUT}
VDRAM1_FB	D11	I	BUCK VDRAM1 feedback pin on V _{OUT}
VS1_FB	E7	I	BUCK VS1 feedback pin

Ball Name	Ball Location	I/O Type	Description
VS2_FB	D16	I	BUCK VS2 feedback pin
VPA_FB	D5	I	BUCK VPA feedback pin on V _{OUT}
GND_VPROC11_FB	D7	I	Remote sense on ground of VPROC11 V _{OUT}
GND_VPROC11	A8, B8	GND	VPROC11 ground
GND_VPROC12_FB	D10	I	Remote sense on ground of VPROC12 V _{OUT}
GND_VPROC12	D8, D9	GND	VPROC12 ground
GND_VCORE_FB	B16	I	Remote sense on ground of VCORE
GND_VCORE	A13, B13	GND	VCORE ground
GND_VGPU_FB	C15	I	Remote sense on ground of VGPU V _{OUT}
GND_VGPU	D12, D13	GND	VGPU ground
GND_VMODEM_FB	E14	I	Remote sense on ground of VMODEM V _{OUT}
GND_VMODEM	G15, G16	GND	VMODEM ground
GND_VDRAM1_FB	E12	I	Remote sense on ground of VDRAM1 V _{OUT}
GND_VDRAM1	H15	GND	VDRAM1 ground
GND_VS1	A3, B3	GND	VS1 ground
GND_VS2	L14	GND	VS2 ground
GND_VPA	B4	GND	VPA ground
GND_SMPS	E1	GND	GND of buck controller
Digital			
DVDD18_IO	L9	PWR	Digital I/O power
DVSS18_IO	L8	GND	Digital I/O power GND
DVDD18_DIG	J8	PWR	VDIG18 output voltage
FSOURCE	L6	PWR	eFuse power source
Interface			
PWRKEY	D2	I	PWRKEY button
HOMEKEY	G13	I	HOMEKEY button
RESETB	D4	O	System reset release signal
WDTRSTB_IN	F12	I	Watchdog reset from the AP
SRCLKEN_IN1	J7	I	Source clock enable pin 1
SRCLKEN_IN0	L7	I	Source clock enable pin 0
SD_CARD_DET_N	J13	I	Voltage source requests input pin, connected to SD card
SCP_VREQ_VAO	H13	I	Voltage source request input pin, connected to SoC
EXT_PMIC_EN2	E5	O	Ext. chip enable pin2
EXT_PMIC_EN1	D3	O	Ext. chip enable pin1
Clock			
RTC32K_2V8	M7	O	VRTC domain 32 kHz clock output
RTC32K_1V8_1	G12	O	VIO18 domain 32 kHz clock output
RTC32K_1V8_0	F10	O	VIO18 domain 32 kHz clock output
XTAL2	P1	I/O	XTAL input 2
XTAL1	N1	I/O	XTAL input 1
XO_WCN	P3	O	26 MHz output to Conn. RF

Ball Name	Ball Location	I/O Type	Description
XO_SOC	P4	O	26 MHz output to SoC
XO_NFC	N4	O	26 MHz output to NFC
XO_EXT	P5	O	26 MHz output to UFS
XO_CEL	R3	O	26 MHz output to Cell. RF
AVSS22_XOBUF	R2	GND	Ground for XO
AVSS22_XO_ISO	N2	GND	Connect to GSUB for DCXO noise isolation
AVSS22_XO	P2	GND	Ground for XO
Audio and AUXADC			
AVDD28_AUD	J3	PWR	Power supply of audio UL
AVDD18_AUXADC	M3	PWR	1.8V power supply of AUXADC
AVDD18_AUD	H2	PWR	1.8V power supply of audio
AVSS28_AUD	J5	GND	Audio UL ground
AVSS18_AUXADC	M4	GND	AUXADC ground
AVSS18_AUD	H1	GND	Audio DL ground
AUXADC_VIN	M2	I	AUXADC input
HP_EINT	J4	I	HPL detection
FLYP	G2	O	Flying capacitor top
FLYN	F2	O	Flying capacitor bottom
CS_P	N6	I	Fuel gauge ADC input pin
CS_N	M5	I	Fuel gauge ADC input pin
AU_VIN2_P	K4	I	Microphone channel 2 positive input
AU_VIN2_N	K3	I	Microphone channel 2 negative input
AU_VIN1_P	L4	I	Microphone channel 1 positive input
AU_VIN1_N	L3	I	Microphone channel 1 negative input
AU_VIN0_P	K1	I	Microphone channel 0 positive input
AU_VIN0_N	L1	I	Microphone channel 0 negative input
AU_V18N	F1	PWR	Audio -1.8V supply
AU_REFN	H5	GND	Audio reference ground
AU_MICBIAS1	L5	O	Microphone bias 1
AU_MICBIAS0	K5	O	Microphone bias 0
AU_LOLP	G5	O	Lineout positive output
AU_LOLN	G6	O	Lineout negative output
AU_HSP	J6	O	Handset positive output
AU_HSN	H6	O	Handset negative output
AU_HPR	G4	O	Earphone right channel output
AU_HPL	H4	O	Earphone left channel output
ACCDT	K6	I	Accessory detection input
Internal Reference and Detection			
VSYSNS	M11	I	VSYS supply input for internal block and UVLO detection
VREF	M12	O	Band-gap reference voltage
GND_VREF	N13	GND	Ground for band-gap

Ball Name	Ball Location	I/O Type	Description
UVLO_VTH	M13	I	UVLO threshold control pin
CHRLDO	K13	O	CHRLDO output voltage
BATON	L12	I	Battery NTC pin for battery and its temperature sensing
BATADC	L13	I	Fuel gauge ADC input pin for battery voltage monitoring
VCDT	K12	I	Fractional charger input voltage for charger detection
PMU_TESTMODE	E8	I	PMU test mode signal (tied to GND in normal operation)
D_GND	F7, F8, F9, G7, G8, G9, H7, H8, H9	GND	Ground
NC	A1, A16, R1, R16	NC	NC

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery pin input ⁽¹⁾	Steady state	-0.5		6	V
	Transient (< 10 ms)	-0.5		7	V
Non-battery power pin ⁽²⁾	Steady state	-0.5		5	V
Signal pins ⁽³⁾	Steady state	-0.5		V _{xx} +0.5 ⁽³⁾	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

(1) Note 1 VSYS_XXX/V_{xxx} (BUCK SW node)/VSYSNS/BATADC -> battery input pin

(2) Note 2 Non-battery power input -> reference Table 1-3 (PWR pin but not connected with battery)

(3) Note 3 V_{xx} = Max. operation voltage (refer to Table 2-3)

2.2 Thermal Characteristics

Table 2-2. Thermal characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal resistance from junction to ambient	In free air		36		°C/W

Note. The device is mounted on an 8-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists the operational range voltages for all MT6366 input/output (I/O) pins.

Table 2-3. Pin voltage range

Ball	Symbol	Voltage Range	Unit
P1	XTAL2	0~2.2	V
N1	XTAL1	-0.2~2.2	V
P3	XO_WCN	0~1.98	V
P4	XO_SOC	0~1.30	V
N4	XO_NFC	0~1.30	V
P5	XO_EXT	0~1.30	V
R3	XO_CEL	0~1.98	V
F12	WDTRSTB_IN	0~1.98	V
P6	VXO22	0~2.42	V
N8	VUSB	0~3.63	V
M11	VSYSSENS	0~5	V
K15, K16	VSYS_VS2	0~5	V
B1, C1	VSYS_VS1	0~5	V
A10, B10	VSYS_VPROC12	0~5	V
A6, B6	VSYS_VPROC11	0~5	V
A5	VSYS_VPA	0~5	V
F14	VSYS_VMODEM	0~5	V
A11, B11	VSYS_VGPU	0~5	V
J16	VSYS_VDRAM1	0~5	V
A15, B15	VSYS_VCORE	0~5	V
E2	VSYS_SMPS	0~5	V
N11	VSRAM_CORE	0~1.4	V
P9	VSYS_LDO2	0~5	V
P7	VSYS_LDO1	0~5	V
R13	VSRAM_PROC12	0~1.4	V
P12	VSRAM_PROC11	0~1.4	V
P14	VSRAM_OTHERS	0~1.4	V
R14	VSRAM_GPU	0~1.4	V
P10	VSIM2	0~5	V
N7	VSIM1	0~5	V
M14	VS2_LDO4	0~2.2	V
P13	VS2_LDO3	0~2.2	V
N14	VS2_LDO2	0~2.2	V
R15	VS2_LDO1	0~2.2	V
D16	VS2_FB	0~5	V
L15, L16	VS2	0~5	V
E4	VS1_LDO1	0~2.2	V
E7	VS1_FB	0~5	V
A2, B2	VS1	0~5	V

Ball	Symbol	Voltage Range	Unit
M8	VRTC28	0~2.98	V
F5	VRF18	0~2.2	V
P16	VRF12_S	0~1.4	V
N15	VRF12	0~1.4	V
M12	VREF	0~1.32	V
E9	VPROC12_FB	0~5	V
A9, B9	VPROC12	0~5	V
D6	VPROC11_FB	0~5	V
A7, B7	VPROC11	0~5	V
D5	VPA_FB	0~5	V
A4	VPA	0~5	V
D15	VMODEM_FB	0~5	V
F15, F16	VMODEM	0~5	V
R10	VMCH	0~5	V
R9	VMC	0~5	V
N9	VIO28	0~5	V
F3	VIO18	0~2.2	V
P11	VIBR	0~5	V
D14	VGPU_FB	0~5	V
A12, B12	VGPU	0~5	V
R7	VFE28	0~5	V
R11	VEMC	0~5	V
E3	VEFUSE	0~2.2	V
P15	VDRAM2	0~1.4	V
D11	VDRAM1_FB	0~5	V
J15	VDRAM1	0~5	V
C16	VCORE_FB	0~5	V
A14, B14	VCORE	0~5	V
R6	VCN28	0~5	V
F6	VCN18	0~2.2	V
K12	VCDT	0~2.94	V
E6	VM18	0~2.2	V
M15	VMDDR	0~1.4	V
N10	VSYS_LDO3	0~5	V
M10	VCN33	0~5	V
M9	VBIF28	0~5	V
M6	VAUX18	0~2.2	V
R5	VAUD28	0~5	V
N16	VA12	0~1.4	V
M13	UVLO_VTH	0~5	V
J7	SRCLKEN_IN1	0~1.98	V
L7	SRCLKEN_IN0	0~1.98	V
G11	SPI_MOSI	0~1.98	V
G10	SPI_MISO	0~1.98	V
F13	SPI_CSN	0~1.98	V

Ball	Symbol	Voltage Range	Unit
F11	SPI_CLK	0~1.98	V
J13	SD_CARD_DET_N	0~1.98	V
H13	SCP_VREQ_VAO	0~1.98	V
M7	RTC32K_2V8	0~2.98	V
G12	RTC32K_1V8_1	0~1.98	V
F10	RTC32K_1V8_0	0~1.98	V
D4	RESETB	0~1.98	V
D2	PWRKEY	0~5	V
E8	PMU_TESTMODE	0~5	V
A1, A16, R1, R16	NC	0~5	V
J4	HP_EINT	0~2.94	V
G13	HOMEKEY	0~1.98	V
L14	GND_VS2	0	V
A3, B3	GND_VS1	0	V
N13	GND_VREF	0	V
D10	GND_VPROC12_FB	0	V
D8, D9	GND_VPROC12	0	V
D7	GND_VPROC11_FB	0	V
A8, B8	GND_VPROC11	0	V
B4	GND_VPA	0	V
E14	GND_VMODEM_FB	0	V
G15, G16	GND_VMODEM	0	V
C15	GND_VGPU_FB	0	V
D12, D13	GND_VGPU	0	V
E12	GND_VDRAM1_FB	0	V
H15	GND_VDRAM1	0	V
B16	GND_VCORE_FB	0	V
A13, B13	GND_VCORE	0	V
E1	GND_SMPS	0	V
L6	FSOURCE	0~1.98	V
G2	FLYP	0~1.98	V
F2	FLYN	-1.98~0	V
E5	EXT_PMIC_EN2	0~5	V
D3	EXT_PMIC_EN1	0~5	V
L8	DVSS18_IO	0~1.98	V
L9	DVDD18_IO	0~1.98	V
J8	DVDD18_DIG	0~1.98	V
F7, F8, F9, G7, G8, G9, H7, H8, H9	D_GND	0	V
N6	CS_P	-0.1~0.1	V
M5	CS_N	-0.1~0.1	V
K13	CHRLDO	0~2.94	V
L12	BATON	0~5	V
L13	BATADC	0~5	V
J5	AVSS28_AUD	0	V

Ball	Symbol	Voltage Range	Unit
R2	AVSS22_XOBUF	0	V
N2	AVSS22_XO_ISO	0	V
P2	AVSS22_XO	0	V
M4	AVSS18_AUXADC	0	V
H1	AVSS18_AUD	0	V
J3	AVDD28_AUD	0~2.94	V
M3	AVDD18_AUXADC	0~1.98	V
H2	AVDD18_AUD	0~1.98	V
M2	AUXADC_VIN	0~1.98	V
K10	AUD_SYNC_MOSI	0~1.98	V
J10	AUD_SYNC_MISO	0~1.98	V
L10	AUD_DAT_MOSI1	0~1.98	V
J9	AUD_DAT_MOSI0	0~1.98	V
H11	AUD_DAT_MISO1	0~1.98	V
J11	AUD_DAT_MISO0	0~1.98	V
L11	AUD_CLK_MOSI	0~1.98	V
H10	AUD_CLK_MISO	0~1.98	V
K4	AU_VIN2_P	0~2.94	V
K3	AU_VIN2_N	0~2.94	V
L4	AU_VIN1_P	0~2.94	V
L3	AU_VIN1_N	0~2.94	V
K1	AU_VIN0_P	0~2.94	V
L1	AU_VIN0_N	0~2.94	V
F1	AU_V18N	-1.98~0	V
H5	AU_REFN	0	V
L5	AU_MICBIAS1	0~2.94	V
K5	AU_MICBIAS0	0~2.94	V
G5	AU_LOLP	-1.98~1.98	V
G6	AU_LOLN	-1.98~1.98	V
J6	AU_HSP	-1.98~1.98	V
H6	AU_HSN	-1.98~1.98	V
G4	AU_HPR	-1.98~1.98	V
H4	AU_HPL	-1.98~1.98	V
K6	ACCDDET	0~2.94	V

2.4 Recommended Operating Range

Table 2-4. Operation condition

Parameter	Condition	Min.	Typ.	Max.	Unit
Ambient temperature (TA)		-30		85	°C
Junction temperature (TJ)		-30		125	°C
Operating input voltage		3.15 (Note)		5	V

Note : This applicable minimum input voltage depends on the detailed test conditions for each function as specified in the electrical characteristics table.

2.5 Electrical Characteristics

- VBAT = 2.6~5V, minimum loads applied on all outputs, unless otherwise noted.
- Typical values are at TA = 25°C.

Table 2-5. General electrical specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Current					
Standby without 32K XTAL	Low-power mode		785	950	μA
Power down leakage current without 32K XTAL	VBAT = 4.5V, Temp = 25°C			95	uA
Under Voltage (UV)					
Under voltage falling threshold		2.55	2.6	2.65	V
Under voltage rising threshold	R = 200K	2.95	3.0	3.05	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			32		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			110		°C

3 MT6366 Packaging

3.1 Package Dimensions

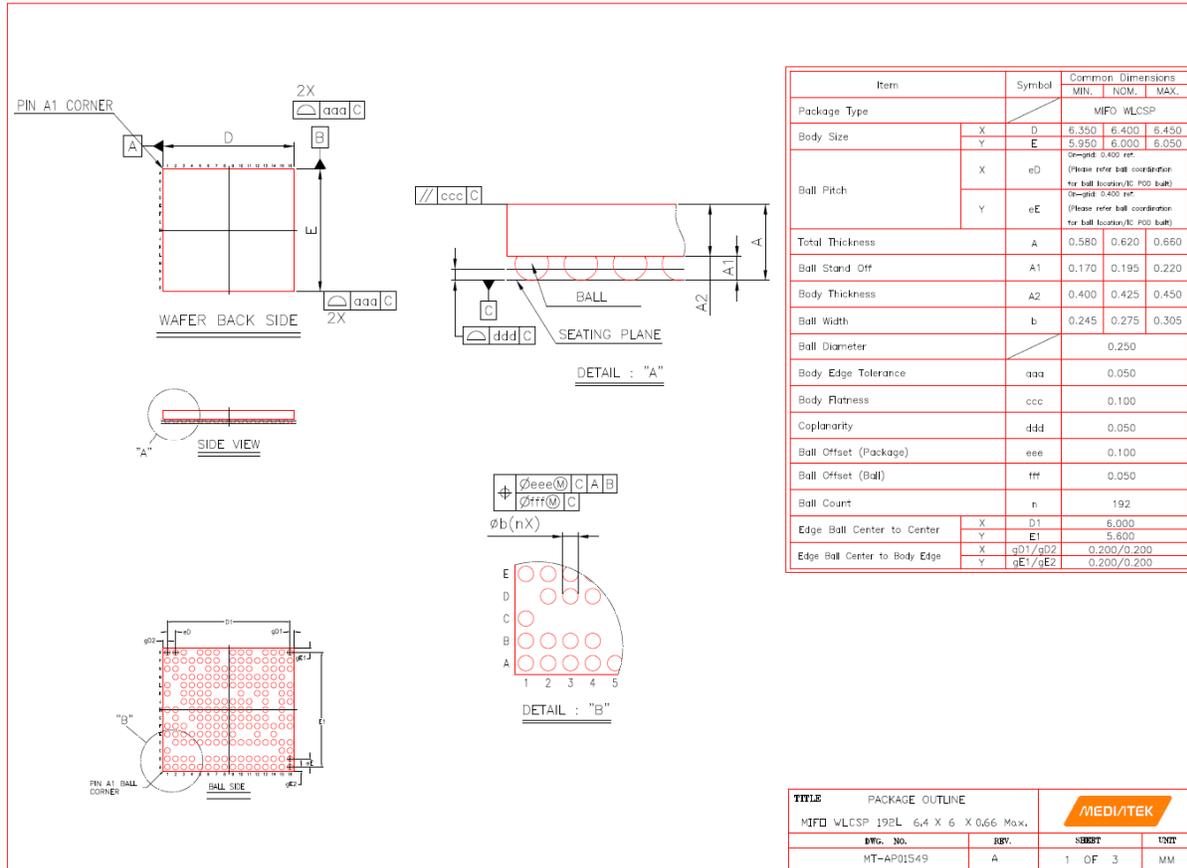


Figure 3-1. Package dimensions

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