LPDDR5X SDRAM

MT62F512M32D1, MT62F512M64D2

Features

- **Architecture**
  - 19.2 GB/s maximum bandwidth per channel
  - Frequency range: 1200–5 MHz (data rate range per pin: 9600–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5/LPDDR5X data interface**
  - Dual x16 channels/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Bank Architecture: Bank Group (BG) mode, and 16-bank (16B) mode supported
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.80V TYP
  - V_{DD2H} = 1.01–1.12V; 1.05V TYP
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
  - V_{DDQ} = 0.50V or 0.45V[1] TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
  - Per byte and per pin DFE support
- **Low power features**
  - Enhanced DVFSC: Enhanced dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
• **Operating Voltage**	F
– $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ}$ (ODT off only):1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V[1]/0.30V	
• **Array Configuration**	
– 512Mb x 32 (512Mb x 16 x 1 Die x 2Ch x 1R)	512M32
– 512Mb x 64 (512Mb x 16 x 1 Die x 4Ch x 1R)	512M64
• **Device configuration**	
– 1 die in package (512Mb32 x 1 die)	D1
– 2 die in package (512Mb32 x 2 die)	D2
• **FBGA RoHS-compliant "green" package**	
– 315-ball TFBGA: 12.4mm x 15.0mm (TYP), seated height 1.1mm (MAX)	DS
– 441-ball TFBGA 14.0mm x 14.0mm (TYP), seated height 1.1mm (MAX)	EK
– 496-ball UFBGA 14.0mm x 12.4mm (TYP), seated height 0.65mm (MAX)	ZX
– 561-ball TFBGA 8.0mm x 12.4mm (TYP), seated height 1.2mm (MAX)	CZ
• Speed grade, cycle time (^{t}WCK)	
– 9600 Mb/s per-pin	-020
– 8533 Mb/s per-pin	-023
– 7500 Mb/s per-pin	-026
• **Operating Temperature:**	
– –25°C ≤ T_C ≤ +85°C	WT
– –40°C ≤ T_C ≤ +95°C	IT
• Revision	:E

Note: 1. V_{DDQ} = 0.45V (TYP) support on all packages up to 7500 Mb/s per-pin.

Part Number Ordering Information

Figure 1: Part Number Chart

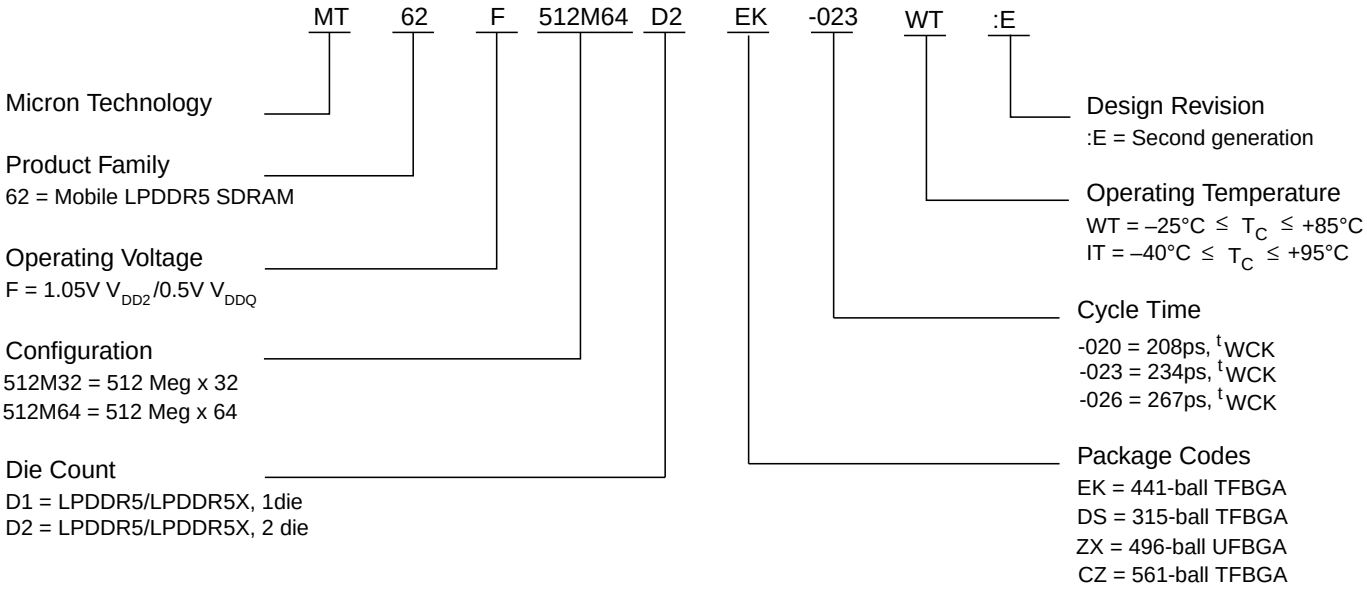

Table 1: Part Number List

Part Number	Total Density (package)	Data Rate per Pin
MT62F512M32D1DS-023 WT:E	2GB (16Gb)	8533 Mb/s
MT62F512M32D1DS-023 WT ES:E		
MT62F512M64D2EK-023 WT:E	4GB (32Gb)	
MT62F512M64D2EK-023 WT ES:E		
MT62F512M64D2CZ-023 WT:E		
MT62F512M64D2CZ-023 WT ES:E		
MT62F512M64D2ZX-023 WT:E		
MT62F512M64D2ZX-023 WT ES:E		
MT62F512M32D1DS-026 WT:E	2GB (16Gb)	7500 Mb/s
MT62F512M64D2EK-026 WT:E	4GB (32Gb)	
MT62F512M64D2CZ-026 WT:E		

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any content defined in this device ID specific data sheet document takes precedence over similar content defined in the general core LPDDR5/LPDDR5X SDRAM data sheet document(s).

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package (x32, 2Ch die)

Die Organization	512M32 (16 Gb/package)
Channel A	x16 mode × 1 Ch of 2Ch die
Channel B	x16 mode × 1 Ch of 2Ch die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Organization in the Package (x64, 2Ch die)

Die Organization	512M64 (32 Gb/package)
Channel A, rank 0	x16 mode × 1 Ch of 2Ch die
Channel B, rank 0	x16 mode × 1 Ch of 2Ch die
Channel C, rank 0	x16 mode × 1 Ch of 2Ch die
Channel D, rank 0	x16 mode × 1 Ch of 2Ch die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 4: Die Addressing

Description	512M32 (16 Gb/package)/512M64 (32 Gb/package)	
Density per channel	8Gb	
Bits per channel	8,589,934,592	
Bank mode	BG mode	16B mode
Configuration	32Mb × 16 DQ × 4 Banks × 4BG	32Mb × 16 DQ × 16 Banks
Number of banks	4	16
Number of bank groups	4	1
Array prefetch bits	256	
Rows per bank	32,768	
Columns	64	
Page size (bytes)	2048	
Native burst length	16	
Number of I/Os	16	
Bank address	BA[1:0]	BA[3:0]
Bank group address	BG[1:0]	–
Row address	R[14:0]	
Column address	C[5:0]	
Burst address	B[3:0]	
Burst starting address boundary	128-bit	

Notes: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.
2. Die addressing is aligned per channel in a 2 channel die

Refresh Requirement Parameters

Table 5: Refresh Requirement Parameters

Parameter	Symbol	8Gb Die	Unit
		BG and 16B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	210	ns
REFRESH cycle time (per bank)	^{t}RFCpb	120	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

CS Rx Relaxed Specification

Table 6: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)														Unit	Note
			67[6]	133	200	266	344	400	467	533	600	688	750	800	937.5	1066.5	1200	
Rx mask																		
CS Rx mask height	vCSIVW	Min	155														mV	2, 7
CS Rx mask width at V_{REF} CS	^{t}CSIVW1	Min	0.3														UI	1
CS Rx mask width at vCSIVW	^{t}CSIVW2	Min	0.22														UI	1
Rx single pulse																		
CS Rx pulse amplitude	vCSIHL_AC	Min	240														mV	3
CS reference voltage	vREFCS		$V_{DD2H}/3$														mV	
CS Rx pulse width	^{t}CSIPW	Min	0.6														UI	
Power down																		
CS V_{IL} during power down/ deep sleep	V_{ILPD}	Max	130														mV	4
CS V_{IH} during power down/ deep sleep	V_{IHPD}	Min	550														mV	5
		Max	V_{DD2H} + 200															

Notes: 1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; No timing requirement above a certain level. vCSIIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.
5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.
6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^{t}CSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.
7. Measured at die pad.

DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 7: DQ Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/ Max	WCK Frequency (MHz)			Unit	Notes
			3750	4266	4800		
DQ Rx mask height	vDIVW	Min	70			mV	1, 2, 3
DQ Rx mask width at $V_{REF(DQ)}$	^{t}DIVW1	Min	0.35			UI	1, 3
DQ Rx mask width at vDIVW	^{t}DIVW2	Min	0.18			UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	^{t}DIPW1	Min	0.51			UI	4
DQ Rx pulse reference	^{t}DIPW2	Min	0.26			UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ± vDIVW/2	^{t}DIHL	Min	0.24			UI	4
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70			mV	
	vDILP1	Max	–70			mV	

Table 7: DQ Rx Mask and Single Input Pulse Specifications (Continued)

Item	Symbol	Min/ Max	WCK Frequency (MHz)			Unit	Notes
			3750	4266	4800		
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55			mV	
	vDILP2	Max	–55			mV	
DQ Vref	VrefDQ	Max	180			mV	
		Min	75			mV	
DQ to DQ Offset	tDQ2DQ	Max	30			ps	5

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (^{t}DIVW1, ^{t}DIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.
5. DQ to DQ offset defined within byte from DRAM pin to internal latch for a given component.

Figure 2: DQ Rx Mask Definition

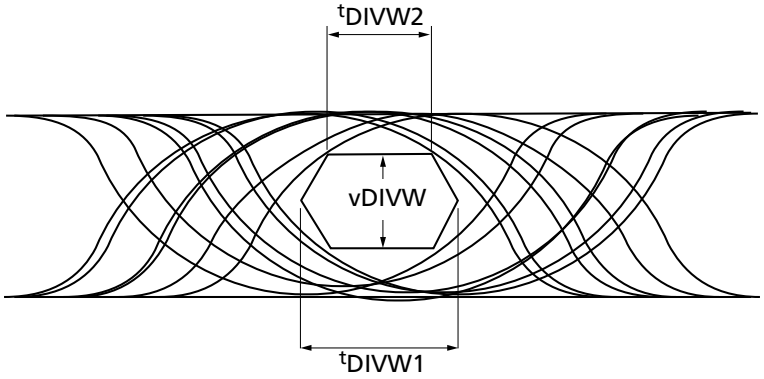
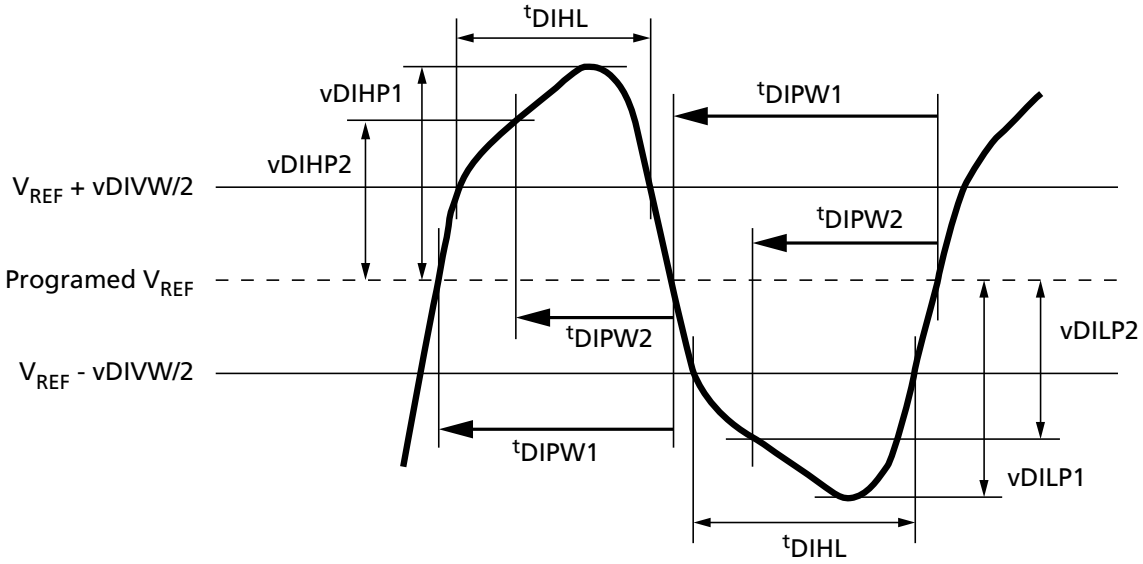


Figure 3: LPDDR5X DQ Single Pulse Definition



Note: 1. vDIHL_AC/2 = vDIHP1 = vDILP1. Programmed $V_{REF(DQ)}$ is defined as percentage of MR14/15 code * V_{DDQ}.

DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Table 8: DQ, DMI, Parity and DBI Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/Max	WCK Frequency (MHz)	Unit	Notes
			3200		
DQ Rx mask height	vDIVW	Min	70	mV	1, 2, 3, 6
DQ Rx mask width at $V_{REF(DQ)}$	tDIVW1	Min	0.35	UI	1, 3
DQ Rx mask width at vDIVW	tDIVW2	Min	0.18	UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	tDIPW1	Min	0.51	UI	4, 6
DQ Rx pulse reference	tDIPW2	Min	0.26	UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ± vDIVW/2	tDIHL	Min	0.24	UI	4, 6
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70	mV	
	vDILP1	Max	–70	mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55	mV	
	vDILP2	Max	–55	mV	
DQ V_{REF}	VREF(DQ)	Min	75	mV	6
		Max	180	mV	6
DQ to DQ offset	tDQ2DQ	Max	30	ps	5

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (tDIVW1, tDIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = tWCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.

5. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
6. When vDIVW is 70mV or more and less than 80mV.

16-Bank Extended Frequency

16-Bank Extended Frequency Description

Micron's LPDDR5 SDRAM device which are marked with 8533 Mb/s per-pin (-023) capability can support frequency set points using 2:1 WCK to CK ratio and above the 1600 MHz limit. Shown in the table below is specification requirements when considering 1867 MHz and 2133 MHz frequencies. This support is not available on 1-alpha process node and earlier Device ID's, this feature can expand capabilities of your system.

Table 9: 16-Bank Operation[1] @ 4.3 Gb/s

Parameter	3733 Mb/s per-pin	Comments	4267 Mb/s per-pin	Comments
RL Set 1/2/3	20/22/24	MR2[3:0] = 1100	23/25/26	MR2[3:0] = 1101
*n*RBTP	6		6	
WL Set A/B	11/19	MR1[7:4] = 1100	12/22	MR1[7:4] = 1101
*n*WR x16/x8	32/34	MR2[7:4] = 1100	37/39	MR2[7:4] = 1101
^{t}WCKPRE_static[2]	5	Follows 7500 data rate	6	Follows 8533 data rate
^{t}WCKPRE_WR_toggle	4	Follows 3200 datarate	4	Follows 3200 data rate
^{t}WCKPRE_RD_toggle	10	Follows 3200 datarate	10	Follows 3200 data rate
^{t}WCKENL_FS	2	Follows 3200 data rate	2	Follows 3200 data rate
^{t}WCKPRE_toggle_FS[3]	14	Minimum	16	Minimum
ODTLon	WL - 4	Follows 3200 data rate	WL - 4	Follows 3200 data rate
ODTLoff[4]	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200 data rate
ODTLoff_RD_DQ	RL - 4	Follows 3200 data rate	RL - 4	Follows 3200 data rate
ODTLoff_RD_RDQS	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010
	RL - 8	MR10 OP[1, 5:4] = 011, 1XX	RL - 8	MR10 OP[1, 5:4] = 011, 1XX
ODTLon_RD_DQ[5]	RL + 6 (BL16), RL + 10 (BL32)		RL + 6 (BL16), RL + 10 (BL32)	
ODTLon_RD_RDQS[6]	RL + 8 (BL16), RL + 12 (BL32)		RL + 8 (BL16), RL + 12 (BL32)	

Notes: 1. Restricted to WCK:CK 2:1 ratio, WCK:CK 4:1 ratio not supported; Link ECC is disabled, and DVFSC/E-DVFSC is disabled.
2. Common for WR/RD/FS.
3. Minimum 1 + RL - (^{t}WCKENL_FS + ^{t}WCKPRE_Static) when CAS to RD is 1CK.
4. (WL + BL/n_min + RU(^{t}WCK2DQI(max)/^{t}CK)).
5. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)).
6. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)) + 2.
7. 8533 MT/s or higher data rated parts support 16-bank mode up to 4267 MT/s with restrictions, all other speed rated parts greater than 3200 MT/s per-pin and less than 8533 MT/s per-pin are restricted from the extended 16B

mode capabilities. Refer to the above table for constraints for operating in 16-bank mode when data rate is greater than 3200 MT/s per-pin and equal to or less than 4267 MT/s per-pin.

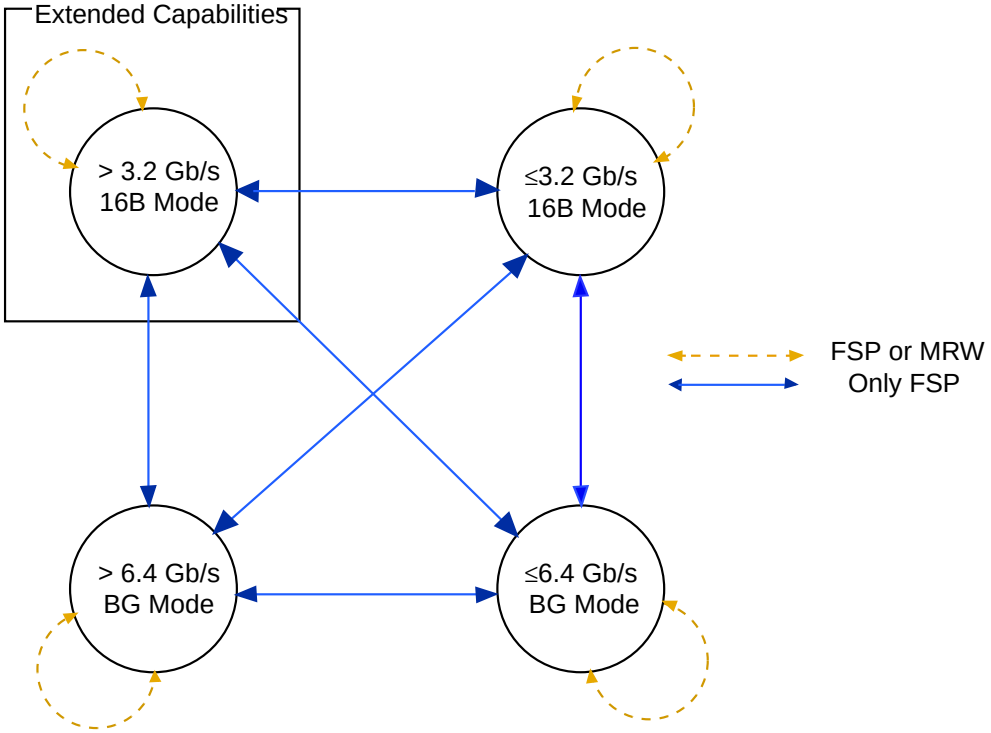
8. When operating in the 16-bank mode, the FSP procedure must be used when setting the data rate above 3.2 Gb/s per-pin even when setting for the first time. For example, if the device is powered-up and initialized for 4266 Gb/s per-pin timing at the initial operation start, the FSP procedure must still be used. See Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities on page 14 for details of FSP usage.

16B/BG Data Rate Change Diagram With FSP Requirements

The following flow chart diagram shows the needed 16-bank (16B) and bank group (BG) data rate change details and how the frequency set protocol (FSP) supports the extended frequency range.

The diagram below represents the device extended capabilities which are extended to 4267 Mb/s per-pin data rate in 16B mode.

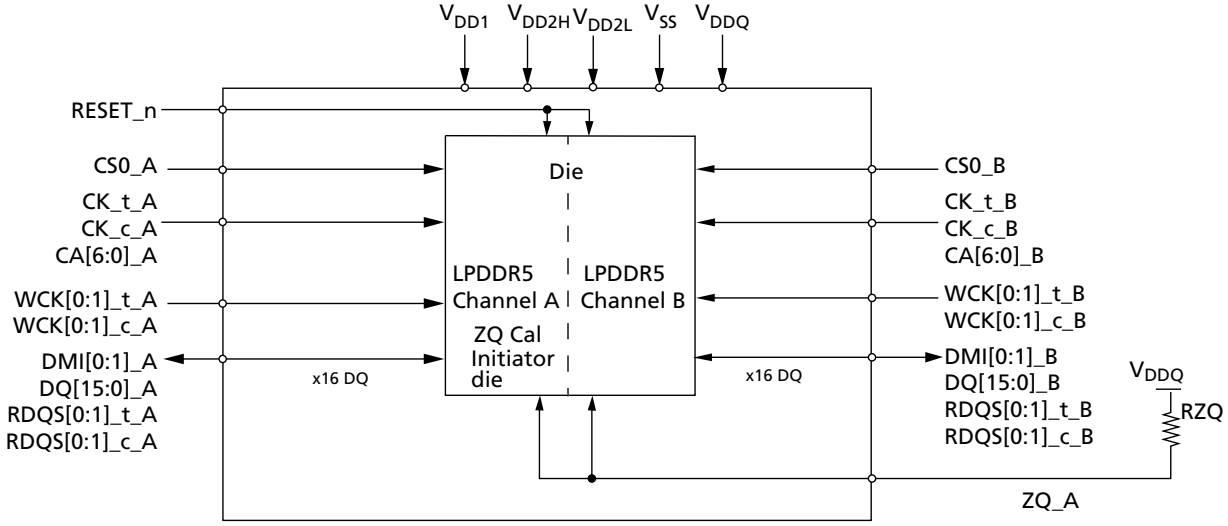
Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities



Package Block Diagrams

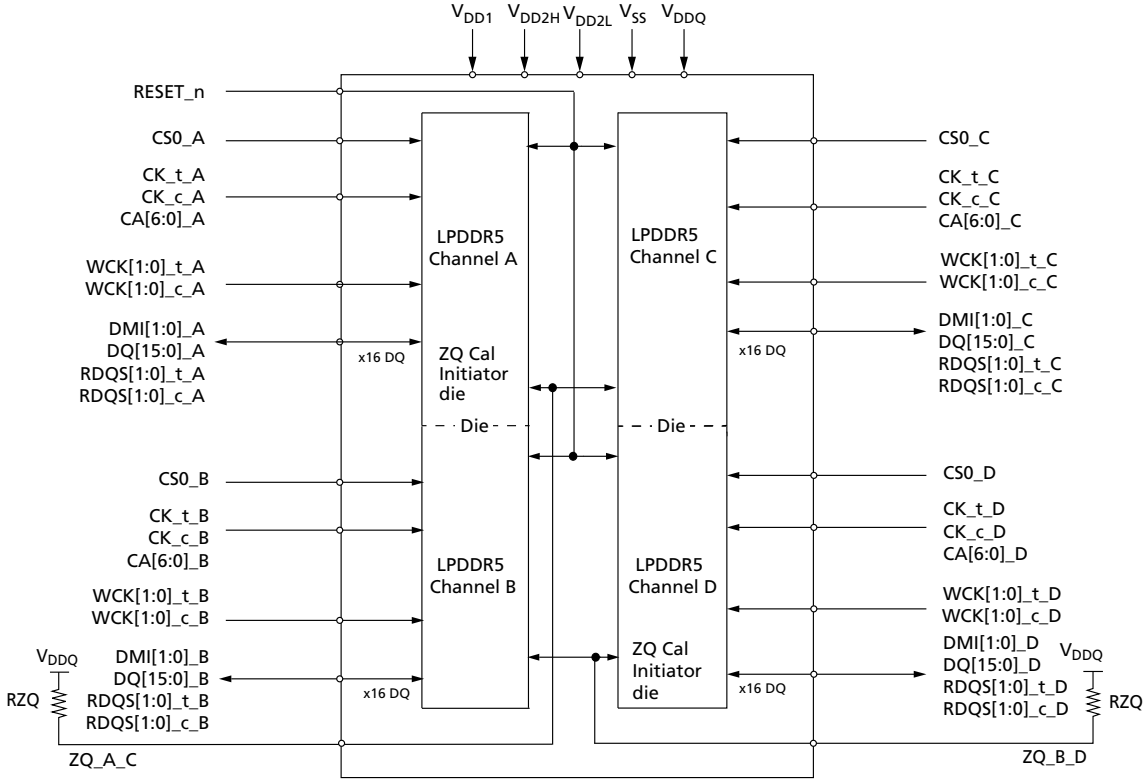
Single Die, Dual Channel, Single Rank

Figure 5: Single-Die, Dual-Channel, Single-Rank Package Block Diagram



Dual Die, Quad Channel, Single Rank

Figure 6: Dual-Die, Quad-Channel, Single-Rank Package Block Diagram



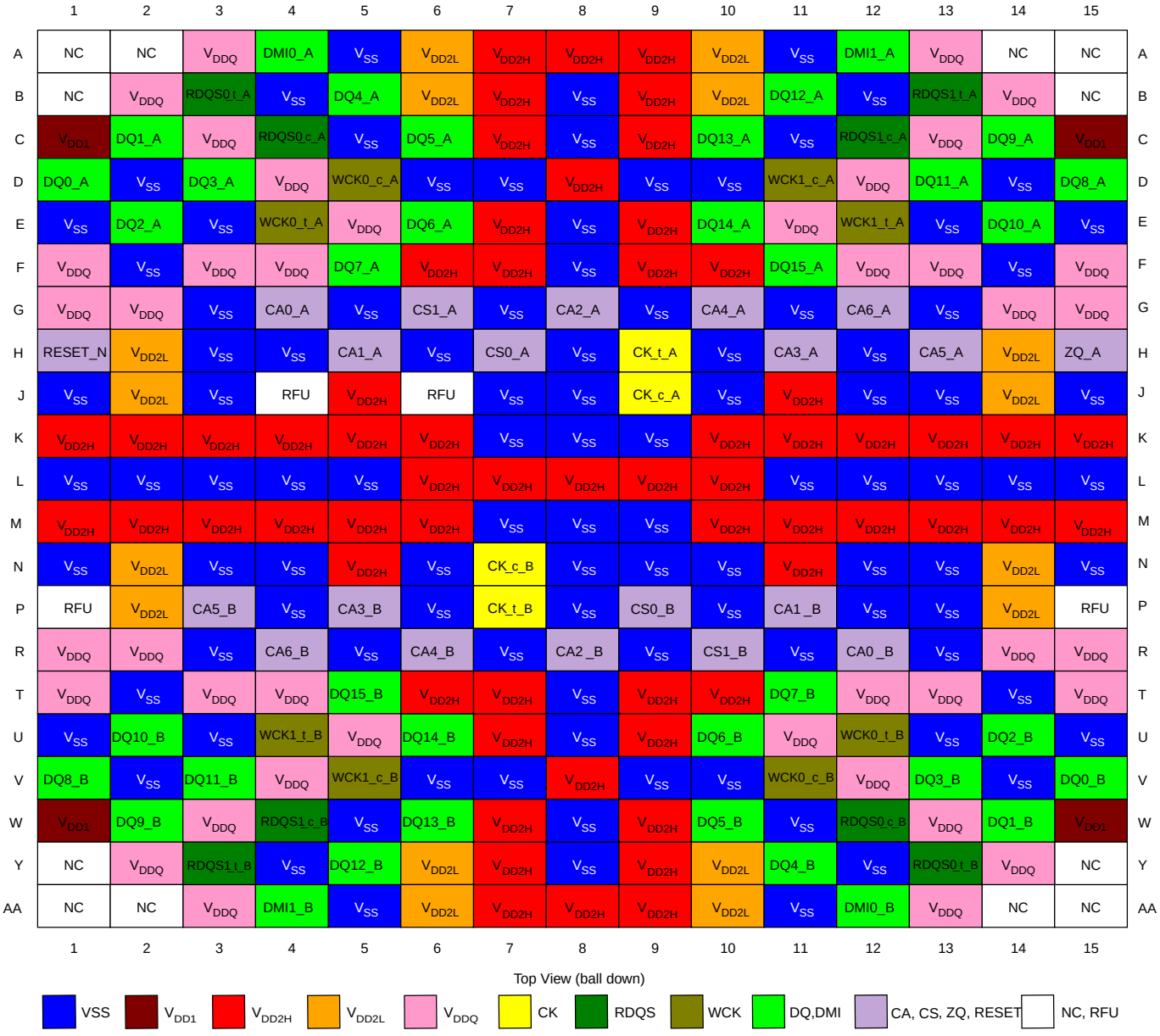
Ball Assignments and Descriptions

315b Dual Channel, 1 Rank, 2 Rank

Table 10: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected.

Figure 7: 315-Ball Dual-Channel Discrete FBGA

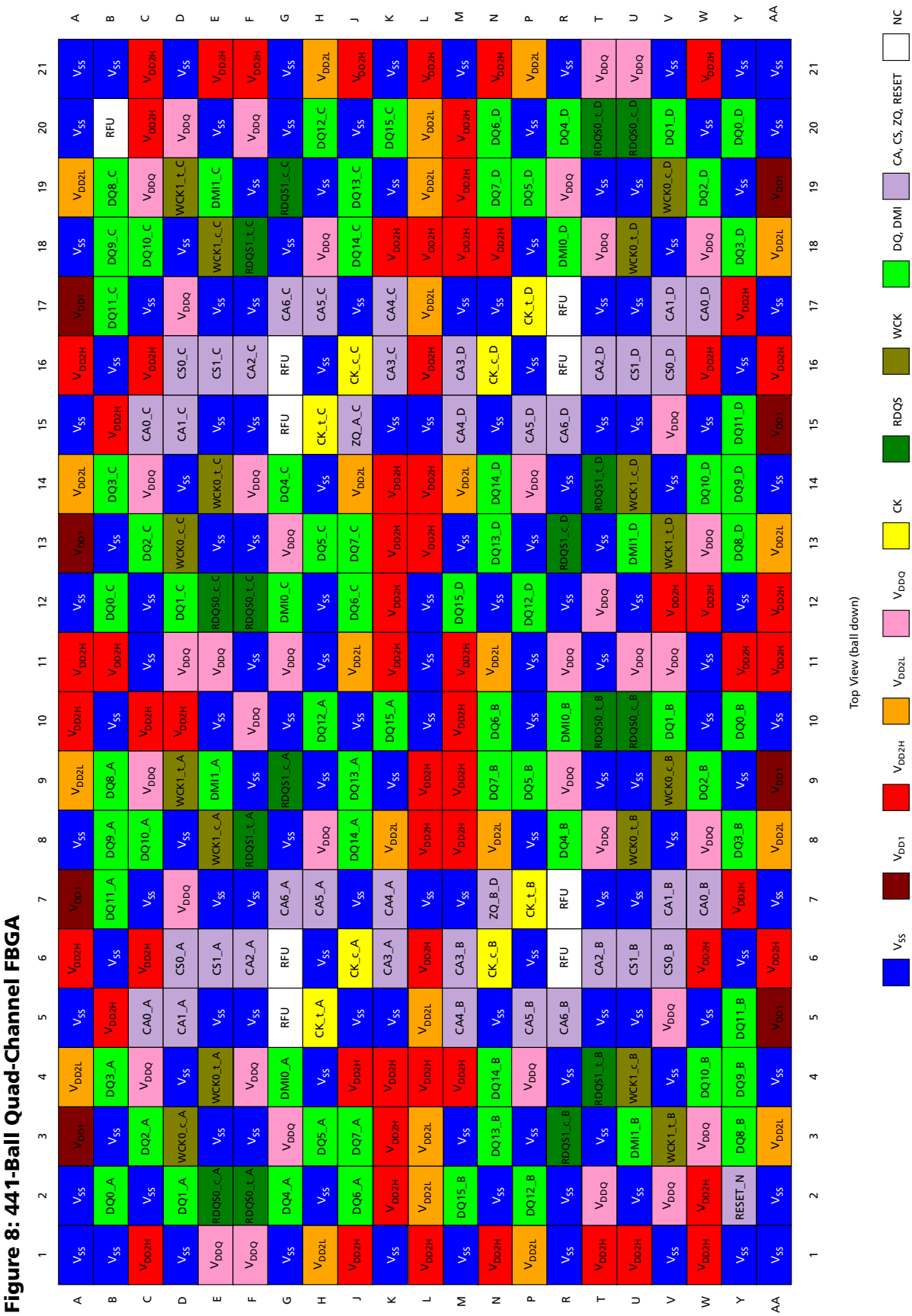


441-Ball Quad-Channel, 1-Rank, 2-Rank

Table 11: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D], CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected

Figure 8: 441-Ball Quad-Channel FBGA

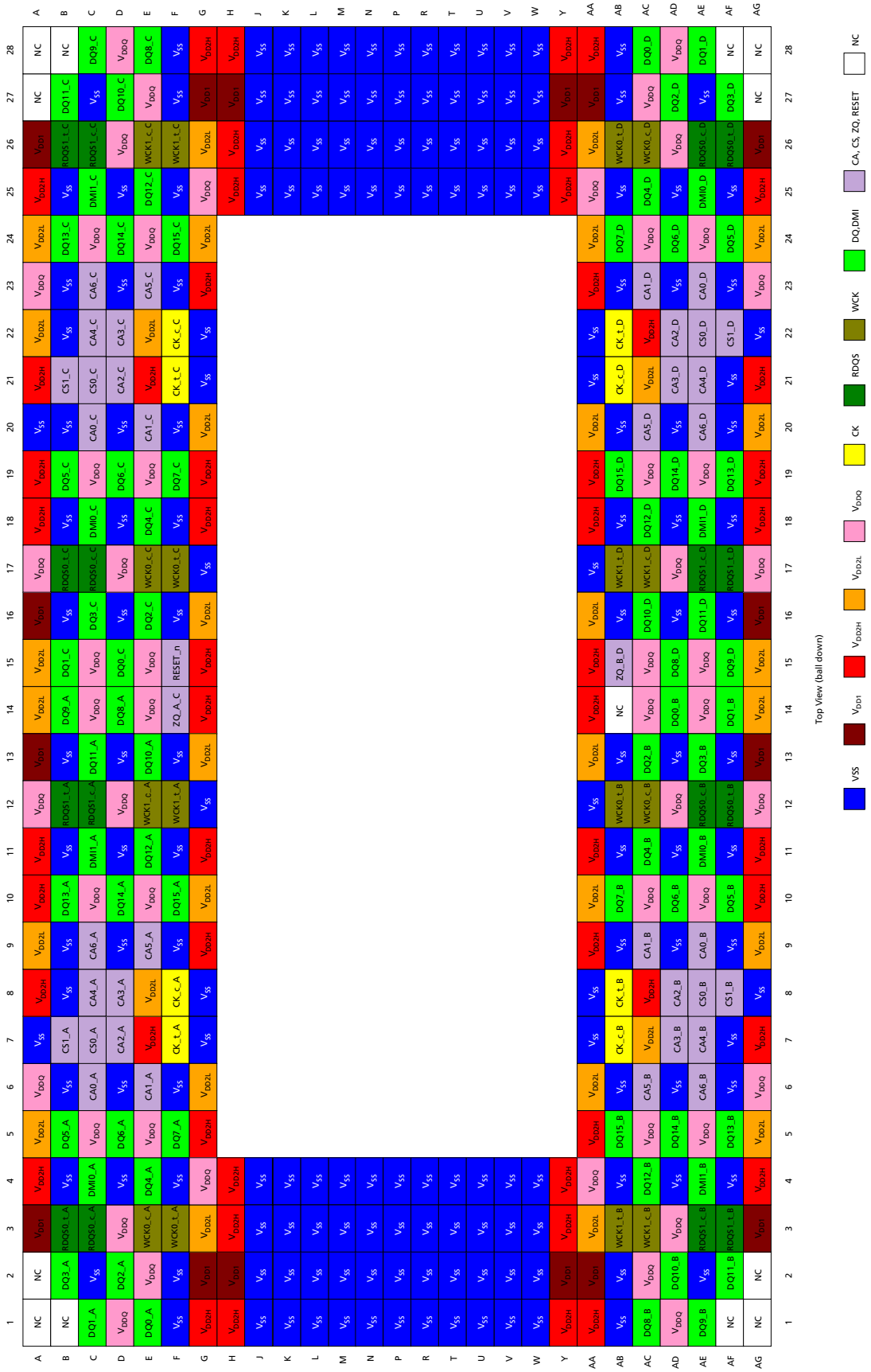


Ball Descriptions and Assignments

Table 12: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D], CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Figure 9: 496-Ball Quad-Channel POP FBGA

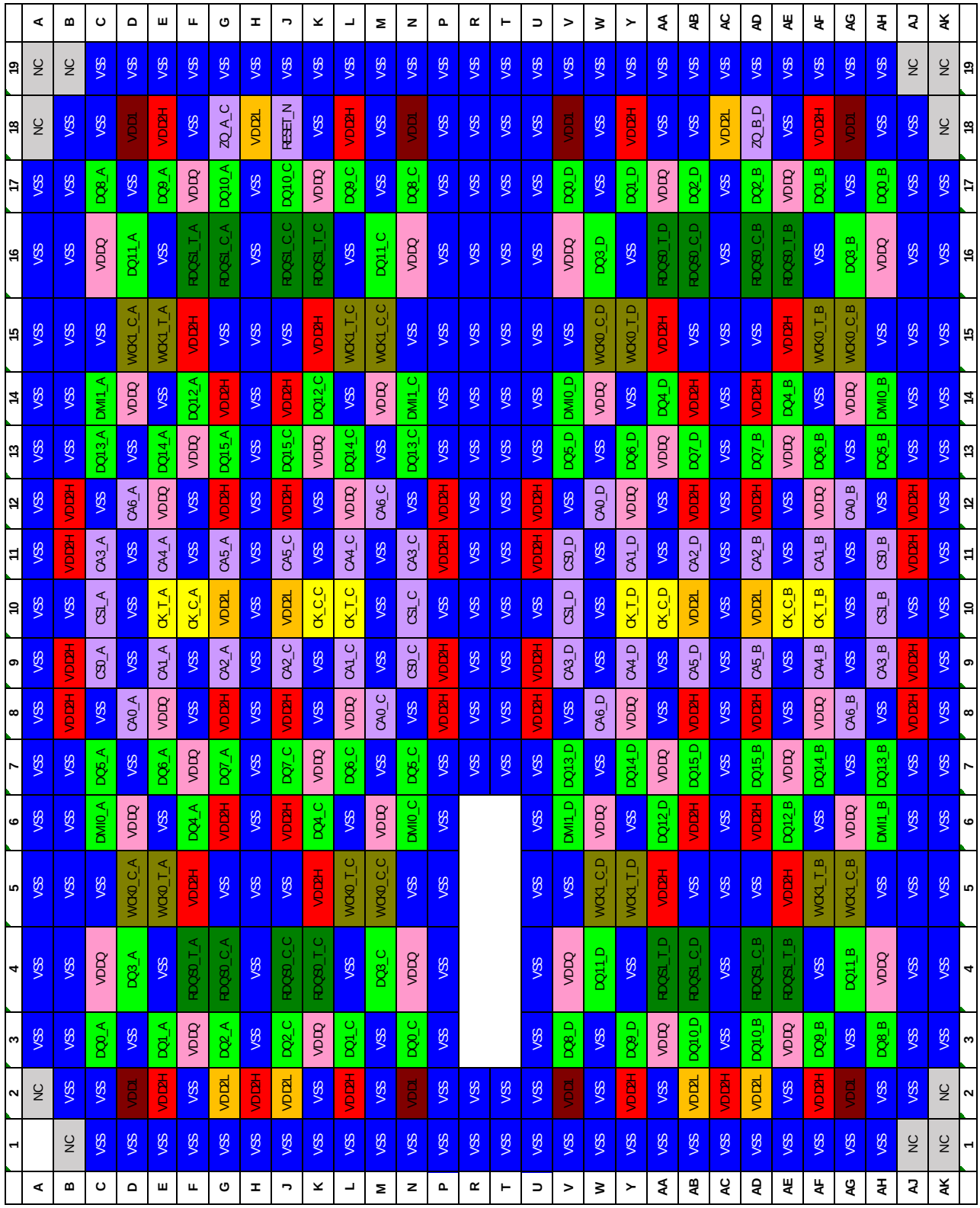


561-Ball Quad-Channel, 1-Rank, 2-Rank

Table 13: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

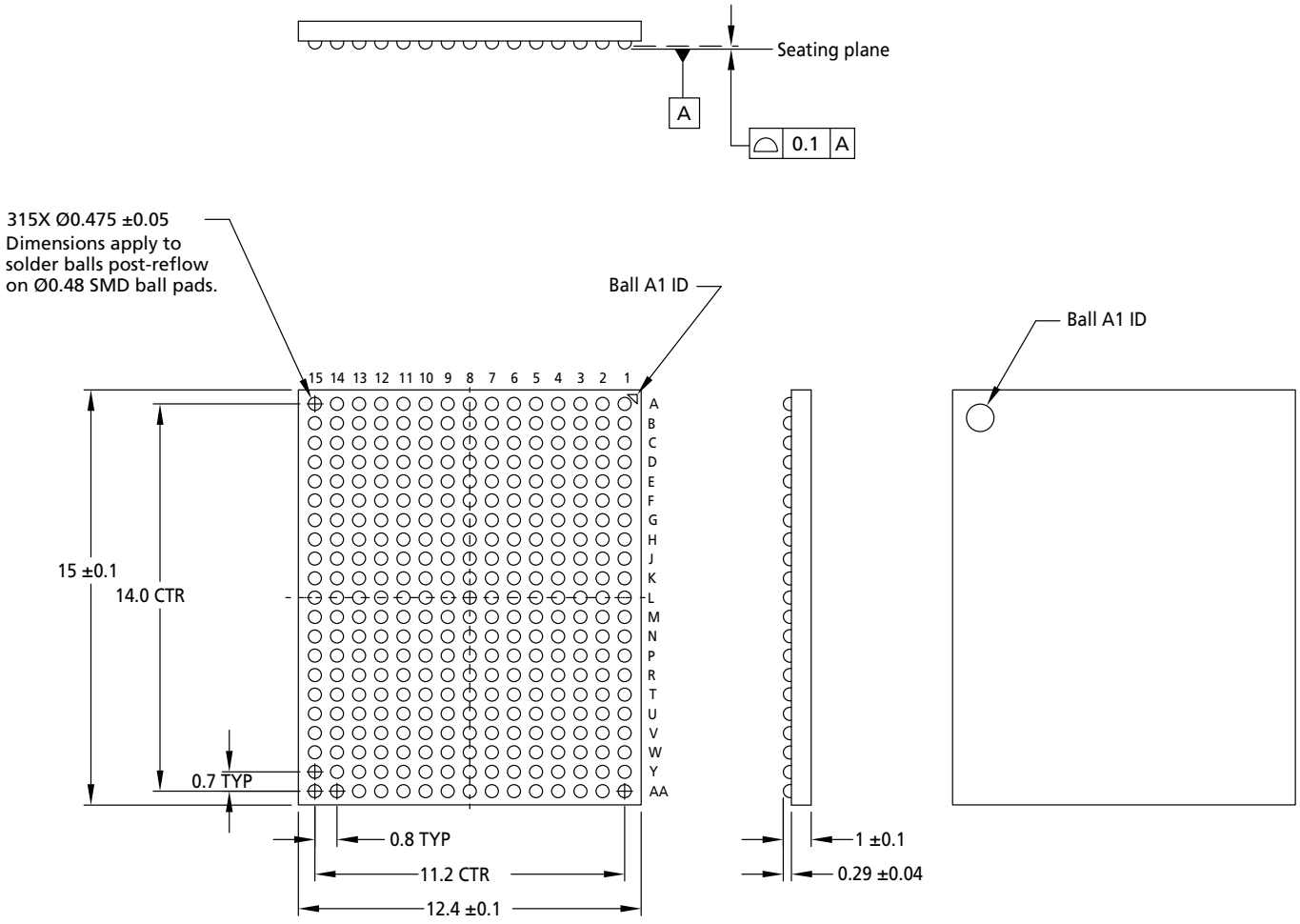
Figure 10: 561-Ball Quad-Channel FBGA



Package Dimensions

315-Ball Package (Package Code: DS)

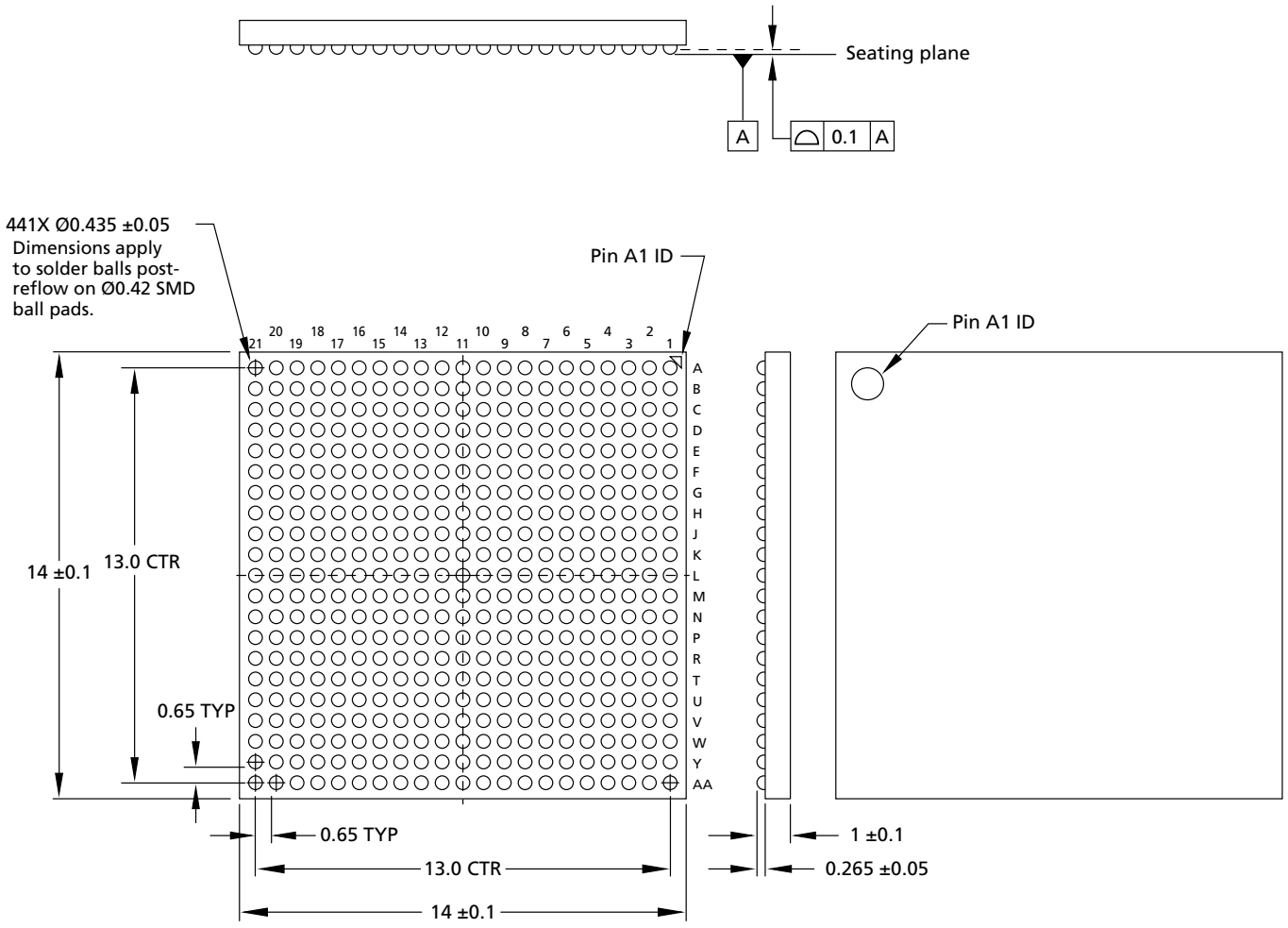
Figure 11: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

441-Ball Package (Package Code: EK)

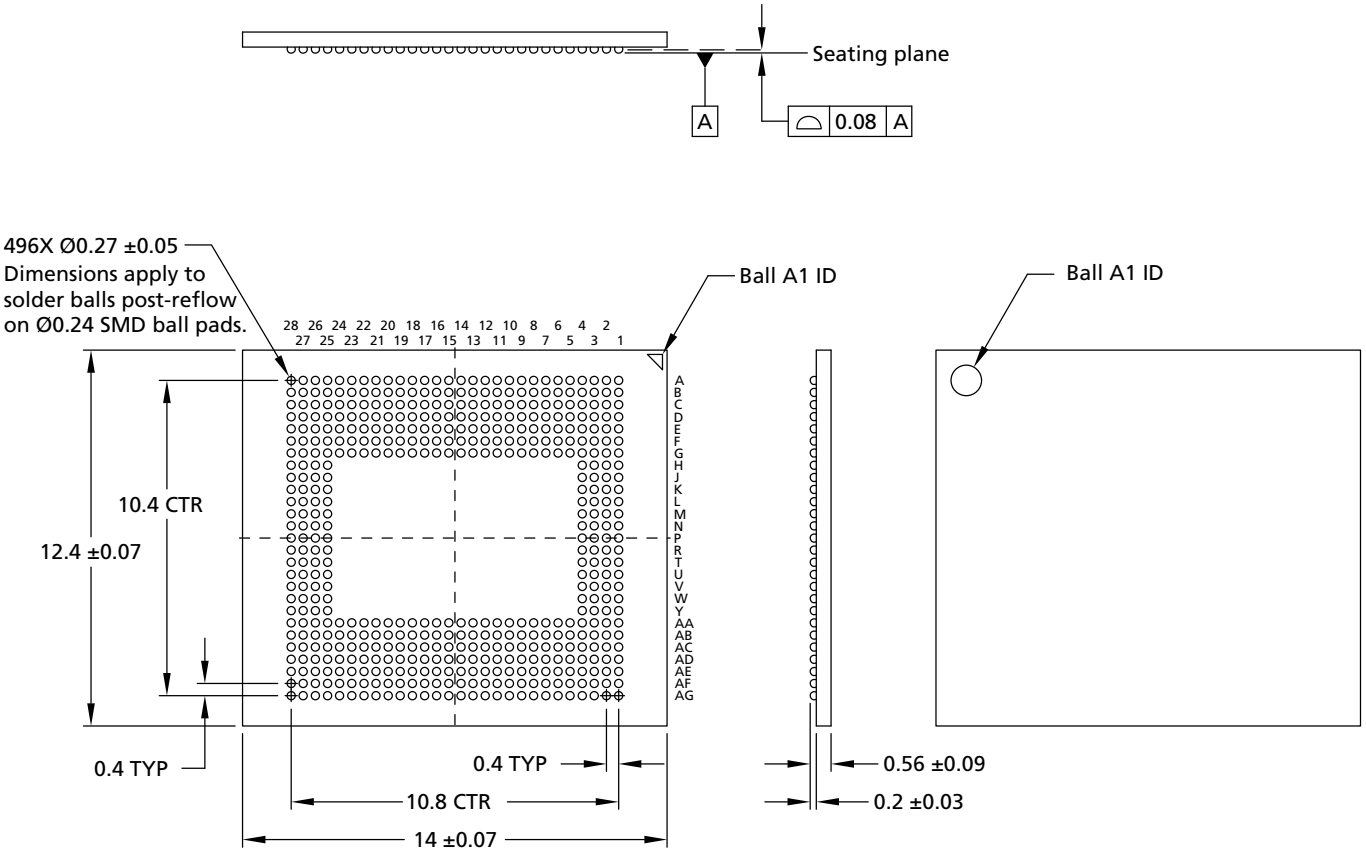
Figure 12: 441-Ball TFBGA – 14.0mm (TYP) x 14.0mm (TYP) x 1.1mm (MAX) (Package Code: EK)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

496-Ball Package (Package Code: ZX)

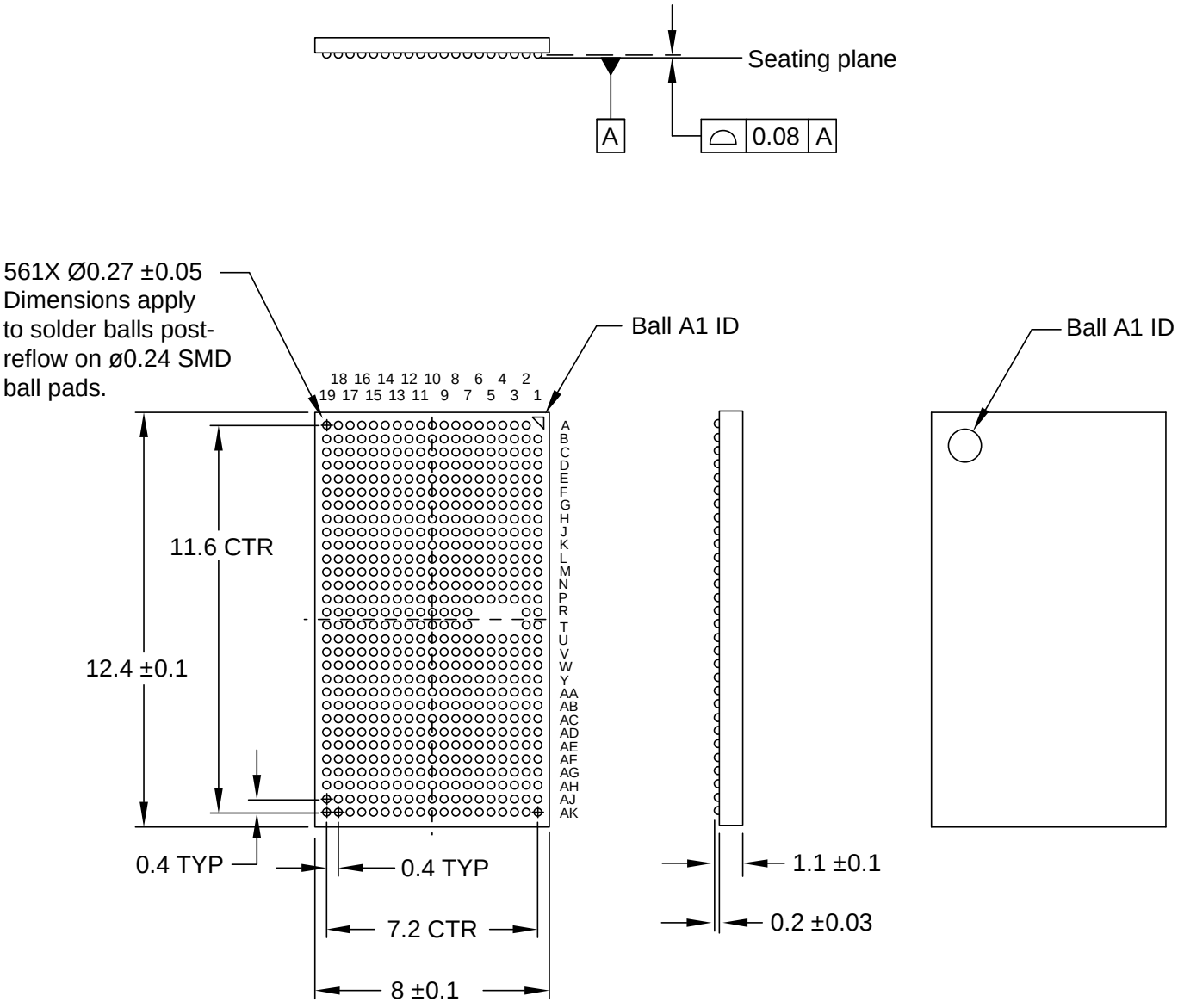
Figure 13: 496-Ball UFBGA – 14.0mm x 12.4mm



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with Ni/Au pads (Sn-3Ag-0.2Cu).

561-Ball Package (Package Code: CZ)

Figure 14: 561-Ball TFBGA – 8.0mm (TYP) × 12.4mm (TYP) × 1.2mm (MAX) (Package Code: CZ)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni)

Package Thermal Impedance

Table 14: Package Thermal Impedance Characteristics

Die Revision	Package	Parameter	Symbol	Value	Unit
Rev E	315-ball, SDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	5.2	°C/W
		Junction-to-board	Θ_{JB}	11.2	°C/W
	441-ball, DDP, package code EK	Junction-to-case (TOP)	Θ_{JC}	2.8	°C/W
		Junction-to-board	Θ_{JB}	6.3	°C/W
	496-ball, DDP, package code ZX	Junction-to-case (TOP)	Θ_{JC}	TBD	°C/W
		Junction-to-board	Θ_{JB}	TBD	°C/W
	561-ball, DDP, package code CZ	Junction-to-case (TOP)	Θ_{JC}	4.9	°C/W
		Junction-to-board	Θ_{JB}	14.3	°C/W

Note: 1. Thermal impedance values provided are for reference only. These values are based on a model and represent a maximum characteristic.

Product-Specific Mode Register Definition

Table 15: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per-pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 512M32, 512M64							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 1b: Device supports Per Pin DFE							
MR1						**DRFM support[3]**	**ARFM support[3]**	**CS ODT OP support**
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
	OP[2] = 0b: Device does not support DRFM							
MR3				**BK/BG ORG**				
	OP[4:3] = 00b: BG mode supported							
	01b: 8B mode not supported							
	10b: 16B Mode supported							
	11b: RFU							
MR4				**Refresh Multiplier** (Note 7)				
	OP[4:0]: Refer to General LPDDR5/LPDDR5X Specification 1 for mode register definitions.							
MR5	**Manufacturer ID**							
	1111 1111b: Micron							
MR6	**Revision ID1**							
	0001 1000b							
MR8	**I/O width**		**Density**				**Device Type[6]**	
	OP[7:6] = 00b: x16 for 512M32, 512M64		OP[5:2] = 0100b: 8Gb				OP[1:0] = 01b: LPDDR5X SDRAM (up to 8533 Mb/s) OP[1:0] = 10b: LPDDR5X SDRAM (up to 9600 Mb/s)	
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							

Table 15: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	WXS				ODTD-CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	DFES				Read DCA			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 5)							
MR26		RDQSTFS						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	RAAMULT		RAAIMT					RFM
	OP[0] = 1b: RFM is required							
	OP[5:1] = 00110b: 48							
	OP[7:6] = 01b: 4X							
MR41					E-DVFSC ODT	DVFSC/E-DVFSC Support		
	OP[2:1] = 10b: Both DVFSC and Enhanced DVFSC mode supported							
	OP[3] = 1b: Enhanced DVFSC ODT option is supported							
MR43		SBEC rule						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	ARFM[3]		RFMSBC		RFMSB		RAADEC	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: Single Bank Mode not supported							
	OP[5:4] = 00b: One RAA counter per two banks (1 of 8)							
	OP[7:6] = 00b: default (00110b: 48), 01b: Level A, 10b: Level B, 11b: Level C							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.
5. Device supports 7-step DFE.
6. Device type only supports Bank Group and 16B modes.

7. MR4:OP[4:0] output from each die in a defined package shall be used to determine the required package level refresh rate. Any other method used to determine a valid refresh rate, places ownership and responsibility of the correct refresh rate on the system developer or end user. TOPER (case surface temperature) shall be used to determine whether operating temperature requirements are being met. Any other method used to determine operating temperature, places ownership and responsibility of the correct operating temperature on the system developer or end user.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions. Data rate in IDD tables is defined as per-pin.

Table 16: WT I_{DD} Parameters – Single Channel of 2 Ch Die

Symbol	Supply	Speed per-pin x16 Mode			Unit	Note
		7500 Mb/s	8533 Mb/s	9600 Mb/s		
I_{DD01}	V_{DD1}	3.5	3.5	3.5	mA	
I_{DD02H}	V_{DD2H}	40	40	40		
I_{DD02L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD0Q}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2P1}	V_{DD1}	1.4	1.4	1.4	mA	
I_{DD2P2H}	V_{DD2H}	2.3	2.3	2.3		
I_{DD2P2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD2PQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2PS1}	V_{DD1}	1.4	1.4	1.4	mA	
$I_{DD2PS2H}$	V_{DD2H}	2.3	2.3	2.3		
$I_{DD2PS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD2PSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2N1}	V_{DD1}	1.3	1.3	1.3	mA	
I_{DD2N2H}	V_{DD2H}	28	28	28		
I_{DD2N2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD2NQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2NS1}	V_{DD1}	1.3	1.3	1.3	mA	
$I_{DD2NS2H}$	V_{DD2H}	28	28	28		
$I_{DD2NS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD2NSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3P1}	V_{DD1}	2.5	2.5	2.5	mA	
I_{DD3P2H}	V_{DD2H}	12	12	12		
I_{DD3P2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD3PQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3PS1}	V_{DD1}	2.5	2.5	2.5	mA	
$I_{DD3PS2H}$	V_{DD2H}	12	12	12		
$I_{DD3PS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD3PSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3N1}	V_{DD1}	2.7	2.7	2.7	mA	
I_{DD3N2H}	V_{DD2H}	35	35	35		
I_{DD3N2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD3NQ}	V_{DDQ}	0.6	0.6	0.6		

Table 16: WT I_{DD} Parameters – Single Channel of 2 Ch Die (Continued)

Symbol	Supply	Speed per-pin			Unit	Note
		x16 Mode				
		7500 Mb/s	8533 Mb/s	9600 Mb/s		
I_{DD4R1}	V_{DD1}	14	16	17	mA	3, 4, 6
I_{DD4R2H}	V_{DD2H}	349	382	416		
I_{DD4R2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD4RQ}	V_{DDQ}	111	121	121.5		
I_{DD4W1}	V_{DD1}	12	14	15.3	mA	3, 6
I_{DD4W2H}	V_{DD2H}	254	280	306		
I_{DD4W2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD4WQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD51}	V_{DD1}	14	14	14	mA	
I_{DD52H}	V_{DD2H}	124	124	124		
I_{DD52L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD5Q}	V_{DDQ}	0.6	0.6	0.6		
I_{DD5AB1}	V_{DD1}	3.5	3.5	3.5	mA	
$I_{DD5AB2H}$	V_{DD2H}	35	35	35		
$I_{DD5AB2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD5ABQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD5PB1}	V_{DD1}	3.5	3.5	3.5	mA	
$I_{DD5PB2H}$	V_{DD2H}	35	35	35		
$I_{DD5PB2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD5PBQ}	V_{DDQ}	0.6	0.6	0.6		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 17: WT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Channel of 2 Ch Die

Symbol	Supply	Speed per-pin	Unit	Note
		x16 Mode		
		3200 Mb/s		
$I_{DD4R-DVFSC1}$	V_{DD1}	8	mA	3, 4, 6
$I_{DD4R-DVFSC2H}$	V_{DD2H}	32		
$I_{DD4R-DVFSC2L}$	V_{DD2L}	100		
$I_{DD4R-DVFSCQ}$	V_{DDQ}	76		

Table 17: WT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Channel of 2 Ch Die (Continued)

Symbol	Supply	Speed per-pin x16 Mode 3200 Mb/s	Unit	Note
$I_{DD4W-DVFSC1}$	V_{DD1}	8	mA	3, 6
$I_{DD4W-DVFSC2H}$	V_{DD2H}	29		
$I_{DD4W-DVFSC2L}$	V_{DD2L}	75		
$I_{DD4W-DVFSCQ}$	V_{DDQ}	0.6		
I_{DD5ED1}	V_{DD1}	13	mA	
$I_{DD5ED2H}$	V_{DD2H}	110		
$I_{DD5ED2L}$	V_{DD2L}	18		
I_{DD5EDQ}	V_{DDQ}	0.6		
$I_{DD5ABED1}$	V_{DD1}	3.3	mA	
$I_{DD5ABED2H}$	V_{DD2H}	18		
$I_{DD5ABED2L}$	V_{DD2L}	14		
$I_{DD5ABEDQ}$	V_{DDQ}	0.6		
$I_{DD5PBED1}$	V_{DD1}	3.3	mA	
$I_{DD5PBED2H}$	V_{DD2H}	18		
$I_{DD5PBED2L}$	V_{DD2L}	14		
$I_{DD5PBEDQ}$	V_{DDQ}	0.6		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFSC enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 18: WT Full-Array Power-Down Self Refresh Current – Single Channel of 2Ch Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I_{DD61}	V_{DD1}	0.17	mA	
	I_{DD62H}	V_{DD2H}	0.42		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.17	mA	
	$I_{DD6DS2H}$	V_{DD2H}	0.42		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		

Table 18: WT Full-Array Power-Down Self Refresh Current – Single Channel of 2Ch Die (Continued)

Temperature	Symbol	Supply	Value	Unit	Notes
45°C	I_{DD61}	V_{DD1}	0.23	mA	
	I_{DD62H}	V_{DD2H}	0.75		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.23	mA	
	$I_{DD6DS2H}$	V_{DD2H}	0.75		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		
65°C	I_{DD61}	V_{DD1}	0.4	mA	
	I_{DD62H}	V_{DD2H}	2.0		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.4	mA	
	$I_{DD6DS2H}$	V_{DD2H}	2.0		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		
85°C	I_{DD61}	V_{DD1}	1.2	mA	
	I_{DD62H}	V_{DD2H}	7.0		
	I_{DD62L}	V_{DD2L}	0.2	mA	4
	I_{DD6Q}	V_{DDQ}	0.6		
	I_{DD6DS1}	V_{DD1}	1.2	mA	
	$I_{DD6DS2H}$	V_{DD2H}	7.0		
	$I_{DD6DS2L}$	V_{DD2L}	0.2	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.6		

Notes: 1. I_{DD6}25/45/65°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. While entering and exiting self-refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and ^{t}ESPD timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Table 19: IT I_{DD} Parameters – Single Channel of 2Ch Die

Symbol	Supply	Speed Grade			Unit	Note
		x16 Mode				
		7500 Mb/s	8533 Mb/s	9600 Mb/s		
I_{DD01}	V_{DD1}	3.8	3.8	3.8	mA	
I_{DD02H}	V_{DD2H}	57	57	57		
I_{DD02L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD0Q}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2P1}	V_{DD1}	1.7	1.7	1.7	mA	
I_{DD2P2H}	V_{DD2H}	4.2	4.2	4.2		
I_{DD2P2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD2PQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2PS1}	V_{DD1}	1.7	1.7	1.7	mA	
$I_{DD2PS2H}$	V_{DD2H}	4.2	4.2	4.2		
$I_{DD2PS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD2PSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2N1}	V_{DD1}	1.5	1.5	1.5	mA	
I_{DD2N2H}	V_{DD2H}	39	39	39		
I_{DD2N2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD2NQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD2NS1}	V_{DD1}	1.5	1.5	1.5	mA	
$I_{DD2NS2H}$	V_{DD2H}	39	39	39		
$I_{DD2NS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD2NSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3P1}	V_{DD1}	2.9	2.9	2.9	mA	
I_{DD3P2H}	V_{DD2H}	16	16	16		
I_{DD3P2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD3PQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3PS1}	V_{DD1}	2.9	2.9	2.9	mA	
$I_{DD3PS2H}$	V_{DD2H}	16	16	16		
$I_{DD3PS2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD3PSQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD3N1}	V_{DD1}	3	3	3	mA	
I_{DD3N2H}	V_{DD2H}	48	48	48		
I_{DD3N2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD3NQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD4R1}	V_{DD1}	14	16	17.5	mA	3, 4, 6
I_{DD4R2H}	V_{DD2H}	387	421	455		
I_{DD4R2L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD4RQ}	V_{DDQ}	111	121	121.5		

Table 19: IT I_{DD} Parameters – Single Channel of 2Ch Die (Continued)

Symbol	Supply	Speed Grade			Unit	Note
		x16 Mode				
		7500 Mb/s	8533 Mb/s	9600 Mb/s		
I_{DD4W1}	V_{DD1}	13	15	16	mA	3, 6
I_{DD4W2H}	V_{DD2H}	287	313	340		
I_{DD4W2L}	V_{DD2L}	0	0	0		
I_{DD4WQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD51}	V_{DD1}	15	15	15	mA	
I_{DD52H}	V_{DD2H}	149	149	149		
I_{DD52L}	V_{DD2L}	0.2	0.2	0.2		
I_{DD5Q}	V_{DDQ}	0.6	0.6	0.6		
I_{DD5AB1}	V_{DD1}	3.5	3.5	3.5	mA	
$I_{DD5AB2H}$	V_{DD2H}	48	48	48		
$I_{DD5AB2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD5ABQ}	V_{DDQ}	0.6	0.6	0.6		
I_{DD5PB1}	V_{DD1}	3.5	3.5	3.5	mA	
$I_{DD5PB2H}$	V_{DD2H}	48	48	48		
$I_{DD5PB2L}$	V_{DD2L}	0.2	0.2	0.2		
I_{DD5PBQ}	V_{DDQ}	0.6	0.6	0.6		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC, Enhanced DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); T_C = –40°C to +95°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 20: IT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Channel of 2 Ch Die

Symbol	Supply	Speed per-pin	Unit	Note
		x16 Mode		
		3200 Mb/s		
$I_{DD4R-DVFSC1}$	V_{DD1}	8	mA	3, 4, 6
$I_{DD4R-DVFSC2H}$	V_{DD2H}	32		
$I_{DD4R-DVFSC2L}$	V_{DD2L}	105		
$I_{DD4R-DVFSCQ}$	V_{DDQ}	76		
$I_{DD4W-DVFSC1}$	V_{DD1}	8	mA	3, 6
$I_{DD4W-DVFSC2H}$	V_{DD2H}	29		
$I_{DD4W-DVFSC2L}$	V_{DD2L}	87		
$I_{DD4W-DVFSCQ}$	V_{DDQ}	0.6		

Table 20: IT I_{DD} Parameters – With Enhanced DVFSC Enabled - Single Channel of 2 Ch Die (Continued)

Symbol	Supply	Speed per-pin x16 Mode 3200 Mb/s	Unit	Note
I_{DD5ED1}	V_{DD1}	14	mA	
$I_{DD5ED2H}$	V_{DD2H}	110		
$I_{DD5ED2L}$	V_{DD2L}	23		
I_{DD5EDQ}	V_{DDQ}	0.6		
$I_{DD5ABED1}$	V_{DD1}	3.3	mA	
$I_{DD5ABED2H}$	V_{DD2H}	22		
$I_{DD5ABED2L}$	V_{DD2L}	22		
$I_{DD5ABEDQ}$	V_{DDQ}	0.6		
$I_{DD5PBED1}$	V_{DD1}	3.3	mA	
$I_{DD5PBED2H}$	V_{DD2H}	22		
$I_{DD5PBED2L}$	V_{DD2L}	22		
$I_{DD5PBEDQ}$	V_{DDQ}	0.6		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFSC enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
6. IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 21: IT Full-Array Power-Down Self Refresh Current – Single Channel of 2 Ch Die

Temperature	Symbol	Supply	Value	Unit	Note
25°C	I_{DD61}	V_{DD1}	0.17	mA	
	I_{DD62H}	V_{DD2H}	0.42		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.17	mA	
	$I_{DD6DS2H}$	V_{DD2H}	0.42		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		
45°C	I_{DD61}	V_{DD1}	0.23	mA	
	I_{DD62H}	V_{DD2H}	0.75		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.23	mA	
	$I_{DD6DS2H}$	V_{DD2H}	0.75		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		
65°C	I_{DD61}	V_{DD1}	0.4	mA	
	I_{DD62H}	V_{DD2H}	2.0		
	I_{DD62L}	V_{DD2L}	0.01	mA	4
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.4	mA	
	$I_{DD6DS2H}$	V_{DD2H}	2.0		
	$I_{DD6DS2L}$	V_{DD2L}	0.01	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.03		
85°C	I_{DD61}	V_{DD1}	1.2	mA	
	I_{DD62H}	V_{DD2H}	7.0		
	I_{DD62L}	V_{DD2L}	0.2	mA	4
	I_{DD6Q}	V_{DDQ}	0.6		
	I_{DD6DS1}	V_{DD1}	1.2	mA	
	$I_{DD6DS2H}$	V_{DD2H}	7.0		
	$I_{DD6DS2L}$	V_{DD2L}	0.2	mA	4
	I_{DD6DSQ}	V_{DDQ}	0.6		

Notes: 1. I_{DD6}25/45/65°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –40°C to +95°C
4. While entering and exiting Self-Refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the Self-Refresh with Power down mode entrance commands are completed and ^{t}ESPD timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Revision History

Rev. G – 05/2025

- Added 496-Ball ZX package

Rev. F – 03/2025

- Updated Mode Register Settings to clarify MR3 settings
- Updated thermal impedance note
- Production data sheet release

Rev. E – 02/2025

- Updated all IDD tables

Rev. D – 01/2025

- Updated the 9600Mbps IDD current values.
- Added thermal impedance values for the CZ package.

Rev. C – 09/2024

- Added RxMask adjusted spec for 9600Mbps data rate.
- Added all 7500Mbps and 8533Mbps IDD values with associated notes to the datasheet
- Disabled DRFM support

Rev. B – 05/2024

- Preliminary data sheet release

Rev. A – 01/2024

- Initial advanced data sheet release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.