

swissbit®

Product Data Sheet

Industrial USB Flash Drive Module

U-500 Series

USB3.1 SuperSpeed, SLC

Commercial and Industrial
Temperature Grade

Date: May 22, 2025
Revision: 1.04



Contents

1. PRODUCT SUMMARY	3
2. GENERAL DESCRIPTION	4
3. ORDERING INFORMATION U-500	5
4. PRODUCT DESCRIPTION	7
4.1 PERFORMANCE SPECIFICATIONS	7
4.2 ENVIRONMENTAL SPECIFICATIONS	7
4.3 DRIVE GEOMETRY SPECIFICATION	9
4.4 REGULATORY COMPLIANCE	9
4.5 NAND FLASH TECHNOLOGIES	10
5. ELECTRICAL INTERFACE.....	11
6. ELECTRICAL SPECIFICATION	12
7. PACKAGE MECHANICAL	14
8. ATA PASS-THROUGH COMMANDS (IDENTIFY DEVICE AND S.M.A.R.T.)	15
8.1 ATA PASS-THROUGH COMMANDS	15
8.2 IDENTIFY DEVICE	15
8.3 S.M.A.R.T. COMMANDS	16
9. MARKING SPECIFICATION.....	18
9.1 TOP VIEW	18
10. PART NUMBER DECODER	19
10.1 MANUFACTURER	19
10.2 MEMORY TYPE	19
10.3 PRODUCT TYPE	19
10.4 DENSITY	19
10.5 PLATFORM	19
10.6 PRODUCT GENERATION	19
10.7 MEMORY ORGANIZATION	19
10.8 TECHNOLOGY	19
10.9 NUMBER OF FLASH CHIPS	19
10.10 FLASH CODE	20
10.11 TEMP. OPTION	20
10.12 DIE CLASSIFICATION	20
10.13 PIN MODE	20
10.14 CONFIGURATION XYZ	20
10.15 OPTION	20
11. REVISION HISTORY	21

U-500 Series – Industrial USB Flash Drive Module (eUSB)

1GB up to 32GByte (SLC)

1. Product Summary

- USB3.1 solid state flash drive for internal 9(10)-pin USB connector terminal
 - Fully compliant with USB specification 3.1 Gen 1 (SuperSpeed, 5Gb/s burst)
 - Fully backward compliant with USB 2.0/1.1 systems (High/Full Speed, 480/12Mb/s burst)
 - Dimension of 26.65 x 36.8mm
 - 2.54mm or 2.00mm connector with keyed pin
 - Mounting hole electrically not connected (optional grounded)
 - Fixed drive (USB hard drive, optional removable)
 - LED for operation indication
 - Write protect switch (optional)
 - Diagnostic features with Life Time Monitoring tool support
 - Firmware update in field possible
- High performance USB3.1 specification
 - Up to 1100 IOPS write and 3000 IOPS read (4KByte transfers)
 - Up to 90 MBytes/s sequential write and 175 MBytes/s read speed
- Power Supply: (Low-power CMOS technology)
 - 3.1 to 5.5V operating voltage
- Optimized FW algorithms especially for high read access and long data retention applications
 - Patented power-off reliability technology
 - Near Miss ECC technology
Minimizes the risk of uncorrectable bit failure over the product life time. Each read command analyzes the ECC margin level and refreshes data if necessary.
 - Read Disturb Management
The read commands per block are monitored and the content is refreshed when critical levels are reached.
 - Wear Leveling technology
Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. As a result the maximum write endurance of the device is guaranteed.
 - Data Care Management
The interruptible background process maintains the user data integrity by compensating Read Disturb effects or Retention degradation due to high temperature effects.
 - UBER <10⁻¹⁷
- High reliability
 - SLC NAND Flash with highest program erase cycles per block
 - Designed with sophisticated firmware architecture for industrial and NetCom market especially 24/7 application like networking, base stations, infrastructure systems, POS/POI, medical and general boot medium use case.
 - The product is optimized for highest reliability and power fail safety.
 - Commercial and industrial temperature range, 0° up to 70°C and -40° up to 85°C
- Controlled BOM & PCN process
- RoHS, REACH compatible, WEEE, CE, FCC compliant
- Customized options like registers, removable device, connector options, write protect switch, grounded mounting hole, conformal coating, densities, uploads, label, security controller etc.



2. General Description

The Swissbit U-500 USB 3.1 embedded USB module provides a robust, high performance, and reliable storage product with industry compatible interface and small form factor. The U-500 SLC technology both enables high NAND flash operation and excellent endurance. The use of page based Flash management and a global wear leveling extends the endurance to unprecedented values for USB products.

The 10-pin connector makes easy integration into existing or newly designed system boards possible. The U-500 is compatible with standard on-board USB connectors that use a single USB 2.0 or USB 3.1 channel. It may not be used in mainboard USB2.0 connectors that support two USB channels per socket. The embedded USB module serves applications which utilize USB products as acceleration cache for HDDs or as a boot media, for example networking and telecommunication systems.

For outdoor use or in poorly ventilated systems the U-500 is available in industrial temperature grade from -40°C to +85°C. Each individual industrial temperature grade module is tested at these corners to verify the temperature resistance.

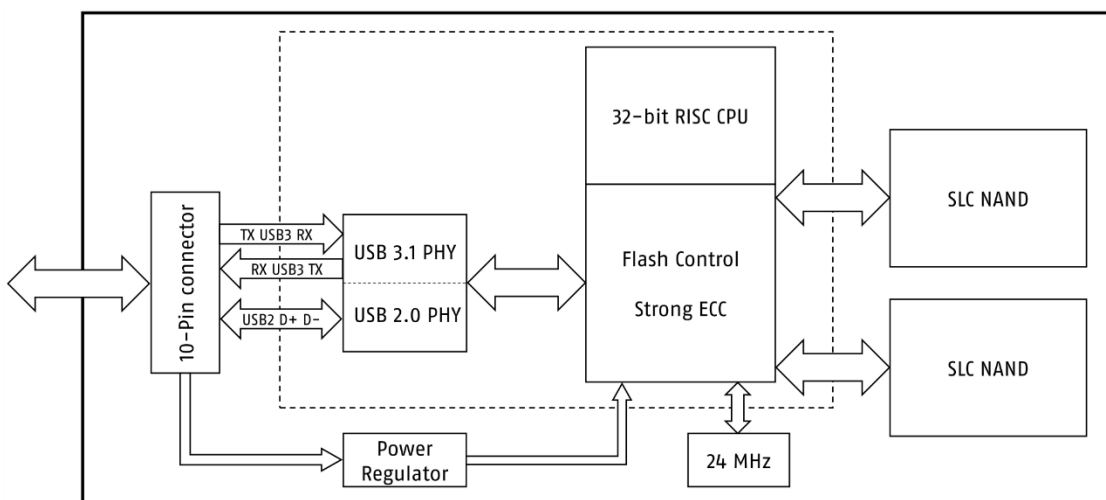
The U-500 firmware includes data care management features which refresh storage areas that are not or only infrequently read. At high temperature storage these areas are prone to retention loss. The firmware monitors the state of the NAND blocks and refreshes those that show a high level of degradation, thus preventing uncorrectable errors. This is an important feature for USB modules that are used as read only boot media.

The U-500 consists of the USB controller, the 10pin connector, power circuitry and different numbers of NAND dies. The 1 to 4GB module uses two TSOP packages, the 8 to 32 GB modules use a single BGA package with two flash channels. All U-500 modules use two flash channels for best performance.

The U-500 can flexibly operate at 3.3V or 5V nominal with $\pm 5\%$ tolerance.

It supports USB 3.1 Gen 1 SuperSpeed and is fully backwards compatible to USB 2.0/1.1 High/Full Speed.

Figure 1: Functional Block Diagram



3. Ordering Information U-500

Please note the three series U-500 (SLC), U-56 (pSLC), U-50 (MLC)

Table 1: Standard Product List

Commercial Temperature	
Capacity	Part Number
1 GBytes	SFUI1024cgAE1T0-C-MS-2y1-STD
2 GBytes	SFUI2048cgAE2T0-C-MS-2y1-STD
4 GBytes	SFUI4096cgAE2T0-C-QT-2y1-STD
8 GBytes	SFUI008GcgAE1T0-C-DB-2y1-STD
16 GBytes	SFUI016GcgAE1T0-C-QC-2y1-STD
32 GBytes	SFUI032GcgAE1T0-C-NC-2y1-STD
Industrial Temperature	
Capacity	Part Number
1 GBytes	SFUI1024cgAE1T0-I-MS-2y1-STD
2 GBytes	SFUI2048cgAE2T0-I-MS-2y1-STD
4 GBytes	SFUI4096cgAE2T0-I-QT-2y1-STD
8 GBytes	SFUI008GcgAE1T0-I-DB-2y1-STD
16 GBytes	SFUI016GcgAE1T0-I-QC-2y1-STD
32 GBytes	SFUI032GcgAE1T0-I-NC-2y1-STD

c = connector, g = product generation, y = firmware revision

Table 2: Available Part Numbers

Commercial Temperature		
Capacity	Part Number	Connector
1 GBytes	SFUI1024J1AE1T0-C-MS-2B1-STD	2.54mm pitch
2 GBytes	SFUI2048J1AE2T0-C-MS-2B1-STD	
4 GBytes	SFUI4096J1AE2T0-C-QT-2A1-STD	
8 GBytes	SFUI008GJ1AE1T0-C-DB-2A1-STD	
8 GBytes	SFUI008GJ1AE1T0-C-DB-2B1-STD	
16 GBytes	SFUI016GJ1AE1T0-C-QC-2A1-STD	
32 GBytes	SFUI032GJ1AE1T0-C-NC-2A1-STD	
32 GBytes	SFUI032GJ1AE1T0-C-NC-2B1-STD	
1 GBytes	SFUI1024K1AE1T0-C-MS-2B1-STD	
2 GBytes	SFUI2048K1AE2T0-C-MS-2B1-STD	
4 GBytes	SFUI4096K1AE2T0-C-QT-2A1-STD	
8 GBytes	SFUI008GK1AE1T0-C-DB-2A1-STD	
16 GBytes	SFUI016GK1AE1T0-C-QC-2A1-STD	
32 GBytes	SFUI032GK1AE1T0-C-NC-2A1-STD	
Industrial Temperature		
Capacity	Part Number	Connector
1 GBytes	SFUI1024J1AE1T0-I-MS-2B1-STD	2.54mm pitch
2 GBytes	SFUI2048J1AE2T0-I-MS-2B1-STD	
4 GBytes	SFUI4096J1AE2T0-I-QT-2A1-STD	
	SFUI4096J1AE2T0-I-QT-2B1-STD	
8 GBytes	SFUI008GJ1AE1T0-I-DB-2A1-STD	
	SFUI008GJ1AE1T0-I-DB-2B1-STD	
16 GBytes	SFUI016GJ1AE1T0-I-QC-2A1-STD	
	SFUI016GJ1AE1T0-I-QC-2B1-STD	
32 GBytes	SFUI032GJ1AE1T0-I-NC-2A1-STD	
	SFUI032GJ1AE1T0-I-NC-2B1-STD	
1 GBytes	SFUI1024K1AE1T0-I-MS-2B1-STD	2.00mm pitch
2 GBytes	SFUI2048K1AE2T0-I-MS-2B1-STD	
4 GBytes	SFUI4096K1AE2T0-I-QT-2A1-STD	
	SFUI4096K1AE2T0-I-QT-2B1-STD	
8 GBytes	SFUI008GK1AE1T0-I-DB-2A1-STD	
	SFUI008GK1AE1T0-I-DB-2B1-STD	
16 GBytes	SFUI016GK1AE1T0-I-QC-2A1-STD	
	SFUI016GK1AE1T0-I-QC-2B1-STD	
32 GBytes	SFUI032GK1AE1T0-I-NC-2A1-STD	

4. Product Description

4.1 Performance Specifications

The drives are optimized for random write access.

Table 3: Typical performance in different transfer modes

Speed	SuperSpeed mode (sequential, typ)	High-Speed mode (sequential, typ)	Full-Speed mode (sequential, typ)	Unit
Burst	5000	480	12	Mbit/s
Read	53...174	36	1.0	MBytes/s
Write	32...91	28 ¹	0.9	

Table 4: SuperSpeed performance

Density	Sequential read (MB/s)	Sequential write (MB/s)	Random read 4k (IOPS)	Random write 4k (IOPS)
1GB	32	14	2290	1500
2GB	54	26	1950	1380
4GB	53	32	1670	940
8GB	163	70	2940	1060
16GB	174	91	2980	1040
32GB	172	79	2950	1030

4.2 Environmental Specifications

4.2.1 Recommended operating conditions

Table 5: Recommended operating conditions

Performance Specifications	Symbol	Min	Typ	Max	Unit
Commercial Operating Temperature	T_A	0	25	70	°C
Industrial Operating Temperature		-40		85	
Storage Temperature	T_S	-40		100 ²	

4.2.2 Reliability and Endurance

Table 6: Reliability

Parameter	Value
Data reliability (UBER)	<10 ⁻¹⁷ bits read
Error correction code (ECC)	correct up to 24-bit errors per 1kB (4GB) correct up to 60-bit errors per 1kB (8-32GB)
MTBF / MTTF	> 3,000,000 hours
Data retention@40°C (JESD 218)	10 years @ 10% life time / 1 years @ life end

¹ Effective speed varies with controller, number and type of flash, host, file size, file system and operating system

² Data loss (retention) is accelerated by high temperature (5 days@100°C is equivalent to 10 years@40°C, i.e. retention acceleration factor is 700)

Table 7: Endurance³

Drive Capacity	TeraBytes Written (TBW) @ Seq. Write 128kB Operation ⁴	TeraBytes Written (TBW) @ Random Write 128kB Operation ⁴	TeraBytes Written (TBW) @ Random Write 4kB Operation ⁴
1 GBytes	96	40	8
2 GBytes	208	62	13
4 GBytes	394	99	25
8 GBytes	806	224	50
16 GBytes	1608	402	95
32 GBytes	3216	816	184

³ The Endurance values depend strongly on the use case, the preconditioning, the operation sequence, use of trim commands and usage level of the flash drive. The given values are for orientation only.

⁴ Sequential write 128kB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

Swissbit AG

Industriestrasse 4
CH-9552 Bronschhofen
(P000000936) (1)
Switzerland

TLP: Swissbit public
no unauthorized distribution

www.swissbit.com/contact

Revision: 1.04

Template: Doc-4991
File: Productsheet-Datasheet-U-500_Rev1.04

4.2.3 Environmental Specifications

Table 8: Environmental conditions

Parameter	Value
Shock	1,500G Peak (JESD22-B110)
Vibration	50G Peak (MIL-STD-883H M2007.3)
Humidity (Temperature Humidity Bias)	85°C, 85% RH, V _{max} , 1000 hours (JESD22-A101)
Temperature Cycling	-40°C to +125°C, 500 cycles (JESD22-A104)
High Temperature Biased Life	125 °C, 1000 hours (JESD22-A108)
Alpha Particle Emission of Controller	< 0.001 CPH/cm ²
Alliance for Telecom. Industry Solutions (ATIS)	125°C for 750 hours, 500G Peak Shock and cross section

4.3 Drive Geometry Specification

Table 9: Drive Geometry

Raw Capacity	Total LBA	User Addressable Bytes
	Decimal	(Unformatted)
1 GBytes	1,960,704	1,003,880,448
2 GBytes	3,921,664	2,007,891,968
4 GBytes	7,843,328	4,015,783,936
8 GBytes	15,663,104	8,019,509,248
16 GBytes	31,326,208	16,039,018,496
32 GBytes	62,533,296	32,017,047,552

4.4 Regulatory Compliance

The U-500 devices comply with the standards listed in the following table.

Table 10: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE – 2014/30/EU FCC – 47 CFR Part 15 UKCA – S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACH	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

4.5 NAND Flash technologies

SLC, pSLC and MLC flash

- Single-level-cell (SLC) flash, 1 bit (2 levels) is stored in each memory cell
- Pseudo Single-level-cell (pSLC) 1 bit (2 levels) is stored in an MLC memory cell by special sequences
- Multi-level-cell (MLC) flash, 2 bit (4 levels) are stored in each memory cell

Table 11: Differences SLC vs pSLC vs MLC

Series	U-500	U-56	U-50	Comment
Technology	SLC	pSLC	MLC	
Endurance	up to 100,000	up to 20,000	up to 3,000	Physical program/erase cycles
Write Performance	Superior	Superior	High	pSLC and SLC have improved write performance due to single bit write
Read Performance	Increased	Increased	High	pSLC and SLC have improved read performance due to single bit read
Reliability	highest	high	normal	Degradation of information has higher impact with 4 programmed levels
Cost	high	medium	low	MLC can store twice the bits per square mm silicon

5. Electrical Interface

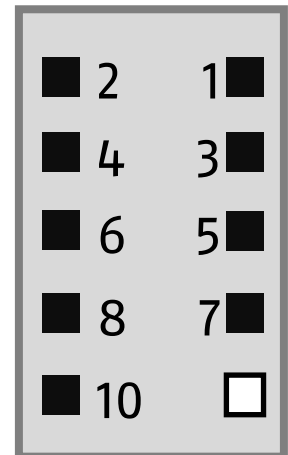
- USB-connector 10pin (2mm or 2.54mm pitch)
- **Do not connect the drives to a standard USB2 host pin header with two USB 2.0 ports!**
If pin 2 has 5V at the host side, it can destroy the USB3 SSRX+ input of the device.
- USB 3.1 Gen1 SuperSpeed interface, USB2.0 high-speed and 1.1 full-speed compatible

Table 12: Electrical pinout from device and host view.

Never connect >1.8V to pin2 and pin4.

Pin	Signal device view	Signal host view	Description host view
1	V_Bus	V_Bus	Operating voltage
2	SSRX+	SSTX+	Host transmit +
3	D-	D-	Data signal pair
4	SSRX-	SSTX-	Host transmit -
5	D+	D+	Data signal pair
6	GND	GND	Ground
7	GND	GND	Ground
8	SSTX+	SSRX+	Host receive +
9	-	-	Keyed at connector
10	SSTX-	SSRX-	Host receive -

See also chapter 7 Package Mechanical



6. Electrical Specification

Table 13: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_Bus	-0.5	6.0	V
Voltage at D+ and D-	V_Data	-0.5	5.0	
Voltage at USB3 pins	V_Data	-0.5	1.8	
Commercial Operating Temperature	T_A	0	70	°C
Industrial Operating Temperature		-40	85	

Table 14: DC characteristics for SuperSpeed operation (T=25°C, V_Bus=5V or 3.3V)

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Supply Voltage (Standard)	V_Bus		3.1	3.3 or 5.0 ⁵	5.50	V
Write current	I_WR	V_Bus=5.0V 1GB (TSOP)		80	95	mA
Read current	I_RD			80	90	
Idle current	I_IDL			60		
Suspend current	I_CCS			1.9		
Write current	I_WR	V_Bus=5.0V 2GB (TSOP)		100	120	
Read current	I_RD			90	115	
Idle current	I_IDL			60		
Suspend current	I_CCS			1.8		
Write current	I_WR	V_Bus=5.0V 4GB (TSOP)		115	150	
Read current	I_RD			95	150	
Idle current	I_IDL			30 ⁶	40	
Suspend current	I_CCS			1.6	2.5	
Write current	I_WR	V_Bus=5.0V 8/16/32GB (BGA)		180	200	
Read current	I_RD			190	210	
Idle current	I_IDL			40 ⁶	50	
Suspend current	I_CCS			2	2.5	

Table 15: DC characteristics for High-Speed operation (T=25°C, V_Bus=5V or 3.3V)

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Supply Voltage (Standard)	V_Bus		3.1	3.3 or 5.0 ⁵	5.50	V
Write current	I_WR	V_Bus=5.0V 4GB (TSOP)		68	90	mA
Read current	I_RD			55	80	
Idle current	I_IDL			26 ⁶	40	
Suspend current	I_CCS			1.6	2.5	
Write current	I_WR	V_Bus=5.0V 8/16/32GB (BGA)		75	100	mA
Read current	I_RD			75	100	
Idle current	I_IDL			34 ⁶	50	
Suspend current	I_CCS			2	2.5	
High Speed Idle Level	V_HSOI	V_Bus=5.0V	-10		10	mV
High Speed Data Signaling LOW	V_HSOL	V_Bus=5.0V	-10		10	
High Speed Data Signaling HIGH	V_HSOH	V_Bus=5.0V	360		440	
Chirp J Level (differential)	V_CHIRPJ	V_Bus=5.0V	360		440	

⁵ The U-5x devices can be supplied with 5V or with 3.3V

⁶ Typically 5 minutes after power on the device performs a background data care management, that needs up to 150mA

Chirp K Level (differential)	V_CHIRPK	V_Bus=5.0V	-440		-360	
------------------------------	----------	------------	------	--	------	--

Table 16: DC characteristics for Full-Speed operation (T=25°C, V_Bus=5V or 3.3V)

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Supply Voltage (5V Type)	V_Bus		3.1	3.3 or 5.0 ⁵	5.50	V
Write current	I_WR	V_Bus=5.0V 4GB (TSOP)		55	80	mA
Read current	I_RD			50	80	
Idle current	I_IDL			26 ⁶	40	
Suspend current	I_CCS			1.6	2.5	
Write current	I_WR	V_Bus=5.0V 8/16/32GB (BGA)		50	80	mA
Read current	I_RD			50	80	
Idle current	I_IDL			34 ⁶	50	
Suspend current	I_CCS			2	2.5	
Input LOW Voltage	V_IL				0.8	V
Input HIGH Voltage	V_IH		2			
Output LOW Voltage	V_OL	RL of 1.5kΩ to 3.6V			0.3	
Output HIGH Voltage	V_OH	RL of 15kΩ to GND	2.8		3.6	
Output Signal Crossover Voltage	V_CRS		1.3		2.0	

7. Package Mechanical

- Standard form factor of PCBs 36.8mm x 26.65mm
- Hole for mechanical fixture (optional grounded)
- 3 additional holes
- LED for operation indication (optional without LED)
- 2 connector types
 - 2.54mm pitch, 7.5mm long standard
 - 2.00mm pitch, 3.68mm long low profile
- Component heights max. 1.4mm on connector side
max. 1.4mm on flash side
- Weight (max.) 5g

Figure 2: Mechanical Dimensions for U-500 1GB-4GB drive

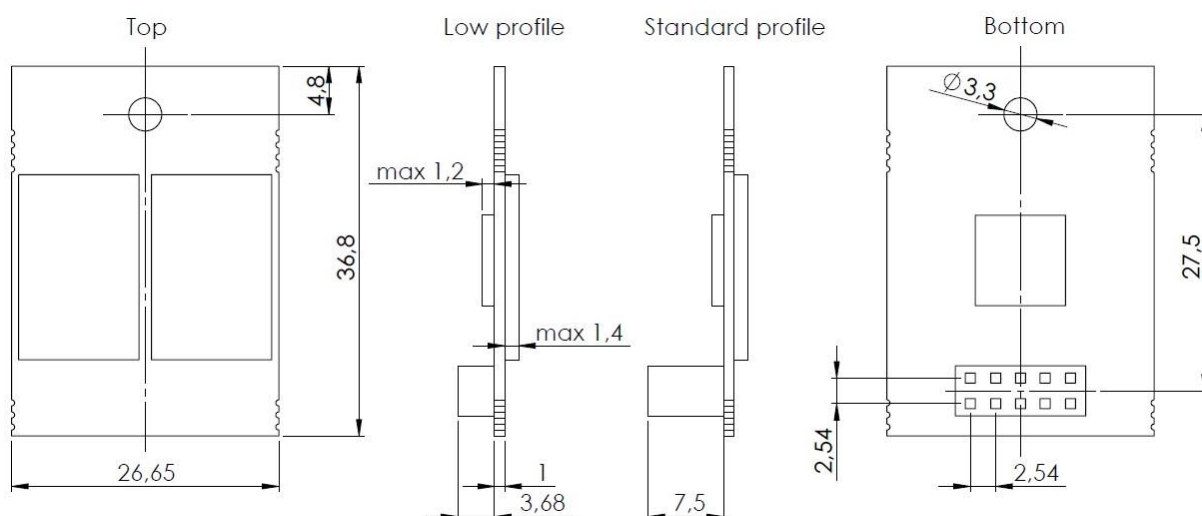
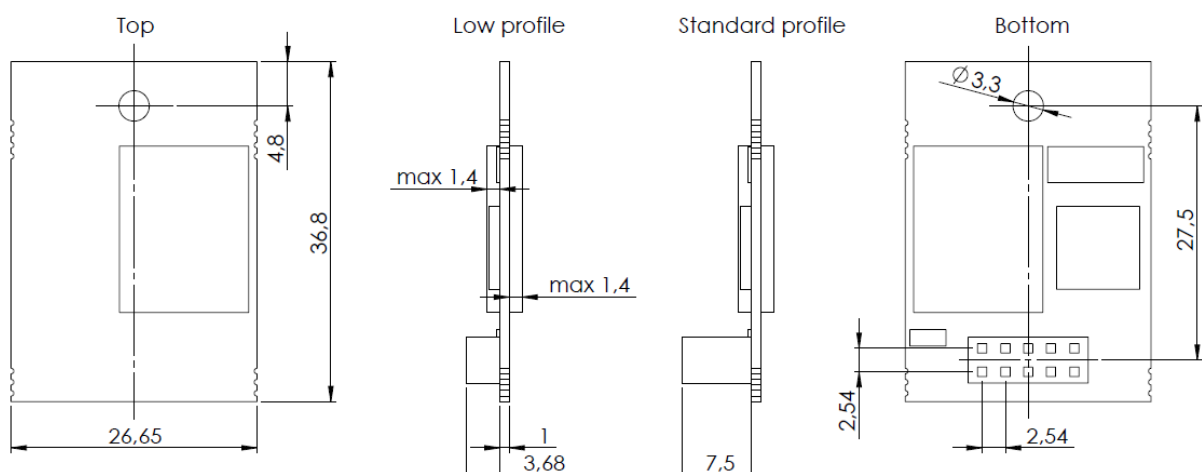


Figure 3: Mechanical Dimensions for U-500 8GB-32GB drives



All dimensions are in millimeters, tolerance: ± 0.15

Table 17: Connector variations

Part number	Connector	Pin 9	Hole	LED
SFUIxxxxlgAExxx-t-xx-xfx-STD	2.54 mm	Key pin	NC (grounded on request)	For operational indication (w/o LED on request)
SFUIxxxxKgAExxx-t-xx-xfx-STD	2.00 mm	Key pin		

g = hardware generation

t = temperature grade (C=0°C to 70°C and I=-40°C to +85°C)

f = firmware generation per product type

Swissbit AG

Industriestrasse 4
CH-9552 Bronschhofen
(P000000936) (1)
Switzerland

TLP: Swissbit public
no unauthorized distribution

www.swissbit.com/contact

Revision: 1.04

Template: Doc-4991

File: Productsheet-Datasheet-U-500_Rev1.04

Page 14 of 21

8. ATA Pass-Through commands (Identify Device and S.M.A.R.T.)

8.1 ATA Pass-Through commands

Additional to the standard SCSI commands the device also supports the ATA Pass-Through commands.

Table 18: ATA PASS-THROUGH(x) commands

SCSI command	OpCode	Description
ATA PASS-THROUGH(12)	A1h	Write and read ATA registers to send commands and read information
ATA PASS-THROUGH(16)	85h	

<http://www.t10.org/ftp/t10/document.04/04-262r8.pdf>

Table 19: ATA register addressing

Offset address	Input	Output	type	Identify device	e.g. SMART commands
0	Data		Word		
1	Feature	Error	Byte	xx	yyh*
2	Sector count		Byte	xx	01h
3	LBA_Low		Byte	xx	xx
4	LBA_Mid		Byte	xx	4Fh
5	LBA_High		Byte	xx	C2h
6	Drive/head		Byte	Eoh	Eoh
7	Command	Status	Byte	ECh	Boh

* see below

8.2 Identify Device

The Identify Device returns a identify sector compatible to ATA and SATA devices.
Here an example of the interpretation of this sector.

Table 20: Identify Device Information

Word(s)	Default Value		Total Bytes	Data Field Type Information
0	0040h		2	Standard Configuration Fixed (optional 848Ah for removable)
...	...	...	...	...
10-19	aaaa*		20	Serial number in ASCII (right-justified)
...	...	...	...	...
23-26	XXXX*		8	Firmware revision in ASCII (big-endian byte order in Word)
27-46	XXXX*		40	Model number in ASCII (right-justified)
...	...	...	...	...
60-61	XXXXh		4	Total number of sectors addressable in LBA mode
...	...	...	...	...
82	0101h		2	Command set: SMART feature set, service interrupt
...	...	...	...	...
85	000Xh		2	Command set enabled: SMART feature set enabled/disabled
...	...	...	...	...
255	XXA5h		2	Integrity Word

* Values depend on device configuration.

8.3 S.M.A.R.T. commands

The intent of the SMART command feature set is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of a near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of the appropriate action.

All S.M.A.R.T. commands have the command code Boh. The different commands are selected by the Feature register.

Table 21: S.M.A.R.T. Features Supported

Operation	Feature	Sect Count	LBA low	LBA mid	LBA high	DRV head	Com-mand
S.M.A.R.T. Read Data	D0h	01h	xx	4Fh	C2h	E0h	Boh
S.M.A.R.T. Read Attribute Thresholds	D1h	01h	xx	4Fh	C2h	E0h	Boh
S.M.A.R.T. Enable Operations	D8h	xx	xx	4Fh	C2h	E0h	Boh
S.M.A.R.T. Disable Operations	D9h	xx	xx	4Fh	C2h	E0h	Boh
S.M.A.R.T. Return Status	DAh	xx	xx	4Fh	C2h	E0h	Boh

All commands were aborted, if the LBA signature is invalid.

8.3.1 S.M.A.R.T. Read Data (D0h)

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following table for the data structure of this sector.

Table 22: S.M.A.R.T. Data Structure

Byte(s)	Value	Description
0-1	0010h	S.M.A.R.T. structure version
2-361	XXh	Attribute entries 1 to 30 (see Table 23)
362	00h	Off-line data collection status (no off-line data collection started)
363	00h	Self-test execution status byte (self-test completed)
364-365	0000h	Total time, in seconds, to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368-369	0003h	S.M.A.R.T. capabilities
370	00h	No Error logging capability
371	00h	Vendor specific
372	00h	Short self-test routine recommended polling time, in minutes
373	00h	Extended self-test routine recommended polling time, in minutes
374-385	00h	Reserved
386-387	0004h	SMART Version
388-510	XXh	Vendor specific
511	XXh	Data structure checksum

8.3.2 S.M.A.R.T. Attribute Entry Structure

Each attribute entry (Bytes 2–361) consists of 12 bytes. See the following table for the data structure of each entry.

Table 23: Attribute Entry

Offset Byte(s)	Value	Description
0	XXh	Attribute ID (see Table 24)
1–2	XXXXh	Flags (little-endian) Bit0: Advisory (0) or Prefailure (1) Bit1: Not used (0) or updated during normal operation (1)
3	XXh	Current value as a percentage 64h = 100%
4	XXh	Worst value as a percentage 64h = 100%
5–8	XXXXh	Raw value (little-endian)
9–11	00h	Reserved

8.3.3 S.M.A.R.T. Attributes

The drives support the S.M.A.R.T. attributes listed in the following table.

The Threshold values can be read out with the S.M.A.R.T. Read Attribute Thresholds command (D1h)

The first attributes (196, 213, 229) are “Pre-Fail” type, while all other are Advisory (Old Age).

Table 24: S.M.A.R.T. Attributes

ID dec	ID hex	Value	Worst	Threshold	Attribute	Description	RAW values Offset 5–10
196	C4h	X%	100	25	Spare Block Count	Number of total available NAND spare blocks	Initial and current number of spare blocks
213	D5h	X%	100	25	Spare Block Count worst channel	Spare block count for the NAND with the lowest number of remaining spare blocks	Initial and current number of spare blocks of the channel with the lowest current number of spare blocks
229	E5h	X%	X%	2	Total Erase Count	Estimated number of total NAND block erases	Estimated number of total NAND block erases
203	CBh	100	100	0	Total ECC Errors	All recorded ECC errors	Total number of ECC errors (correctable and uncorrectable)
204	CCh	100	100	0	Correctable ECC Errors	Total recorded ECC errors that were corrected during the life of the drive	Total number of correctable ECC errors
199	C7h	100	100	0	UDMA CRC Errors	Dummy attribute, included for legacy reasons	This value is fixed at 0.
232	E8h	100	100	0	Total Number of Reads	Total number of NAND READ commands	Total number of NAND READ commands
12	0Ch	100	100	0	Power-On Count	Count of power-on events	Number of power cycles
241	F1h	100	100	0	Total LBAs Written	Total amount of data written to the drive	Total number of LBAs written to the disk, divided by 65536
242	F2h	100	100	0	Total LBAs Read	Total amount of data read from the drive	Total number of LBAs read from the disk, divided by 65536
214	D6h	100	100	0	Management Block status	Total number of times the management block has been updated	Management block write count
194	C2h	X°C	Max °C	0	Temperature Status	Device temperature in Celsius (°C)	Current/Min/Max temperature

* These threshold values are changeable using the Write Attribute Thresholds command.

8.3.4 S.M.A.R.T. Read Attribute Thresholds (D1h)

When the drive receives the S.M.A.R.T. Read Attribute Thresholds subcommand, it returns one sector (512 bytes) of data similar as S.M.A.R.T. Read data sector, but with the threshold value in offset 1 of each attribute (see Table 24)

8.3.5 S.M.A.R.T. Enable Operations (D8h)

This command enables access to the S.M.A.R.T. capabilities of the drive. The state of SMART (enabled or disabled) is preserved across power cycles.

8.3.6 S.M.A.R.T. Disable Operations (D9h)

This command disables access to the S.M.A.R.T. capabilities of the drive. The state of SMART (enabled or disabled) is preserved across power cycles.

8.3.7 S.M.A.R.T. Return Status (DAh)

Table 25: S.M.A.R.T. Return Status

Operation	Feature	Sect Count	LBA low	LBA mid	LBA high	DRV head	Com-mand
Command S.M.A.R.T. Return Status	DAh	xx	xx	4Fh	C2h	Eoh	Boh
Response							
S.M.A.R.T. Return Status OK	xx	xx	xx	4Fh	C2h	xx	xx
S.M.A.R.T. Return Status Pre-FAIL*	xx	xx	xx	F4h	2Ch	xx	xx

* If a threshold exceeded condition exists for either the Spare Block Count Worst Channel attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. In this case the drive should be replaced soon.

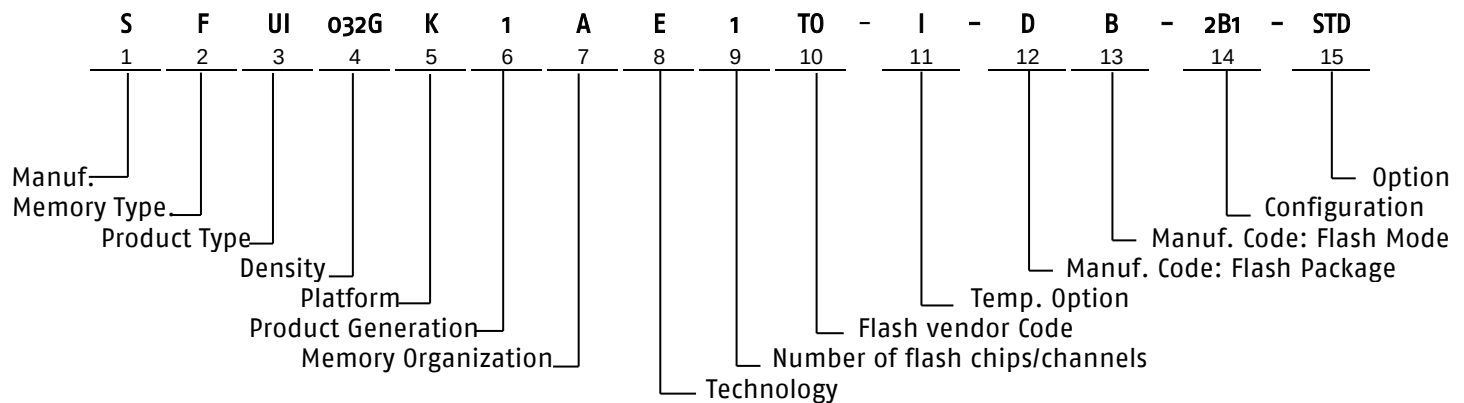
9. Marking Specification

9.1 Top View



9.1.1 Figure 1: U-500 top view (example)

10. Part Number Decoder



10.1 Manufacturer

Swissbit	S
----------	---

10.2 Memory Type

Flash	F
-------	---

10.3 Product Type

U-xxx USB Flash Drive Module (Internal)	UI
---	----

10.4 Density

1 GB	1024
2 GB	2048
4 GB	4096
8 GB	008G
16 GB	016G
32 GB	032G

10.5 Platform

U-xxx – 2.54mm plug	J
U-xxx – 2.00mm plug	K

10.6 Product Generation

10.7 Memory Organization

x8	A
----	---

10.8 Technology

U-5xx technology	E
------------------	---

10.9 Number of Flash chips

1 Flash	1
2 Flash	2

10.10 Flash Code

Toshiba / Kioxia	T0
------------------	----

10.11 Temp. Option

Industrial Temp. Range -40°C to 85°C	I
Commercial Temp. Range 0°C to 70°C	C

10.12 DIE Classification

	SLC	MLC/pSLC
MONO (single die package)	M	G
DDP (dual die package)	D	L
QDP (quad die package)	Q	H
ODP (octal die package)	N	O

10.13 PIN Mode

	BGA	TSOP
Single nCE & R/nB	A	S
Dual nCE & Dual R/nB	B	T
Quad nCE & Quad R/nB	C	-

10.14 Configuration XYZ

X → Setting

Removable Drive	1
Fixed Drive	2

Y → Firmware revision

Revision 1	A
Revision 2	B

Z → Optional setting

Default (SLC or MLC)	1
pSLC (pseudo SLC)	P

10.15 Option

Swissbit standard 3.3 / 5 V supply	STD
Customized version	XXX

11. Revision History

Table 26: Document Revision History

Date	Revision	Description	Revision Details
05-June-2018	1.00	First release	Doc. req. no. 2242
26-January-2023	1.01	Added new FW revision products	Doc. req. no. 6014
23-July-2024	1.02	Wrong part number removed	Doc. req. no. 7285
21-August-2024	1.03	Table 2 has been updated	
22-May-2025	1.04	Added 1GB & 2GB variants	

Disclaimer:

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of Swissbit AG ("SWISSBIT"). The information in this document is subject to change without notice. SWISSBIT assumes no responsibility for any errors or omissions that may appear in this document and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SWISSBIT makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SWISSBIT does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SWISSBIT products in applications not intended by SWISSBIT, said customer must contact an authorized SWISSBIT representative to determine SWISSBIT willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SWISSBIT. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SWISSBIT.

ALL PRODUCTS SOLD BY SWISSBIT ARE COVERED BY THE PROVISIONS APPEARING IN SWISSBIT'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SWISSBIT MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

© 2025 SWISSBIT AG All rights reserved.