EZ-PD™ CCG7DC (CYPD7272-68LQXQ) multiport charger and adapter solution (REF_CCG7DC_120W_2C) test report

Product_sales code – REF_CCG7DC_120W_2C

Devices – EZ-PD™ CCG7DC (CYPD7272-68LQXQ)

About this document

Scope and purpose

This test report provides test results of EZ-PD™ CCG7DC (CYPD7272-68LQXQ) USB Type-C Power Delivery (PD) and buck-boost controller-based 120 W dual-port adapter solution (REF_CCG7DC_120W_2C).

Intended audience

This test report is intended for the charger and adapter application hardware designers using EZ-PD™ CCG7DC (CYPD7272-68LQXQ) USB Type-C PD and buck-boost controller.

Abbreviations and definitions

Table 1 Abbreviations and definitions

Abbreviation	Definition
CC-CV	constant current-constant voltage
CE	conducted emission
CH'x'	oscilloscope channel numbers
DCM	discontinuous current mode
DP/DM	USB data positive/data negative lines
DUT/EUT	device under test/equipment under test
FCCM	forced continuous conduction mode
FET	MOSFET (metal oxide semiconductor field effect transistor)
Io/I_{OUT}	output current of the DUT
NGDO	NFET gate driver output
OCP	overcurrent protection
OVP	overvoltage protection
P1/P2/P3	port #1/port #2/port #3
PAT	power adapter tester
PDO	power delivery output
P-P	peak-to-peak
PPS	programmable power supply

About this document

Abbreviation	Definition
PSM	pulse skip mode
SCP	short-circuit protection
SW1	buck converter switch node
UI	user interface
V_{BUS_C}	bus voltage at USB Type-C
V_{BUS_C}/V_{OUT}	output voltage of the DUT
V_{IN}/V_{IN_DC}	input DC voltage to the DUT
USB PD	Universal Serial Bus Power Delivery

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1 Introduction

The EZ-PD™ CCG7DC (CYPD7272-68LQXQ) 120 W dual-port adapter solution (REF_CCG7DC_120W_2C) test report provides the electrical performance parameters like efficiency, ripple, regulation, constant voltage, constant current operation, output current transient response, output voltage transition, startup turn-on delay, startup rise time, and fault protections. This test report also provides the thermal performance of REF_CCG7DC_120W_2C at room temperature.

EZ-PD™ CCG7DC is a highly integrated dual-port USB Type-C PD solution with an integrated buck-boost controller. Following are the key features of EZ-PD™ CCG7DC:

- Complies with the latest USB Type-C and USB-PD specifications and is targeted at charger and adapter applications
- CCG7DC integration reduces the bill of materials (BOM). Additionally, provides the footprint-optimized solution for the charger and adapter
- Integrated gate drivers for V_{BUS} NFET on the provider path or for the buck bypass switch control
- Includes hardware-controlled protection features on the V_{BUS}
- Supports a wide input voltage range (4 V to 24 V with 40-V tolerance) and programmable switching frequency (150 kHz to 600 kHz) in an integrated PD solution
- Integrates monitoring, protection, and communication features that are needed to build a robust charger and adapter USB-C charging system

CCG7DC is the most programmable USB-PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128-kB flash, 16-kB RAM, and 32-kB ROM that leaves most of the flash available for user application. It also includes various analog and digital peripherals such as analog to digital converters (ADCs), pulse-width modulators (PWMs), I2C/SPI/UART interfaces, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging or event data recording.

The Power Delivery (PD) technology is designed to provide the fastest charging possible through a USB Type-C (USB-C) cable. The USB-PD Standard Power Range (SPR) standard defines the maximum power that can be delivered over a USB-C cable up to 100 W. This allows for providing multiple USB-C ports (Figure 1) on universal AC-DC adapters that can charge a wide range of devices, from smartphones to gaming laptops, power tools, and even e-bikes.

However, these new requirements for higher power and multiport have presented challenges for the converter topologies used until now. Electromagnetic compatibility, power factor correction, standby power, and average efficiency are just a few factors that need to be considered to ensure that the chargers and adapters are both effective and efficient. The size (and consequently, the power density), as well as load sharing and scaling up multiple ports, have also become more critical factors for design engineers and users. The power efficiency of USB-C chargers and adapters plays a crucial role in determining their power density. Hence, converter topology, usage model, integration, and flexibility of controller functionalities are all key factors to consider when selecting the right adapter architecture.

A typical block diagram of a multiport adapter is illustrated in Figure 1. The front-end AC-DC converter is responsible for producing the requested output voltage while ensuring power factor correction (PFC) at the front end for up to 120 W of power. On the other hand, the buck converter (connected at the output of the AC-DC converter) ensures that the defined USB-C PD specifications and performance are met for multiport adapter applications.

Introduction

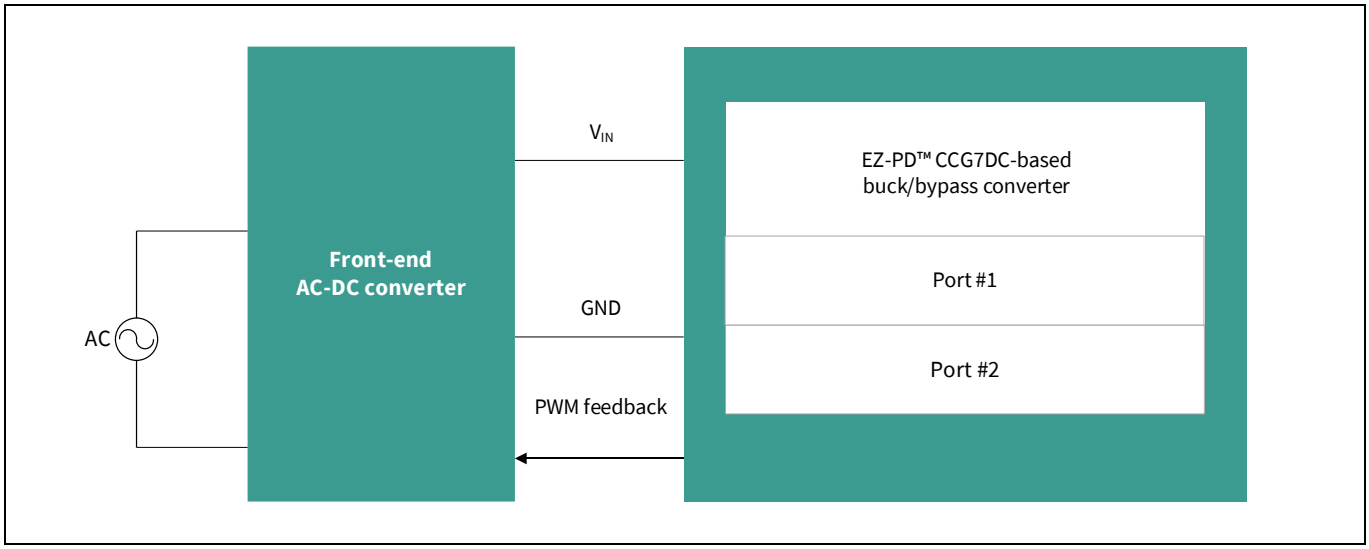


Figure 1 High-level block diagram of a multiport adapter

The XDP™ XDPS2221 [9] controller is a highly integrated device including the valley-switching PFC controller, the HFB (asymmetrical half-bridge) controller, and three gate drivers for the main switches. The internal handshaking between the PFC and HFB controller, and the adaptive bus voltage setting makes this controller a perfect fit for applications with wide AC input and wide output voltage range, such as USB PD adapters and battery chargers. The engineering report of XDP™ 140 W USB PD reference board with PFC+hybrid flyback combo IC XDPS2221 can be referenced for additional details [9].

The EZ-PD™ CCG7DC is designed to support a dual USB PD/PPS port, featuring an integrated buck controller and gate driver, allowing easy scaling to multiport output.

A high-level block diagram of the EZ-PD™ CCG7DC-based adapter and charger solution is shown in Figure 2 and Figure 3.

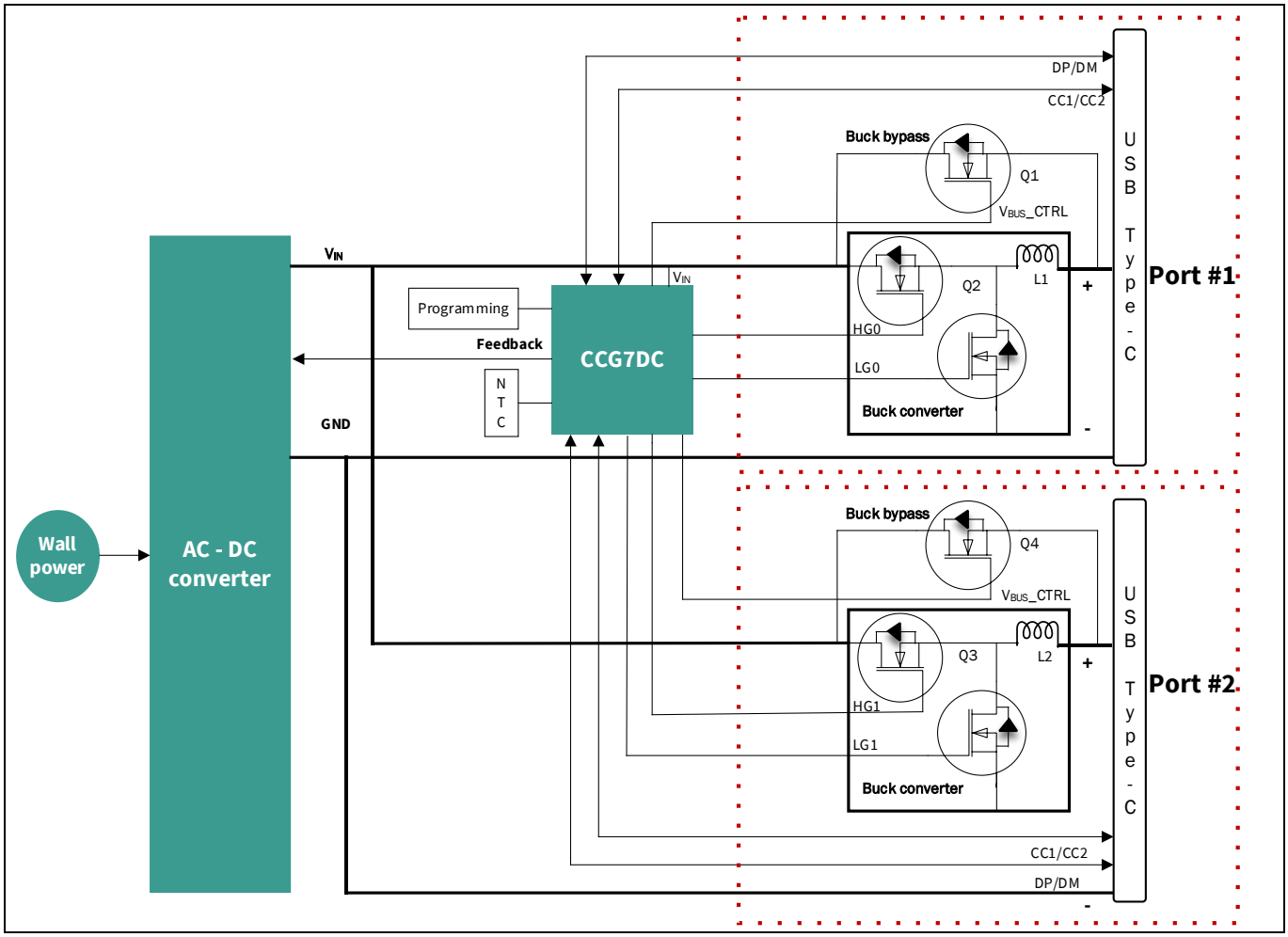


Figure 2 High-level block diagram of EZ-PD™ CCG7DC-based charger and adapter solution

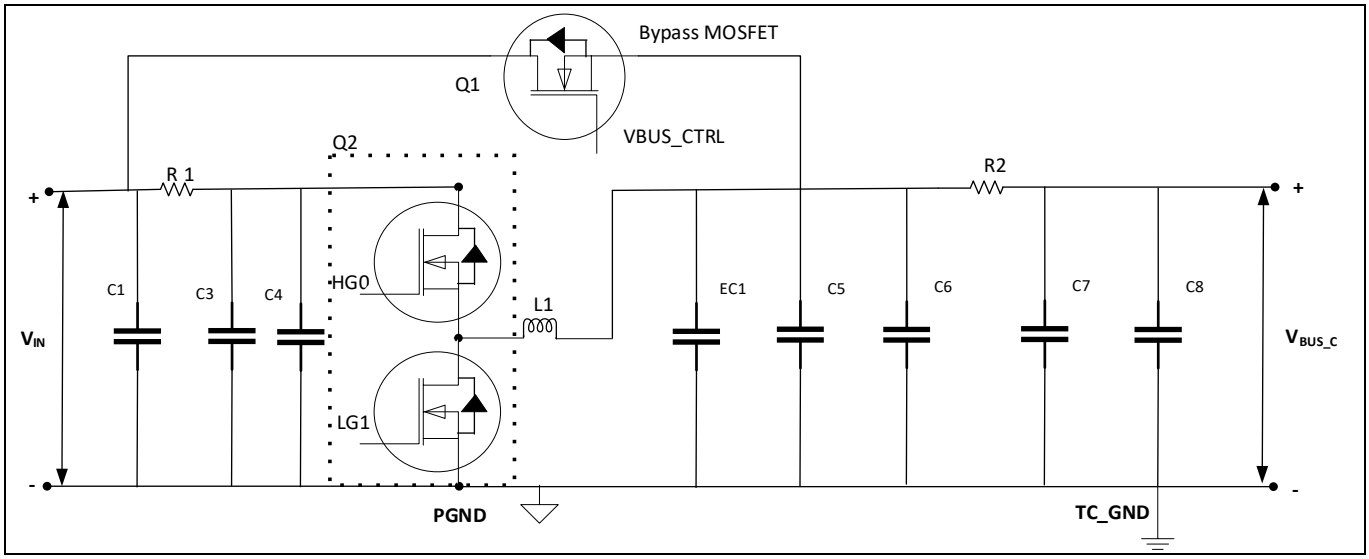


Figure 3 High-level block diagram of EZ-PD™ CCG7DC buck topology with bypass FET

Table 2 Critical components BOM

Designator	Description	Part number	Manufacturer
U1	EZ-PD™ CCG7DC dual-port USB Type-C with PD and buck-boost controller	CYPD7272-68LQXQ	Infineon Technologies
Q2, Q3	Mosfet Array 40V 45A (Tj) 41W (Tc) Surface Mount	IAUC45N04S6N070HATMA1	Infineon Technologies
Q1, Q4	MOSFET N-CH 40V 15A/40A TSDSON	BSZ063N04LS6ATMA1	Infineon Technologies
L1, L2	6.8 µH Shielded Drum Core, Wire wound Inductor 7.2 A 13.5mOhm	74439358068	Würth Elektronik
C5, C6, C42, C43, C1, C2	CAP CER 10 µF 50V X7R 1206	CL31B106KBHNNNE	Samsung Electronics
C7, C44	CAP CER 0.1 µF 50V X7R 0603	885012206095	Würth Elektronik
C8, C45, C40, C41	CAP CER 4.7UF 50V X7R 0805	C2012X7R1H475K125AC	TDK Corporation
EC1, EC2	330 µF 25 V Aluminum - Polymer Capacitors Radial	EEH-ZK1E331UP	Panasonic Electronic Components
R1, R15	Current sense resistors - SMD 0.005 Ω 1% 1.5 W	KRL3216E-C-R005-F-T1	Susumu
R2, R16	RES 0.005 Ω 1 W 0805 WIDE	KRL2012E-M-R005-F-T5	Susumu

Table 3 Test results description

Test results	Description
Single port power management test results of REF_CCG7DC_120W_2C	Port #1 performance results with REF_CCG7DC_120W_2C
Two port power management test results of REF_CCG7DC_120W_2C	Two port performance results with REF_CCG7DC_120W_2C
Single port power management test results of XDPS2221+REF_CCG7DC_120W_2C	Port #1 performance results with XDPS2221+REF_CCG7DC_120W_2C
Dual-port power management test results of XDPS2221+REF_CCG7DC_120W_2C	Two port performance results with XDPS2221+REF_CCG7DC_120W_2C

Table 4 PCB details of REF CCG7DC_100W_R2 daughterboard

PCB layer	Copper thickness	Details
Top layer	2 oz.	Components, power traces
Second layer	2 oz.	High-frequency traces, control signal traces
Third layer	2 oz.	Ground layer
Bottom layer	2 oz.	Components, power traces
Board size	–	61 mm × 28.94 mm
Board thickness	–	1.6 mm

Table 5 PCB details of REF_CCG7DC_BASE_120W_3C_R2 baseboard

PCB layer	Copper thickness	Details
Top layer	2 oz.	Components, power traces
Second layer	2 oz.	High-frequency traces, control signal traces
Third layer	2 oz.	Ground layer
Bottom layer	2 oz.	Components, power traces
Board size	–	65 mm × 37.19 mm
Board thickness	–	1.6 mm

The EZ-PD™ CCG7DC-based multiport charger and adapter baseboard with one daughterboard is shown in Figure 4. The baseboard with one daughterboard can operate up to 120 W, with each port that can operate up to 100 W.

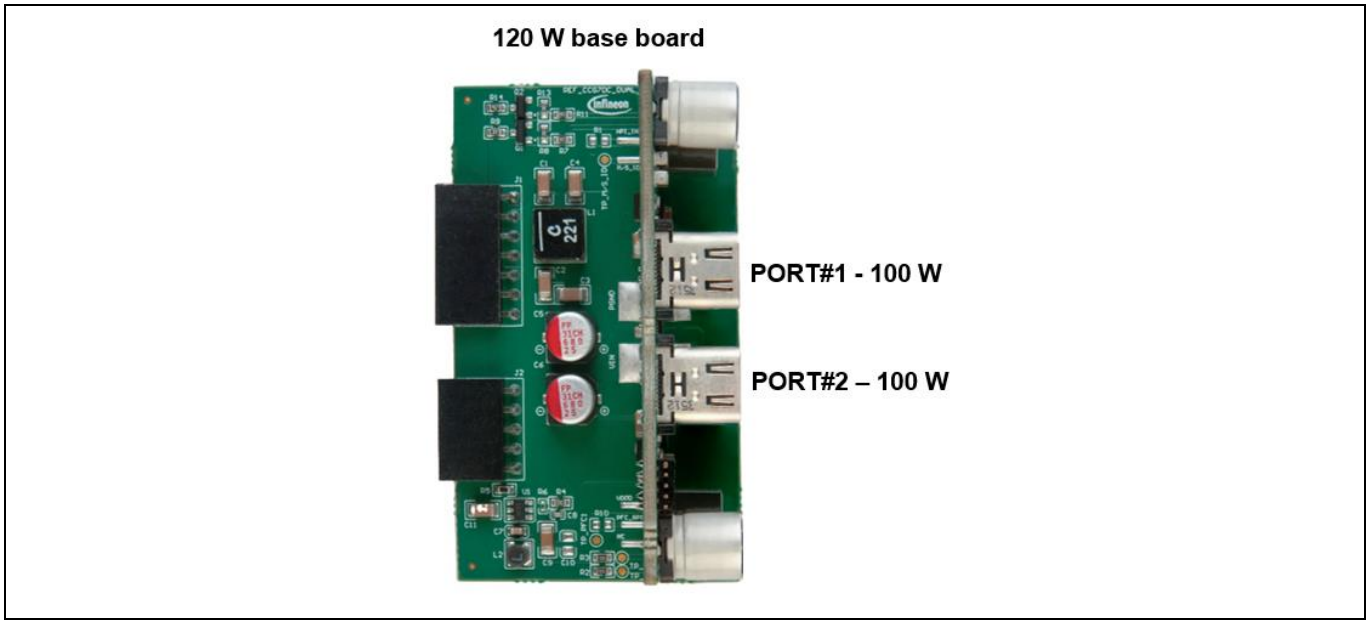


Figure 4 EZ-PD™ CCG7DC multiport charger and adapter solution baseboard integrated with a single EZ-PD™ CCG7DC 120 W daughterboard

The EZ-PD™ CCG7DC controller-based standalone daughterboard is shown in Figure 5. Each daughterboard can deliver the power up to 100 W with a maximum load current of 5.0 A.

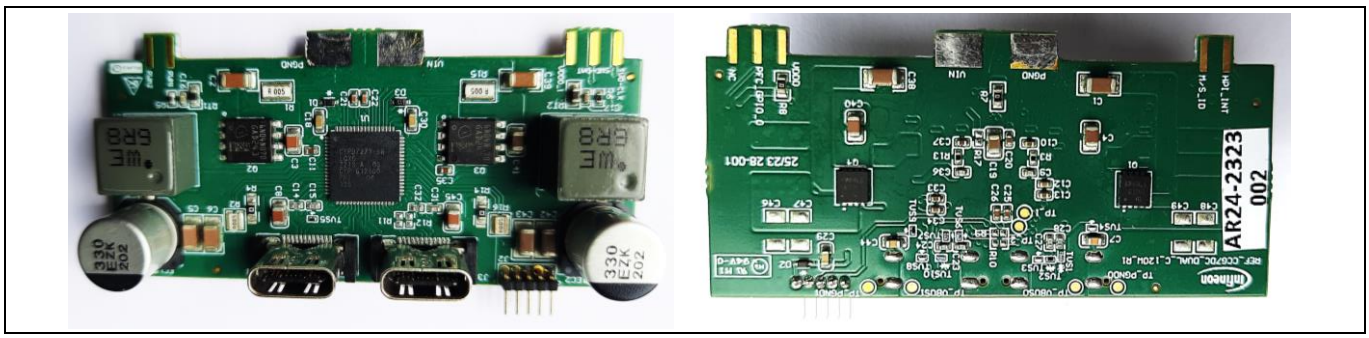


Figure 5 Standalone EZ-PD™ CCG7DC 100 W (each port) daughterboard

Introduction

The XDPS2221+EZ-PD™ CCG7DC 2 port 120 W AC/DC charger and adapter is shown in Figure 6. The total power is 120 W, and each port can deliver power up to 100 W with a maximum load current of 5.0 A.

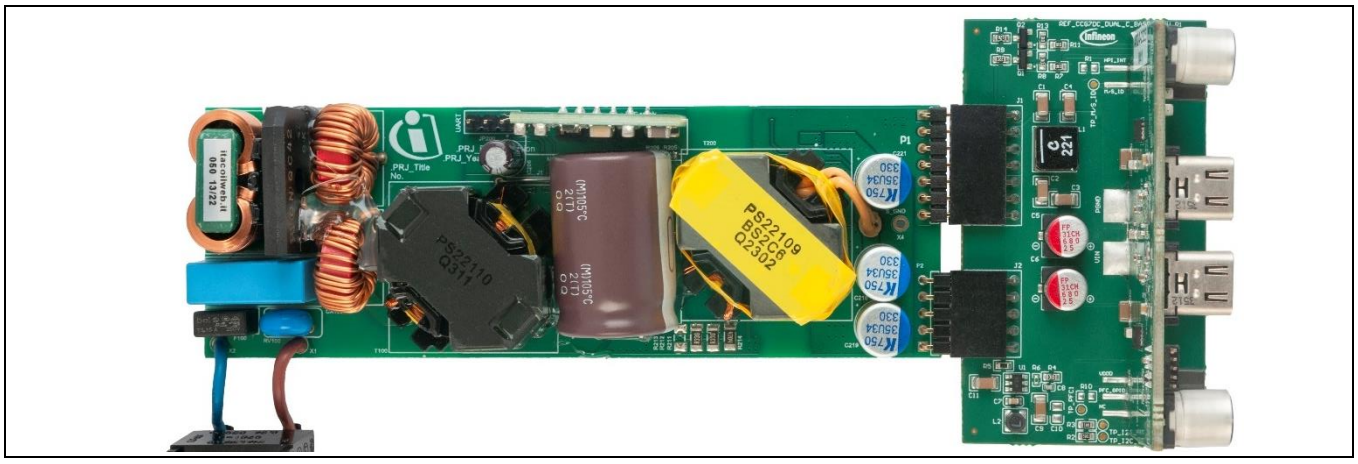


Figure 6 XDPS2221+EZ-PD™ CCG7DC two port 120 W AC/DC charger and adapter

2 CCG7DC multiport charger and adapter solution (REF_CCG7DC_120W_2C) specifications

Table 6 Test specifications

Parameter	Value
Input voltage	5.0 V_{DC}–22.5 V_{DC}
Max output power	120 W system power with baseboard + daughterboard 100 W on each port with a max load current of 5.0 A
Output voltage	• Fixed PDOs: 5.0 V/5.0 A; 9.0 V/5.0 A; 15.0 V/5.0 A; 20.0 V/5.0 A • AVS: 9.0 V to 20 V/5.0 A • PPS: 5.0 V to 16.0 V, 5.0 A; 5.0 V to 21.0 V, 5.0 A (PPS power limited)
Peak efficiency	>98%
Protections	• Input overvoltage protection • Input undervoltage protection • V_{BUS_C} overvoltage protection (OVP) • V_{BUS_C} undervoltage protection (UVP) • Overcurrent protection (OCP) • Short-circuit protection (SCP) • Overtemperature protection (OTP) • V_{BUS_C} to CC short protection
Charging standards supported	• USB-C PD v3.2 including programmable power supply (PPS) mode • Apple charging 2.4 A • Qualcomm QC 2.0, 3.0, 4.0, 5.0 • Samsung AFC • USB BC 1.2

3 Test setup

The REF_CCG7DC_120W_2C solution board, firmware version details, and CCG7DC configuration details are shown in Table 7.

Table 7 DUT hardware and software configurations

DUT contents	Description	Remarks
Hardware configuration		
REF_CCG7DC_120W_2C	Rev.1	Circuit schematics
Firmware		
Firmware version	Power_SDK_4.1	–
CCG7DC configuration		
System clock	24 MHz	Default configuration
Gate drive strength – Pull-up drive strength: LG1 = 2.9 Ω, HG1 = 3.3 Ω Pull-down drive strength: LG1 = 3.1 Ω, HG1 = 3.4 Ω	0x7	Default configuration
Spread spectrum – triangle	10%	Default configuration (nominal switching frequency of 350 kHz)

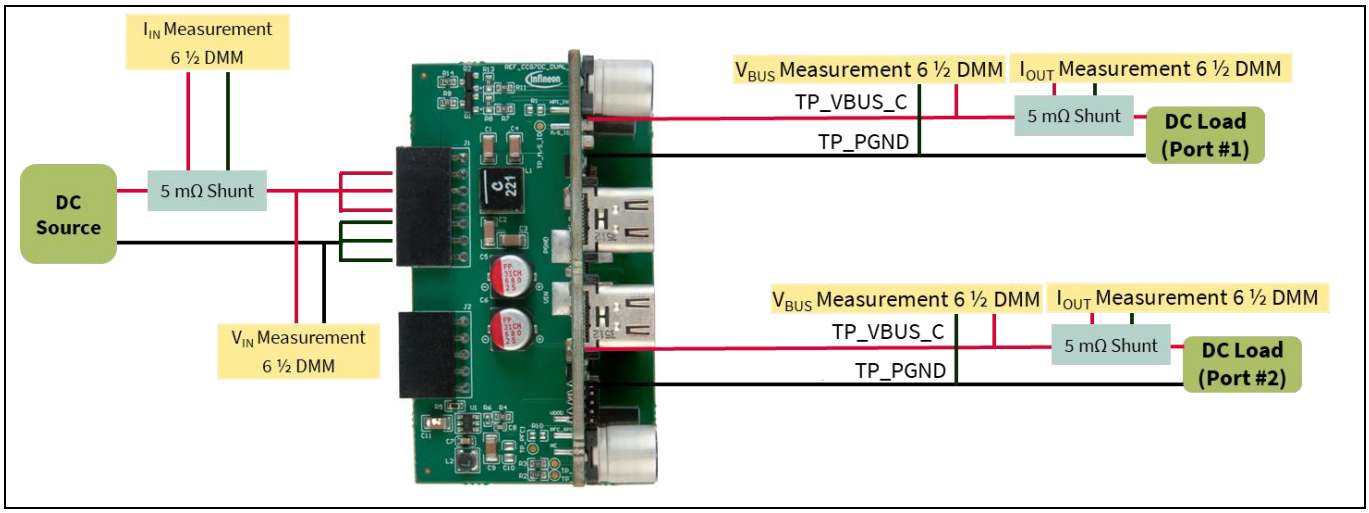


Figure 7 Test equipment connected to the standalone EZ-PD™ CCG7DC multiport charger and adapter solution board

3.1 DUT setup

The DUT is connected to a CY7113 EZ-PD™ PMG1-S3 Prototyping Kit using a USB Type-C cable. Once a successful connection is established, the EZ-PD™ PMG1-S3 UI does a PDO discovery and displays the results.

The REF_CCG7DC_120W_2C solution board is preconfigured with below PDOs:

- **Fixed PDOs:** 5.0 V/5.0 A; 9.0 V/5.0 A; 15.0 V/5.0 A; 20.0 V/5.0 A
- **AVS:** 9.0 V to 20 V/5.0 A
- **PPS:** 5.0 V to 16.0 V, 5.0 A; 5.0 V to 21.0 V, 5.0 A (PPS power limited)

Choose a suitable pre-configured PDO or configure a new one using the EZ-PD™ Configuration Utility. Tests in the following sections use pre-configured PDOs. For more details on PAT tester, see the CY7113 EZ-PD™ PMG1-S3 Prototyping Kit webpage.

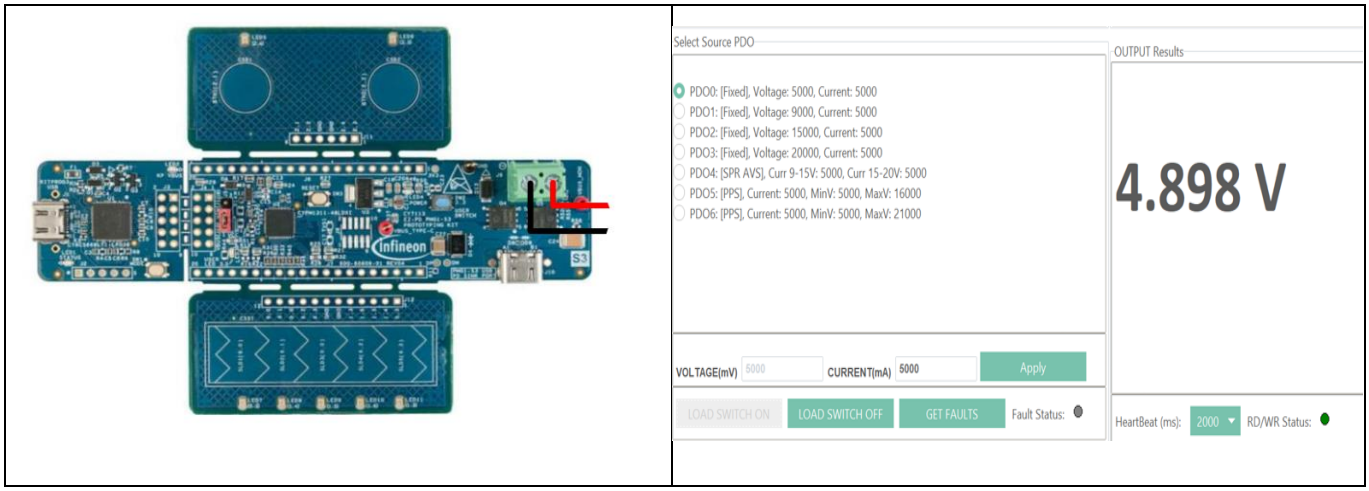


Figure 8 PAT tester and user interface

3.2 Test equipment

The test equipment used to measure the efficiency, ripple, regulation, and transient response are shown in Table 8.

Table 8 Test equipment details

Test setup	Description
Programmable DC source	GwINSTEK PSB 2400L
Oscilloscope	LECROY 8108HD
Data logger ($I_{IN,}$ V_{IN}, V_{BUS}, and I_{OUT})	Keysight 34970 A
Electronic load	GwINSTEK PEL-3021
Input current (I_{IN} and I_{OUT}) measurement shunt	Vishay Y14730R00500B0R
Power meter	Hioki PW3335
AC source	GWinstek ASR2100

4 Single port power management test results of REF_CCG7DC_120W_2C

Following is the efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup section.

Here, only port #1 was loaded with 5 A current.

4.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 9.

Table 9 Peak efficiency

V_{BUS_C} (V)	V_{IN} = 16.5 V	V_{IN} = 22.5 V
05.00 V	95.00% - 2.50 A	94.24% - 3.12 A
09.00 V	96.98% - 3.12 A	96.24% - 3.75 A
12.00 V	97.91% - 2.37 A	97.12% - 3.56 A
15.00 V	98.39% - 2.50 A	97.80% - 3.12 A
20.00 V	–	98.62% - 2.50 A
21.00 V	–	98.84% - 2.81 A

Note: Peak efficiency: 98.84% (At V_{IN} = 22.5 V_{DC}, V_{BUS_C} = 21 V, I_{OUT} = 2.81 A).

Full load efficiency test results are tabulated in Table 10.

Table 10 Full load efficiency

V_{BUS_C} (V)	V_{IN} = 16.5 V	V_{IN} = 22.5 V
5.00 V	94.23% - 5.00 A	93.67%- 5.00 A
9.00 V	96.56% - 5.00 A	96.05% - 5.00 A
12.00 V	97.56% - 4.75 A	97.02% - 4.75 A
15.00 V	98.01% - 5.00 A	97.63% - 5.00 A
20.00 V	–	98.34% - 5.00 A
21.00 V	–	98.62% - 4.50 A

4.2 Efficiency graphs

Efficiency measurements were taken at 22.5 V_{DC} input to the DUT with V_{BUS_C} PDO, PPS voltages of 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and 16.5 V_{DC} input to the DUT with V_{BUS_C} PDO, PPS voltages of 5 V, 9 V, 12 V, 15 V. The port was loaded from 0 A to the maximum rated output current of 5 A. The efficiency and power loss graphs are based on the test setup of Figure 97.

Efficiency and losses at 16.5 V_{DC} input, with V_{BUS_C} 5 V, 9 V, 12 V, 15 V and I_{OUT} 0 A to 5 A maximum on the port is as shown in the Figure 9.

Efficiency and losses at 22.5 V_{DC} input, with V_{BUS_C} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V and I_{OUT} 0 A to 5 A maximum on the port is as shown in the Figure 10.

4.2.1 Efficiency and power losses at 16.5 V_{DC} input

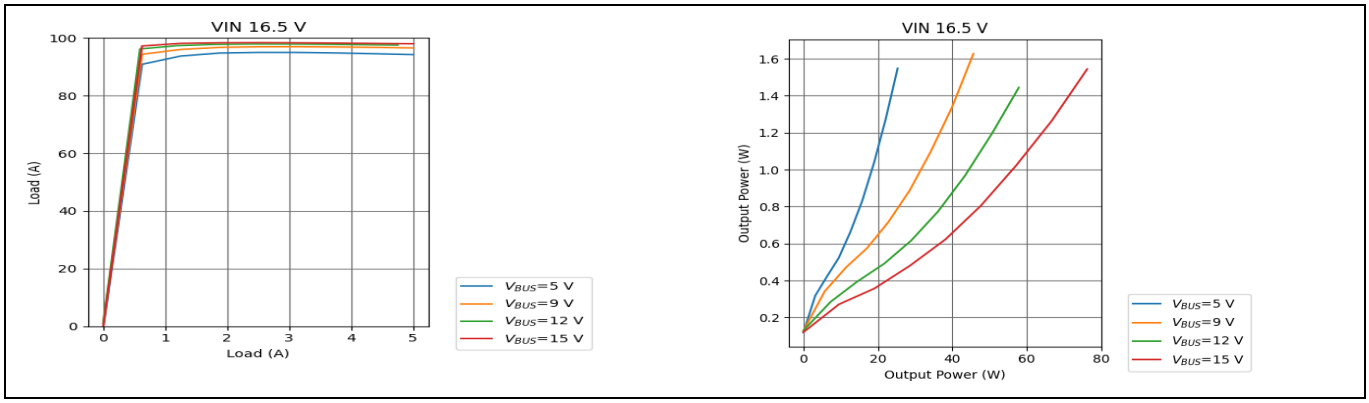


Figure 9 Efficiency and power losses at 16.5 V_{DC} input

4.2.2 Efficiency and power losses at 22.5 V_{DC} input

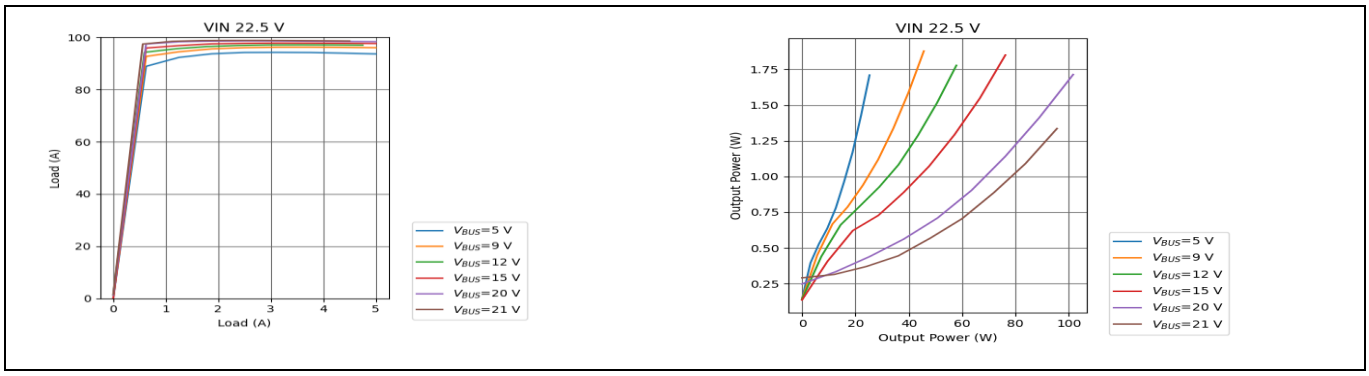


Figure 10 Efficiency and power losses at 22.5 V_{DC} input

4.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

4.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured at 0 A and 5 A load currents are shown in Figure 11 and Figure 12.

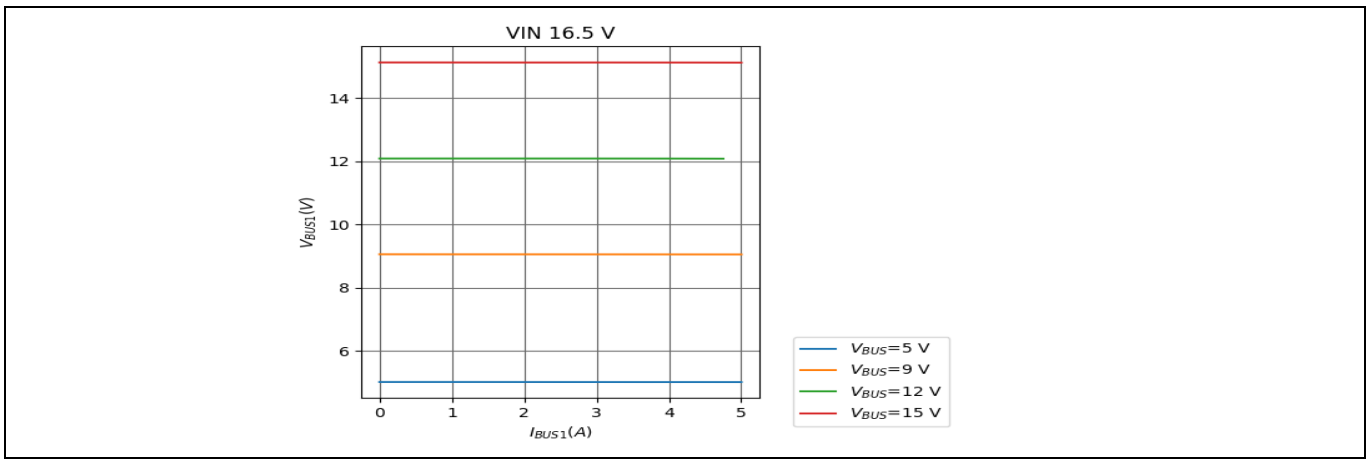


Figure 11 CV regulation at 16.5 V_{DC} input

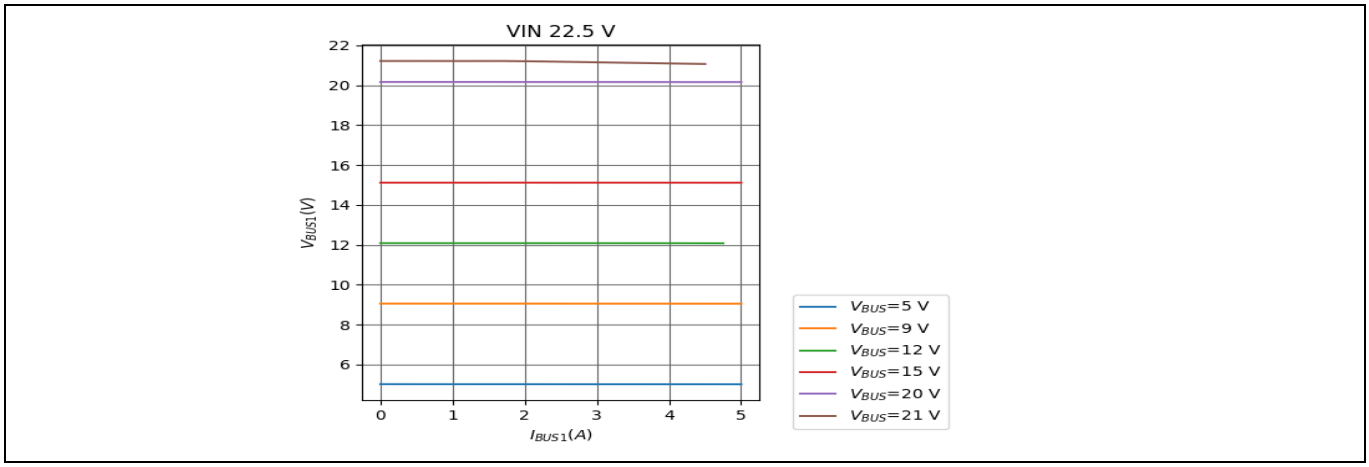


Figure 12 CV regulation at 22.5 V_{DC} input

4.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of port measured at 3 A and 5 A output currents are shown in Figure 13, Figure 14, Figure 15, and Figure 16.

4.3.3 CC regulation curve at 16.5 V_{DC} input and rated output current of 3 A

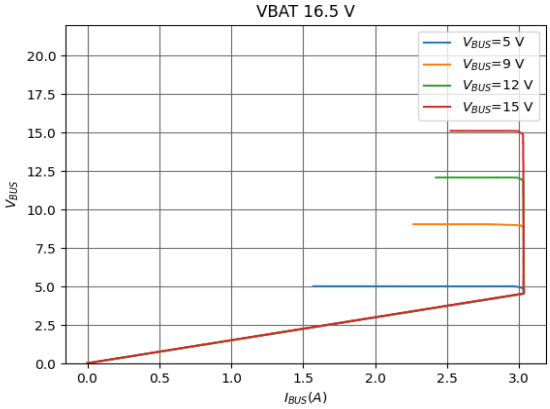


Figure 13 CC regulation curve at 16.5 V_{DC} input and 3 A output current

4.3.4 CC regulation curve at 22.5 V_{DC} input and rated output current of 3 A

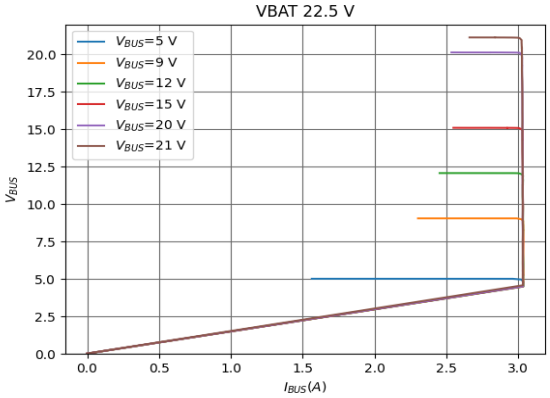


Figure 14 CC regulation curve at 22.5 V_{DC} input and 3 A output current

4.3.5 CC regulation curve at 16.5 V_{DC} input and rated output current of 5 A

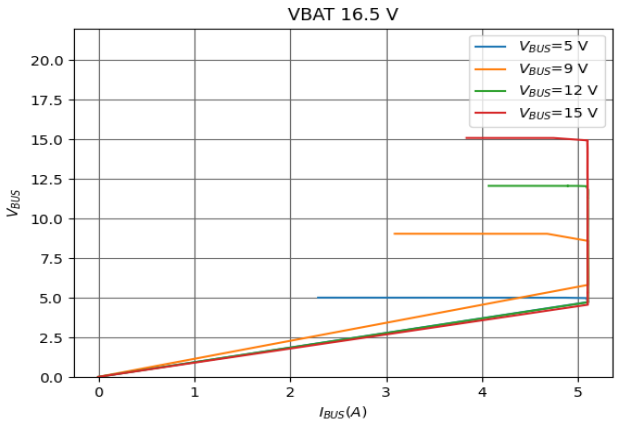


Figure 15 CC regulation curve at 16.5 V_{DC} input and 5 A (full load) output current

4.3.6 CC regulation curve at 22.5 V_{DC} input and rated output current of 5 A

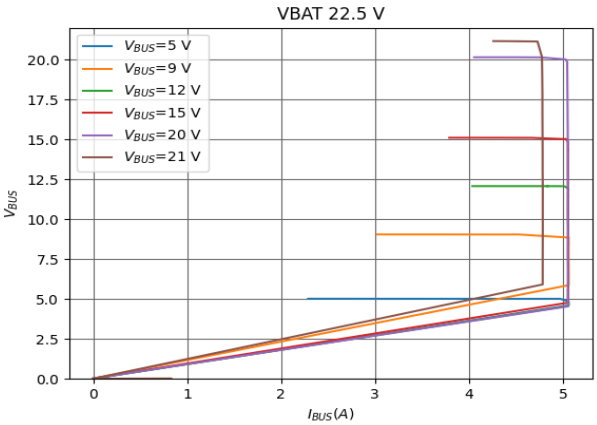


Figure 16 CC regulation curve at 22.5 V_{DC} input and 5 A (full load) output current

4.4 Output voltage regulation

Output voltage regulation measured at V_{IN} = 16.5 V_{DC}, 22.5 V_{DC}, V_{BUS_C} = 5 V, 9 V, 12 V, 15 V, 20 V, 21 V;

I_{OUT} = 0 A and 5 A are shown in Table 11 and Table 12.

Table 11 Regulation at 16.5 V_{DC} input

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 16.5 V % Regulation
0.00	5.005	0.14%
5.00	4.998	
0.00	9.011	0.07%
5.00	9.005	
0.00	12.019	0.03%
4.75	12.015	
0.00	15.037	0.01%
5.00	15.035	

Table 12 Regulation at 22.5 V_{DC} input

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 22.5 V % Regulation
0.00	5.005	0.14%
5.00	4.998	
0.00	9.01	0.05%
5.00	9.005	
0.00	12.018	0.04%
4.75	12.013	
0.00	15.035	0.007%
5.00	15.034	
0.00	20.058	0.04%
5.00	20.049	
0.00	21.043	0.05%
4.50	21.033	

4.5 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors using a short ground loop connected to the probe.

4.5.1 Output voltage ripple measurement test setup

Ripple has been measured using the oscilloscope probe as shown in Figure 17.

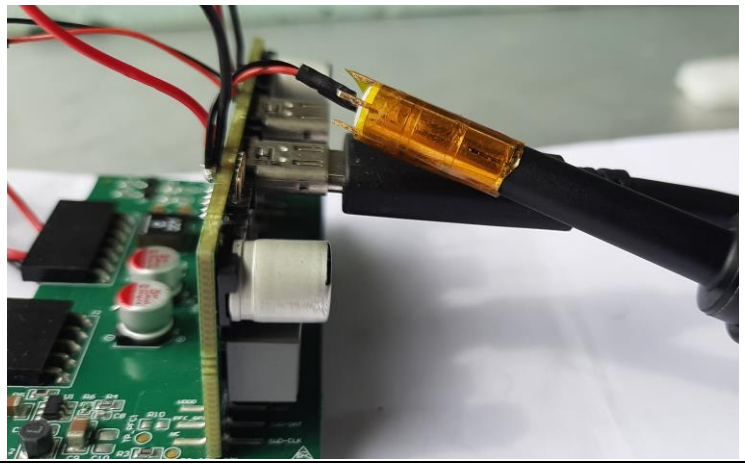


Figure 17 Output voltage ripple measurement test setup

4.5.2 Output voltage ripple peak-to-peak (mV)

Output voltage peak-to-peak ripple is tabulated in Table 13 and Table 14.

Table 13 Peak-to-peak ripple (mV) at V_{IN} = 16.5 V

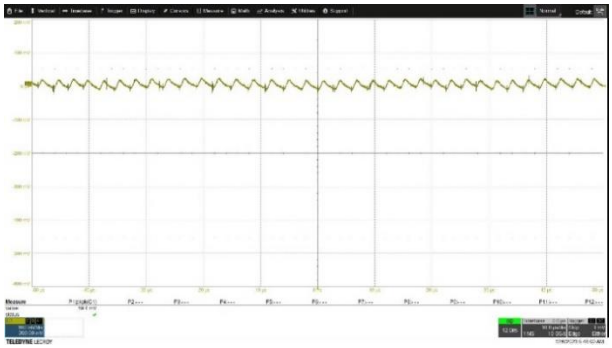
V_{BUS_C} – I_{OUT}	V_{IN} = 16.5 V Ripple (mV)
05.0 V – 0.00 A	46.297
05.0 V – 5.00 A	59.583
09.0 V – 0.00 A	60.47
09.0 V – 5.00 A	55.947
12.0 V – 0.00 A	53.146
12.0 V – 4.75 A	58.761
15.0 V – 0.00 A	49.663
15.0 V – 5.00 A	73.923

Table 14 Peak-to-peak ripple (mV) at V_{IN} = 22.5 V

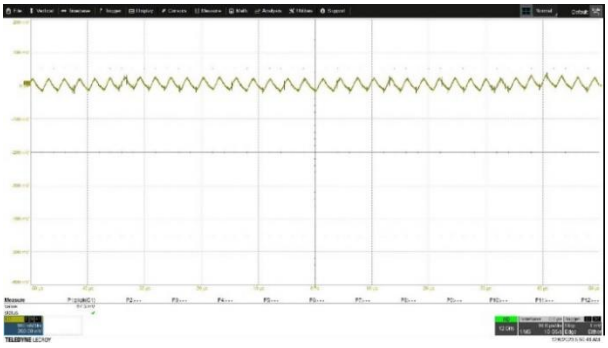
V_{BUS_C} – I_{OUT}	V_{IN} = 22.5 V Ripple (mV)
05 V – 0.00 A	58.697
05 V – 5.00 A	59.352
09 V – 0.00 A	44.305
09 V – 5.00 A	67.319
12 V – 0.00 A	40.347
12 V – 4.75 A	62.05
15 V – 0.00 A	67.498
15 V – 5.00 A	94.225
20 V – 0.00 A	10.704
20 V – 5.00 A	71.7
21 V – 0.00 A	49.792
21 V – 4.75 A	43.47

4.5.3 Output voltage ripple peak-to-peak measurement graphs

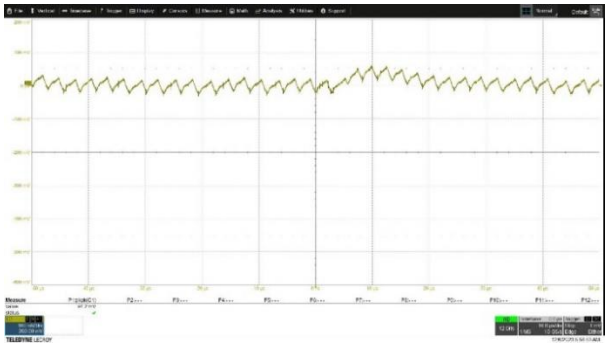
Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 18 and Figure 19.



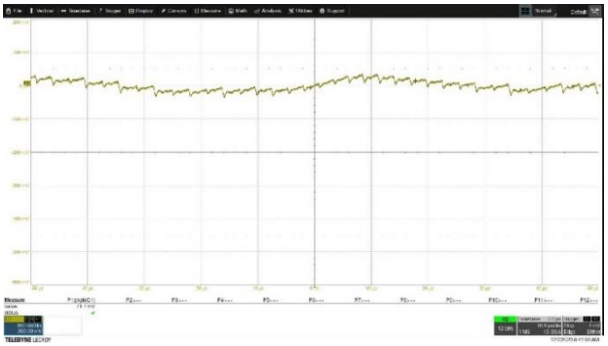
V_{IN}: 22.5 V; V_{BUS_C}: 05 V; I_{OUT}: 5 A



V_{IN}: 22.5 V; V_{BUS_C}: 09 V; I_{OUT}: 5 A

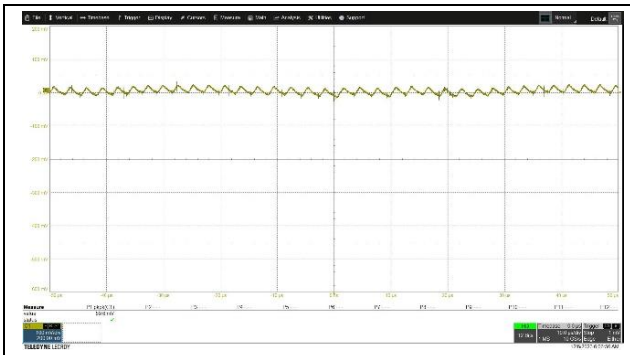


V_{IN}: 22.5 V; V_{BUS_C}: 15 V; I_{OUT}: 5 A

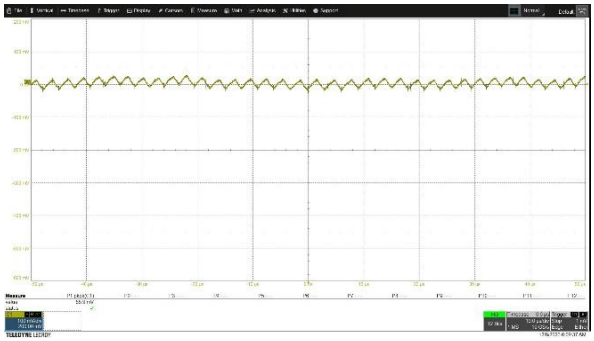


V_{IN}: 22.5 V; V_{BUS_C}: 20 V; I_{OUT}: 5 A

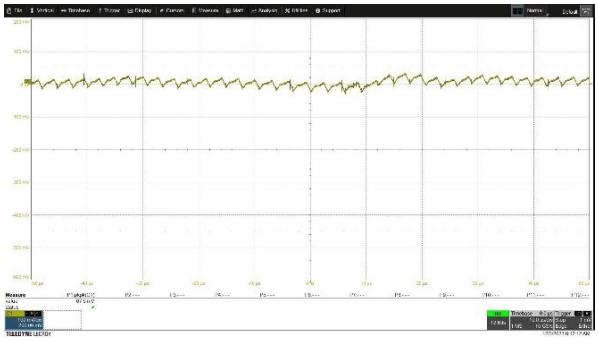
Figure 18 Ripple measurement – input voltage: 22.5 V_{DC} (CH1: V_{BUS_C})



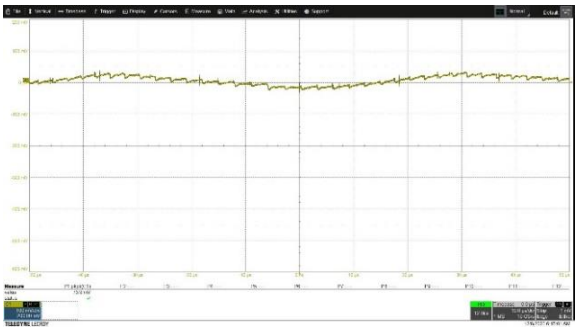
V_{IN}: 16.5 V; V_{BUS_C}: 05 V; I_{OUT}: 5 A



V_{IN}: 16.5 V; V_{BUS_C}: 09 V; I_{OUT}: 5 A



V_{IN}: 16.5 V; V_{BUS_C}: 12 V; I_{OUT}: 4.75 A



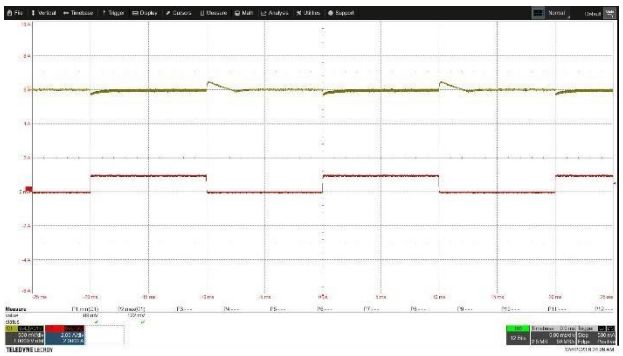
V_{IN}: 16.5 V; V_{BUS_C}:15 V; I_{OUT}: 5 A

Figure 19 Ripple measurement – input voltage: 16.5 V_{DC} (CH1: V_{BUS_C})

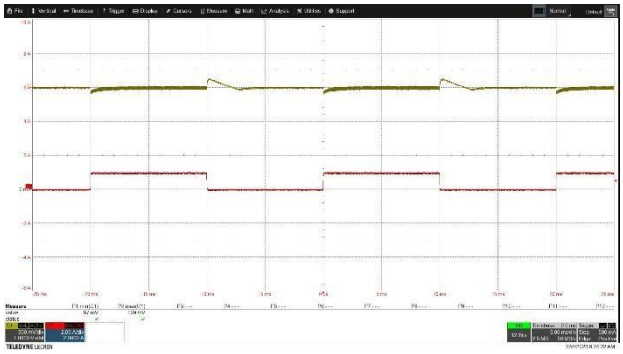
4.6 Output voltage dynamic response waveforms

V_{IN}: 22.5 V, output voltage response when the output current is from 0 A–1 A–0 A is shown in Figure 20.

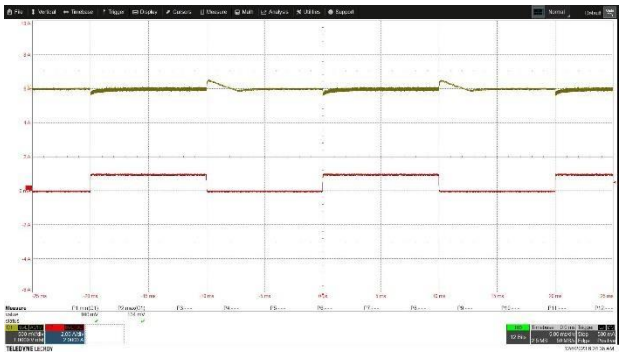
V_{IN}: 22.5 V, output voltage response when the output current is from 3.5 A–4.5 A–3.5 A is shown in Figure 21.



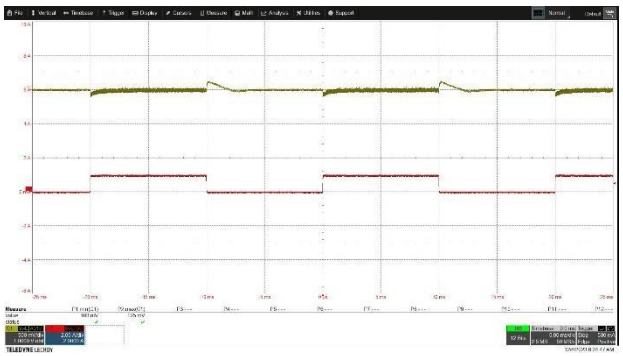
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



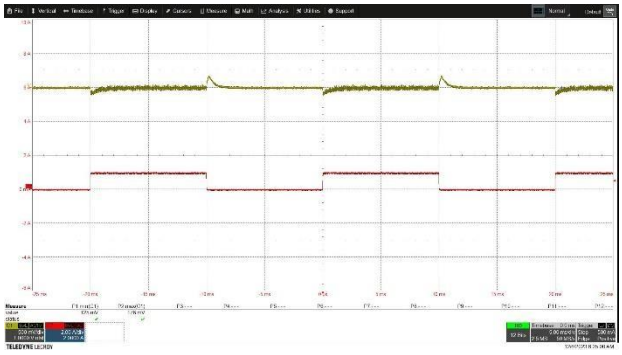
V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

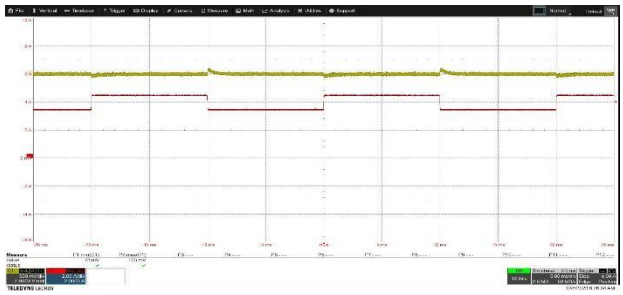


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

Figure 20 Output dynamic response waveforms – input 22.5 V_{DC}; load current transition 0 A to 1 A to 0 A

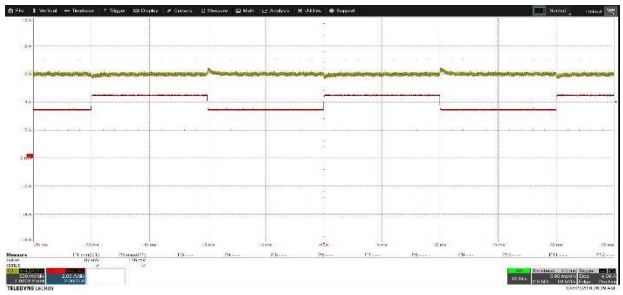
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

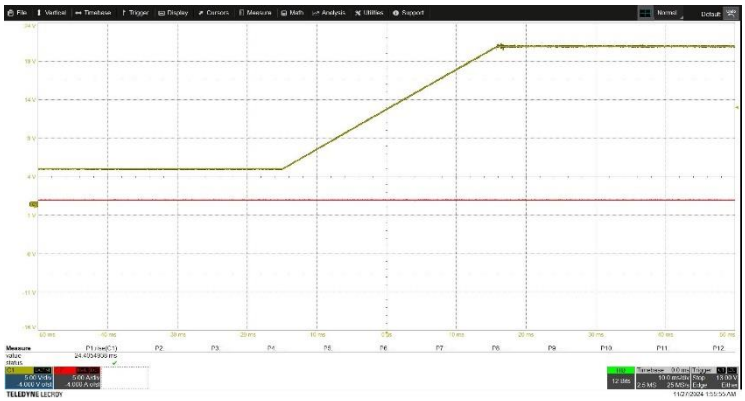


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

Figure 21 Output dynamic response waveforms – input 22.5 V_{DC}; load current transition 3.5 A to 4.5 A to 3.5 A

4.7 Output voltage transition

Output voltage transition at 22.5 V_{DC} input and load 1 A is measured as shown in Figure 22, Figure 23, Figure 24, and Figure 25.

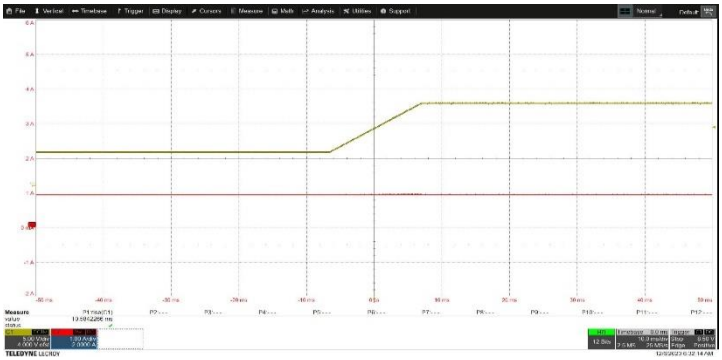


I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 22 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 21.0 V

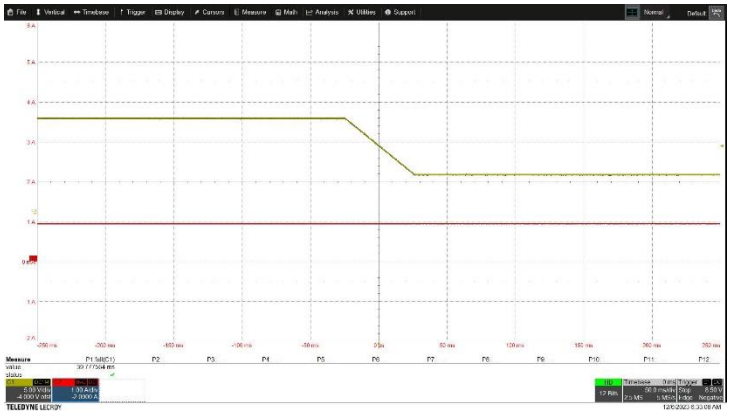
I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 23 Input 22.5 V_{DC}; V_{BUS_C} transition from 21.0 V to 5.0 V



I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 24 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 12 V

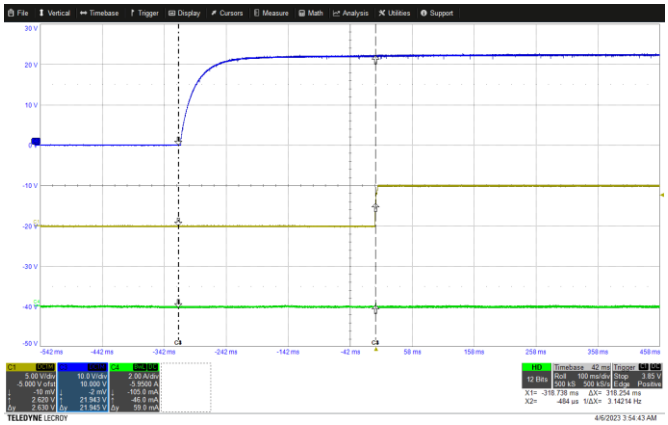


I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 25 Input 22.5 V_{DC}; V_{BUS_C} transition from 12 V to 5 V

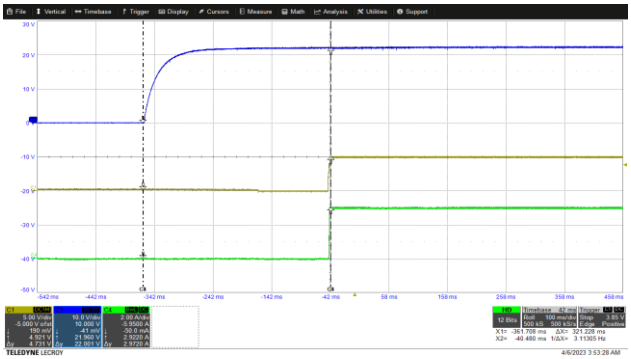
4.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 3-A load as shown in Figure 26 and Figure 27.



CH1: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT}

Figure 26 Input 22.5 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 0 A



CH1: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT}

Figure 27 Input 22.5 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 3 A

4.9 Stress test waveforms

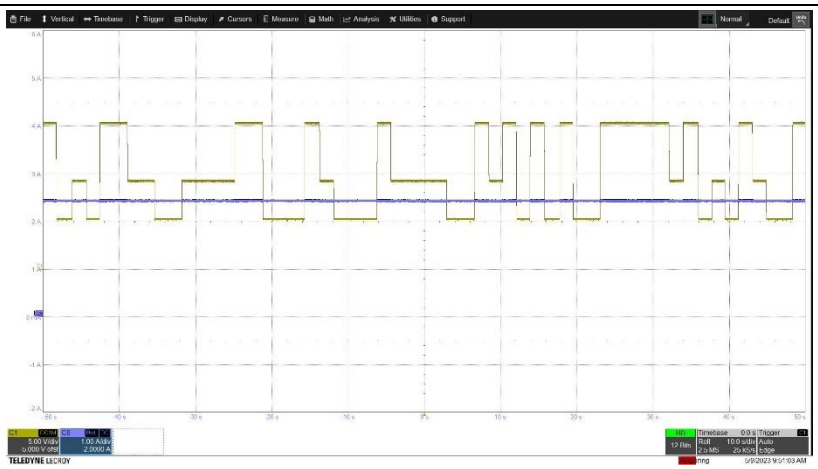
The REF_CCG7DC_120W_2C solution board with one port connected was subjected to electrical stress conditions.

- **Electrical stress test #1** V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5.0 V–21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 4 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 28

CH1: V_{BUS_C}; CH7: I_{OUT}

Figure 28 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5.0 V–21 V (PPS) and vice versa; I_{OUT} = 0 A to 4 A with 1 A step

- **Electrical stress test #2** V_{IN}= 22.5 V_{DC}; V_{BUS_C} – randomly changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A for a duration of 60 minutes. Captured waveforms are shown in Figure 29



CH1: V_{BUS_C}; CH6: I_{OUT}

Figure 29 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A

5 Two port power management test results of REF_CCG7DC_120W_2C

Following is the efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup section. Here, both the ports were loaded with equal amount of current.

5.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 15.

Table 15 Peak efficiency

V_{BUS_C} (V)	V_{IN} = 22.5 V
05.00 V	94.03% - 2*3.12 A
09.00 V	95.93% - 2* 3.12 A
12.00 V	96.82% - 2* 2.85 A
15.00 V	97.47% - 2*3.00 A
20.00 V	98.40% - 2*2.25 A
21.00 V	98.64% - 2*2.06 A

*Note: Peak efficiency: 98.64% (At V_{IN} = 22.5 V_{DC}, V_{BUS_C} = 21 V, I_{OUT} = 2*2.06 A).*

Full load efficiency test results are tabulated in Table 16.

Table 16 Full load efficiency

V_{BUS_C} (V)	V_{IN} = 22.5 V
05.00 V	93.35% - 2*5.00 A
09.00 V	95.50% - 2*5.00 A
12.00 V	96.82% - 2*2.85 A
15.00 V	97.40% - 2*4.00 A
20.00 V	98.38% - 2*3.00 A
21.00 V	98.61% - 2*2.75 A

5.2 Efficiency graphs

Efficiency measurements were taken at 22.5 V_{DC} input to the DUT; V_{BUS_C} PDO, PPS voltages are 5 V, 9 V, 12 V, 15 V, 20 V, and 21 V for both the ports.

Each port was loaded from 0 A to the maximum output current to make total system power 120 W. The efficiency is based on the test setup of Figure 97.

5.2.1 Efficiency at 22.5 V_{DC} input

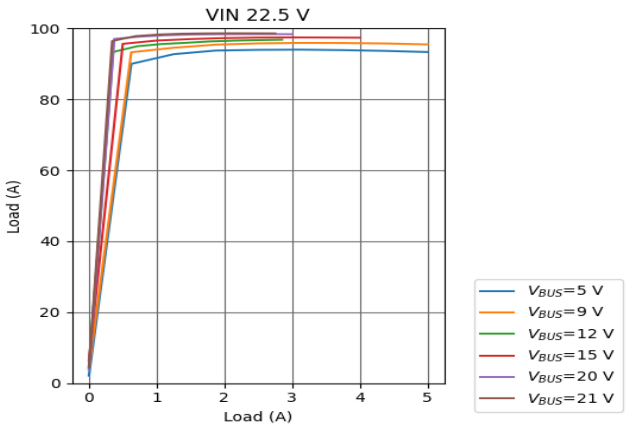


Figure 30 Efficiency at 22.5 V_{DC} input

5.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

5.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A to maximum load currents that each port can take to have maximum system power of 120 W, is shown in Figure 31 and Figure 32.

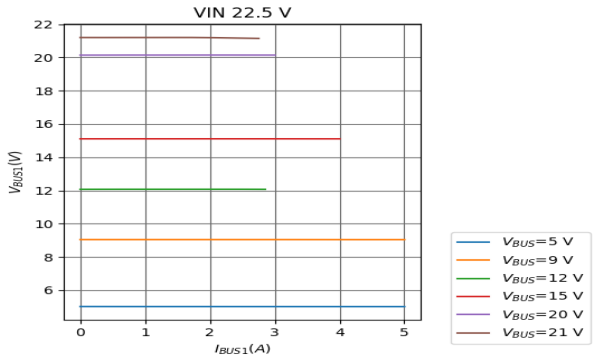


Figure 31 CV regulation at 22.5 V_{DC} input port #1

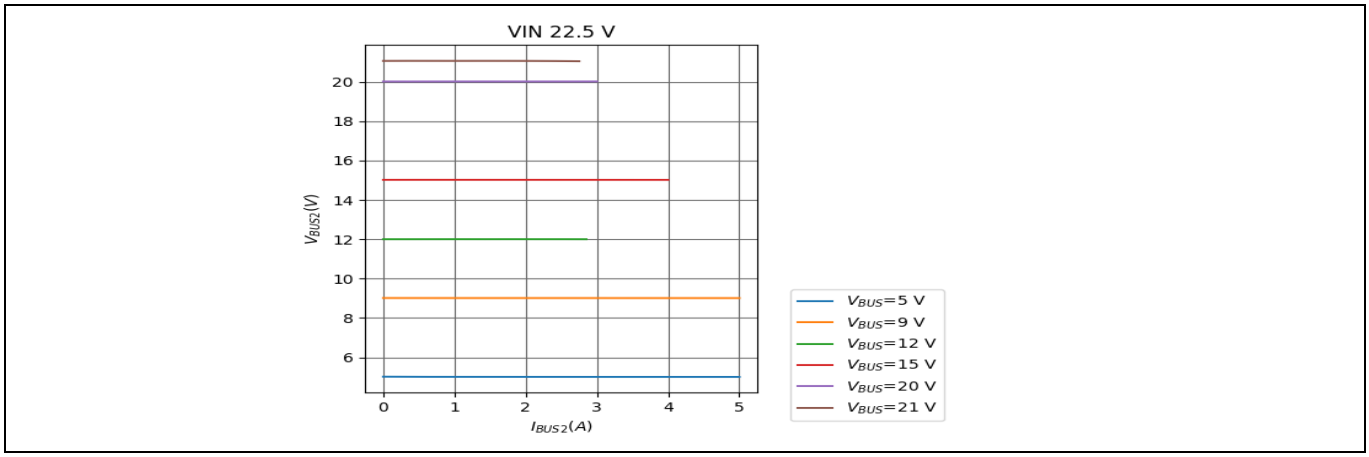


Figure 32 CV regulation 22.5 V_{DC} input port #2

5.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of each port measured at 1.5 A output current is shown in Figure 33.

5.3.3 CC regulation curve at 22.5 V_{DC} input and rated output current of 1.5 A

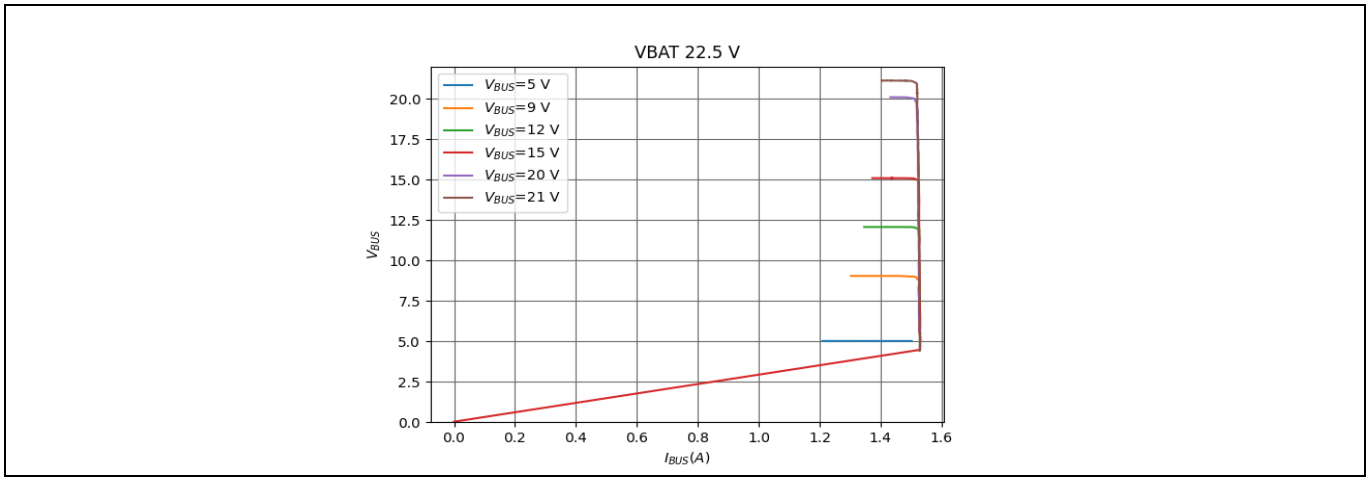


Figure 33 CC regulation curve at 22.5 V_{DC} input and 1.5 A output current

5.4 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors using a short ground loop connected to the probe.

5.4.1 Output voltage ripple peak-to-peak (mV)

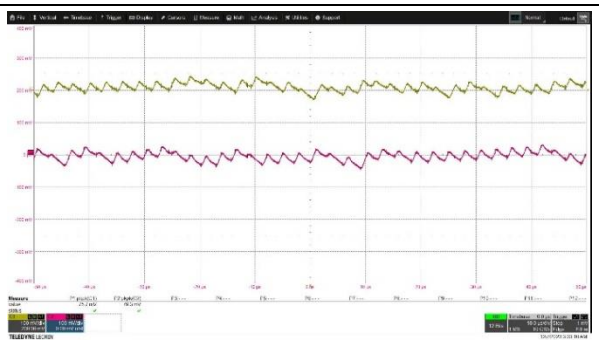
Output voltage peak-to-peak ripple is tabulated in Table 17.

Table 17 Peak-to-peak ripple (mV) at 22.5 V input

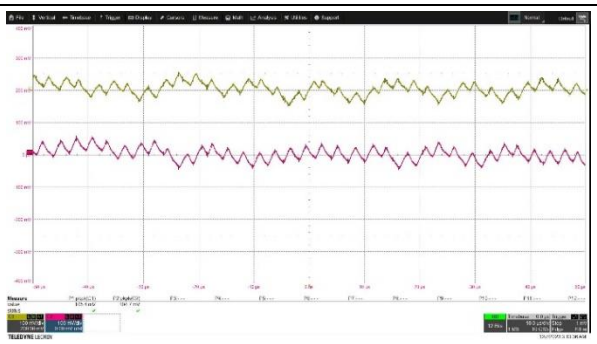
V_{BUS_C} - I_{OUT}	Port #1 ripple (mV)	Port #2 ripple (mV)
05.0 V – 0.00 A	21.18	15.61
05.0 V – 5.00 A	75.72	79.32
09.0 V – 0.00 A	21.83	14.07
09.0 V – 5.00A	105.44	104.66
12.0 V – 0.00 A	51.45	66.12
12.0 V – 2.85 A	84.15	106.73
15.0 V – 0.00 A	55.18	64.53
15.0 V – 4.00 A	119.88	113.71
20.0 V – 0.00 A	24.65	29.25
20.0 V – 3.00 A	67.71	76.18
21.0 V – 0.00 A	47.13	39.95
21.0 V – 2.75 A	55.54	46.66

5.4.2 Output voltage ripple peak-to-peak measurement graphs

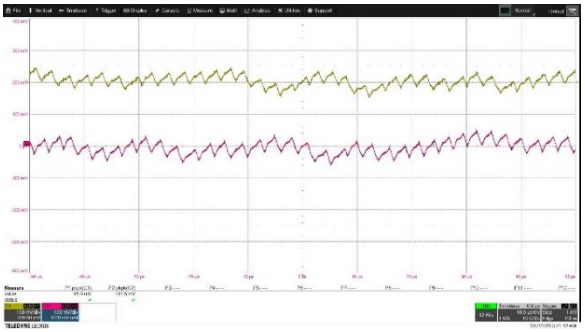
Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 34.



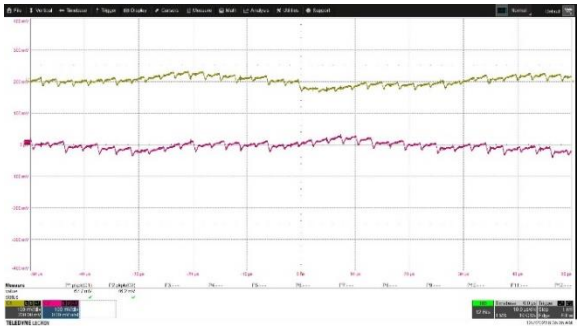
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 5 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); I_{OUT}: 5 A



Port #1 V_{BUS_C}: 15 V (CH1); port #2 V_{BUS_C}: 15 V (CH2); I_{OUT}: 4 A



Port #1 V_{BUS_C}: 20 V (CH1); port #2 V_{BUS_C}: 20 V (CH2); I_{OUT}: 3 A

Figure 34 Ripple measurement – input voltage = 22.5 V_{DC}

5.5 Output voltage regulation

Output voltage regulation measured at V_{IN}= 22.5 V_{DC}, V_{BUS_C}= 5 V, 9 V, 12 V, 15 V, 20 V, 21 V and I_{OUT} = 0 A to maximum current is shown in Table 18.

Table 18 Regulation at 22.5 V_{AC} input

I_{OUT} (A)	Port #1 V_{BUS_C} (V_{DC})	Port #1 % Regulation	I_{OUT} (A)	Port #2 V_{BUS_C} (V_{DC})	Port #2 % Regulation
0.00	5.005	0.120%	0.00	5.02	0.239%
5.00	4.999		5.00	5.008	
0.00	9.011	0.055%	0.00	9.03	0.066%
5.00	9.006		4.40	9.024	
0.00	12.025	0.008%	0.00	12.037	0.075%
2.85	12.024		2.56	12.028	
0.00	15.048	0.007%	0.00	15.047	0.020%
4.00	15.042		2.66	15.044	
0.00	20.056	0.029%	0.00	20.088	0.030%
3.00	20.05		2.00	20.082	

5.6 Output voltage dynamic response waveforms

At V_{IN} = 22.5 V, output voltage response when the output current is from 0 A–1 A–0 A is shown in Figure 35.

Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

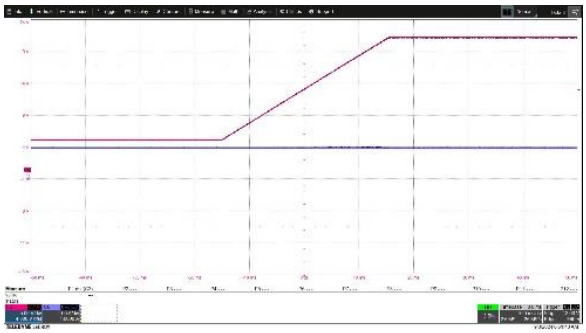
Port #1 V_{BUS_C}: 15 V (CH1); port #2 V_{BUS_C}: 15 V(CH2); I_{OUT}: 0 A to 1 A to 0 A

Port #1 V_{BUS_C}: 20 V (CH1); port #2 V_{BUS_C}: 20 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

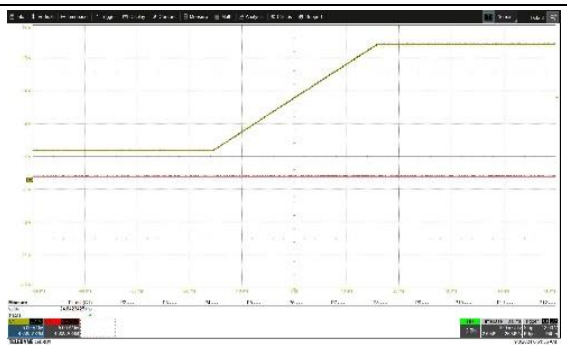
Figure 35 Output dynamic response waveforms - input 22.5 V_{DC}; load current transition 0 A to 1 A to 0 A

5.7 Output voltage transition

Output voltage transition at 22.5 V_{DC} input and load 1 A is measured as shown in Figure 36, Figure 37, and Figure 38.



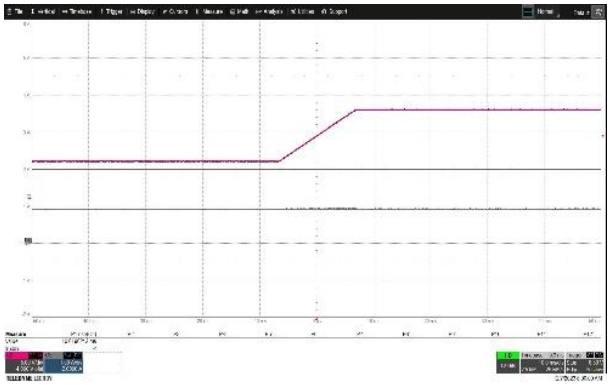
Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH7: I_{OUT})



Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH5: I_{OUT})

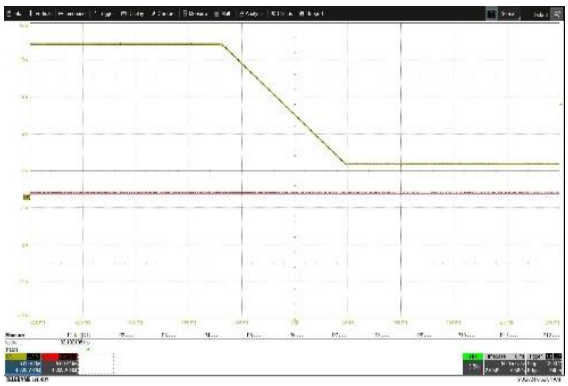
Figure 36 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 21 V

Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH7: I_{OUT})

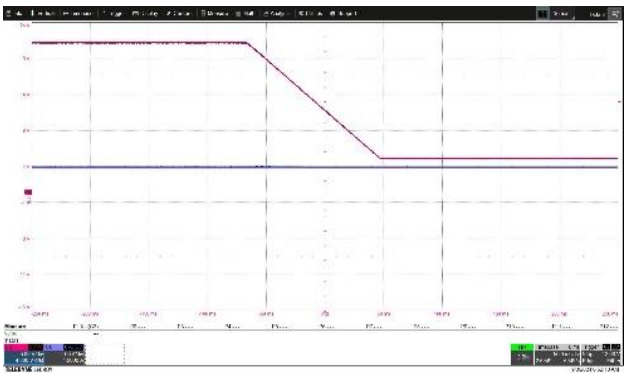


Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH5: I_{OUT})

Figure 37 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 12 V



Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

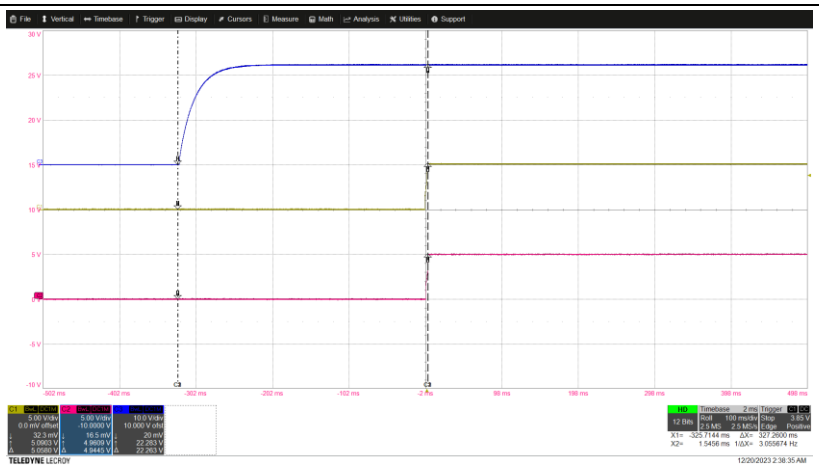


Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT})

Figure 38 Input 22.5 V_{DC}; V_{BUS_C} transition from 21 V to 5.0 V

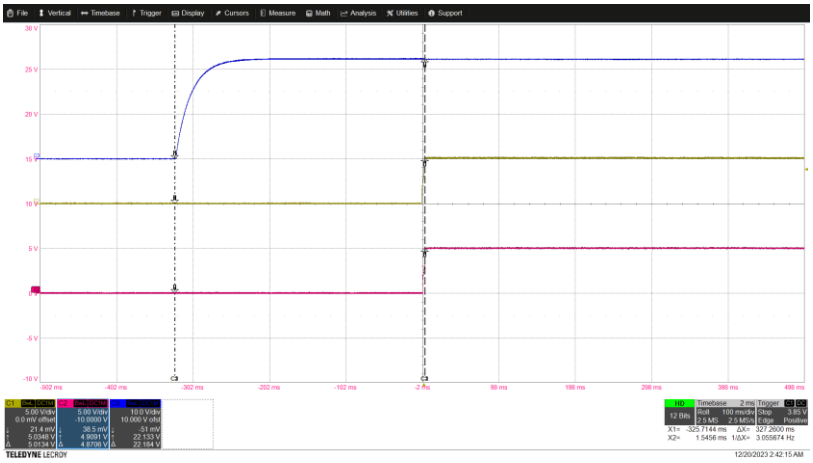
5.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load is shown in Figure 39 and Figure 40.



CH1: port #1 V_{BUS_C}; CH2: port #2 V_{BUS_C}; CH3: V_{IN}

Figure 39 Input 230 V_{AC}; V_{BUS_C}: 5 V; I_{OUT}: 0 A



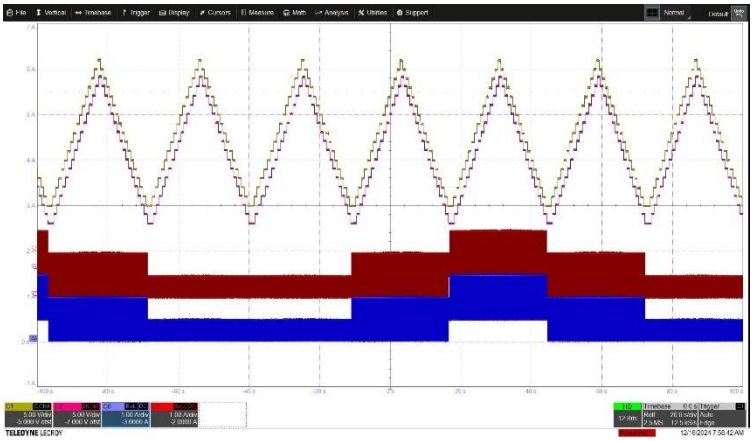
CH1: port #1 V_{BUS_C}; CH2: port #2 V_{BUS_C}; CH3: V_{IN}

Figure 40 Input 230 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 1 A

5.9 Stress test waveforms

The REF_CCG7DC_120W_2C solution board with two ports connected was subjected to the following electrical stress conditions:

- **Electrical stress test #1** V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5.0 V–21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 41



CH1: port #1 V_{BUS_C}; CH7: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH6: port #2 I_{OUT}

Figure 41 V_{IN} = 22.5 V_{DC}; V_{BUS_C}: continuously changing from 5.0 V–21 V (PPS) vice versa; I_{OUT} = 0 to 4 A with 1 A step

- **Electrical stress test #2** V_{IN} = 22.5 V_{DC}; V_{BUS_C}: randomly changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A for a duration of 60 minutes. Captured waveforms are shown in Figure 42

CH1: port #1 V_{BUS_C}; CH6: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH5: port #2 I_{OUT}

Figure 42 V_{IN} = 22.5 V_{DC}; V_{BUS_C}: continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A

6 Single port power management test results of XDPS2221+REF_CCG7DC_120W_2C

Following is the efficiency captured by connecting XDPS2221 to REF_CCG7DC_120W_2C. Here, only port #1 was loaded with 5 A current.

6.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 19.

Table 19 Peak efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
05.0 V	89.23% - 3.75 A	89.62% - 3.75 A
09.0 V	90.93% - 4.37 A	92.59% - 4.37 A
12.0 V	92.37% - 4.20 A	93.46% - 4.20 A
15.0 V	92.61% - 4.37 A	93.93% - 3.75 A
20.0 V	93.99% - 4.37 A	95.45% - 3.75 A
21.0 V	92.79% - 4.50 A	94.07% - 4.50 A

Note: Peak efficiency: 95.45% (At V_{IN} = 230 V_{AC}, V_{BUS_C} = 20 V, I_{OUT} = 3.75 A).

Full load efficiency test results are tabulated in Table 20.

Table 20 Full load efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
05.00 V	88.90% - 5.00 A	89.61% - 5.00 A
09.00 V	90.79% - 5.00 A	92.44% - 5.00 A
12.00 V	92.18% - 4.80 A	93.40% - 4.80 A
15.00 V	92.56% - 5.00 A	93.49% - 5.00 A
20.00 V	93.89% - 5.00 A	94.59% - 5.00 A
21.00 V	92.79% - 4.50 A	94.07% - 4.50 A

Four-point efficiency average test results are tabulated in Table 21.

Table 21 Efficiency 4-pt average

Parameter	DOE level VI limit	EU (CoC) Tier 2	Unit	Test conditions	Test results (%)	
					230 V/50 Hz	Remarks
Four-point average efficiency (Average of 25%, 50%, 75%, and 100% load)	84.25	85.00	%	V_{BUS} = 05.0 V; I_{OUT} = 5.00 A	88.48 %	Pass
	87.73	88.85	%	V_{BUS} = 09.0 V; I_{OUT} = 5.00 A	91.36 %	Pass
	88.00	89.00	%	V_{BUS} = 12.0 V; I_{OUT} = 4.75 A	92.08 %	Pass
	88.00	89.00	%	V_{BUS} = 15.0 V; I_{OUT} = 5.00 A	92.53 %	Pass
	88.00	89.00	%	V_{BUS} = 20.0 V; I_{OUT} = 5.00 A	93.41 %	Pass
	88.00	89.00	%	V_{BUS} = 21.0 V; I_{OUT} = 4.50 A	91.68 %	Pass

6.2 Efficiency graphs

Efficiency measurements were taken at 115 V/60 Hz, and 230 V/50 Hz AC input to the DUT; V_{BUS_C} PDO, PPS voltages are 5 V, 9 V, 12 V, 15 V, 20 V, and 21 V. The port was loaded from 0 A to the maximum rated output current of 5 A.

Efficiency and power losses at 230 V AC input, V_{BUS_C} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 5 A maximum on the port is shown in Figure 43.

Efficiency and power losses at 115 V AC input, V_{BUS_C} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 5 A maximum on the port is shown in Figure 44.

6.2.1 Efficiency at 230 V_{AC} input and 50 Hz frequency

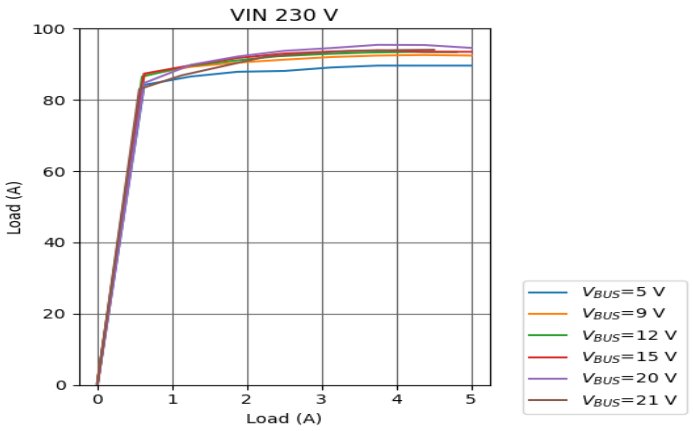


Figure 43 Efficiency and power losses at 230 V_{AC} input

6.2.2 Efficiency at 115 V_{AC} input and 60 Hz frequency

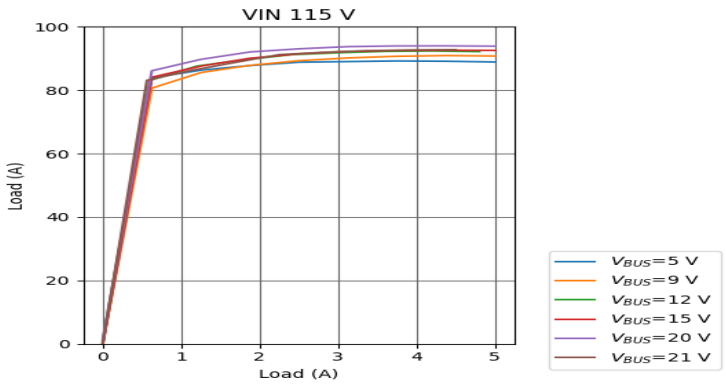


Figure 44 Efficiency and power losses at 115 V_{AC} input

6.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

6.3.1 Output voltage regulation (CV mode)

The output constant voltage regulation (CV mode) measured from 0 A and 5 A load currents are as shown in Figure 45 and Figure 46.

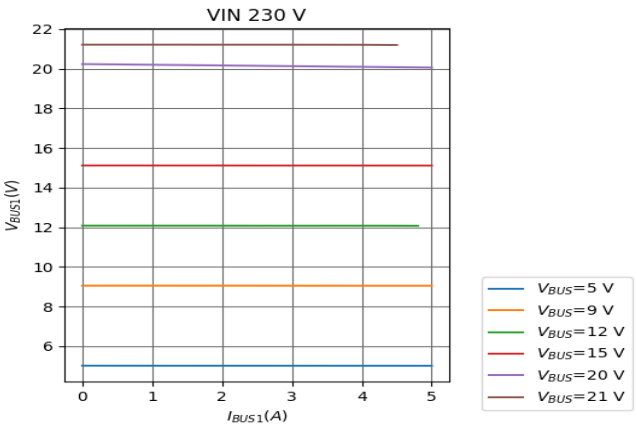


Figure 45 CV regulation at 230 V_{AC} input

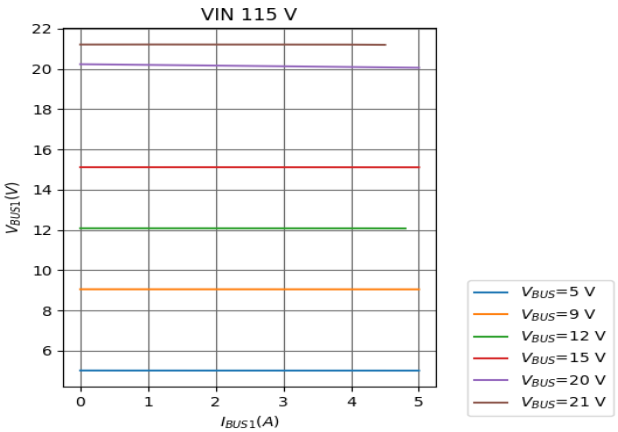


Figure 46 CV regulation at 115 V_{AC} input

6.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of port measured at 3 A and 5 A output currents is shown in Figure 47 and Figure 48.

6.3.3 CC regulation curve at 230 V_{AC} input, 50 Hz frequency and rated output current of 3 A

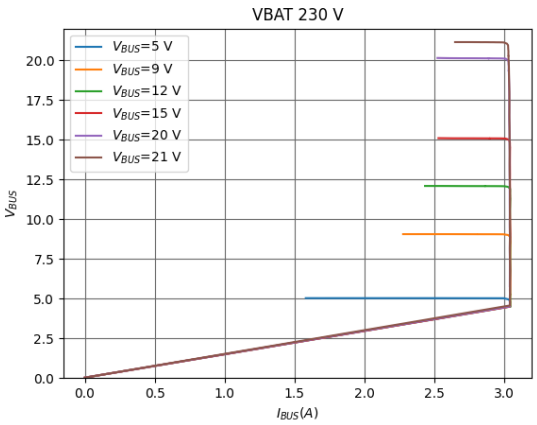


Figure 47 CC regulation curve at 230 V_{AC} input and 3 A output current

6.3.4 CC regulation curve at 230 V_{AC} input, 50 Hz frequency and rated output current of 5 A

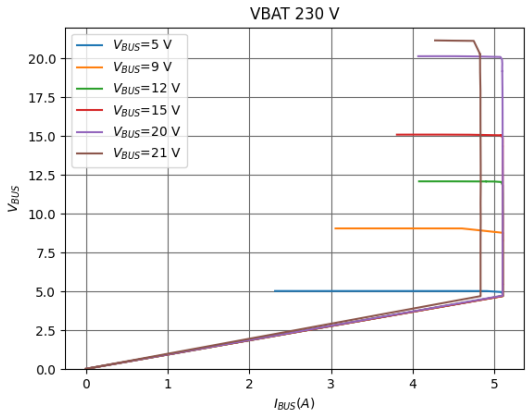


Figure 48 CC regulation curve at 230 V_{AC} input and 5 A output current

6.4 Output voltage regulation

Output voltage regulation measured at V_{IN} = 230 V_{AC} and 115 V_{AC}, V_{BUS_C}: 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} = 0 A and 5 A is shown in Table 22.

Table 22 Regulation at V_{IN} = 230 V_{AC}

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 230 V_{AC} % Regulation	I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 115 V_{AC} % Regulation
0.00	5.022821	0.11%	0.00	5.022584	0.12%
5.00	5.017409		4.75	5.016709	
0.00	9.058319	0.039%	0.00	9.057114	0.049%
5.00	9.054725		4.75	9.052594	
0.00	12.087863	0.07%	0.00	12.085916	0.066%
4.80	12.079316		4.80	12.077909	
0.00	15.12057	0.035%	0.00	15.118514	0.032%
5.00	15.11516		5.00	15.113646	
0.00	20.236464	0.877%	0.00	20.234191	0.872%
5.00	20.060431		5.00	20.059132	
0.00	21.214979	0.073%	0.00	21.21249	0.067%
4.50	21.199399		4.50	21.1981	

6.5 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors using a short ground loop connected to the probe.

6.5.1 Output voltage ripple peak-to-peak (mV)

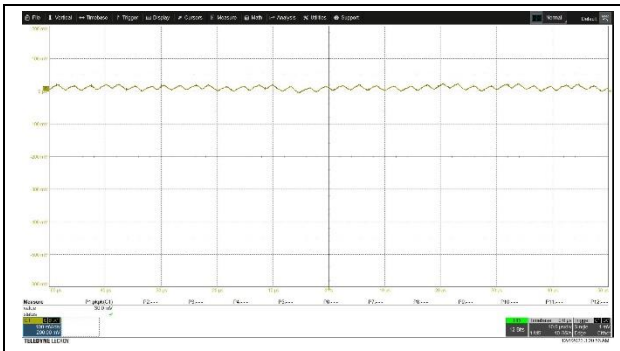
Output voltage peak-to-peak ripple tabulated in Table 23.

Table 23 Peak-to-peak ripple (mV) at 115 V_{AC} and 230 V_{AC}

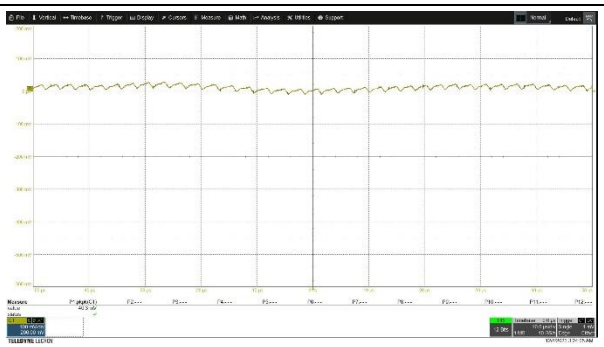
V_{BUS_C} - I_{OUT}	V_{IN} = 115 V_{AC} Ripple (mV)	V_{BUS_C} - I_{OUT}	V_{IN} = 230 V_{AC} Ripple (mV)
05.0 V – 0.00 A	7.453	05.0 V – 0.00 A	7.401
05.0 V – 5.00 A	27.768	05.0 V – 5.00 A	30.042
09.0 V – 0.00 A	11.141	09.0 V – 0.00 A	9.008
09.0 V – 5.00 A	65.738	09.0 V – 5.00 A	40.296
12.0 V – 0.00 A	11.693	12.0 V – 0.00 A	14.006
12.0 V – 4.75 A	84.498	12.0 V – 4.75 A	57.656
15.0 V – 0.00 A	17.925	15.0 V – 0.00 A	15.548
15.0 V – 5.00 A	132.761	15.0 V – 5.00 A	99.648
20.0 V – 0.00 A	52.811	20.0 V – 0.00 A	20.084
20.0 V – 5.00 A	69.76	20.0 V – 5.00 A	55.497
21.0 V – 0.00 A	22.782	21.0 V – 0.00 A	23.515
21.0 V – 4.50 A	108.437	21.0 V – 4.50 A	107.897

6.5.2 Output voltage ripple peak-to-peak measurement graph

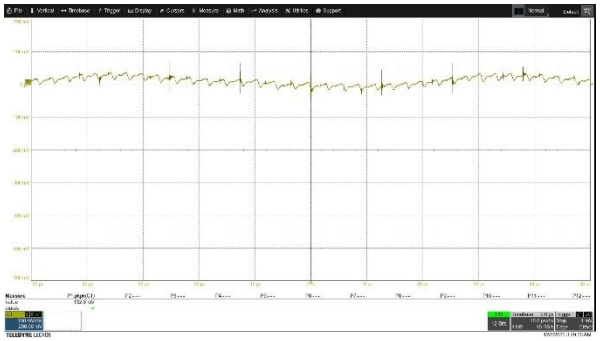
Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 49 and Figure 50.



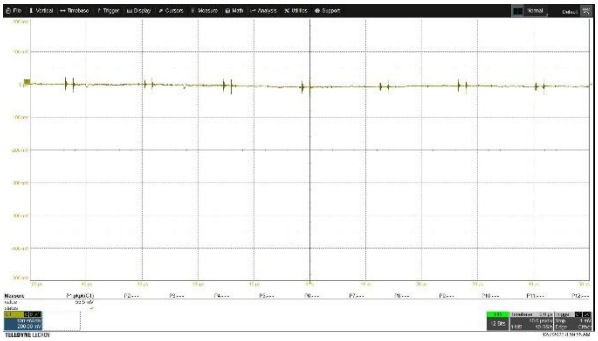
V_{IN}: 230 V_{AC}; V_{BUS_C}: 05 V, I_{OUT}: 5 A



V_{IN}: 230 V_{AC}; V_{BUS_C}: 09 V, I_{OUT}: 5 A

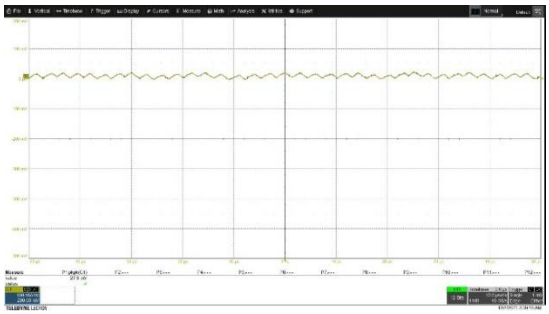


V_{IN}: 230 V_{AC}; V_{BUS_C}: 15 V, I_{OUT}: 5 A

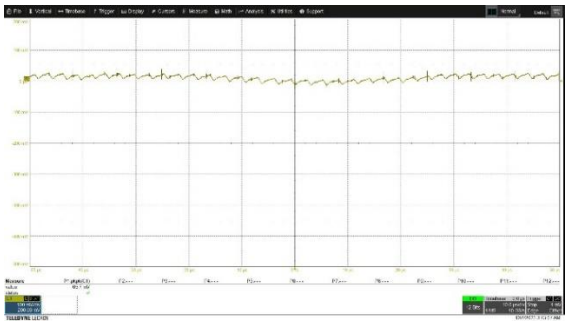


V_{IN}: 230 V_{AC}; V_{BUS_C}: 20 V, I_{OUT}: 5 A

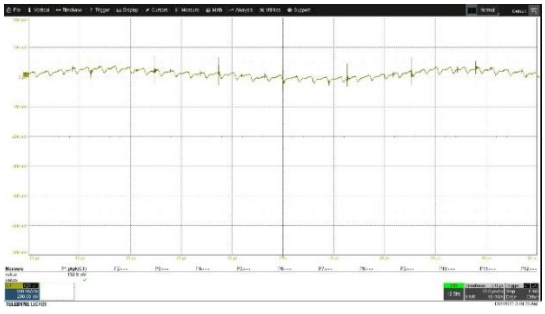
Figure 49 Ripple measurement – input voltage = 230 V_{AC} (CH1: V_{BUS_C})



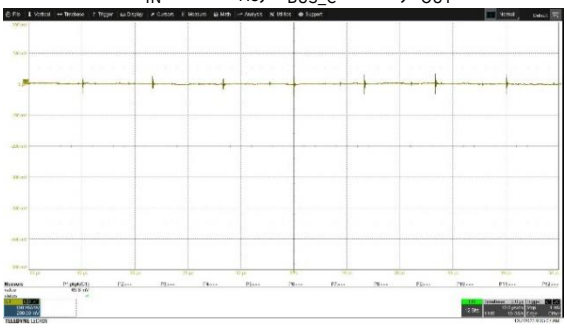
V_{IN}: 115 V_{AC}; V_{BUS_C}: 05 V, I_{OUT}: 5 A



V_{IN}: 115 V_{AC}; V_{BUS_C}: 09 V, I_{OUT}: 5 A



V_{IN}: 115 V_{AC}; V_{BUS_C}: 15 V, I_{OUT}: 5 A



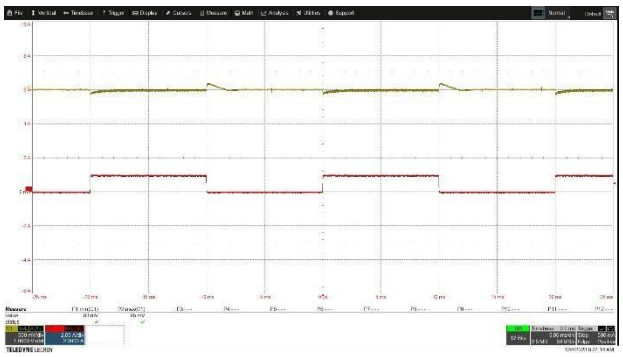
V_{IN}: 115 V_{AC}; V_{BUS_C}: 20 V, I_{OUT}: 5 A

Figure 50 Ripple measurement – input voltage = 115 V_{AC} (CH1: V_{BUS_C})

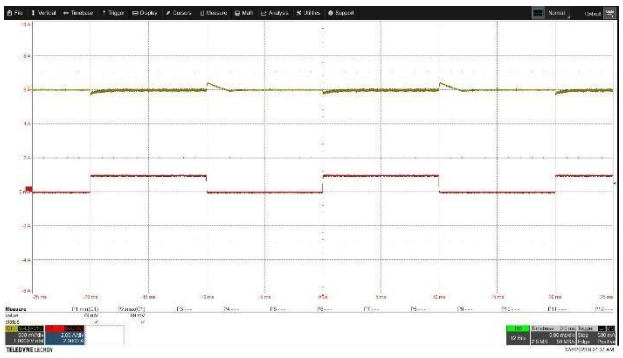
6.6 Output voltage dynamic response waveforms

At V_{IN} = 230 V_{AC}/50 Hz, output voltage response when the output current is from 0 A–1 A–0 A, is as shown in Figure 51.

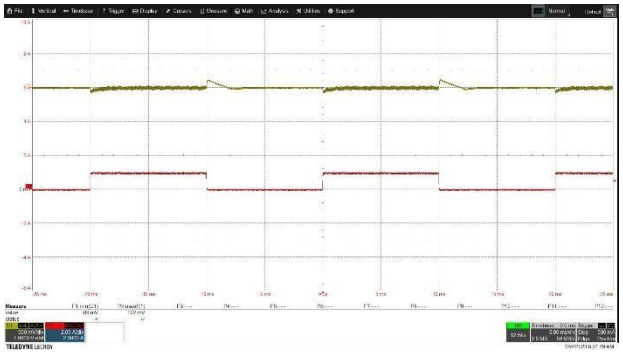
At V_{IN} = 115 V_{AC}/60 Hz, output voltage response when the output current is from 3.5 A–4.5 A–3.5 A is as shown in Figure 52.



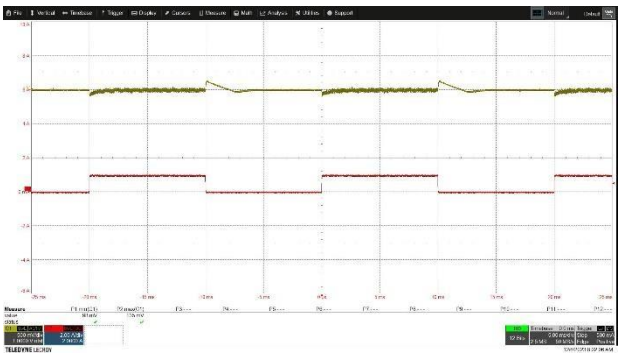
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



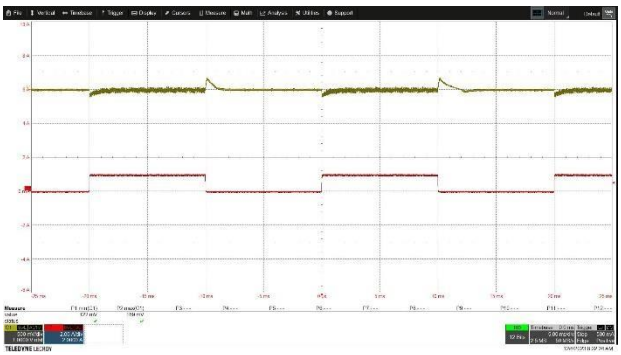
V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



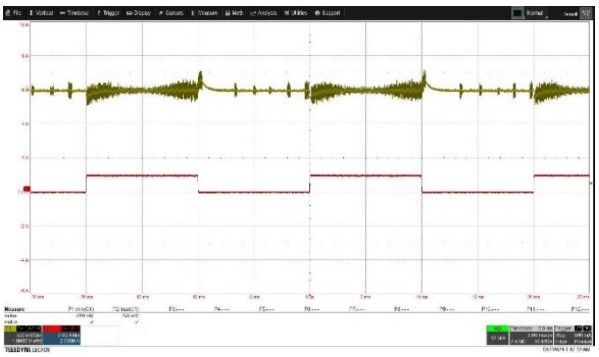
V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT}) I_{OUT})



V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

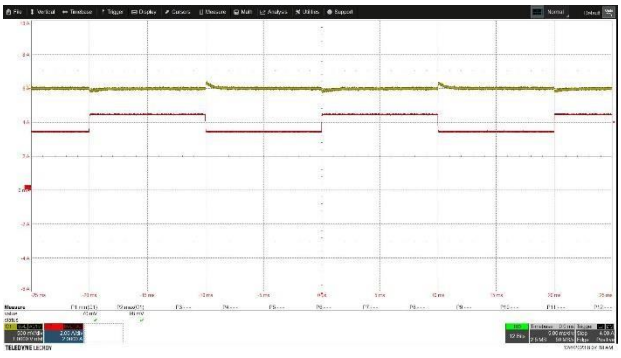


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

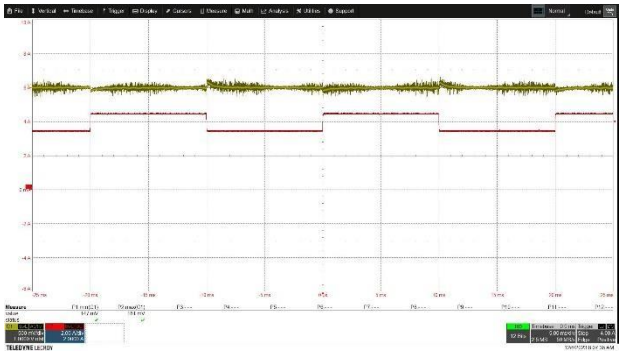


V_{BUS_C}: 21.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

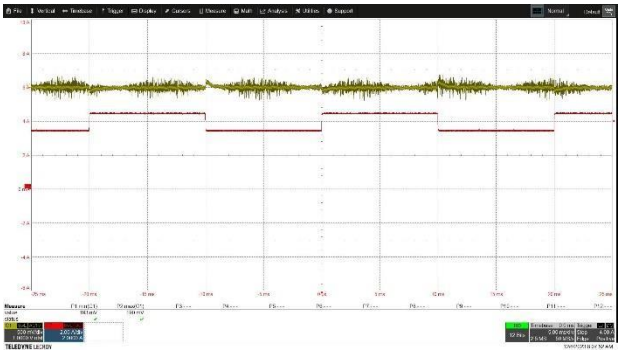
Figure 51 Output dynamic response waveforms – input 230 V_{AC}; load current transition 0 A to 1 A to 0 A



V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

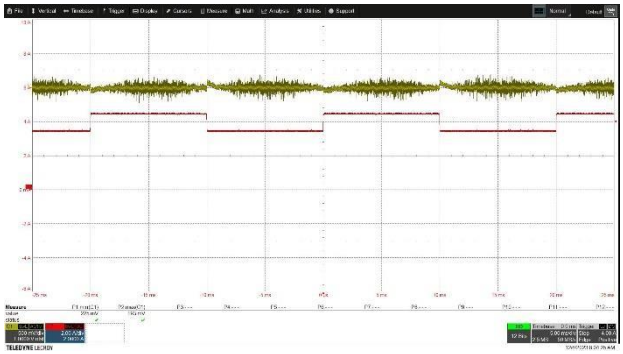


V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

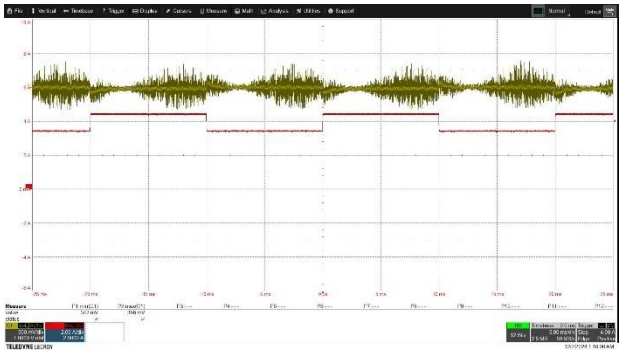


V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

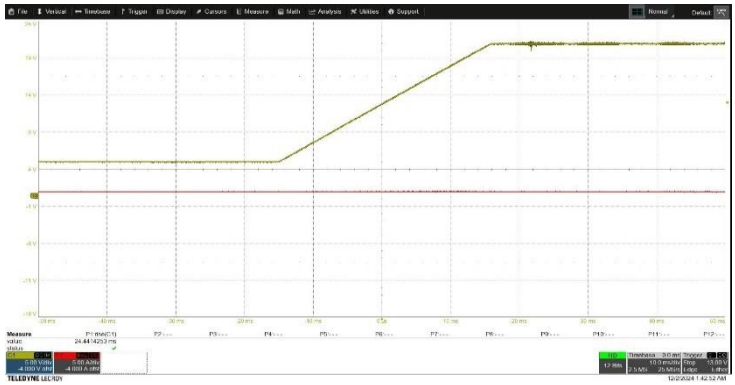


V_{BUS_C}: 21.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

Figure 52 Output dynamic response waveforms – input 115 V_{AC}; load current transition 3.5 A to 4.5 A to 3.5 A

6.7 Output voltage transition

Output voltage transition at 230 V_{AC} input and load 1 A is measured as shown in Figure 53, Figure 54, Figure 55, and Figure 56.



I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 53 Input 230 V_{AC}; V_{BUS_C} transition from 5.0 V to 21.0 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 54 Input 230 V_{AC}; V_{BUS_C} transition from 21.0 V to 5.0 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

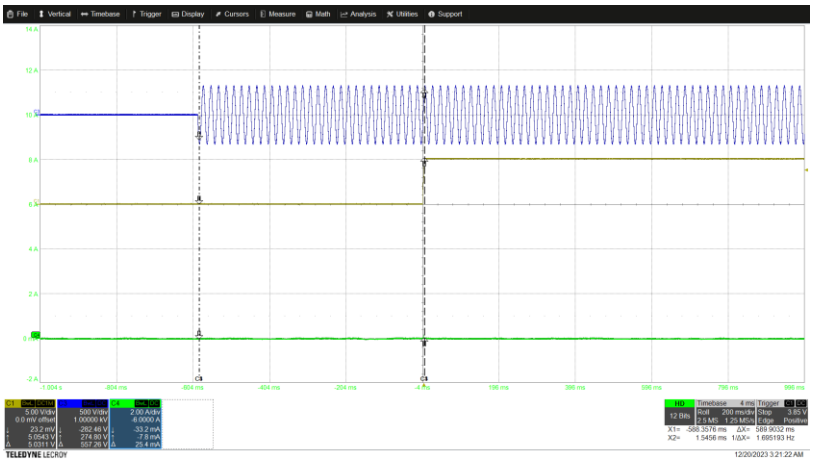
Figure 55 Input 230 V_{AC}; V_{BUS_C} transition from 5.0 V to 12 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 56 Input 230 V_{AC}; V_{BUS_C} transition from 12 V to 5 V

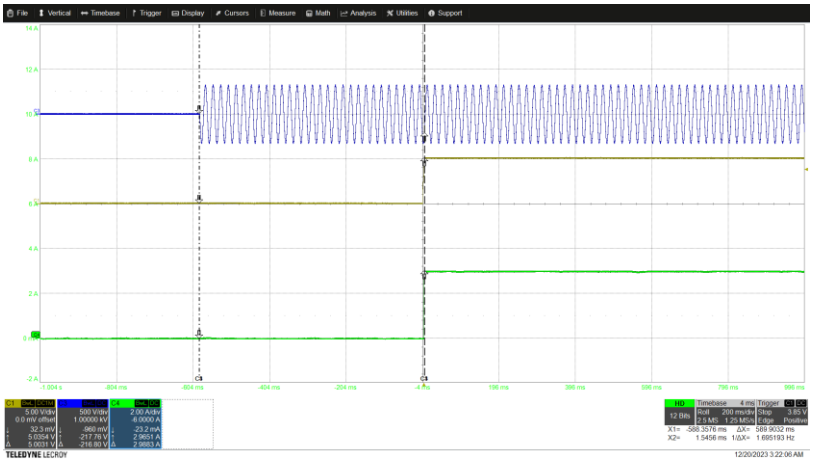
6.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load, is as shown in Figure 57 and Figure 58.



CH3: V_{IN}; CH1: Port #1 V_{BUS}; CH4: Port #1 I_{OUT}

Figure 57 Input 230 V_{AC}; V_{BUS_C} = 5 V; I_{OUT} = 0 A



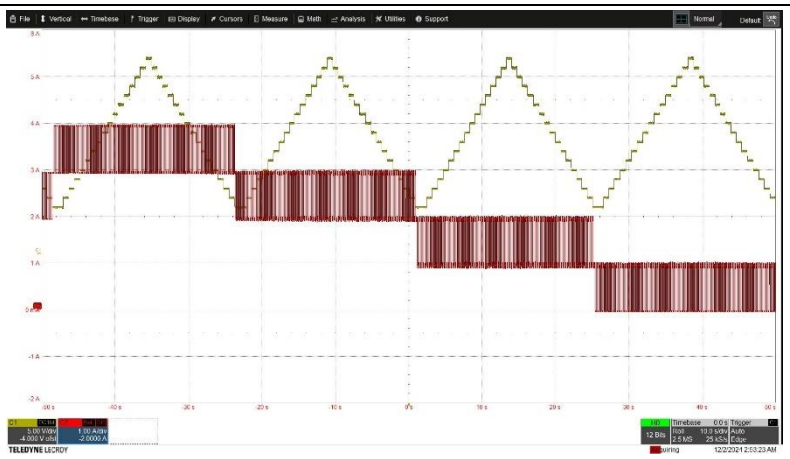
CH3: V_{IN}; CH1: Port #1 V_{BUS}; CH4: Port #1 I_{OUT}

Figure 58 Input 230 V_{DC}; V_{BUS_C} = 5 V; I_{OUT} = 1 A

6.9 Stress test waveforms

The XDPS2221+REF_CCG7DC_120W_2C solution board with one port connected was subjected to electrical stress conditions.

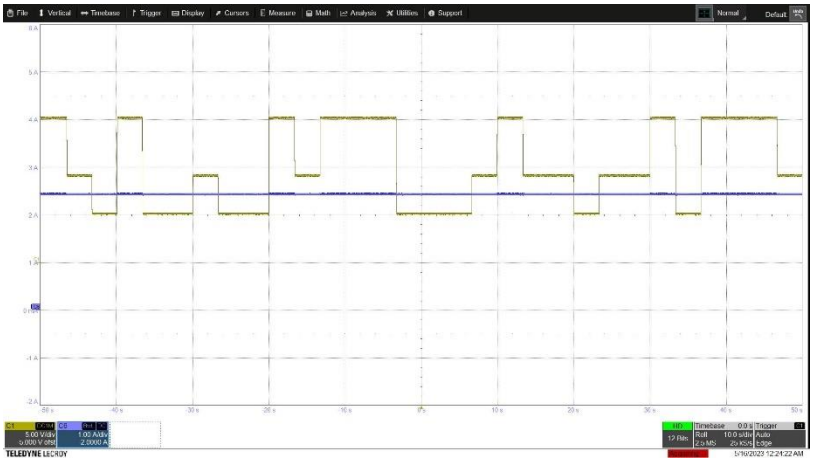
- **Electrical stress test #1** V_{IN} = 230 V_{AC}; V_{BUS_C}: continuously changing from 5.0 V–21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 59



CH1: V_{BUS_C}; CH7: I_{OUT}

Figure 59 V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 5.0 V–21 V (PPS) vice versa; I_{OUT} = 0 A to 2 A with 1 A step

- **Electrical stress test #2** V_{IN} = 230 V_{AC}; V_{BUS_C} – randomly changing from 5 V–9 V–15V (PDO); I_{OUT} = 1 A for a duration of 60 minutes. Captured waveforms are shown in Figure 60



CH1: V_{BUS_C}; CH6: I_{OUT}

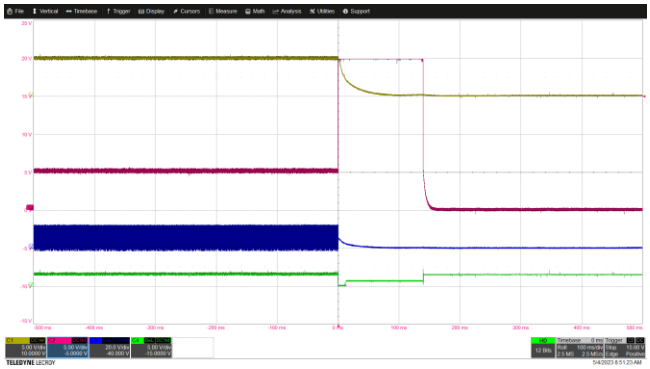
Figure 60 V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 1 A

6.10 Faults test waveforms

XDPS2221+REF_CCG7DC_120W_2C was subjected to supported fault protections and the results are displayed in the following section.

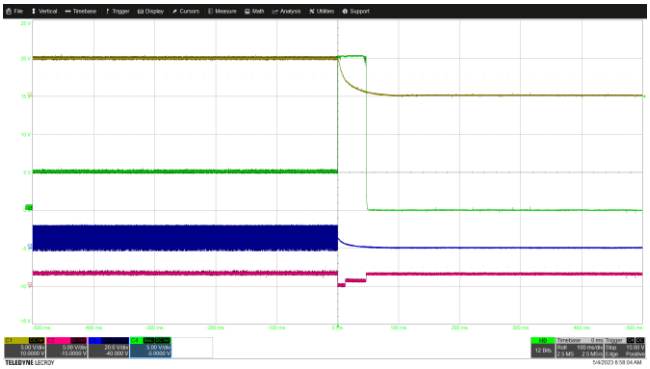
6.10.1 V_{BUS_C} to CCx line faults test waveforms

V_{BUS_C} to CC active line fault is shown in Figure 61, where V_{IN} = 230 V_{AC}; Port #1 V_{BUS_C} = 5 V.



V_{BUS_C} to CC2 fault

CH1: Port #1 V_{BUS_C}; CH2: CC2; CH3: HG0; CH4: CC1

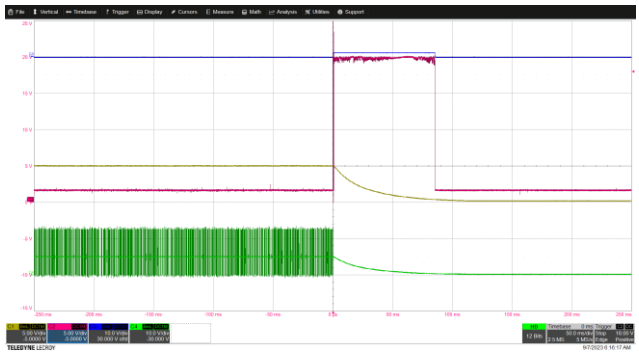


V_{BUS_C} to CC1 fault

CH1: Port #1 V_{BUS_C}; CH2: CC2; CH3: HG0; CH4: CC1

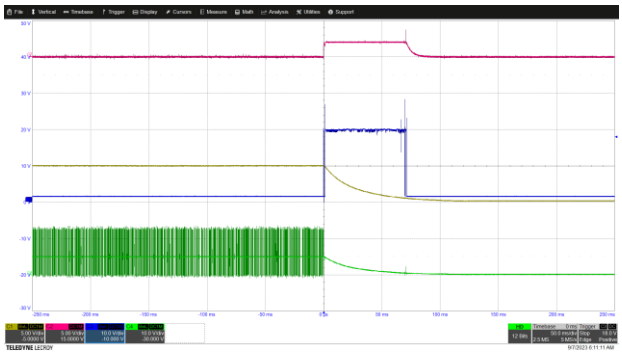
Figure 61 Port #1 V_{BUS_C} to CC line fault

V_{BUS_C} to CC active line fault is shown in Figure 62, where V_{IN} = 230 V_{AC}; port #2 V_{BUS_C} = 5 V.



V_{BUS_C} to CC2 fault

CH1: Port #2 V_{BUS_C}; CH2: CC1; CH4: HG1; CH3: CC2



V_{BUS_C} to CC1 fault

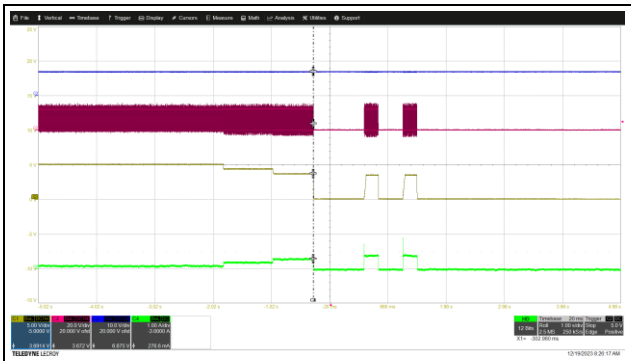
CH1: Port #2 V_{BUS_C}; CH2: CC1; CH4: HG1; CH3: CC2

Figure 62 Port #2 V_{BUS_C} to CC line fault

6.10.2 Output undervoltage protection (UVP)

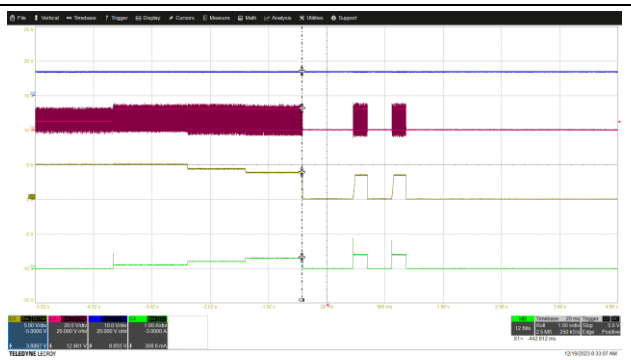
DUT output undervoltage protection waveforms are shown in Figure 63.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



Port #1 V_{BUS_C} UVP

CH1: Port #1 V_{BUS_C}; CH2: HG_0 (wrt GND); CH3: VDDD; CH4: I_{OUT}



Port #2 V_{BUS_C} UVP

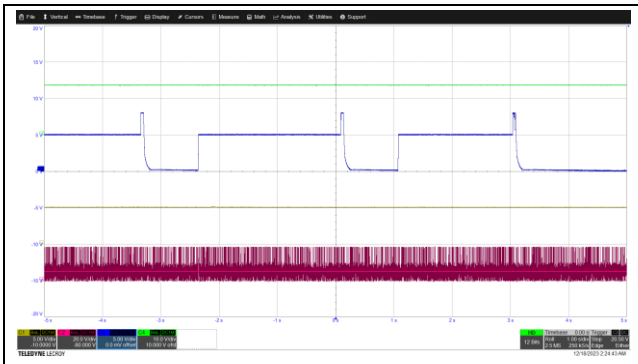
CH1: Port #2 V_{BUS_C}; CH2: HG_1 (wrt GND); CH3: VDDD; CH4: I_{OUT}

Figure 63 Output undervoltage protection

6.10.3 Output overvoltage protection (OVP)

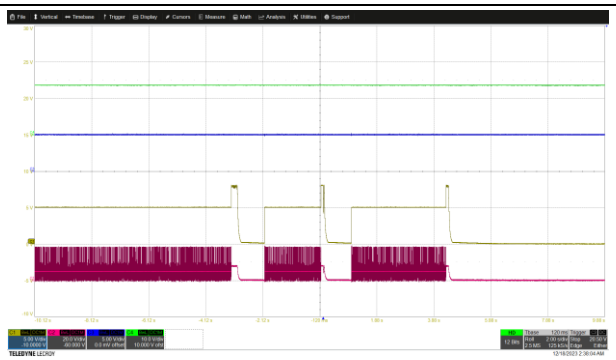
DUT output overvoltage protection waveforms are shown in Figure 64.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V, I_{OUT} = 0 A



Port #2 V_{BUS_C} OVP

CH1: Port #1 V_{BUS_C}; CH2: HG_0 (wrt GND); CH3: Port #2 V_{BUS_C}; CH4: I_{OUT}



Port #1 V_{BUS_C} OVP

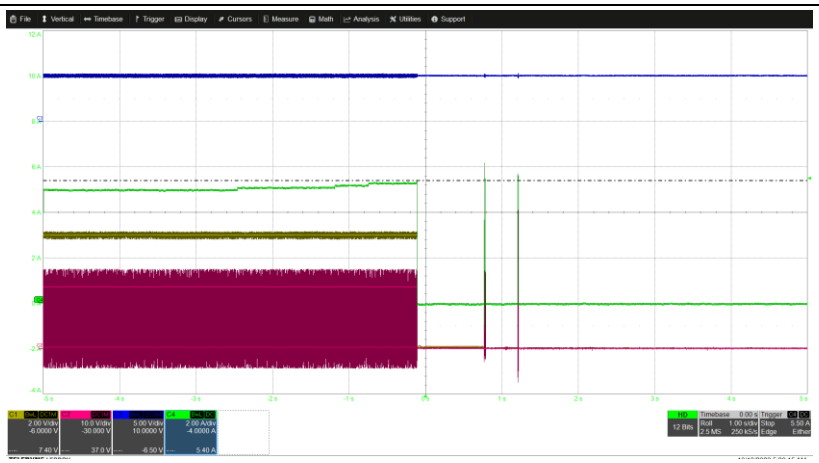
CH1: Port #2 V_{BUS_C}; CH2: HG_1 (wrt GND); CH3: Port #2 V_{BUS_C}; CH4: I_{OUT}

Figure 64 Output overvoltage protection

6.10.4 Output overcurrent protection (OCP)

DUT output overcurrent protection waveforms are shown in Figure 65.

Test conditions: V_{IN} = 230 V_{AC}; Port #1 V_{BUS_C} = 5.0 V



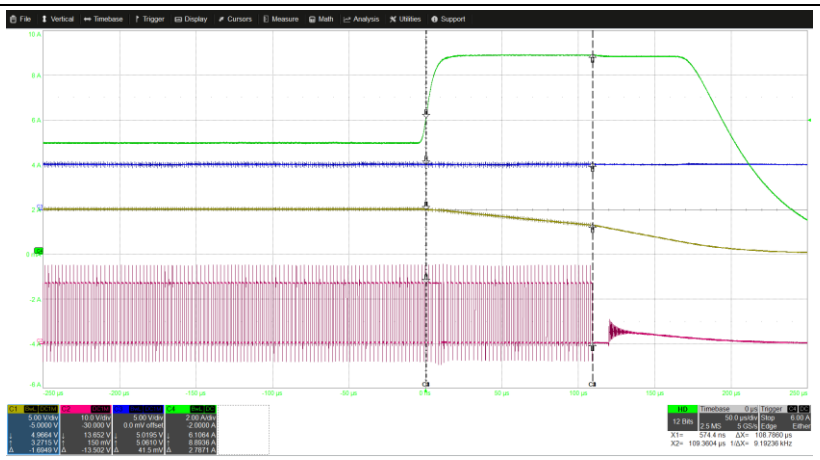
CH1: Port #1 V_{BUS_C}; CH2: HG0 (wrt GND); CH3: VDDD; CH4: Port #1 I_{OUT}

Figure 65 Output overcurrent protection

6.10.5 Output short-circuit protection (SCP)

DUT output short-circuit protection waveforms are shown in Figure 66.

Test conditions: V_{IN} = 230 V_{AC}; Port #1 V_{BUS_C} = 5.0 V



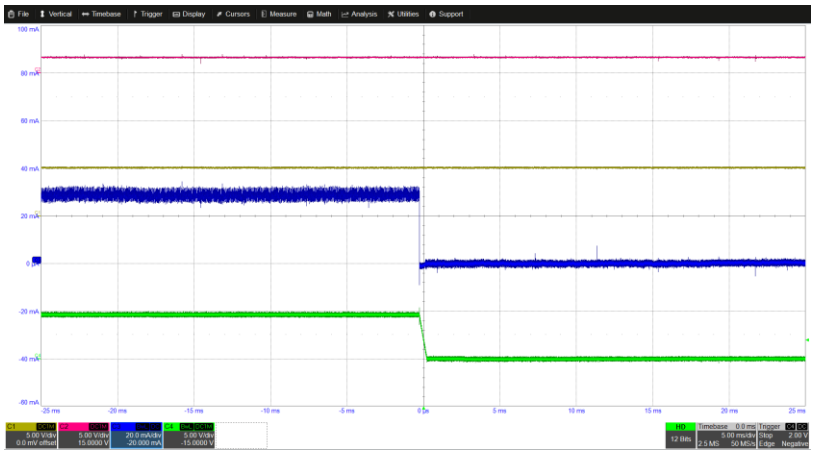
CH1: Port #1 V_{BUS_C}; CH2: HG1 (wrt GND); CH3: VDDD; CH4: Port #1 I_{OUT}

Figure 66 Output short-circuit protection

6.10.6 V_{CONN} overcurrent protection (OCP)

DUT V_{CONN} overcurrent protection waveform when port #1 is connected, is as shown in Figure 67.

Test conditions: V_{IN} = 230 V_{AC}; Port #1 V_{BUS_C} = 5.0 V



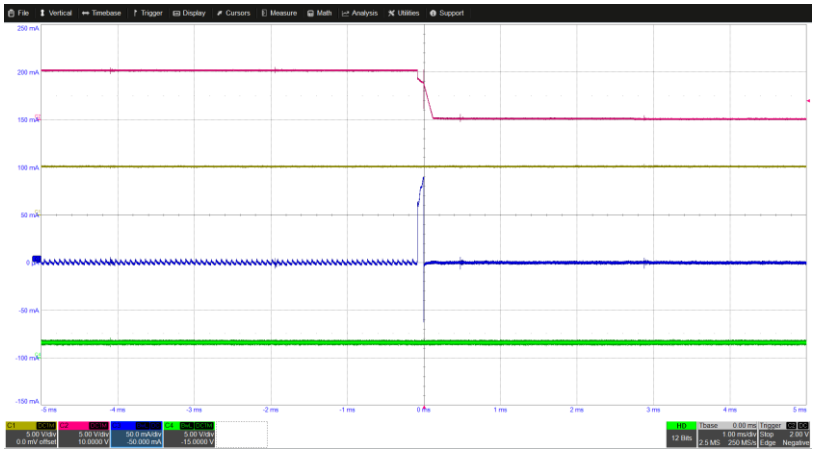
CH1: Port #1 V_{BUS_C}; CH2: CC2; CH3: I_{LOAD} on CC1 line; CH4: CC1

Figure 67 V_{CONN} overcurrent protection

6.10.7 V_{CONN} short-circuit protection (SCP)

DUT V_{CONN} short-circuit protection waveforms when port #1 is connected is shown in Figure 68.

Test conditions: V_{IN} = 230 V_{AC}; Port #1 V_{BUS_C} = 5.0 V



CH1:Port #1 V_{BUS_C}; CH2: CC1; CH3: I_{LOAD} on CC1 line; CH4: CC2

Figure 68 V_{CONN} short-circuit protection

6.11 Stand-by power consumption

REF_CCG7DC_120W_2C solution Solution Board measured currents are tabulated as follows.

Table 24 Stand-by Power

V_{in}	Time [min]	Power [mW]
230 V, 50 Hz	5	67
115 V, 60 Hz	5	41

6.12 Light load requirements

The EuP Lot 6 results of XDPS2221+REF_CCG7DC_120W_2C solution board are tabulated in Table 25.

Table 25 EuP Lot 6 results

V_{IN}(AC)/Frequency	P_{IN} (avg)	V_{BUS_C}	I_{OUT}	P_{OUT}	Efficiency (%)
230 V, 50 Hz	0.49 W	5.01	0.05	0.25	52.14
230 V, 50 Hz	0.50 W	20.23	0.0125	0.26	51.23
115 V, 60 Hz	0.48 W	5.01	0.05	0.25	53.45
115 V, 60 Hz	0.50 W	20.23	0.0125	0.26	51.13

7 Dual-port power management test results of XDPS2221+REF_CCG7DC_120W_2C

Following is the efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup section. Here, both the ports were loaded with equal amount of current.

7.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 26.

Table 26 Peak efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
05.0 V	89.96% - 2*2.50 A	90.73% - 2*2.50 A
09.0 V	91.27% - 2*3.75 A	92.99% - 2*2.50 A
12.0 V	92.56% - 2*2.10 A	93.68% - 2*2.45 A
15.0 V	92.71% - 2*2.00 A	93.83% - 2*2.50 A
20.0 V	94.02% - 2*2.25 A	95.03% - 2*2.25 A
21.0 V	92.83% - 2*2.45 A	94.25% - 2*2.80 A

*Note: Peak efficiency: 95.03% (At V_{IN} = 230 V_{AC}, V_{BUS_C} = 21 V, I_{OUT} = 2*2.25 A).*

Full load efficiency test results are tabulated in Table 27.

Table 27 Full load efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
05.0 V	87.91% - 2*5.00 A	89.77% - 2*5.00 A
09.0 V	90.38% - 2*5.00 A	91.29% - 2*5.00 A
12.0 V	92.32% - 2*2.80 A	92.83% - 2*2.80 A
15.0 V	91.71% - 2*4.00 A	93.12% - 2*4.00 A
20.0 V	92.60% - 2*3.00 A	94.24% - 2*3.00 A
21.0 V	92.74% - 2*2.80 A	94.25% - 2*2.80 A

Four-point efficiency average test results are tabulated in Table 28.

Table 28 Efficiency 4-pt average

Parameter	DOE level VI limit	Unit	Test conditions	Test results (%)	
				230 V/50 Hz	Remarks
Four-point average efficiency (Average of 25%, 50%, 75%, and 100% load)	86.00	%	V_{BUS} = 5.0 V in all 2 ports; total P_{OUT} = 50 W	89.82 %	Pass
	86.00	%	V_{BUS} = 9 V in all 2 ports; total P_{OUT} = 90 W	91.78 %	Pass
	86.00	%	V_{BUS} = 12 V in all 2 ports; total P_{OUT} = 68 W	92.08 %	Pass
	86.00	%	V_{BUS} = 15 V in all 2 ports; total P_{OUT} = 120 W	92.87 %	Pass
	86.00	%	V_{BUS} = 20 V in all 2 ports; total P_{OUT} = 120 W	93.72 %	Pass
	86.00	%	V_{BUS} = 21 V in all 2 ports; total P_{OUT} = 120 W	92.29 %	Pass

7.2 Efficiency graphs

Efficiency measured at 230 V_{AC}/50 Hz input to the DUT; V_{BUS_C} PDO, PPS voltages are 5 V, 9 V, 12 V, 15 V, and 20 V for all the two ports is shown in Figure 69.

Efficiency measured at 115 V_{AC}/60 Hz input to the DUT; V_{BUS_C} PDO, PPS voltages are 5 V, 9 V, 12 V, 15 V, and 20 V for all the two ports is shown in Figure 70.

Each port was loaded from 0 A to the maximum output current to make the total system power 120 W.

The efficiency is based on the test setup of Figure 98.

7.2.1 Efficiency and power losses at 230 V_{AC}/50 Hz input

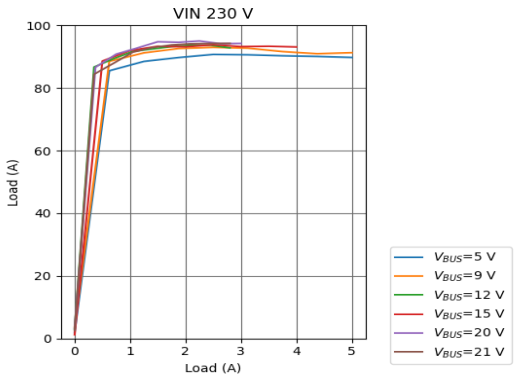


Figure 69 Efficiency at 230 V_{AC} input

7.2.2 Efficiency and power losses at 115 V_{AC}/60 Hz input

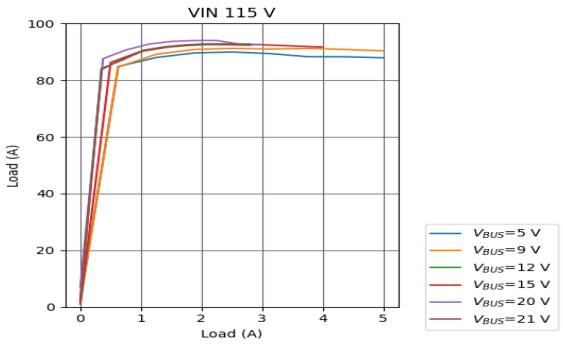


Figure 70 Efficiency at 115 V_{AC} input

7.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

7.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A to maximum load currents that each port can take to have maximum system power of 120 W is shown in Figure 71 and Figure 72.

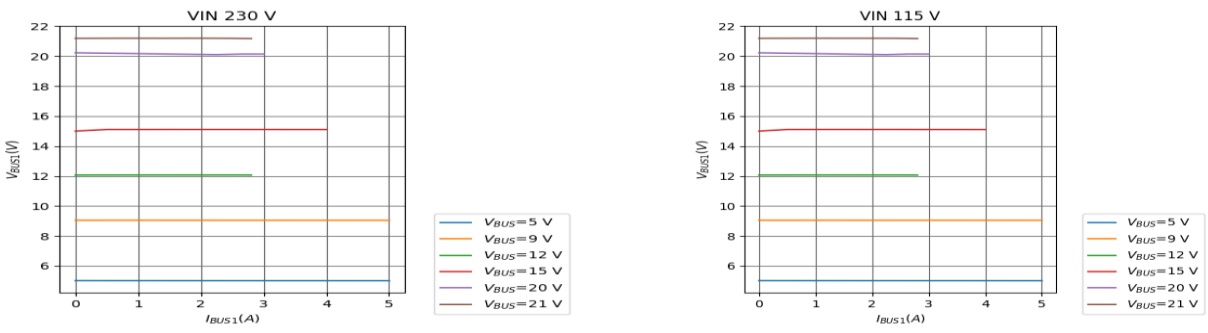


Figure 71 CV regulation at 230 V_{AC} and 115 V_{AC} input of port #1

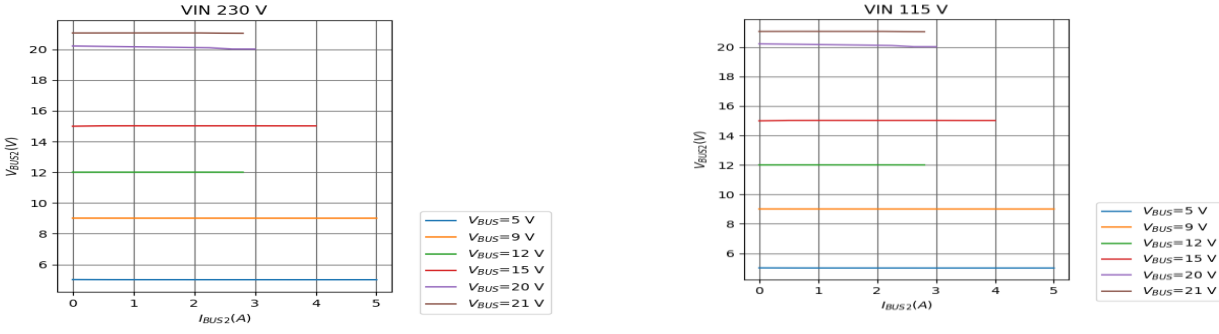


Figure 72 CV regulation 230 V_{AC} and 115 V_{AC} input of port #2

7.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of each port measured at 1.5 A output currents are shown in Figure 73 and Figure 74.

7.3.3 CC regulation curve at 230 V_{AC} input and rated output current of 1.5 A

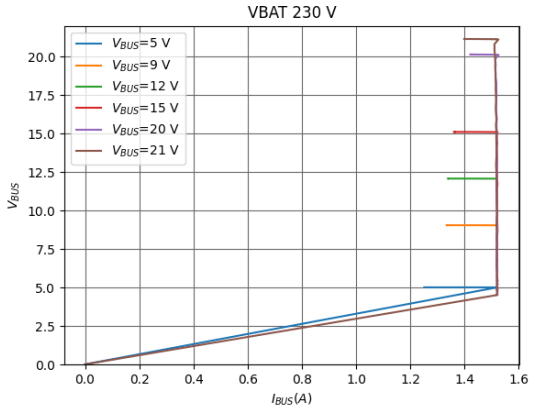


Figure 73 CC regulation curve at 230 V_{AC} input and 1.5 A output current

7.3.4 CC regulation curve at 115 V_{AC} input and rated output current of 1.5 A

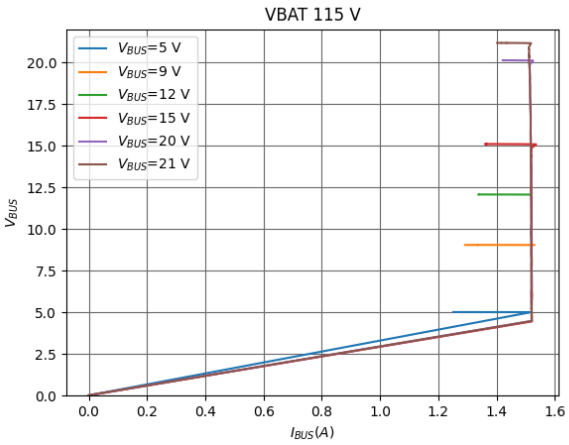


Figure 74 CC regulation curve at 115 V_{AC} input and 1.5 A output current

7.4 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors using a short ground loop connected to the probe.

7.4.1 Output voltage ripple peak-to-peak (mV)

Output voltage peak-to-peak ripple is tabulated in Table 29 and Table 30.

Table 29 Peak-to-peak ripple (mV) at 115 V_{AC} input

V_{BUS_C} – I_{OUT}	Port #1 ripple (mV)	Port #2 ripple (mV)
05.0 V – 0.00 A	7.337	6.129
05.0 V – 5.00 A	63.117	63.734
09.0 V – 0.00 A	6.348	6.617
09.0 V – 5.00 A	95.253	95.305
12.0 V – 0.00 A	11.809	10.113
12.0 V – 2.80 A	51.668	59.031
15.0 V – 0.00 A	9.663	10.331
15.0 V – 4.00 A	93.082	98.209
20.0 V – 0.00 A	59.121	54.443
20.0 V – 3.00 A	69.439	56.409
21.0 V – 0.00 A	23.964	22.846
21.0 V – 2.80 A	138.274	137.939

Table 30 Peak-to-peak (mV) ripple at 230 V_{AC} input

V_{BUS_C} - I_{OUT}	Port #1 ripple	Port #2 ripple
05.0 V – 0.000 A	7.748	6.348
05.0 V – 5.000 A	68.115	69.721
09.0 V – 0.000 A	7.234	6.605
09.0 V – 5.000 A	102.064	119.141
12.0 V – 0.000 A	12.695	9.92
12.0 V – 2.800 A	67.357	62.487
15.0 V – 0.000 A	11.115	12.374
15.0 V – 4.000 A	113.705	105.764
20.0 V – 0.000 A	25.121	10.061
20.0 V – 3.000 A	25.93	19.506
21.0 V – 0.000 A	69.028	54.482
21.0 V – 2.800 A	81.71	101.164

7.5 Output voltage regulation

Output voltage regulation measured at V_{IN} = 230 V_{AC}, V_{BUS_C} = 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} = 0 A to maximum current is shown in Table 31.

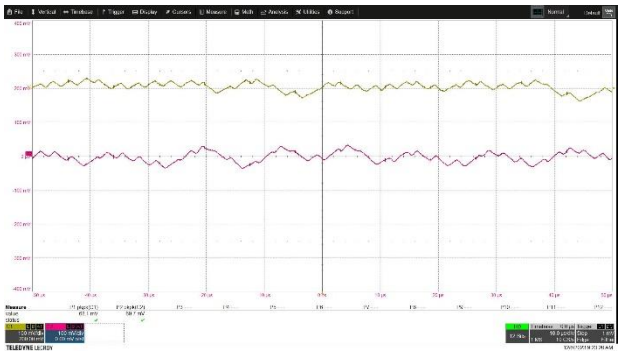
Table 31 Regulation at 230 V_{AC} input

I_{OUT} (A)	Port #1 V_{BUS_C} (V_{DC})	Port #1 % Regulation	I_{OUT} (A)	Port #2 V_{BUS_C} (V_{DC})	Port #2 % Regulation
0.00	5.022552	0.131%	0.00	5.015741	0.228%
5.00	5.015967		5.00	5.004303	

I_{OUT} (A)	Port #1 V_{BUS_C} (V_{DC})	Port #1 % Regulation	I_{OUT} (A)	Port #2 V_{BUS_C} (V_{DC})	Port #2 % Regulation
0.00	9.048947	0.031%	0.00	9.016107	0.045%
5.00	9.046138		5.00	9.012007	
0.00	12.068063	0.005%	0.00	12.0039	0%
2.80	12.068713		2.80	12.0039	
0.00	15.107154	0.010%	0.00	15.0248	0.025%
4.00	15.105639		4.00	15.02103	
0.00	20.225536	0.417%	0.00	20.22456	0.997%
3.00	20.141577		3.00 A	20.02483	
0.00	21.191068	0.063%	0.00 A	21.06967	0.098%
2.80	21.17776		2.80 A	21.04912	

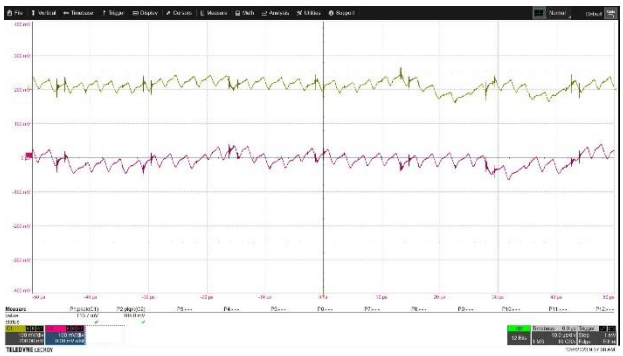
7.5.1 Output voltage ripple peak-to-peak measurement graphs

Output voltage peak-to-peak ripple waveforms for 230 V_{AC} and 115 V_{AC} at full load are shown in Figure 75 and Figure 76 respectively.

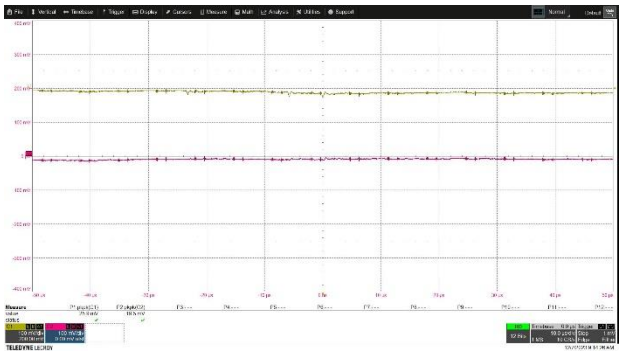


Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 5 A

Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); I_{OUT}: 5 A

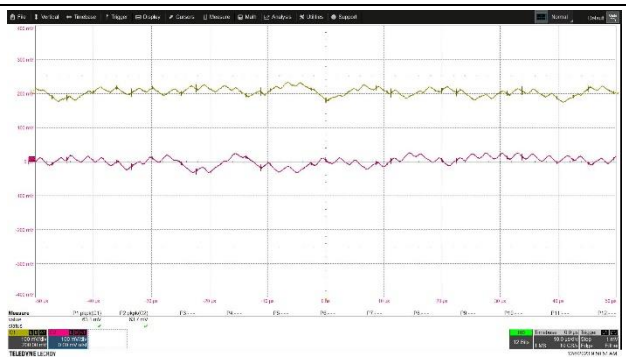


Port #1 V_{BUS_C}: 15 V (CH1); port #2 V_{BUS_C}: 15 V (CH2); I_{OUT}: 4 A

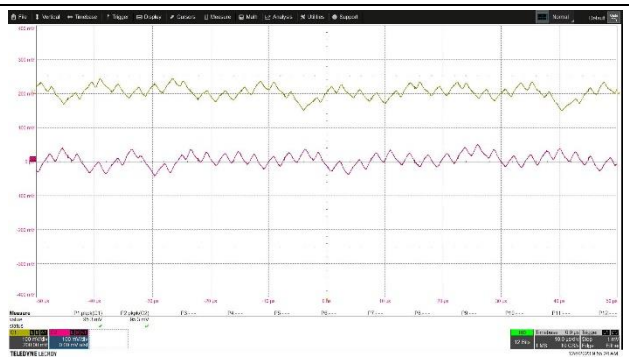


Port #1 V_{BUS_C}: 20 V (CH1); port #2 V_{BUS_C}: 20 V (CH2); I_{OUT}: 3 A

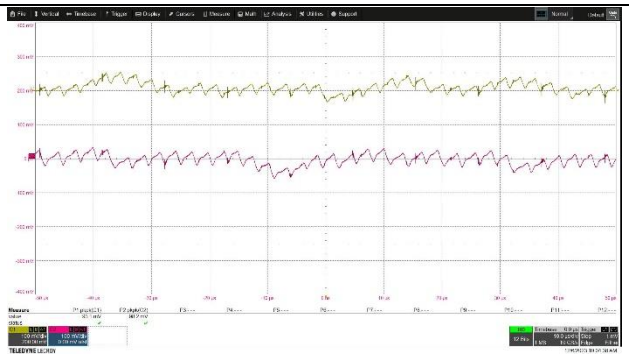
Figure 75 Ripple measurement – input voltage = 230 V_{AC}



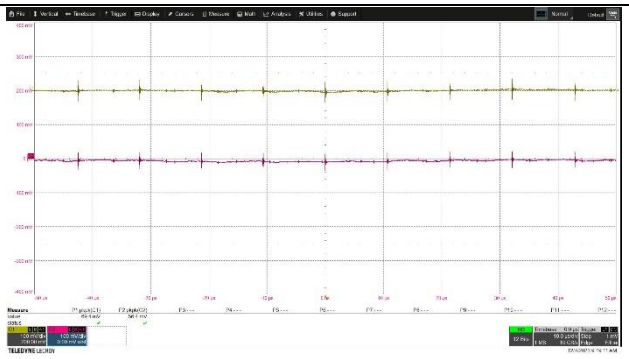
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 5 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); I_{OUT}: 5 A



Port #1 V_{BUS_C}: 15 V (CH1); port#2 V_{BUS_C}: 15 V (CH2); I_{OUT}: 4 A



Port #1 V_{BUS_C}: 20 V(CH1); port #2 V_{BUS_C}: 20 V (CH2); I_{OUT}: 3 A

Figure 76 Ripple measurement – input voltage = 115 V_{AC}

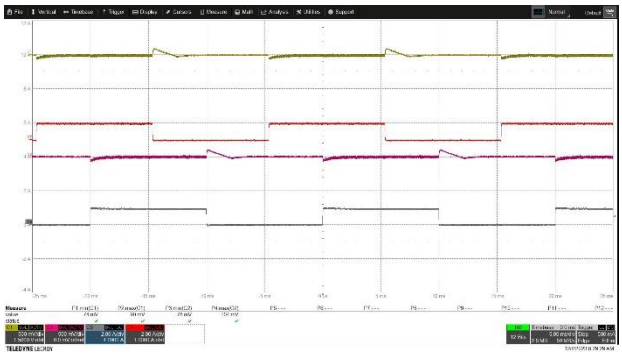
7.6 Output voltage dynamic response waveforms

At V_{IN} = 230 V, output voltage response when the output current is from 0 A–1 A–0 A is shown in Figure 77.

At V_{IN} = 115 V, output voltage response when the output current is from 0 A–1 A–0 A is shown in Figure 78.

Port #1: V_{BUS_C} (CH1); I_{OUT} (CH7); Port #2: V_{BUS_C} (CH2); I_{OUT} (CH5)

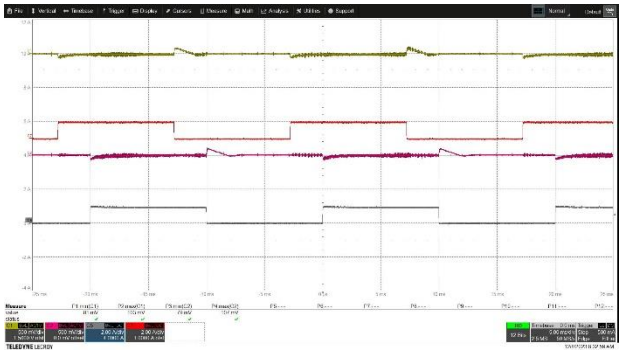
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 0 A to 1 A to 0 A



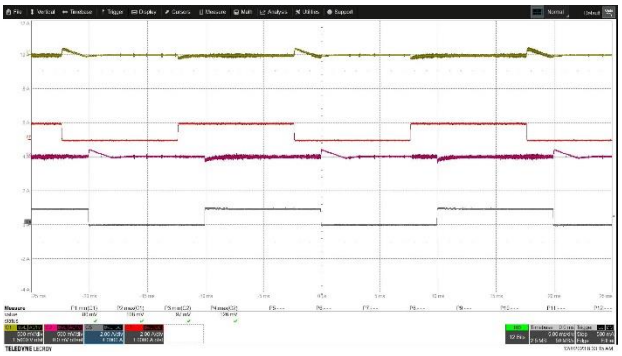
Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Port #1 V_{BUS_C}: 12 V (CH1); port #2 V_{BUS_C}: 12 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

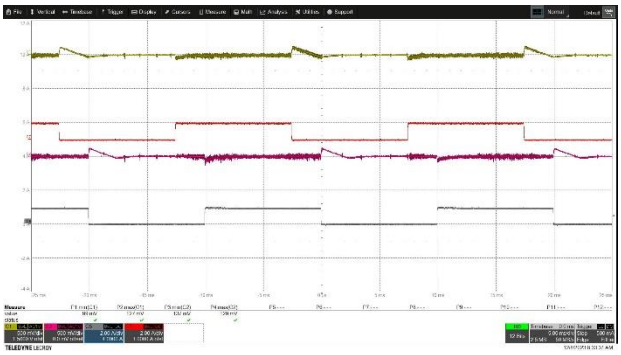
Figure 77 Output dynamic response waveforms - input 230 V_{AC}; load current transition from 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); I_{OUT}: 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); I_{OUT}: 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 12 V (CH1); port #2 V_{BUS_C}: 12 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Figure 78 Output dynamic response waveforms - input 115 V_{AC}; load current transition from 0 A to 1 A to 0 A

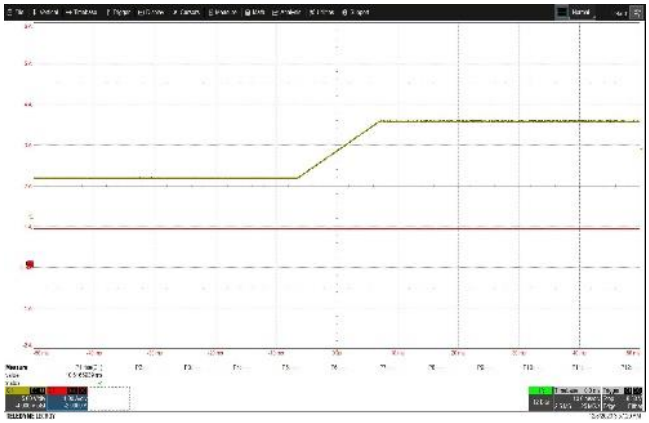
7.7 Output voltage transition

Output voltage transition at 230 V_{AC} input and 1 A load is measured and is as shown in Figure 79, Figure 80, and Figure 81.

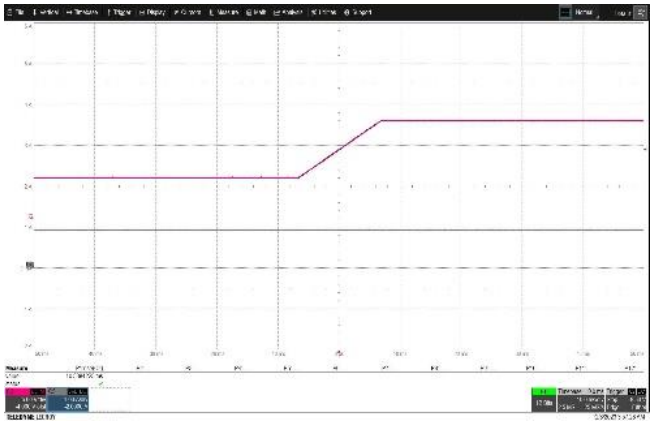
Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH7: I_{OUT})

Port #2; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH6: I_{OUT})

Figure 79 Input 230 V_{AC}; V_{BUS_C} transition from 5.0 V to 21 V



Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH7: I_{OUT})



Port #2; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH6: I_{OUT})

Figure 80 Input 230 V_{AC}; V_{BUS_C} transition from 5.0 V to 12 V

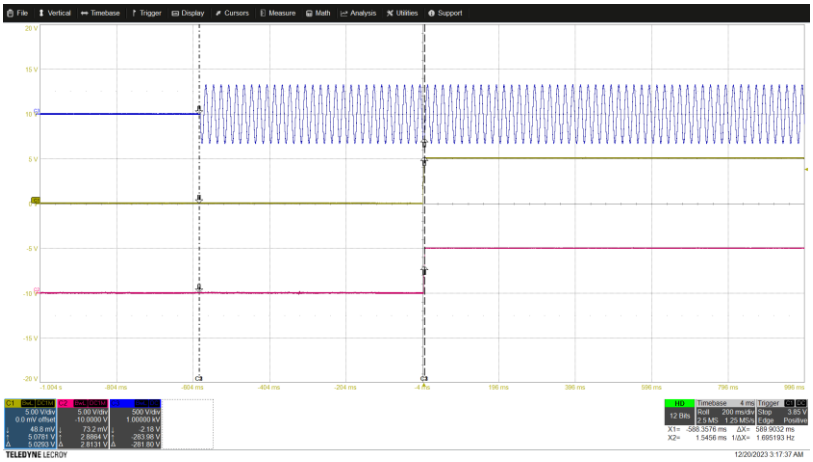
Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH7: I_{OUT})

Port #2; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH6: I_{OUT})

Figure 81 Input 230 V_{AC}; V_{BUS_C} transition from 12.0 V to 5.0 V

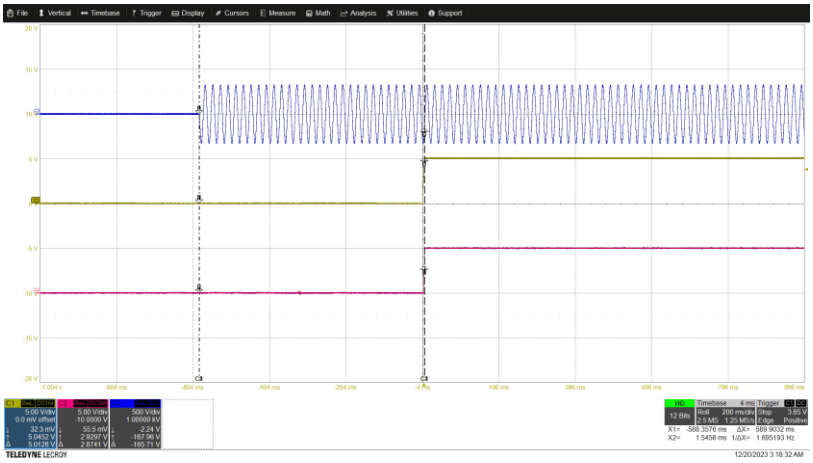
7.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load is as shown in Figure 82 and Figure 83.



CH3: V_{IN}; CH1: Port #1 V_{BUS}; CH2: Port #2 V_{BUS}

Figure 82 Input 230 V_{AC}; V_{BUS_C} = 5 V; I_{OUT} = 0 A



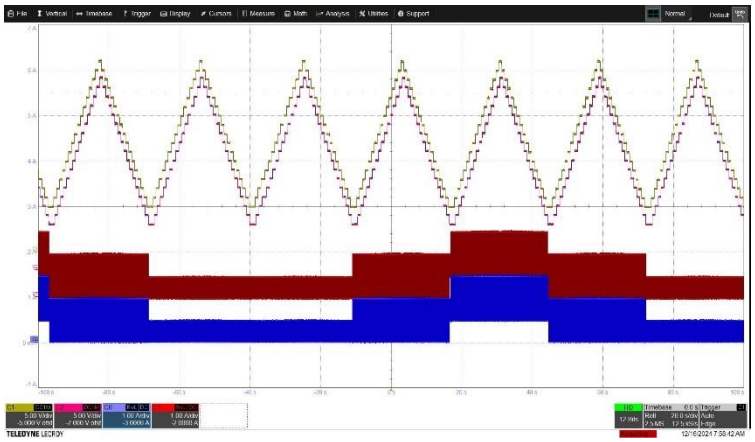
CH3: V_{IN}; CH1: Port #1 V_{BUS}; CH2: Port #2 V_{BUS}

Figure 83 Input 230 V_{AC}; V_{BUS_C} = 5 V; I_{OUT} = 3 A

7.9 Stress test waveforms

The XDPS2221+REF_CCG7DC_120W_2C solution board with two ports connected was subjected to the following electrical stress conditions.

- **Electrical stress test #1** V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 5.0 V–21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 84



CH1: port #1 V_{BUS_C}; CH7: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH6: port #2 I_{OUT}

Figure 84 V_{IN} = 230V_{AC}; V_{BUS_C} – continuously changing from 5.0 V–21 V (PPS) and vice versa; I_{OUT} = 0 A to 4 A with 1 step

- **Electrical stress test #2** V_{IN}= 22.5 V_{DC}; V_{BUS_C}: randomly changing from 5 V to 9 V to 15 V (PDO); I_{OUT}: 1 A for a duration of 60 minutes. Captured waveforms are shown in Figure 85

CH1: port #1 V_{BUS_C}; CH6: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH5: port #2 I_{OUT}

Figure 85 V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 1 A

8 Thermal performance

The following section displays the DUT temperature measurements captured at ambient temperature.

8.1 Thermal image

- Test condition: V_{IN} = 23.2 V_{DC}, port #1 V_{BUS_C} = 20 V, port #1 I_{OUT} = 3 A , port #2 V_{BUS_C} = 20 V, port #2 I_{OUT} = 3 A
- Lab ambient temperature: 24.3°C and thermal scan captured in open-frame after 60 minutes (see Figure 86 and Table 32)

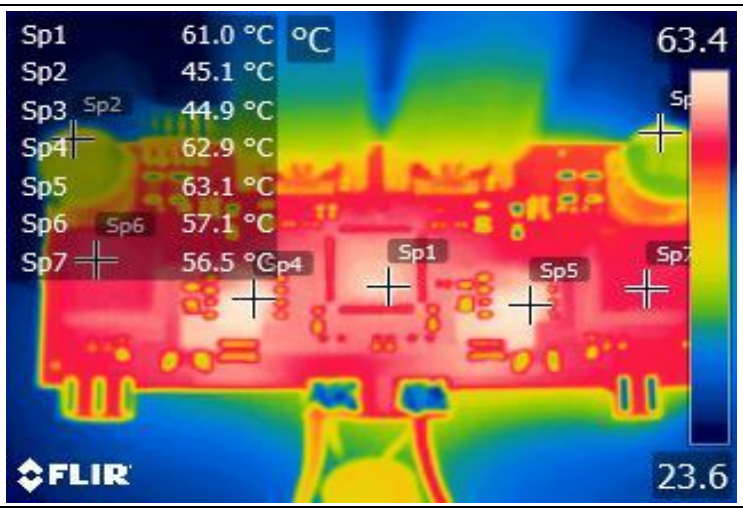


Figure 86 DUT thermal image at ambient temperature, V_{IN} = 23.2 V_{DC}; Port #1, V_{BUS_C} = 20 V and I_{OUT} = 3 A; Port #2, V_{BUS_C} = 20 V and I_{OUT} = 3 A

Table 32 Temperature measurement

Markers	Designator	Component	Temperature (°C)
Sp1	U1	CCG7DC	61.0
Sp2	EC1	Port #1 output capacitor	45.1
Sp3	EC2	Port #2 output capacitor	44.9
Sp4	Q2	Port #1 MOSFET	62.9
Sp5	Q3	Port #2 MOSFET	63.1
Sp6	L1	Port #1 power inductor	57.1
Sp7	L2	Port #2 power inductor	56.5

9 Bode plots

The following Bode plot results are captured by connecting XDPS2221 to REF_CCG7DC_120W_2C.

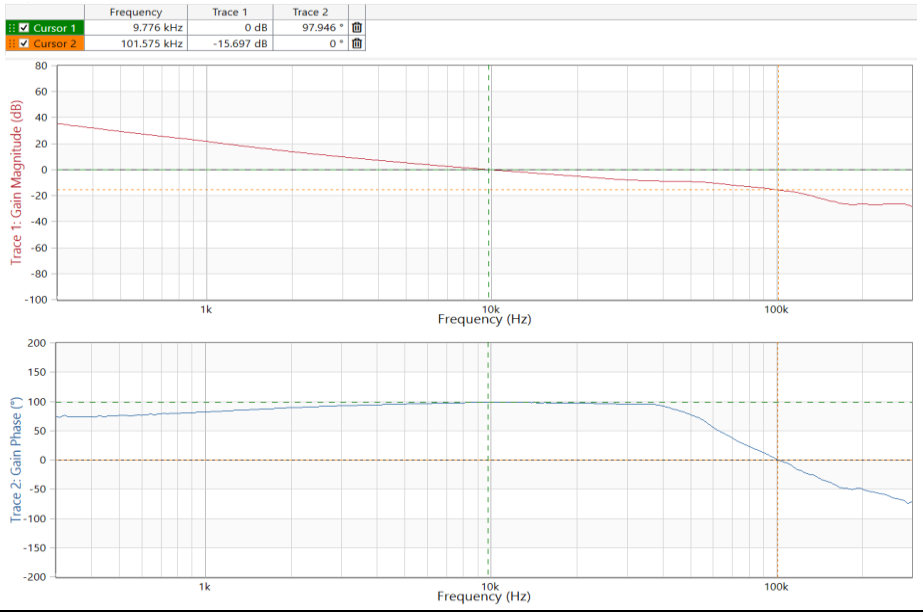


Figure 87 Port #1 Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 5 V, I_{OUT} = 5 A

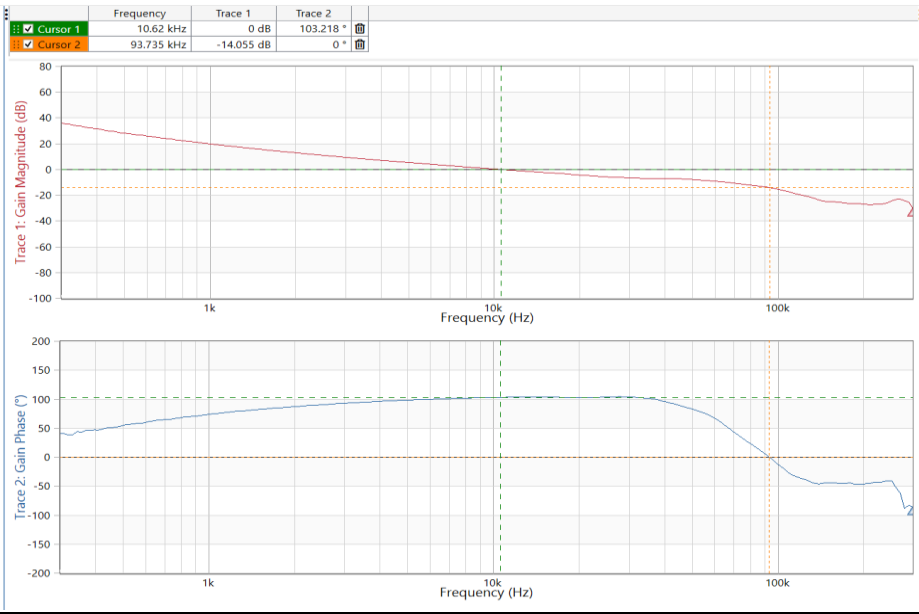


Figure 88 Port #1 Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 9 V, I_{OUT} = 5 A

Bode plots

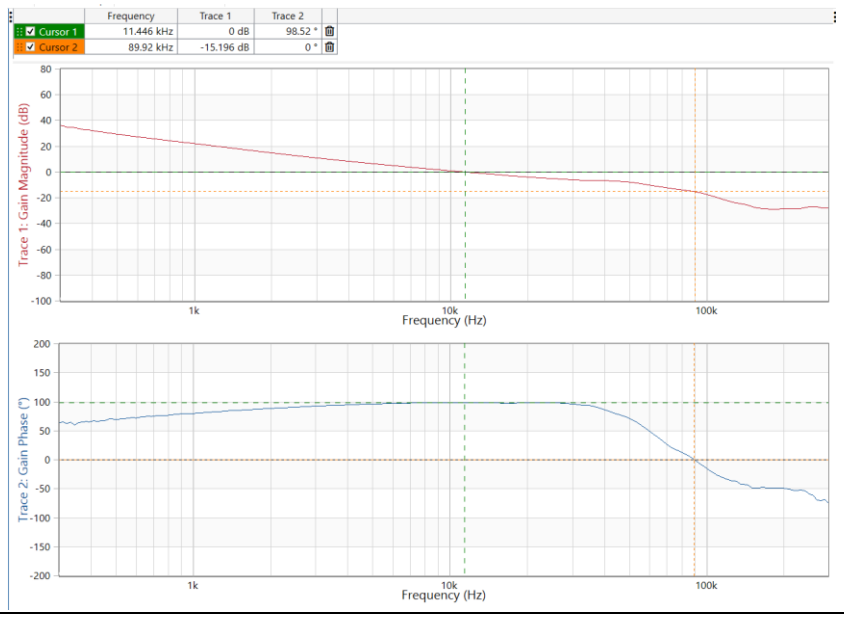


Figure 89 Port #1 Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 12 V, I_{OUT} = 5 A

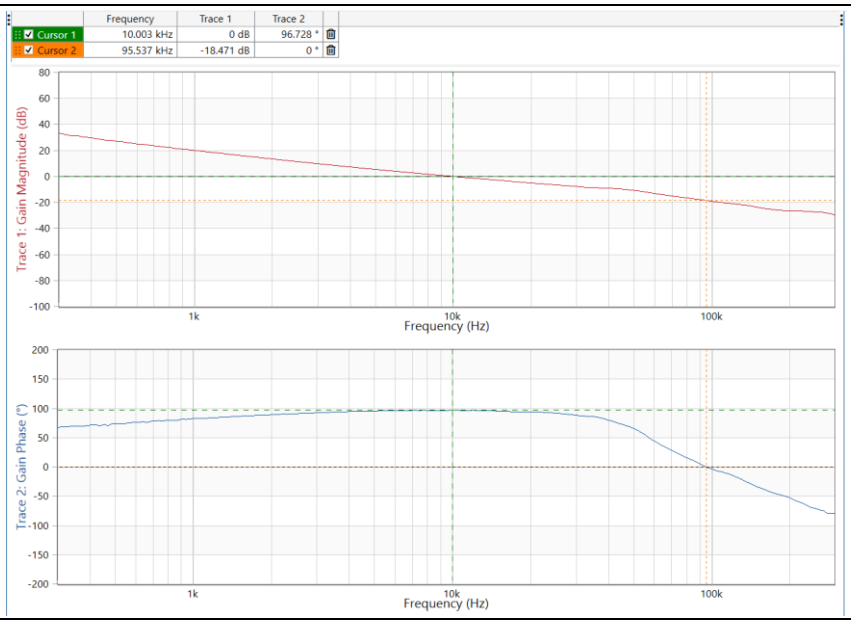


Figure 90 Port #1 Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 15 V, I_{OUT} = 5 A

10 USB-IF pre-compliance tests

Note: USB PD source detailed test reports are available based on request.

10.1 QuadraMAX

10.1.1 Test setup

- **QuadDraw version:** 0.9.8930
- **Test input voltage conditions:** 12 V_{DC}

Table 33 QuadraMAX - USB PD source test results

Test	Description	Result
TD SPT.1	Load test	Pass
TD SPT.2	Capabilities test	Pass
TD SPT.3	Hard reset test	Pass
TD SPT.5	OCP test	Pass
TD SPT.6	PPS voltage step test	Pass
TD SPT.7	PPS current limit test	Pass

10.2 Ellisys

10.2.1 Test setup

- The test was run using the Ellisys USB Explorer 350 Examiner V3.1.8999

Table 34 Ellisys - USB PD source test results

Test	Result
USB Type-C Tests	Pass
Merged USB PD protocol tests	Pass
Merged USB PD protocol VDM tests	Pass

10.3 GRL

- The test was run using USB PD and Type-C tester and analyzer (GRL-USB-PD-C2)
- The GRL-PD-C2 Browser software release version 1.6.25.0 was used to run these tests

Table 35 GRL - USB PD source test results

Test	Result
USB PD Compliance Test Specification	Pass

10.4 Lecroy

- The test was run using Voyager M310e
- USB Compliance v7.82 build 1187 and USB Protocol Suite v9.50 build 4754 Beta was used to run the tests

Table 36 Lecroy - USB PD source test results

Test	Result
USB Type-C – USB IF	Pass
USB Power Delivery – USB IF	Pass

11 EMI Tests results

Note: *CISPR 32 Class-B conducted emission tests are performed when both the port loaded with 120 W Max.*

11.1 XDPS2221 + REF_CCG7DC_DUAL_C_120W_R1 Master Port EMI

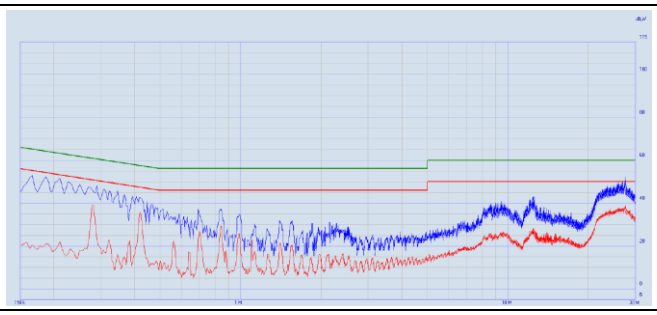


Figure 91 CISPER 32 Class-B CE tests on Port#1 and Port#2, V_{BUS}: 5 V 5 A, V_{IN}: 230 V_{AC}/50Hz

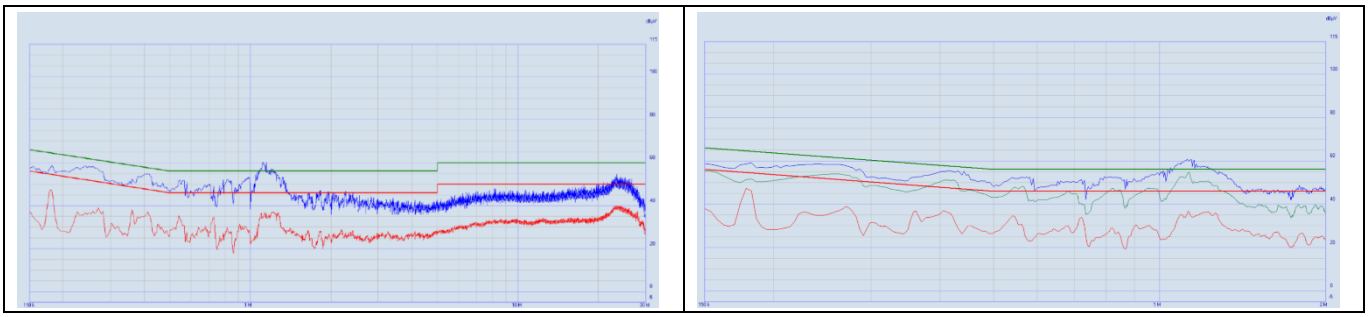


Figure 92 CISPER 32 Class-B CE tests on Port#1 and Port#2, V_{BUS}: 9 V 5 A, V_{IN}: 230 V 50 Hz; Right: QP

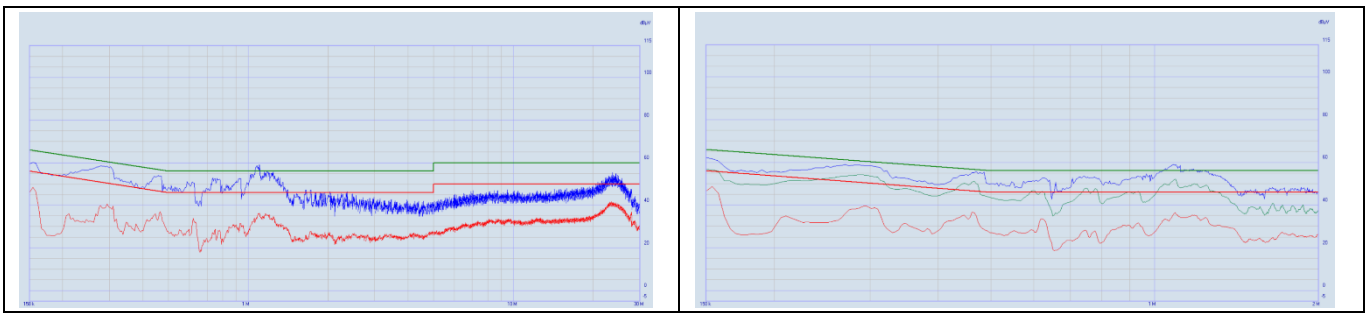


Figure 93 CISPER 32 ClassB CE tests on Port#1 and Port#2, V_{BUS}: 15 V 4 A, V_{IN}: 230 V 50 Hz; Right: QP

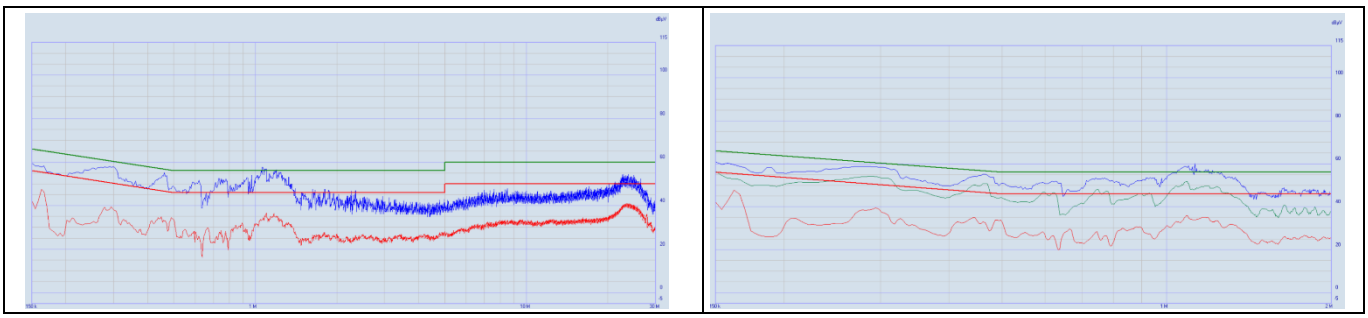


Figure 94 CISPER 32 Class -B CE tests on Port#1 and Port#2, V_{BUS}: 20 V 3 A, V_{IN}: 230 V 50 Hz; Right: QP

12 Circuit schematics

The following sections contain the schematics used for the test equipment setup.

12.1 REF_CCG7DC_120W_2C_R1

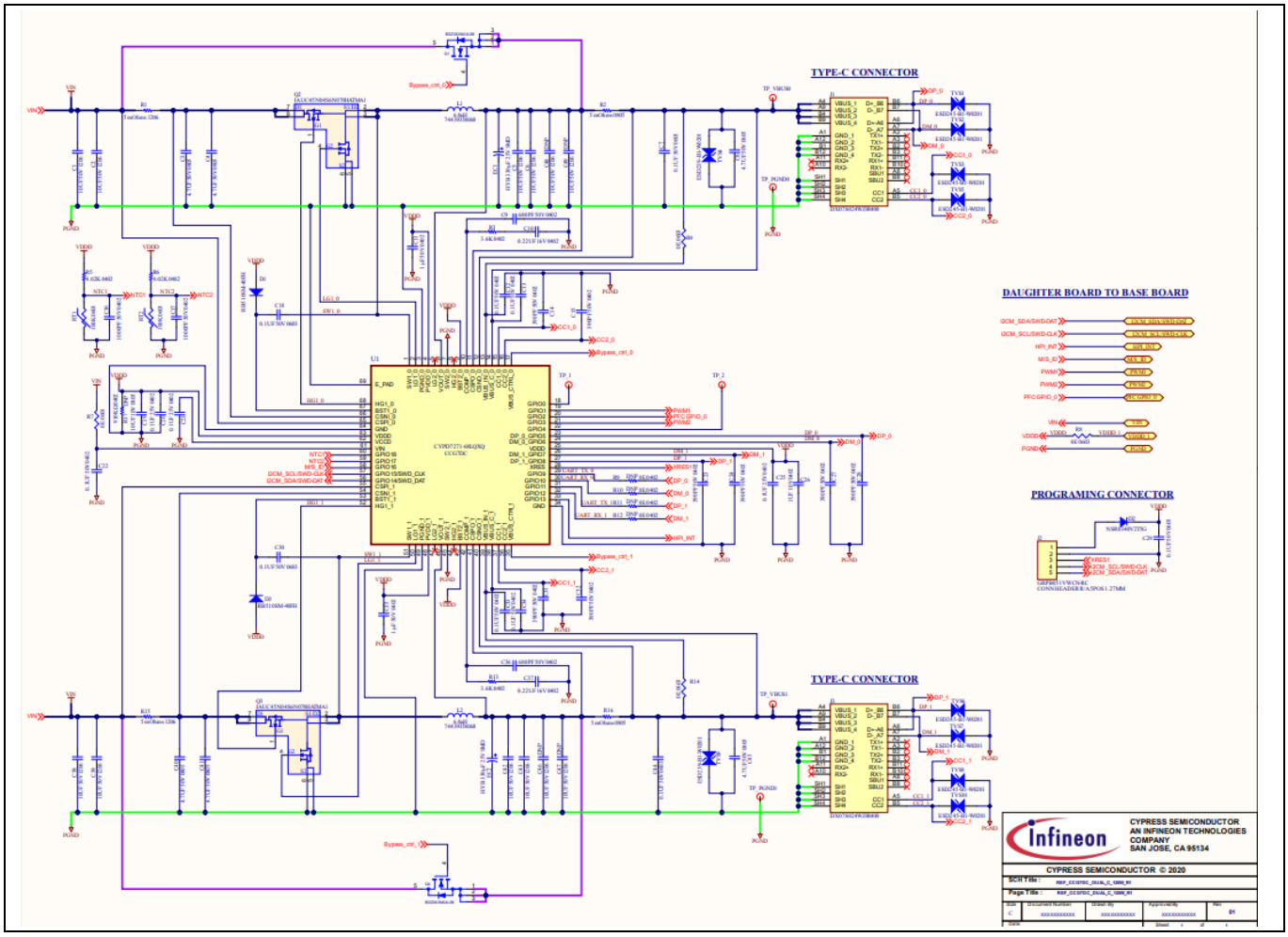


Figure 95 Standalone EZ-PD™ CCG7DC 120 W daughterboard

12.2 REF_CCG7DC_120W_2C_BASE_120W_R1

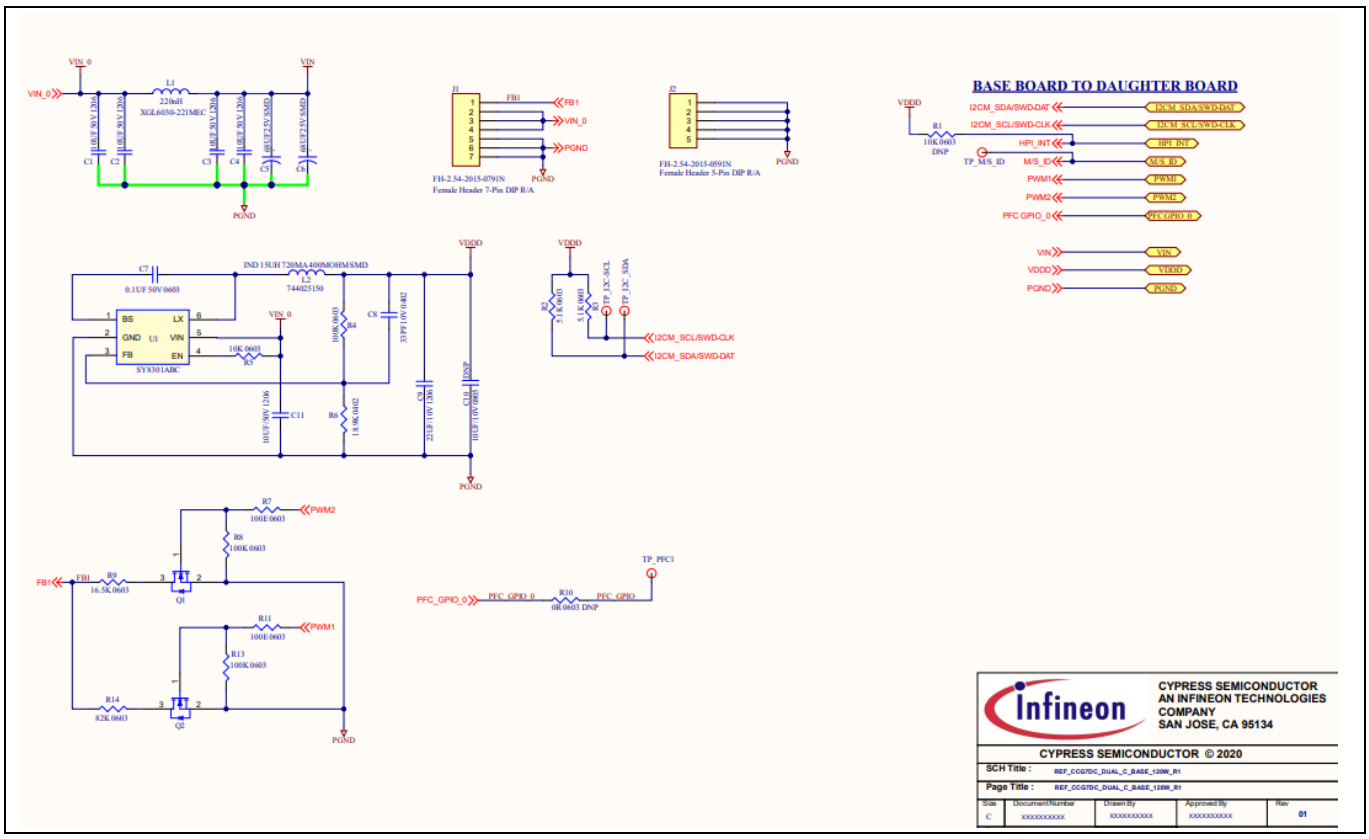


Figure 96 CCG7DC 120 W baseboard

13 Appendix: Efficiency measurement test setup

Efficiency measurements are captured with the test setup of REF_CCG7DC_120W_2C board input connector to output connector; measurement points are shown in the following sections.

13.1 Efficiency measurement – input connector to the USB Type-C connector on the board

Efficiency measurement connection is done as shown in Figure 97 and Figure 98. For single port measurement, port #1 is connected, and other ports are disconnected. For dual port measurement, port #1 and port #2 are connected.

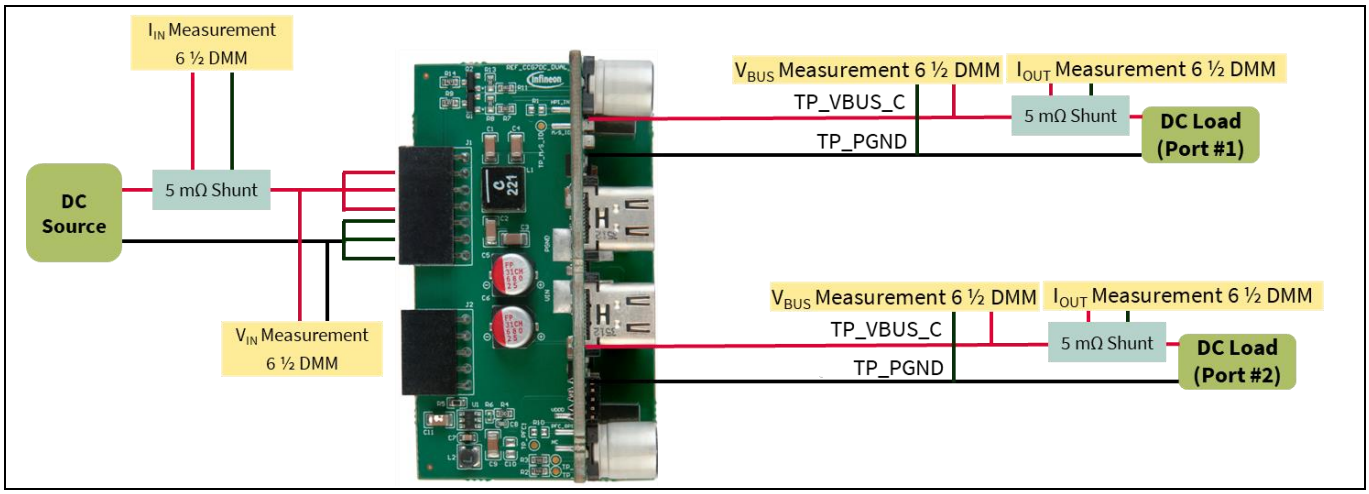


Figure 97 Efficiency measurement of standalone multiport DC-DC converter – input connector to the USB Type-C connector on the board

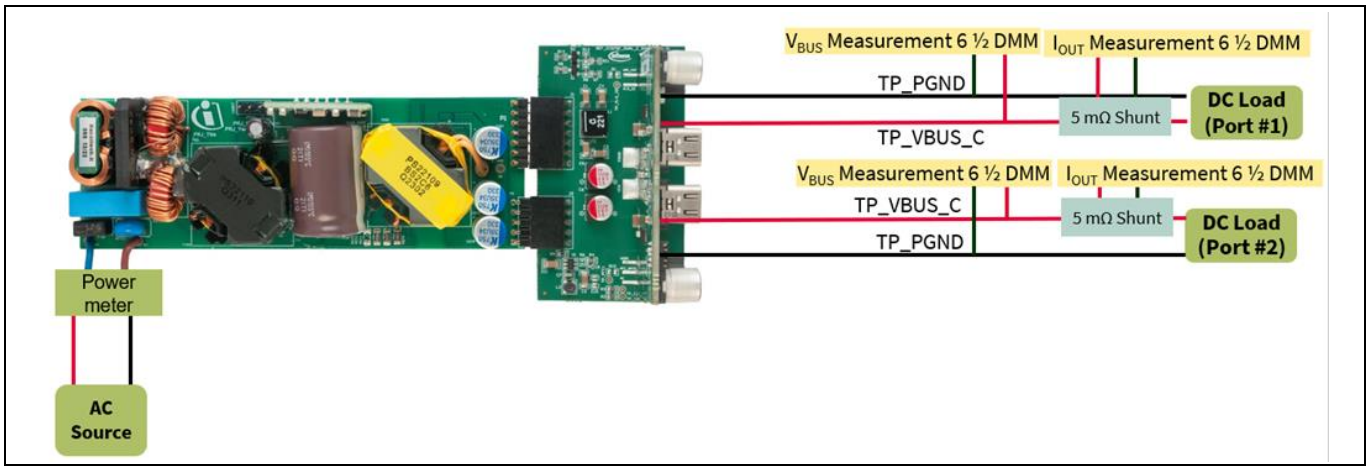


Figure 98 Efficiency measurement of AC-DC multiport adapter and charger – input connector to the USB Type-C connector on the board

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[2] USB Implementers Forum, Inc.: *USB Type-C and connector specification (Release 2.2)*

[3] Infineon Technologies AG: EZ-PD™ Configuration Utility

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[5] Infineon Technologies AG: *EZ-PD™ CCG7SC Single-port USB-C Power Delivery & DC-DC controller*; Available online

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[9] Infineon Technologies AG: *XDP™ XDPS2221*; Available online

Revision history

Document revision	Date	Description of changes
**	2024-01-23	Initial release
*A	2024-03-13	Updated reference design nomenclature to “REF_CCG7DC_120W_2C” Updated document title
*B	2025-02-14	Updated test results

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