

Datasheet

Vela IF310

Version 0.1

PRELIMINARY

Revision History

Version	Date	Notes	Contributors	Approver
1.0	25 Oct 2025	Preliminary release	Jacky Kuo	

PRELIMINARY

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1 Scope

This document describes the key hardware aspects of the Ezurio Vela IF310 Series wireless modules providing high-speed 4-wire UART interface for Bluetooth® / Bluetooth® LE connections. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Infineon CYW55310 data sheet issued on February 21, 2023, along with other documents provided by Infineon.

Note: The information in this document is subject to change. Please contact Ezurio to obtain the most recent version of this document.



2 General Description

Built on Infineon’s AIROC™ CYW55310, the Vela IF310 brings together Bluetooth Classic (BR/EDR) and the full Bluetooth 6.0 LE feature set—including LE Audio with LC3, Isochronous Channels, Auracast, LE Coded & 2 MPHY and Advertising Extensions—so you can refresh legacy Classic designs and embrace the latest LE Audio opportunities with one module.

A 192 MHz ARM® Cortex-M33, integrated audio interfaces, up to +10 dBm output power and a very flexible HCI UART interface for a variety of hosted/hostless SW architecture options deliver a low-risk, fast-to-market platform for demanding medical or industrial audio and data applications.

Engineered for high-reliability environments, the Vela IF310 is the answer to connectivity challenges where failure is not an option. Whether it’s minimizing downtime in clinical settings or ensuring interference-resistant audio in industrial spaces, this module is built to perform. Its rugged -40 °C to +85 °C operation, robust security features including TrustZone® and CryptoCell-312, and versatile footprint options reflect Ezurio’s commitment to dependable, application-ready solutions. Combined with our personal, hands-on support through every stage of development, the Vela IF310 doesn’t just deliver technology—it delivers peace of mind.

Table 1: Product ordering information

Part	Description
453-00390R	Module, Vela IF310, Integrated Antenna, Tape and Reel
453-00390C	Module, Vela IF310, Integrated Antenna, Cut Tape
453-00391R	Module, Vela IF310, MHF4, Tape and Reel
453-00391C	Module, Vela IF310, MHF4, Cut Tape
453-00392R	Module, Vela IF310, Trace Pin, Tape and Reel
453-00392C	Module, Vela IF310, Trace Pin, Cut Tape
453-00390-K1	Development Kit, Module, Vela IF310, Integrated Antenna
453-00391-K1	Development Kit, Module, Vela IF310, MHF4

3 Features Summary

The Ezurio Vela IF310 series device features are described in [Table 2](#).

Table 2: Vela IF310 series wireless module features

Feature	Description
Variants	<ul style="list-style-type: none"> • Integrated Ignion antenna variant • MHF4 connector variant • Trace Pin variant
Bluetooth subsystem	<ul style="list-style-type: none"> • Complies with Bluetooth® core specification version 6.0 • Includes support for basic data rate (BR), EDR 2 Mbps and 3 Mbps, extended synchronous connection-oriented • Bluetooth® LE 1 Mbps, 2 Mbps and LE Long Range (LE-LR) • Up to 10dBm EIRP output power • Excellent receiver sensitivity (-108 dBm for Bluetooth® LE-LR-S8 125 Kbps)
Microcontroller (MCU)	<ul style="list-style-type: none"> • Powerful Arm® Cortex®-M33 core • Bluetooth® stack in ROM allowing standalone operation without any external MCU • 2-MB on-chip ROM memory for program storage and boot ROM • 768-KB on-chip RAM memory for data scratch-pad and patch RAM code • AES-128 security system
Peripherals	<ul style="list-style-type: none"> • Up to 22 GPIOs • TDM, I2S, PCM and UART interfaces • I2C¹ and Wi-Fi coexistence¹ supports • HFP codec interface controller: <ul style="list-style-type: none"> ▪ Supported by PCM and I2S transports and bidirectional operations. ▪ Supported by PCM <ul style="list-style-type: none"> ➢ Sample rates 8k for NBS and 16k for wideband speech (WBS) supported. ➢ Sample width is limited to 16-bits. ➢ Synchronization clock width of 1 or 3 (short or long). ➢ Bit clocks of 128k, 256k, 512k, 1024k and 2048k. ▪ Support by I2S <ul style="list-style-type: none"> ➢ Support bit clocks of 256k (NBS) and 512k (WBS). • A2DP codec controller: <ul style="list-style-type: none"> ▪ Supported by I2S transport in a single direction, either in or out but not both. ▪ Two channels, left and right. Mono is not support. ▪ Sample rate: 44.1k or 48k. ▪ Sample width is limited to 16-bits. ▪ Supports bit clocks of 32 times the sample rate, 1.4112M (44.1k) or 1.536M (48k) and not adjustable.
Power management	<ul style="list-style-type: none"> • On-chip power-on reset (POR) • Integrated buck (DC-DC) and low drop out (LDO) regulators • On-chip software-controlled power management unit • On-chip 32 kHz low power oscillator (LPO) with optional external 32 kHz crystal oscillator support

Note¹, The I2C interface and the Wi-Fi coexistence pins are multiplexed with the BT_GPIO pins. In the default firmware configuration, both functions cannot be supported.

4 Specifications

Table 3: Vela IF310 Specifications

Feature	Description						
Physical Interface	84-pin LGA package (Including 4 thermal ground pads under the package)						
Bluetooth/BLE Interface	Host Controller Interface (HCI) using high speed UART						
Main Chip	Infineon CYW55310IUBGT 143-pin WLGA package (Including 4 thermal ground pads under the package)						
Input Voltage Requirements	3.3V Typ., 3.0V Min., 4.8V Max.						
I/O Signalling Voltage	Set to 1.8V only, by the power domains connected to VDDIO						
Operating Temperature	-40° to +85°C (-40° to +185°F)						
Operating Humidity	Less than 85% RH (non-condensing)						
Storage Temperature	-40° to +125°C (-40° to +257°F)						
Storage Humidity	Less than 60% RH (non-condensing)						
MSL (Moisture Sensitivity Level)	4 (module), N/A (DVK)						
Maximum Electrostatic Discharge	4kV Indirect application (In compliance with EN 301489)						
Size - mm	All variants: 16mm x 12mm x 1.9 mm						
Weight - g (oz.)	0.0003g (Integrated Antenna) 0.0001g (MHF4)						
Bluetooth Media	Frequency Hopping Spread Spectrum (FHSS)						
Bluetooth Standards	Bluetooth Core 6.0 (at point of launch)						
Bluetooth Data Rates Supported	1, 2, 3 Mbps, 500 Kbps, 125 Kbps						
Bluetooth Modulation	GFSK @ 1 Mbps (BR) $\pi/4$ -DQPSK @ 2 Mbps (EDR) 8-DPSK @ 3 Mbps (EDR) GFSK @ LE-1 Mbps, LE-2 Mbps, LE-LR-500 Kbps, LE-LR-125 Kbps						
Regulatory Certifications	FCC, IC, CE, UKCA, RCM, Japan, and Korea, Bluetooth SIG						
Compliance	<table border="0"> <tr> <td>ACMA AS/NZS 2772.2:2016 Amd 1:2018 AS/NZS 4268:2017+Amd 1:2021</td> <td>FCC FCC Part 15, Subpart B, Class B 47 CFR FCC Part 2.1091 47 CFR FCC Part 15.247</td> </tr> <tr> <td>CE EN 62479:2010 EN 50663:2017 EN 300 328 V2.2.2 EN 62368-1</td> <td>Japan Article 2 Paragraph 1 Item 19</td> </tr> <tr> <td>EMC ICES-003 Issue 7, Class B EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4</td> <td>Korea TBD</td> </tr> </table>	ACMA AS/NZS 2772.2:2016 Amd 1:2018 AS/NZS 4268:2017+Amd 1:2021	FCC FCC Part 15, Subpart B, Class B 47 CFR FCC Part 2.1091 47 CFR FCC Part 15.247	CE EN 62479:2010 EN 50663:2017 EN 300 328 V2.2.2 EN 62368-1	Japan Article 2 Paragraph 1 Item 19	EMC ICES-003 Issue 7, Class B EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4	Korea TBD
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EMC ICES-003 Issue 7, Class B EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4	Korea TBD						
Certifications	Bluetooth® SIG Qualification 						
Warranty	One Year Warranty						

All specifications are subject to change without notice

5 Frequency Reference

The Vela IF310 module **requires** a 32.768 KHz reference oscillator for the sleep clock. An external 32.768 KHz precision oscillator which meets the requirements listed in **Table 4 must be used**.

Table 4: External 32.768 KHz sleep clock specification

Parameter	LPO clock	Unit
Nominal input frequency	32.768	KHz
Frequency accuracy	±250	ppm
Duty cycle	30-70	%
Input signal amplitude	200-3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	> 100 K	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10000	ppm

6 Block Diagram

The Vela IF310 uses Infineon's CYW55310 chipset, which is highly integrated. The module provides three types of RF connectivity options: RF connector type, PCB printed antenna type, and Trace pin type, to accommodate different application needs. In addition, its simplified external circuitry helps reduce overall product size. The module only requires two power inputs, 3.3V and 1.8V, a 32.768 kHz signal, and a "BT_REG_ON" control signal. Vela IF310 provides a wide range of comprehensive interfaces to meet customer application requirements and achieves a highly integrated module in an ultra-compact size (12 mm x 16 mm).

Figure 1 shows the block diagram of the Vela IF310 module.

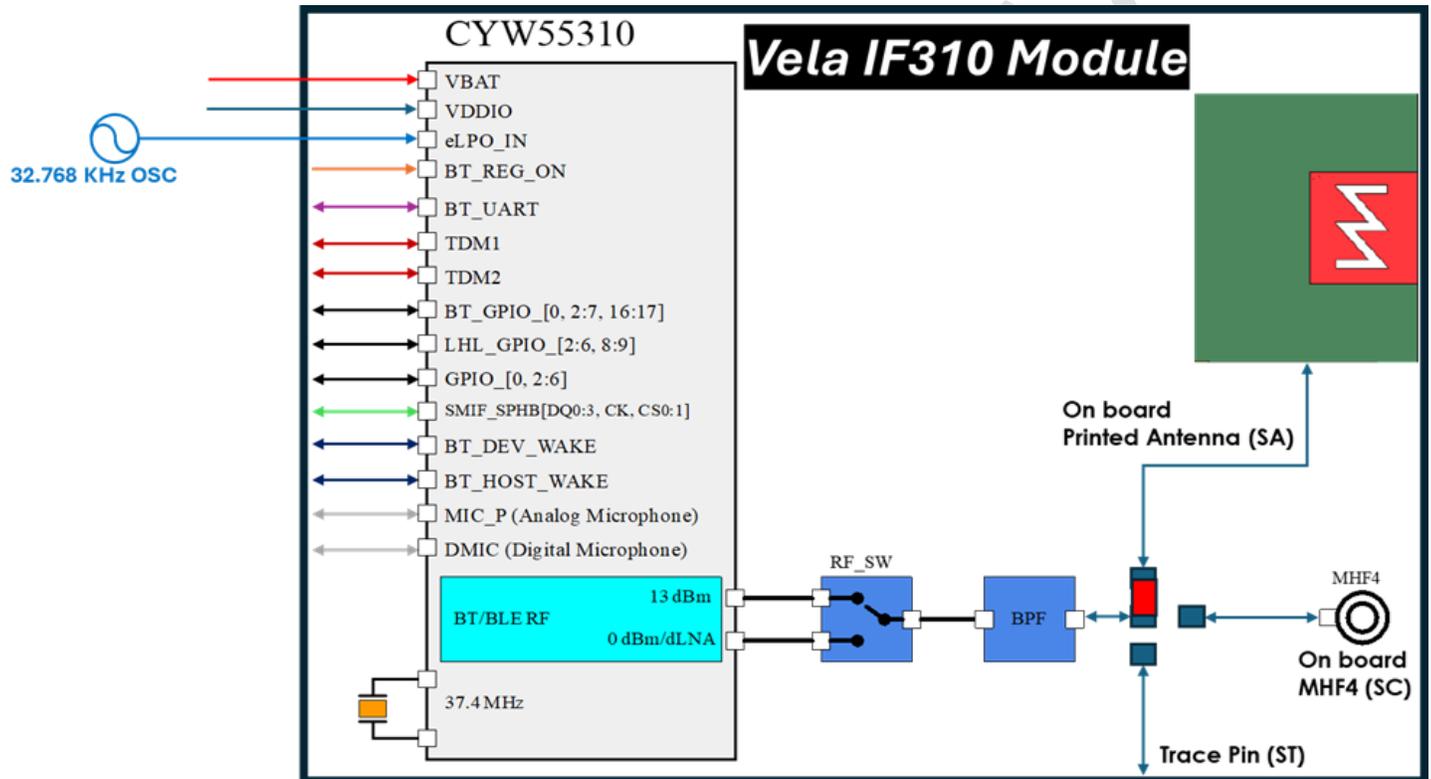


Figure 1: Vela IF310 Module Block diagram

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 5 summarizes the absolute maximum ratings, and Table 6 lists the recommended operating conditions for the Vela IF310 series wireless module. Absolute maximum ratings are the values beyond which permanent damage to the device may occur. Operating the device outside the specified maximum ratings or recommended operating conditions may cause damage and void the warranty.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 5: Absolute maximum ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	-0.5		6.0	V
VDDIO	DC supply voltage for digital I/O	-0.5		2.2	V

7.2 Recommended Operating Conditions

Table 6: Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VBAT	Power supply for Internal Regulators	3.0 ²	3.3	4.8	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8	1.89	V
T-ambient	Ambient temperature	-40	25	85	°C

Note²: IF310 is functional across this range of voltage. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13 V < VBAT < 3.5 V.

7.3 General DC Electrical Characteristics

Table 7 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 7: General DC electrical characteristics (VDDIO supply voltage operating range is defined in Table 6)

Symbol	Parameter	Min	Typ	Max	Unit
Digital I/O pins ³	Input high voltage (VIH)	0.65 x VDDIO	–	–	V
	Input low voltage (VIL)	–	–	0.35 x VDDIO	
	Output high voltage @ 2 mA (VOH)	VDDIO-0.4V	–	–	
	Output low voltage @ 2 mA (VOL)	–	–	0.45	
BT_REG_ON pins	Input high voltage	1.2	–	VBAT	V
	Input low voltage	–	–	0.3	

Note³: Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

8 RF Characteristics

8.1 Bluetooth Radio Characteristics

Table 8 through Table 11 describe the Bluetooth Basic Rate (BR) / EDR / BLE transmitter performance and receiver performance, and current consumption conditions at 25°C.

Table 8: Basic Rate (BR) and EDR transmitter performance (VBAT = 3.3V, VDDIO = 1.8V)

Test Parameter	Conditions	Min	Typ	Max	Bluetooth Spec.	Unit
Frequency Range	–	2402	–	2480	$2400 \leq f \leq 2480$	MHz
TX Output Power ⁴ (Test at MHF4 connector)	BR	–	5.5 4.5 5	7.6 6.5	~ +20	dBm
	EDR 2M	–	2.5	4		
	EDR 3M	–	2.5	4		
Max EIRP	–	–	–	10	–	dBm

Table 9: Basic Rate (BR) receiver performance (VBAT = 3.3V, VDDIO = 1.8V)

Test Parameter	Conditions	Min	Typ	Max	Bluetooth Spec.	Unit
Frequency Range	–	2402	–	2480	$2400 \leq f \leq 2480$	MHz
RX Sensitivity ^{5,6}	GFSK, BER $\leq 0.1\%$, 1 Mbps	–	-91	-89.5	≤ -70	dBm
Maximum Input	–	–	–	-20	≥ -20	dBm

Table 10: Enhanced Data Rate (EDR) receiver performance (VBAT = 3.3V, VDDIO = 1.8V)

Test Parameter	Conditions	Min	Typ	Max	Bluetooth Spec.	Unit
Frequency Range	–	2402	–	2480	$2400 \leq f \leq 2480$	MHz
RX Sensitivity ^{5,6}	$\pi/4$ -DQPSK, BER $\leq 0.01\%$, 2 Mbps	–	-93.5	-92	≤ -70	dBm
	8-DPSK, BER $\leq 0.01\%$, 3 Mbps	–	-87.5	-86	≤ -70	dBm

Table 11: Bluetooth LE RF Specifications (VBAT = 3.3V, VDDIO = 1.8V)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
Rx sensitivity ^{5,6}	GFSK, 30.8% PER, 1 Mbps	–	-97	-95.5	dBm
	GFSK, 30.8% PER, 2 Mbps	–	-93.5	-92	
	GFSK, 30.8% PER, 500 Kbps (S = 2)	–	-102	-100.5	
	GFSK, 30.8% PER, 125 Kbps (S = 8)	–	-107	-105.5	
TX Output Power ⁴ (Test at MHF4 connector)	1 Mbps	–	5.5 4.5 5	7.6 6.5	dBm
	2 Mbps	–	5.5 4.5 5	7.6 6.5	
	500 Kbps (S = 2)	–	5.5 4.5 5	7.6 6.5	
	125 Kbps (S = 8)	–	5.5 4.5 5	7.6 6.5	
Max EIRP	–	–	–	10	dBm

Note⁴: The Bluetooth LE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

Note⁵: Dirty TX is off.

Note⁶: Tolerance could be up to +/- 2.5 dB across operating temperature.

8.2 Transmitter and Receiver Current Consumption

All measured current consumption values are based on the specifications in Section 8.1:

- BR/EDR TX current consumption is measured at the “Max” output power defined in [Table 8](#).
- BR/EDR RX current consumption measurement is performed with the DUT in continuous receiving mode.
- LE and LE-LR TX current consumption is measured at the “Max” output power defined in [Table 11](#).
- LE and LE-LR RX current consumption measurement is performed with the DUT in continuous receiving mode.

Table 12: Bluetooth and Bluetooth LE current consumption

Operating Mode	Data Rate	VBAT = 3.3V	VDDIO = 1.8V	Unit
Transmitter	DH5	19.31	0.1	mA
	2DH5	19.67	0.1	
	3DH5	19.67	0.1	
	LE 1 Mbps	17.36	0.1	
	LE 2 Mbps	15.34	0.1	
	LE-LR 500 Kbps	15.14	0.1	
	LE-LR 125 Kbps	20.14	0.1	
Receiver	DH5	9.26	0.1	mA
	2DH5	9.34	0.1	
	3DH5	9.35	0.1	
	LE 1 Mbps	9.91	0.1	
	LE 2 Mbps	10.25	0.1	
	LE-LR 500 Kbps	10.89	0.1	
	LE-LR 125 Kbps	10.89	0.1	

Note: Current consumption is measured at average of the TX-on time

9 Host Interface Specifications

9.1 High-Speed UART Specifications

The Vela IF310 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The UART supports the Bluetooth® HCI UART specification. The default baud rate is 115.2 Kbaud.

Table 13: UART timing specifications

Reference	Characteristics	Min	Typ	Max	Units
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	

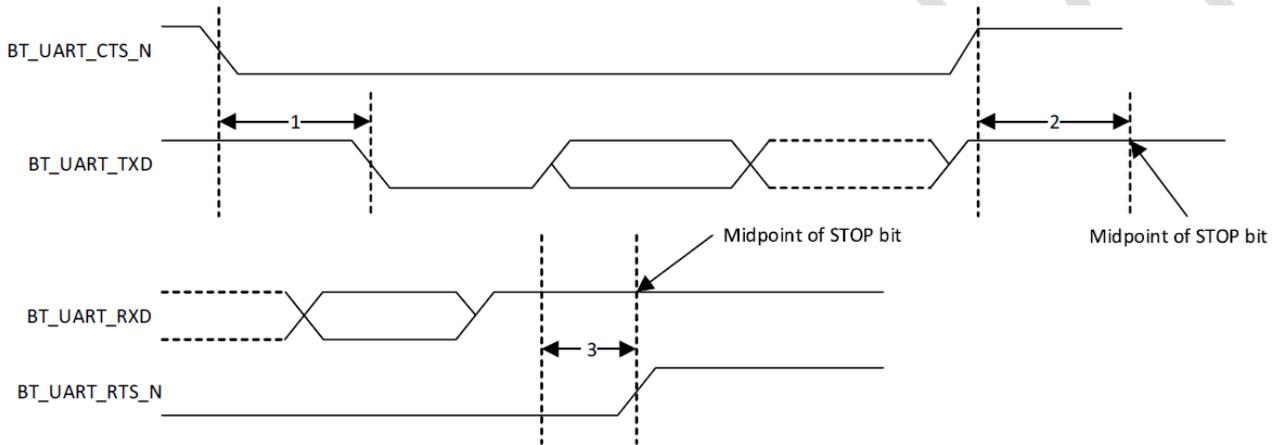


Figure 2: UART timing diagram

9.2 PCM Interface

The Vela IF310 supports two independent PCM interfaces that share the pins with the I2S interfaces. The PCM interface can connect to linear PCM codec devices in master/slave mode. In master mode, IF310 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to IF310.

Figure 3 and Table 13 show the PCM timing diagram and specifications in the Master mode, while Figure 4 and Table 14 show the PCM timing and specifications in the Slave mode.

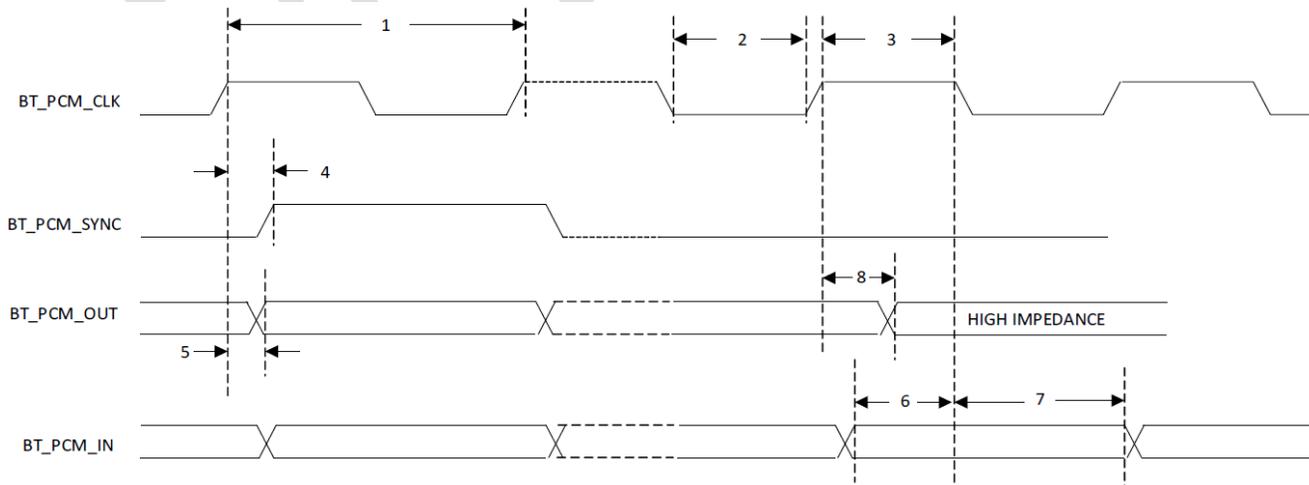


Figure 3: PCM timing diagram (Short frame sync, master mode)

Table 14: PCM interface timing specifications (Short frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Units
1	PCM bit clock frequency	—		12.0	MHz
2	PCM bit clock LOW	41		—	ns
3	PCM bit clock HIGH	41		—	
4	BT_PCM_SYNC delay	0		25.0	
5	BT_PCM_OUT delay	0	—	25.0	
6	BT_PCM_IN setup	8.0		—	
7	BT_PCM_IN hold	8.0		—	
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0		25.0	

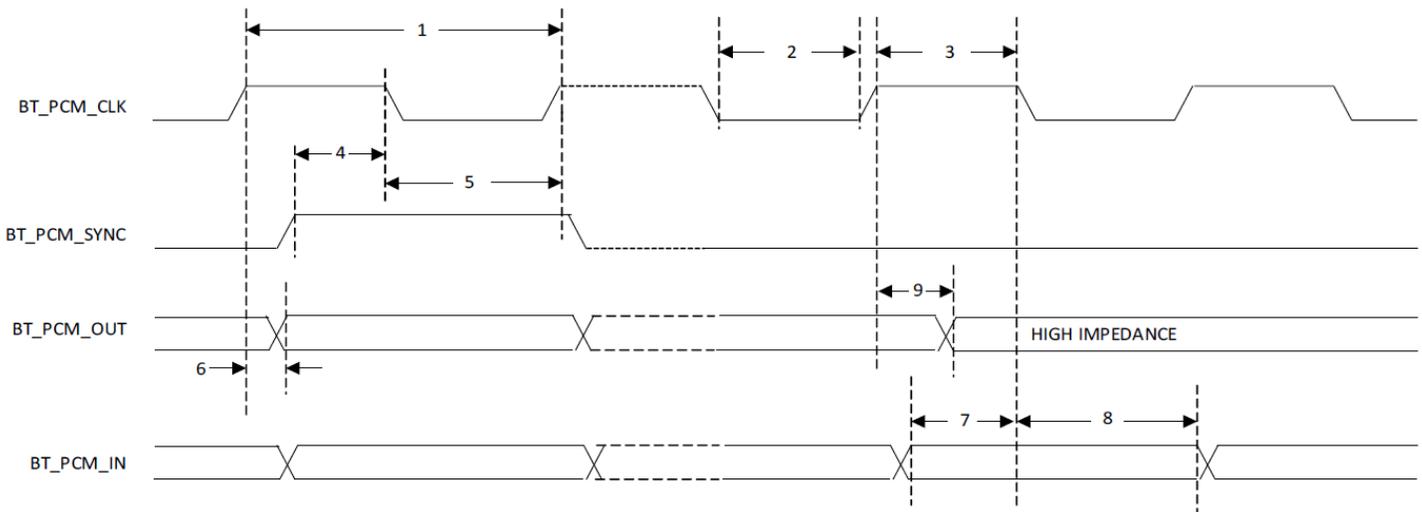


Figure 2: PCM timing diagram (Short frame sync, slave mode)

Table 15: PCM interface timing specifications (Short frame sync, slave mode)

Reference	Characteristics	Min	Typ	Max	Units
1	PCM bit clock frequency	—		12.0	MHz
2	PCM bit clock LOW	41.0		—	ns
3	PCM bit clock HIGH	41.1		—	
4	BT_PCM_SYNC setup	8.0		—	
5	BT_PCM_SYNC hold	8.0		—	
6	BT_PCM_OUT delay	0	—	25.0	
7	BT_PCM_IN setup	8.0		—	
8	BT_PCM_IN hold	8.0		—	
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0		25.0	

10 Power-up sequence and timing

The Vela IF310 has a signal- "BT_REG_ON" that allows the host to control power consumption by enabling or disabling the internal regulator blocks. Figure 5 indicates proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

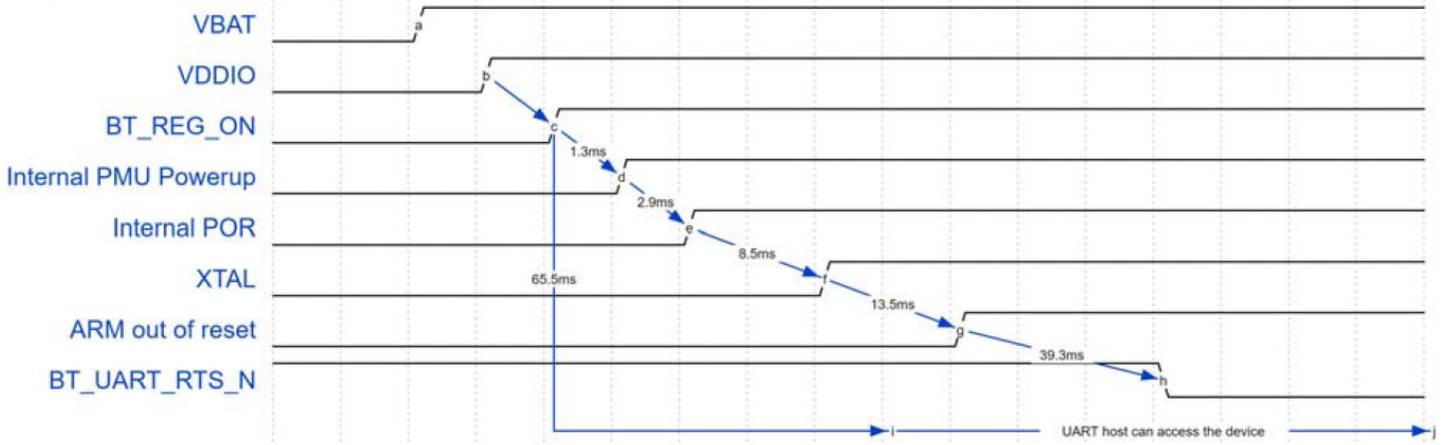


Figure 5: Vela IF310 bootup sequence

11 Module Mechanical and PCB Footprint

Note: There are three module variants: Integrated Antenna, MHF4 connector, and Trace Pin. *It is important to ensure you are using the correct version on your design.*

11.1 Integrated Antenna Variant Mechanical Definition

The module dimensions of integrated antenna variant module is 12 x 16 x 1.9 mm. Detail drawings are shown in Figure 6.

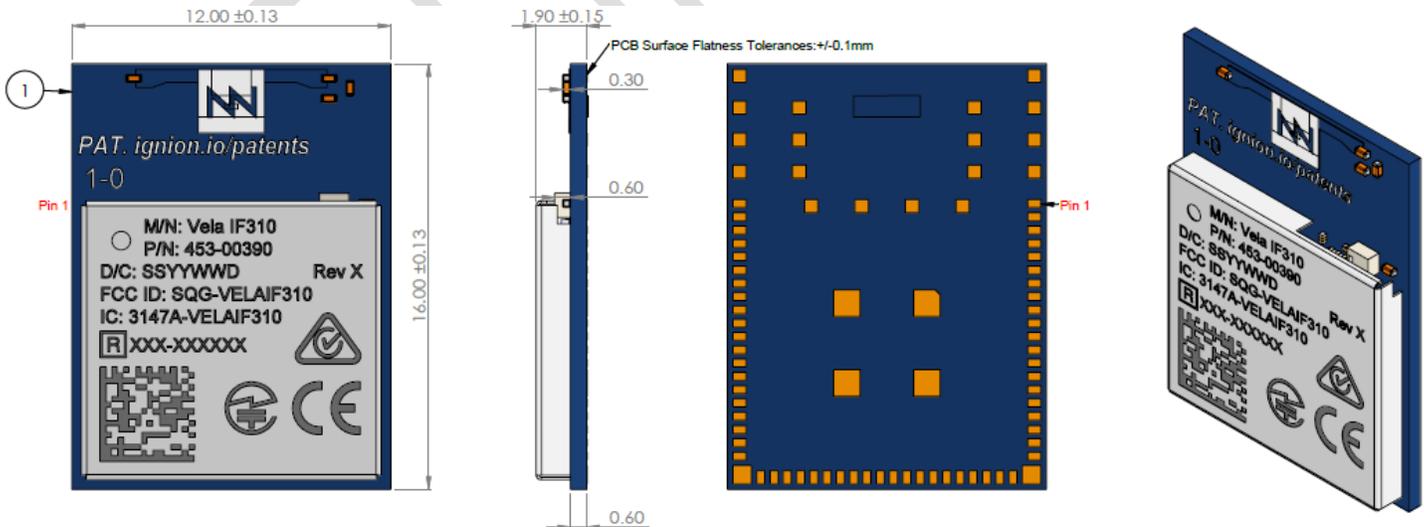


Figure 6: Mechanical Details - Integrated Antenna Variant (453-00390)

11.2 MHF4 Connector Variant Mechanical Definition

The module dimensions of MHF4 connector variant module is 12 x 16 x 1.9 mm. Detail drawings are shown in Figure 7.

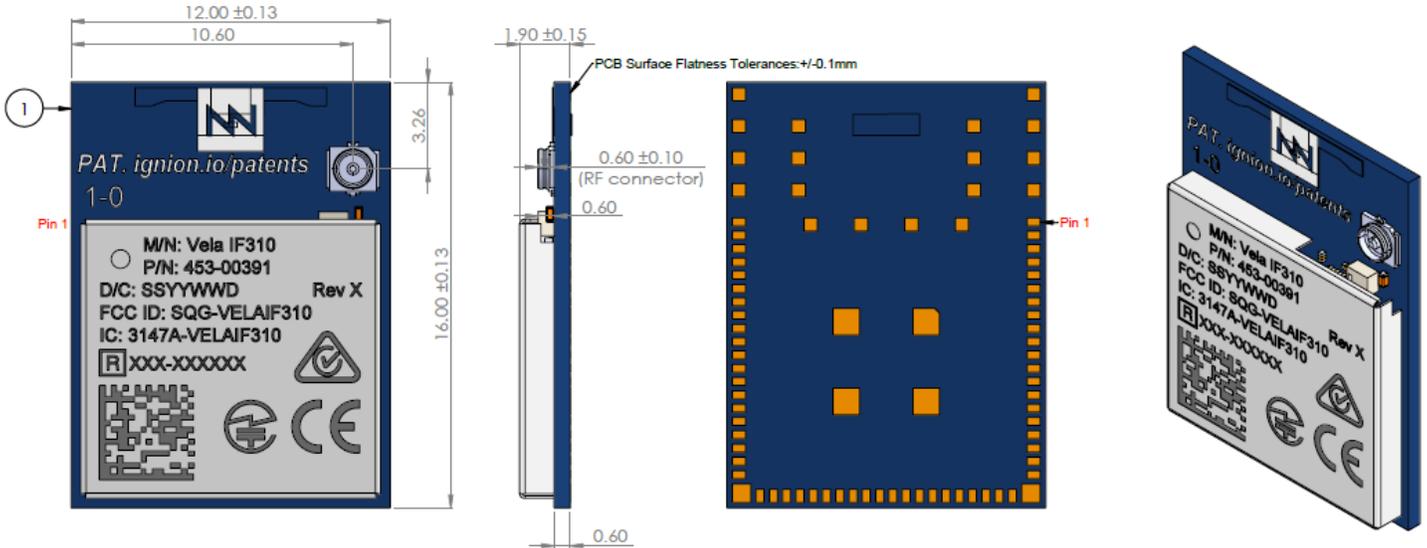


Figure 7: Mechanical Details - MHF4 Connector Variant (453-00391)

11.3 Trace Pin Variant Mechanical Definition

The module dimensions of Trace Pin variant module is 12 x 16 x 1.9 mm. Detail drawings are shown in Figure 8.

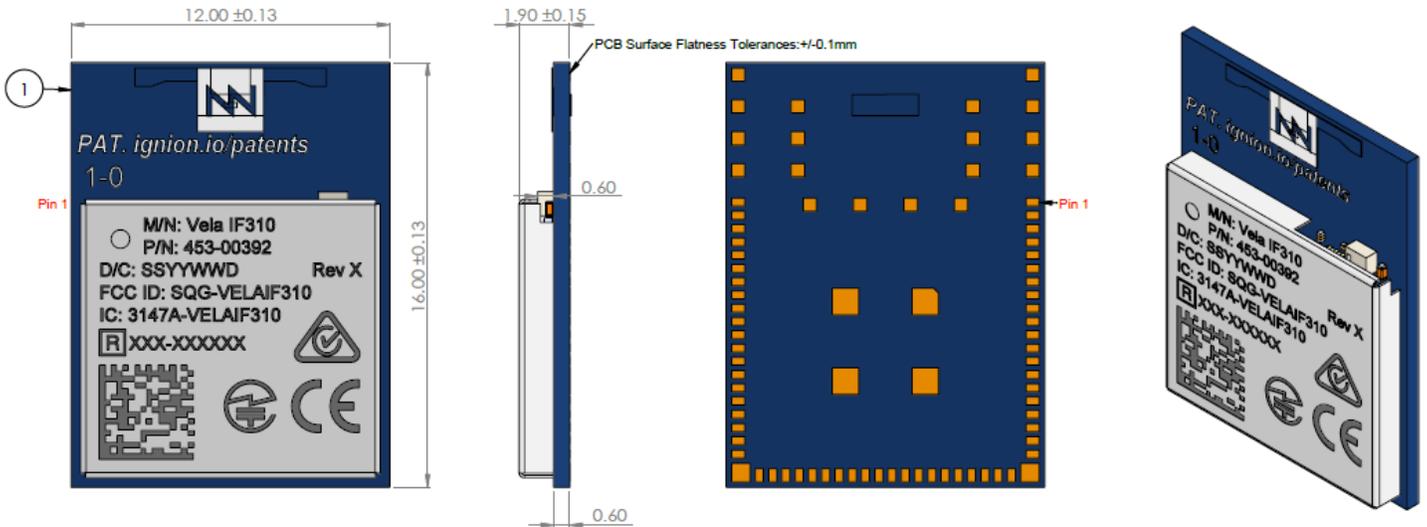


Figure 8: Mechanical Details - Trace Pin Connector Variant (453-00392)

11.4 Module PCB Footprint

The PCB footprint dimensions apply to all module variants, including the Integrated Antenna, MHF4 Connector, and Trace Pin variants.

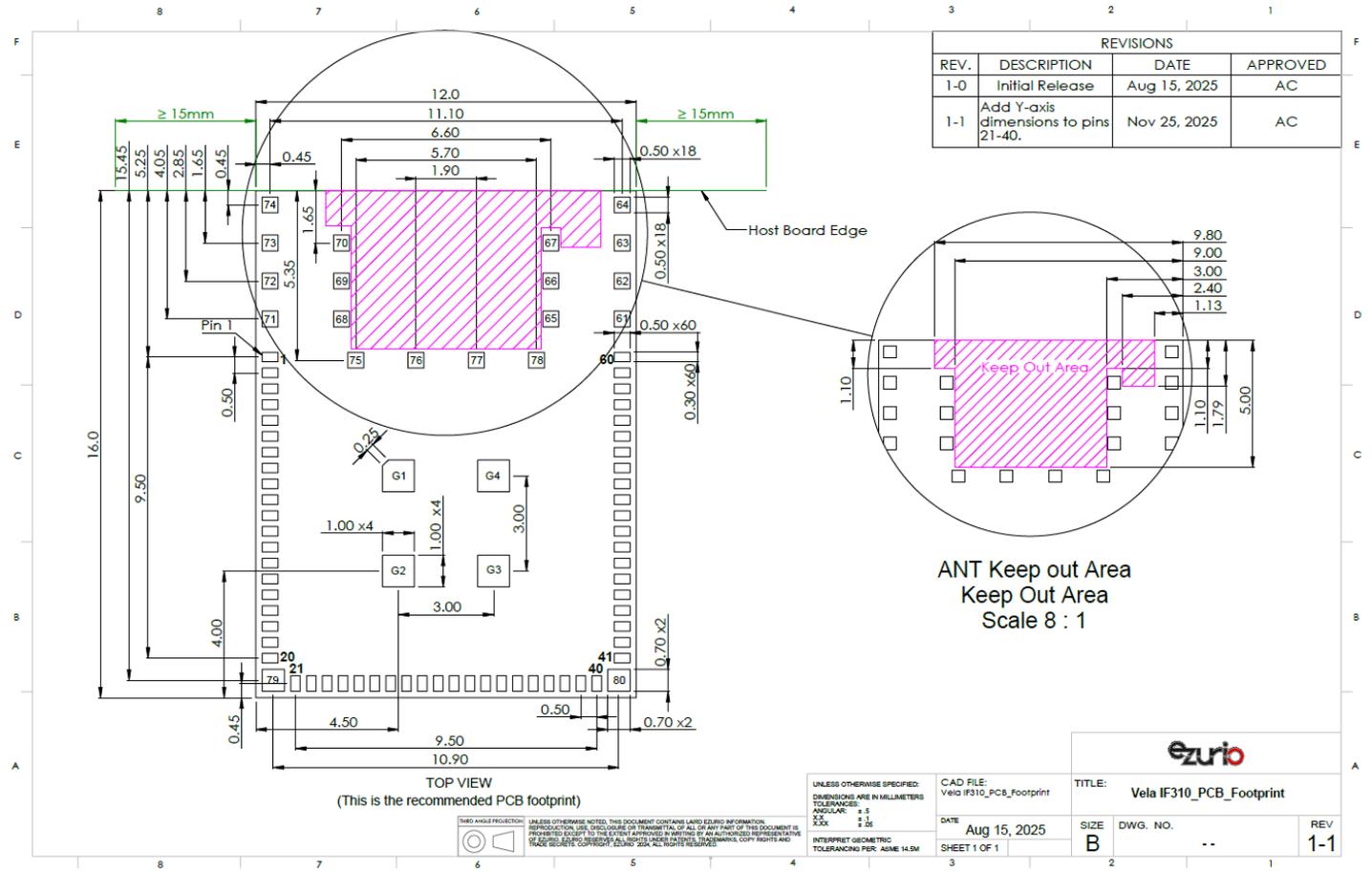


Figure 9: Vela IF310 module PCB footprint (Top view)

12 Module Pin Definition

The pin definitions apply to all module variants, including the Integrated Antenna, MHF4 Connector, and Trace Pin variants.

Table 16: Vela IF310 module pin definitions

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
1	GND	-	-	GROUND	GND
2	GPIO_3	I/O	VDDIO	General-purpose input / output pin	NC
3	GPIO_2	I/O	VDDIO	General-purpose input / output pin	NC
4	GPIO_0	I/O	VDDIO	General-purpose input / output pin	NC
5	GPIO_4	I/O	VDDIO	General-purpose input / output pin	NC
6	GPIO_6	I/O	VDDIO	General-purpose input / output pin	NC
7	GPIO_5	I/O	VDDIO	General-purpose input / output pin	NC
8	BT_UART_RXD	I	VDDIO	UART Serial Input. Serial data input for the HCI UART interface	NC
9	BT_UART_RTSn	O	VDDIO	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.	NC
10	BT_UART_TXD	O	VDDIO	UART Serial Output. Serial data output for the HCI UART interface.	NC
11	BT_UART_CTSn	I	VDDIO	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface	NC
12	GND	-	-	GROUND	GND
13	VDDIO	PWR	1.8V	DC voltage supply for all I/O pins	NC
14	BT_GPIO_6	I/O	VDDIO	Bluetooth general purpose input / output pin <ul style="list-style-type: none"> This pin can be configured as the I2C_SDA function, but additional firmware support is required. This pin combines with pin 24 to form an I2C bus. 	NC
15	BT_GPIO_5	I/O	VDDIO	Bluetooth general-purpose input / output pin	NC
16	BT_GPIO_4	I/O	VDDIO	Bluetooth general-purpose input / output pin <ul style="list-style-type: none"> This pin can be configured as the WLAN_ACTIVE function for 3-wire coexistence, but additional firmware support is required. This pin works with pin 17 and pin 18 to form a 3-wire coexistence bus. 	NC
17	BT_GPIO_3	I/O	VDDIO	Bluetooth general-purpose input / output pin <ul style="list-style-type: none"> This pin can be configured as the BT_PRIORITY function for 3-wire coexistence, but additional firmware support is required. This pin works with pin 16 and pin 18 to form a 3-wire coexistence bus. 	NC
18	BT_GPIO_2	I/O	VDDIO	Bluetooth general-purpose input / output pin <ul style="list-style-type: none"> This pin can be configured as the BT_ACTIVE function for 3-wire coexistence, but additional firmware support is required. This pin works with pin 16 and pin 17 to form a 3-wire coexistence bus. 	NC
19	VBAT	PWR	3.3V	DC supply for module.	-

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
				<ul style="list-style-type: none"> This pin can accept voltage ranges from 3.0 V to 4.8 V. Optimal RF performance is guaranteed between 3.13 V and 3.5 V. 	
20	VBAT	PWR	3.3V	DC supply for module. <ul style="list-style-type: none"> This pin can accept voltage ranges from 3.0 V to 4.8 V. Optimal RF performance is guaranteed between 3.13 V and 3.5 V. 	-
21	BT_REG_ON	I	VDDIO	Enable IF310 module. There is an internal 50 KOhm pull down resistor on this signal	-
22	BT_GPIO_17	I/O	VDDIO	Bluetooth general-purpose input / output pin	NC
23	BT_GPIO_16	I/O	VDDIO	Bluetooth general-purpose input / output pin	NC
24	BT_GPIO_7	I/O	VDDIO	Bluetooth general purpose input / output pin <ul style="list-style-type: none"> This pin can be configured as the I2C_CLK function, but additional firmware support is required. This pin combines with pin 14 to form an I2C bus. 	NC
25	BT_GPIO_0	I/O	VDDIO	Bluetooth general-purpose input / output pin	NC
26	GND	-	-	GROUND	GND
27	MIC_P	I	VDDIO	ADC microphone positive input	NC
28	GND	-	-	GROUND	GND
29	TDM2_SCK	I/O	VDDIO	TDM2 interface slave clock	NC
30	TDM2_WS	I/O	VDDIO	TDM2 interface word select	NC
31	TDM2_MCK	I/O	VDDIO	TDM2 interface master clock	NC
32	TDM2_DO	I/O	VDDIO	TDM2 interface data out	NC
33	TDM2_DI	I/O	VDDIO	TDM2 interface data in	NC
34	SMIF_SPHB_CS0_N_34	O	VDDIO	SMIF chip select 0, active-low output	NC
35	SMIF_SPHB_DQ3_35	I/O	VDDIO	SMIF data line 3	NC
36	SMIF_SPHB_DQ2_36	I/O	VDDIO	SMIF data line 2	NC
37	SMIF_SPHB_CK_37	O	VDDIO	SMIF clock output	NC
38	SMIF_SPHB_DQ1_38	I/O	VDDIO	SMIF data line 1	NC
39	SMIF_SPHB_DQ0_39	I/O	VDDIO	SMIF data line 0	NC
40	SMIF_SPHB_CS1_N_40	O	VDDIO	SMIF chip select 1, active-low output	NC
41	DMIC_CK	I/O	VDDIO	Digital microphone clock	NC
42	DMIC_DQ	I/O	VDDIO	Digital microphone data	NC
43	TDM1_DI	I/O	VDDIO	TDM1 interface data in	NC
44	TDM1_WS	I/O	VDDIO	TDM1 interface word select	NC
45	TDM1_MCK	I/O	VDDIO	TDM1 interface master clock	NC
46	TDM1_SCK	I/O	VDDIO	TDM1 interface slave clock	NC
47	TDM1_DO	I/O	VDDIO	TDM1 interface data out	NC

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
48	LHL_GPIO_9	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
49	LHL_GPIO_3	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
50	LHL_GPIO_2	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
51	LHL_GPIO_6	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
52	LHL_GPIO_8	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
53	LHL_GPIO_5	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
54	LHL_GPIO_4	I/O	VDDIO	Miscellaneous general-purpose input / output	NC
55	eLPO_IN	I	VDDIO	External sleep clock input (32.768 KHz)	-
56	BT_HOST_WAKE	O	VDDIO	Host Wake-up <ul style="list-style-type: none"> The signal from IF310 module to host 	NC
57	BT_DEV_WAKE	I	VDDIO	Bluetooth Device Wake-up <ul style="list-style-type: none"> The signal from host to IF310 module 	NC
58	GND	-	-	GROUND	GND
59	BT_ST	O	-	RF port for the Trace Pin type	NC
60~80	GND	-	-	GROUND	GND
G1~G4	GND	-	-	GROUND	GND

13 Reference Schematic Design

Note: It is recommended to put a 10uF bypass capacitor in the VBAT (pin 19 and pin 20) and VDDIO (pin 13).

A 32.768 KHz external signal is required to be connected to the "eLPO_IN" pin (pin 55). The detailed specifications of the 32.768 kHz clock are provided in [Table 4](#).

A 10K Ohm pull-up resistor is required to be connected to the "BT_REG_ON" pin (pin 21) for the module to work properly. The "BT_REG_EN" voltage operating range is defined in [Table 7](#).

BT_UART signals (x4) are required for flashing EZ-Serial and HCI firmware.

When using a "Trace Pin" type module, it's recommended to reserve space for an external PI-type matching circuit.

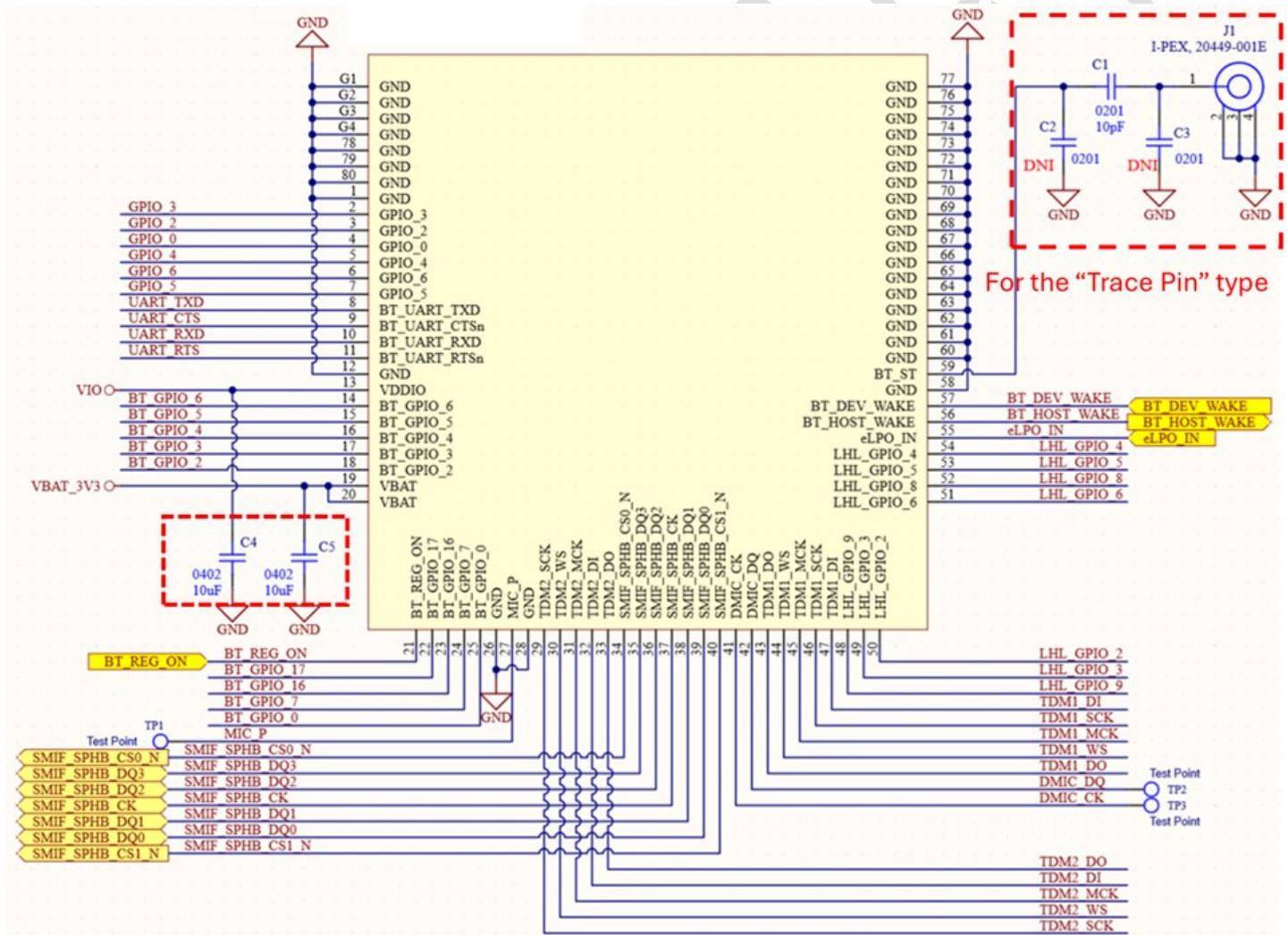


Figure 10: Vela IF310 schematic

14 Flashing Firmware

Vela IF310 firmware programming is done via the HCI UART.

There are two tools to flash a Vela IF310 module detailed in the following link:

TBD

ifx_flasher_cli.exe is a command line tool for flashing Vela IF310 DVK and loose modules. It will auto detect a DVK, but you can also specify a com port for a loose module. When specifying a com port, the cli bypasses the DVK probe auto detect. You can use the `-c` option with the cli to specify a com port.

When flashing a loose module via a particular com port the following should be noted:

- Flashing uses BT_UART_TXD, BT_UART_RXD, BT_UART_CTS, BT_UART_RTS
- Flow control is mandatory.
- Reset line is also required to be able to enter programming mode.
- UART settings are 115200, 8, N, 1
- CTS needs to be low during a reset to enter programming mode.

15 RF Layout Design Guidelines

15.1 General Consideration

The following is a list of RF layout design guidelines and recommendations when installing an Ezurio radio into your device.

- Do not run the antenna cables directly above or directly below the radio.
- Do not place any parts or run any high-speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB insulation between these two antennas.
- Ensure that there is the maximum allowable spacing by separating the antenna connectors on the Ezurio radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Be sure to put a 10uF capacitor on EACH power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU working correctly.

Use proper electro-static-discharge (ESD) procedures when installing the Ezurio radio module. To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.

15.2 Layout Recommendations for Integrated Antenna Variant

The following are recommended for layout of the integrated antenna variant of the Vela IF310:

1. Align module edge with PCB edge.
2. To maintain antenna radiation efficiency, you should reserve a keep-out area on all PCB routing layers, as shown in Figure 11. For detailed dimensions, refer to Figure 9.

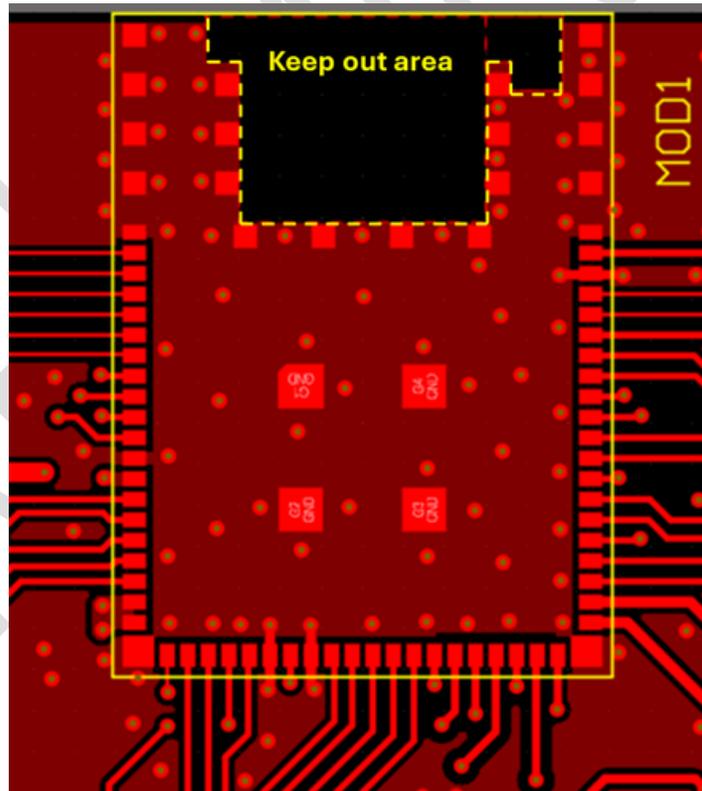


Figure 11: Integrated antenna variant layout keep out area

16 Application Note for Surface Mount Modules

16.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Vela IF310 part numbers – 453-00171R and 453-00172R are shipped as Tape / Reel, with a reel containing 1,000 pcs.

16.2 Module Packaging Configuration

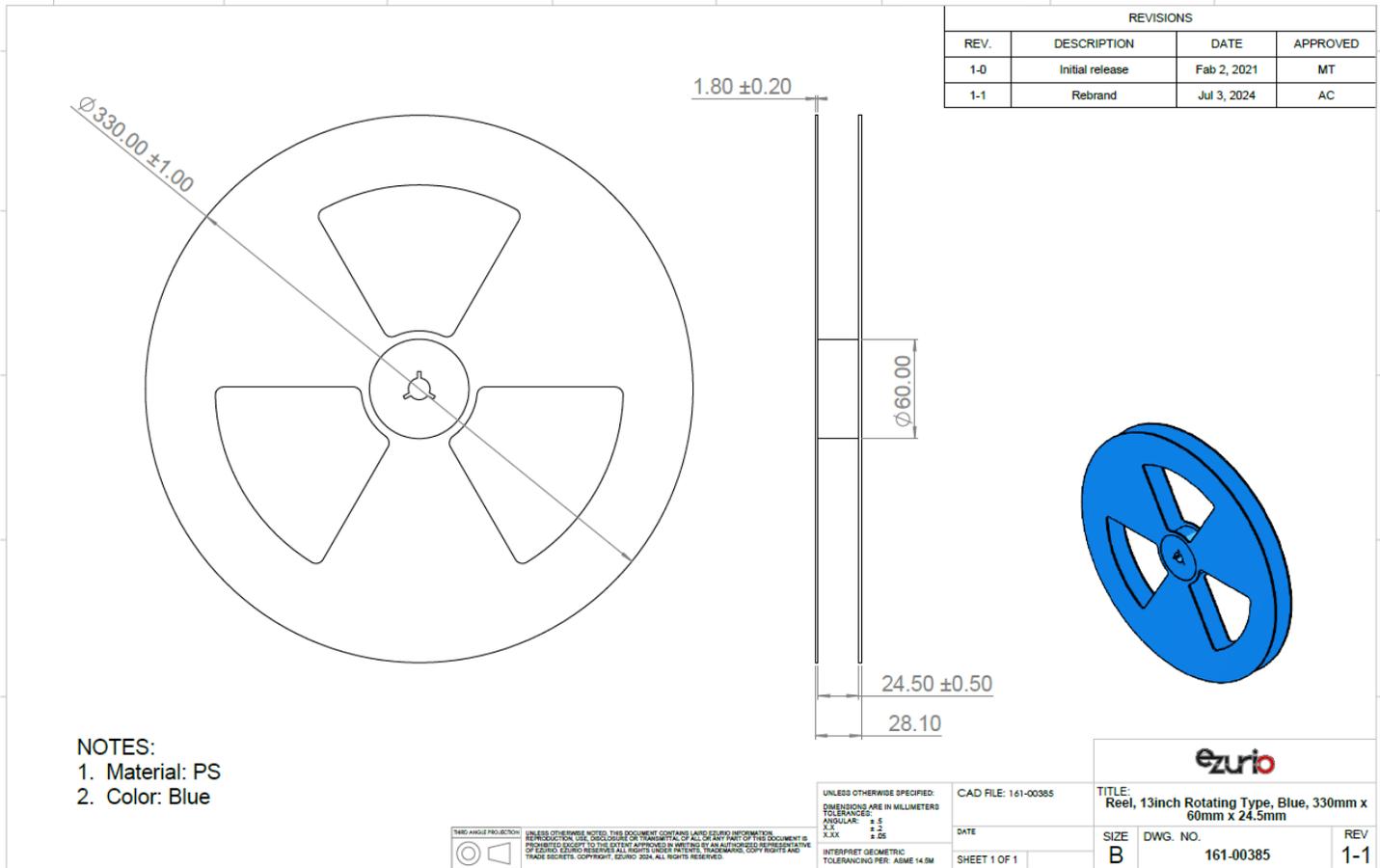
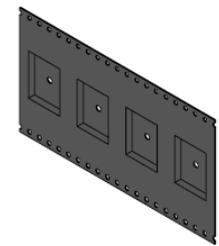
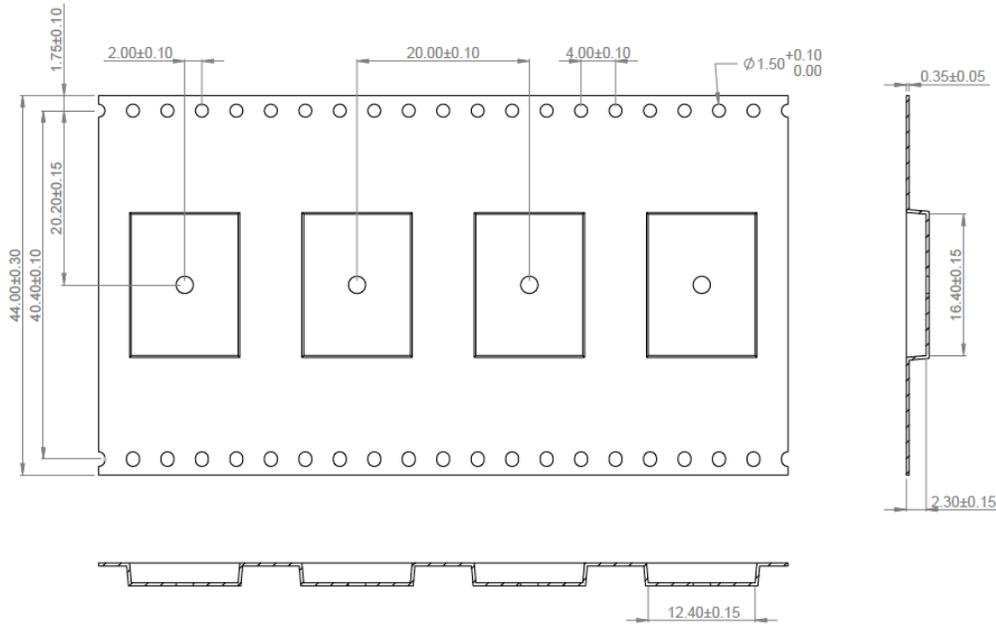


Figure 3: Reel specifications – 1,000 pieces per reel

REVISIONS			
REV.	REVISION NOTE	RELEASED DATE	REVISED BY
1-0	Initial release	Dec 1, 2025	IT



- Notes:
1. Material: Conductive polystyrene, Black
 2. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
 3. Carrier camber not to exceed 1 mm in 250 mm.
 4. All dimensions meet EIA-481-D requirements.
 5. Packing length per 13" reel : 21 Meters.
 6. Component loader per 13" reel : 1000 pcs.



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UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
ANGULAR: \pm
XX \pm
XXX \pm

CAD FILE: 161-00581
DATE
SHEET 1 OF 1 Unit: mm

TITLE: Carrier Tape, Conductive Polystyrene, Black, 12.4mm x 16.4mm x 2.3mm		
SIZE B	DWG. NO. 161-00581	REV 1-0

Figure 4: Carrier Tape specifications for Integrated Antenna Variant

NO.	ITEM NUMBER	REV.	DESCRIPTION	QTY.
1	453-00390	0-2	Module, Vela IF310, Integrated Antenna	1000
2	161-00373	1-1	Bag, ESD and Moisture Barrier, Silver, 520mm x 420mm x 0.15mm	1
3	161-00374	1-1	Box, Single-Wall Corrugated E Flute, 338mm x 343mm x 65mm	1
4	161-00375	1-1	Carton, Double-Wall, AB Flute, 368mm x 354mm x 362mm	1
5	161-00385	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 60mm x 24.5mm	1
6	161-00387	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indicator, 38mm x 105mm	1
7	161-00020	1-0	Desiccant, Silica Gel, 66g, 125mm x 80mm	1
8	160-00560	1-0	Label, Bag and Reel, Product Identifier, Vela IF310, 80mm x 51mm	3
9	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
10	161-00019	1-0	Cover Tape, Anti-static Polyester, 37.5mm x 0.055mm	1
11	161-00581	1-0	Carrier Tape, Conductive Polystyrene, Black, 12.4mm x 18.4mm x 2.3mm	1
12	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
13	160-02075	1-1	Label, Caution ESD, Yellow, 51mm x 51mm	1

REV.	REVISION NOTE	REVISIONS	
		RELEASED DATE	REVISED BY
1-0	Initial release	Dec 3, 2025	IT

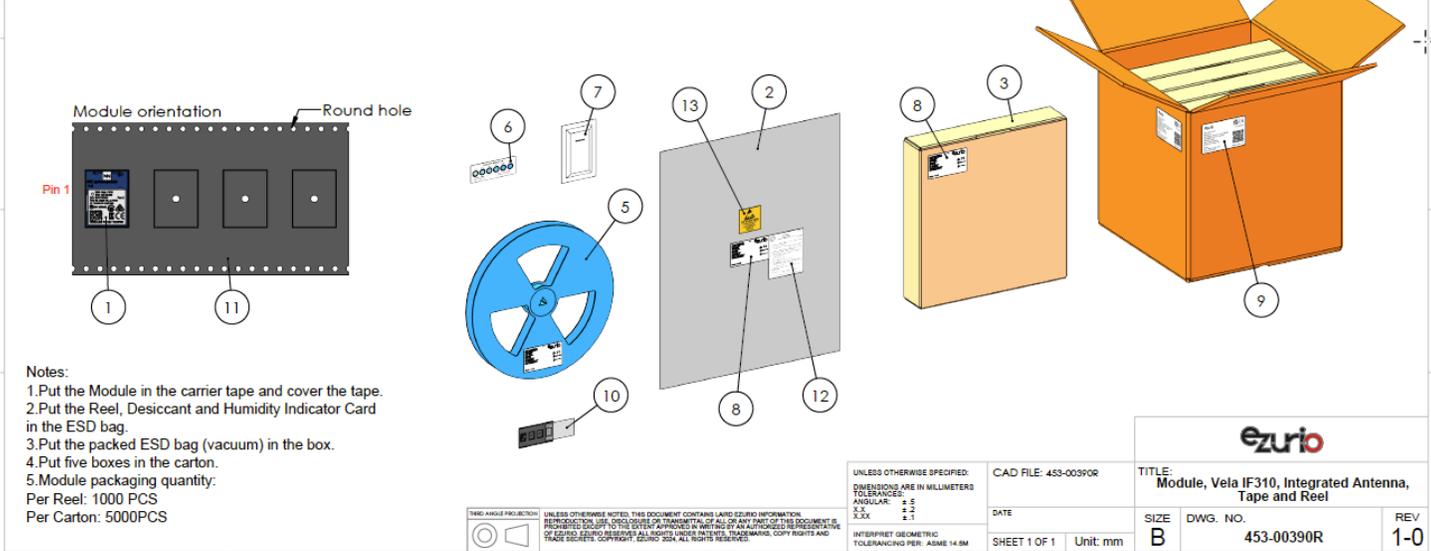


Figure 5: Vela IF310 Packaging Process for Integrated Antenna Variant

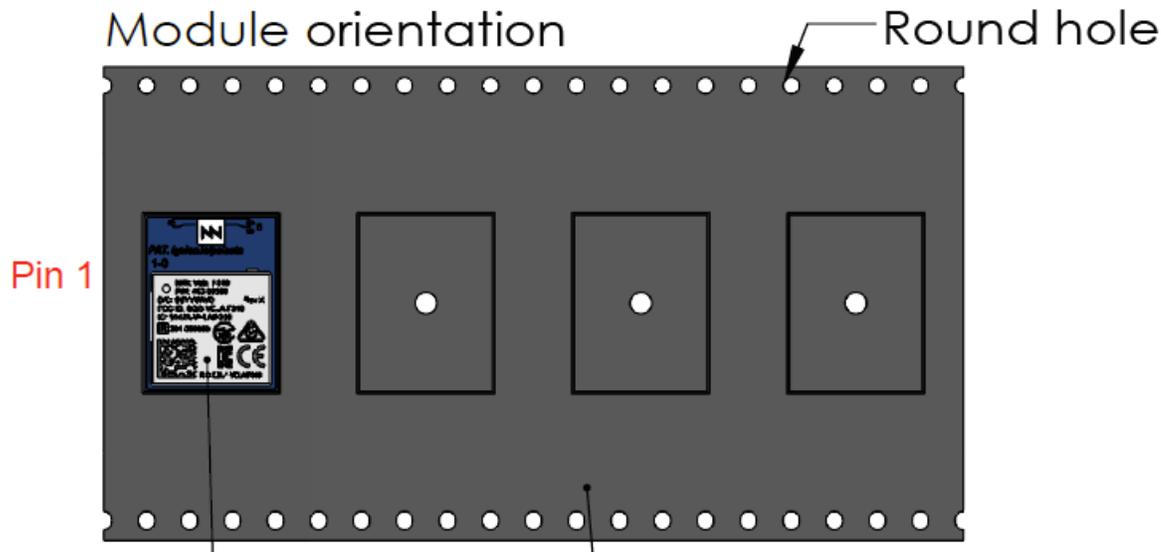


Figure 6: Module Orientation in Carrier Tape Pocket, Integrated Antenna Variant

NO.	ITEM NUMBER	REV.	DESCRIPTION	QTY.
1	453-00391	0-2	Module, Vela IF310, MHF4	1000
2	161-00373	1-1	Bag, ESD and Moisture Barrier, Silver, 520mm x 420mm x 0.15mm	1
3	161-00374	1-1	Box, Single-Wall Corrugated E Flute, 338mm x 343mm x 69mm	1
4	161-00375	1-1	Carton, Double-Wall, AB Flute, 368mm x 354mm x 362mm	1
5	161-00385	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 60mm x 24.5mm	1
6	161-00387	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indicator, 38mm x 105mm	1
7	161-00020	1-0	Desiccant, Silica Gel, 96g, 125mm x 80mm	1
8	160-00560	1-0	Label, Bag and Reel, Product Identifier, Vela IF310, 86mm x 51mm	3
9	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
10	161-00019	1-0	Cover Tape, Anti-static Polyester, 37.5mm x 0.055mm	1
11	161-00561	1-0	Carrier Tape, Conductive Polystyrene, Black, 12.4mm x 16.4mm x 2.3mm	1
12	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
13	160-02075	1-1	Label, Caution ESD, Yellow, 51mm x 51mm	1

REVISIONS			
REV.	REVISION NOTE	RELEASED DATE	REVISED BY
1-0	Initial release	Dec 3, 2025	IT

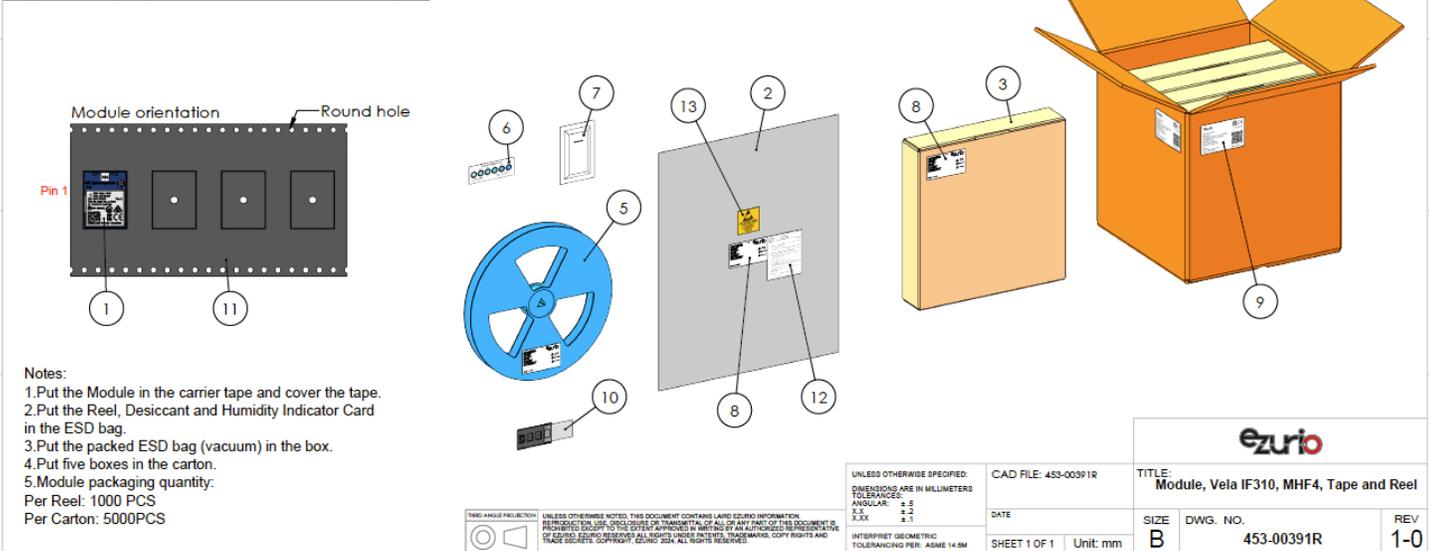


Figure 7: Vela IF310 Packaging Process for MHF4 Variant

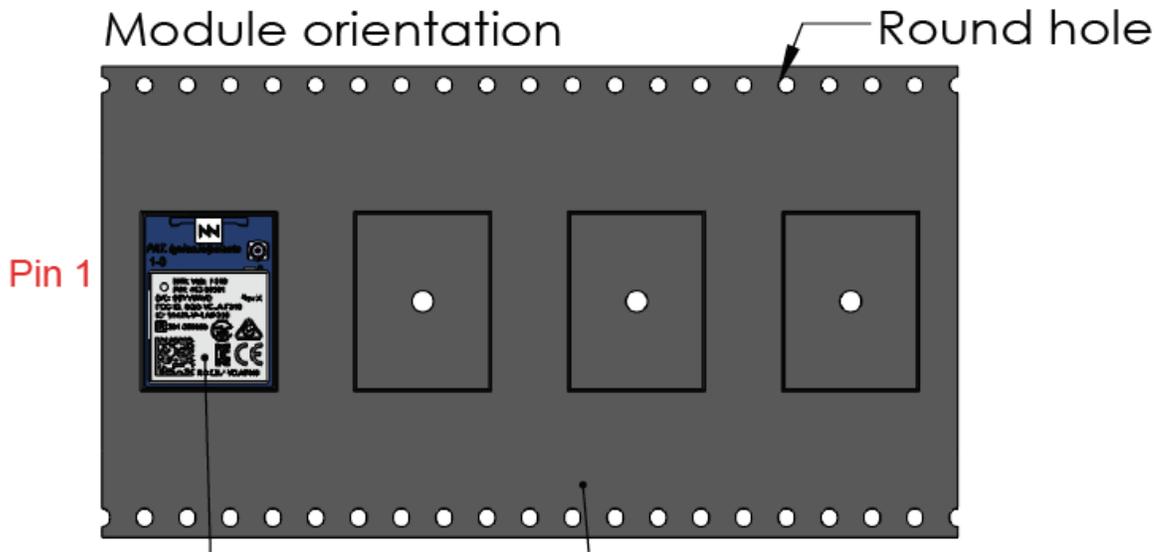


Figure 8: Module Orientation in Carrier Tape Pocket, MHF4 Variant

16.4 Labeling

The following labels are placed on the anti-static bag. The Vela IF310 solder-down modules are classified as MSL4 devices.

Figure 11: Moisture Sensitivity Level Label



Figure 12: Product Identifier Label

The following labels are placed on the pizza box.



Figure 13: Product Identifier Label

The following labels are placed on the master shipping carton.



Figure 14: Standard Shipping Carton Label

16.5 Required Storage Conditions

16.5.1 Prior to Opening the Dry Packing

The following are required storage conditions *prior to opening the dry packing*:

- Normal temperature: 5~40 °C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

16.5.2 After Opening the Dry Packing

The following are required storage conditions *after opening the dry packing* (to prevent moisture absorption):

- Storage conditions for one-time soldering:
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
 - Storage conditions following opening and prior to performing the 1st reflow:
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: A hours or less after opening
 - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: B hours or less after completion of the 1st reflow

Note: Should keep A+B within 72 hours.

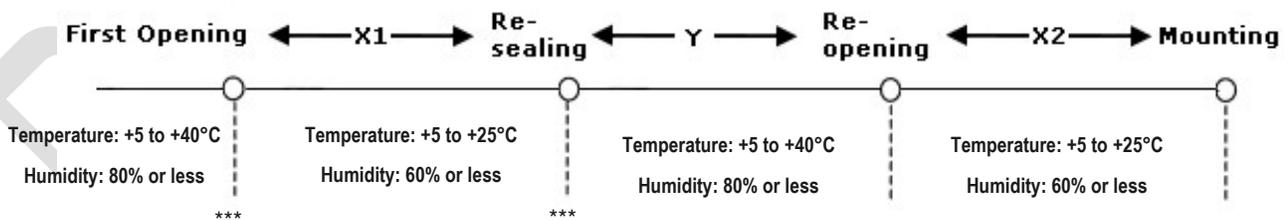
16.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
 - X1+X2 – Refer to **After Opening the Dry Packing** storage requirements. Keep is X1+X2 within 72 hours.
 - Y – Keep within two weeks or less.

16.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40°C and <80% relative humidity.

- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <math> < 30^{\circ}\text{C}</math> and <math> < 60\%</math> relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125°C ($\pm 5^{\circ}\text{C}$).

16.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

16.7.1 Soldering

Note: When soldering, the stencil thickness should be $\geq 0.1\text{ mm}$.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point - IC package surface
- Temperature profile:

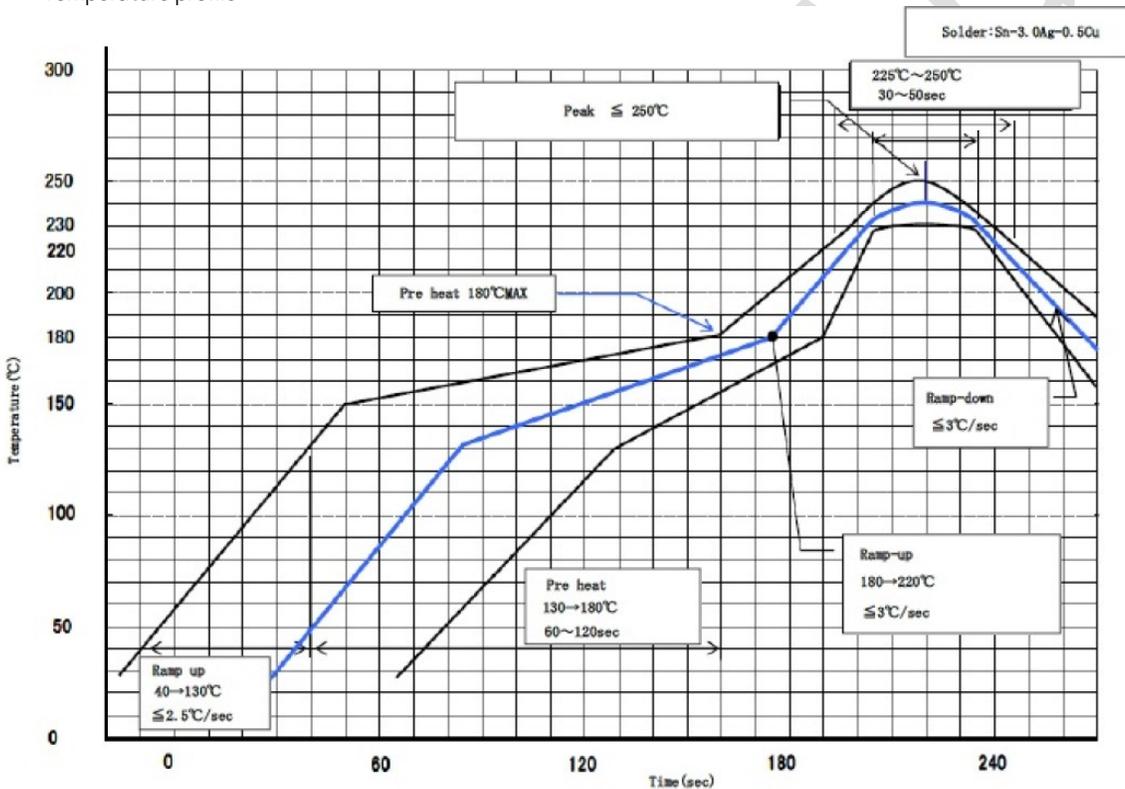


Figure 15: Temperature profile

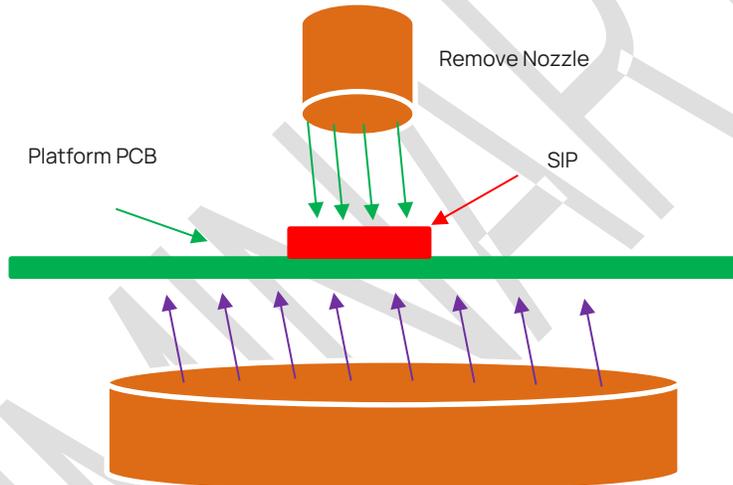
- Ramp-up: 40-130 °C. Less than 2.5 °C/sec
- Pre heat: 130-180 °C 60-120 sec, 180 °C MAX
- Ramp-up: 180-220 °C. Less than 3 °C/sec
- Peak Temperature: MAX 250 °C
 - 225 °C ~ 250 °C, 30 ~ 50 sec
- Ramp-down: Less than 3 °C/sec

16.7.2 Cautions When Removing the SIP from the Platform for RMA

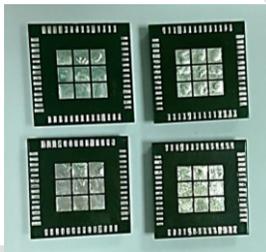
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
 - Set the hot plate at 280 °C.
 - Put the platform on the hot plate for 8~10 seconds.
 - Remove the SIP from platform.
- Two-side components platform:
 - Use two hot air guns
 - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
 - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.

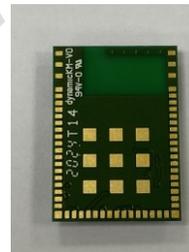


- Remove the residue solder under the bottom side of SIP. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Example SIP with residue solder on the bottom



(Accepted for RMA analysis)

Example Module, no residue solder

- Remove and clean the residue flux as needed.

16.7.3 Precautions for Use

- Opening/handling/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The Vela IF310 modules are MSL 4 rated.

17 Reliability Test

17.1 Climatic And Dynamic Reliability Test

Table 4: Climatic and Dynamic Reliability Test Results for Vela IF310 Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 85°C Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	Pass
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	Pass

17.2 Reliability MTBF Prediction

Table 5: MTBF Predictions for Vela IF310 Modules

Ezurio Part Number	Environment	Standard	Test Result 45 °C (Hours)
453-00390R	Ground, Fixed, Uncontrolled	Telcordia Issue 3	
453-00390C			
453-00391R			
453-00391C			
453-00392R			
453-00392C			
453-00390R	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	
453-00390C			
453-00391R			
453-00391C			
453-00392R			
453-00392C			
Ezurio Part Number	Environment	Standard	Test Result 85 °C (Hours)
453-00390R	Ground, Fixed, Uncontrolled	Telcordia Issue 3	
453-00390C			
453-00391R			
453-00391C			
453-00392R			
453-00392C			
453-00390R	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	
453-00390C			
453-00391R			
453-00391C			
453-00392R			
453-00392C			

18 Regulatory

Full regulatory information on the Vela IF310, including the Regulatory Information Guide, grants, and test reports are available on the [Vela IF310 product page](#) (coming soon).

The Vela IF310 holds current certifications in the following countries:

Table 6: Vela IF310 Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-VELAIF310
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-VELAIF310
Japan (MIC)	201-250863
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	R-C-EZU1-VELAIF310

18.1 Certified Antennas for the Vela IF310

Table 7: Certified Antennas for Vela IF310 Modules

Model	MPN	Manufacturer	Type	Connector	Peak Gain (2400 – 2500 MHz)
NanoBlue	EBL2400A1-10MH4L	Ezurio (Laird Connectivity)	PCB Antenna	IPEX MHF4	2 dBi
FlexPIFA	001-0022	Ezurio (Laird Connectivity)	Planar Inverted-F Type	IPEX MHF4	2 dBi
EDA-8709-2G4C1-B27-CY	EDA-8709-2G4C1-B27-CY (Ezurio Part#0600-00057)	MAG.LAYERS	Dipole	IPEX MHF4	2.32 dBi
mFlexPIFA	EFA2400A3S-10MH4L	Ezurio (Laird Connectivity)	Planar Inverted-F Type	IPEX MHF4	2 dBi
i-FlexPIFA	EFG2401A3S-10MH4L	Ezurio (Laird Connectivity)	PIFA	IPEX MHF4	2 dBi
PCB Trace	NN00-101	IGNION	Printed Antenna	N/A	3.2 dBi

19 Ordering Information

Table 8: Vela IF310 Ordering Part Numbers

Part	Description
453-00390R	Module, Vela IF310, Integrated Antenna, Tape and Reel
453-00390C	Module, Vela IF310, Integrated Antenna, Cut Tape
453-00391R	Module, Vela IF310, MHF4, Tape and Reel
453-00391C	Module, Vela IF310, MHF4, Cut Tape
453-00392R	Module, Vela IF310, Trace Pin, Tape and Reel
453-00392C	Module, Vela IF310, Trace Pin, Cut Tape
453-00390-K1	Development Kit, Module, Vela IF310, Integrated Antenna
453-00391-K1	Development Kit, Module, Vela IF310, MHF4

19.1 General Comments

This is a preliminary datasheet. Please check with Ezurio for the latest information before commencing a design. If in doubt, ask. For additional information visit [Vela IF310 product page](#).

20 Bluetooth Qualification Process

20.1 Overview

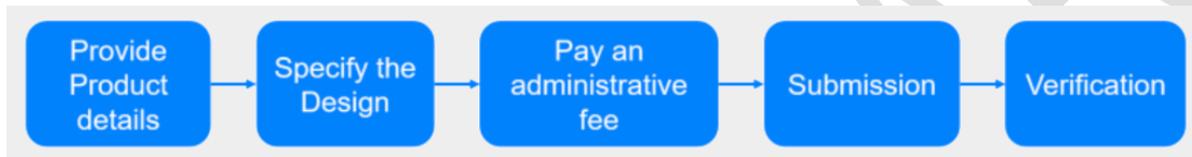
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the [Qualification Program Reference Document \(QPRD\) v3](#).

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: [Apply for Adopter Membership](#)

20.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the [Qualification Program Reference Document v3](#)).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

20.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: <https://qualification.bluetooth.com/>
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
 - Project Name (this can be the product name or the Bluetooth Design name).
 - Product Description
 - Model Number

- Product Publication Date (the product publication date may not be later than 90 days after submission)
 - Product Website (optional)
 - Internal Visibility (this will define if the product will be visible to other users prior to publication)
 - If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.
4. Specify the Design:
- Do you include any existing Design(s) in your Product? Answer Yes, I do.
 - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
 - Select 'I'm finished entering DN's
 - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
 - What do you want to do next? Answer, 'Combine unmodified Designs'.
 - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
 - An active TCRL will be selected for the design.
 - Perform the Consistency Check, which should result in no inconsistencies
 - If there are any inconsistencies these will need to be resolved before proceeding
 - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
- a. As no modifications have been made to the combined designs the tool should report the following message:
'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
 - b. Save and go to Product Qualification fee
6. Product Qualification Fee:
- It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
 - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
 - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
 - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
- Some automatic checks occur to ensure all submission requirements are complete.
 - To complete the listing any errors must be corrected
 - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
 - Now select 'Complete the Submission'.
 - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
 - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
- a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:

<https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/>

20.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + AIROC™ Bluetooth Host Software Stack (Ezurio Vela IF310-based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Vela IF310	Ezurio			
AIROC™ Bluetooth Host Software Stack	Infineon	D065385	223736	https://qualification.bluetooth.com/ListingDetails/194929

20.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the [Getting Started](#) page, Actions, Qualify More Products. The tool will take you through the updating process.

21 453-00171 Integrated Printed Antenna Performance

The following are details and plots of the measured radiation performance of the antenna on the Vela IF310 module with integrated printed antenna (part numbers 453-00171R and 453-00171C).

21.1 Summary of Antenna Performance

Technical Feature	2400 MHz – 2500 MHz
Average Efficiency	>60 %
Peak Gain	3.2
VSWR	< 3:1
Radiation Pattern	Omnidirectional
Polarization	Linear
Weight (approx.)	0 g.
Temperature	-40 to +125°C
Impedance	50 Ω
Dimensions (L x W x H)	2.5 mm x 2.4 mm x 0.6 mm

Note: The result is measured with Ezurio DVK part # 453-00171-K1.

21.2 2.4GHz Radiated Performance and Peak Gain

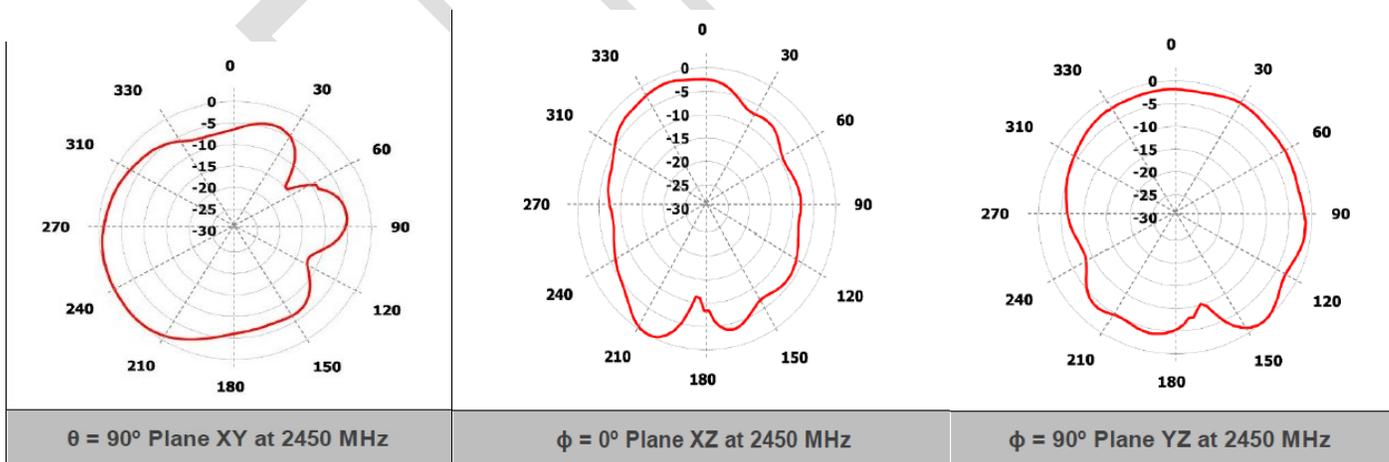
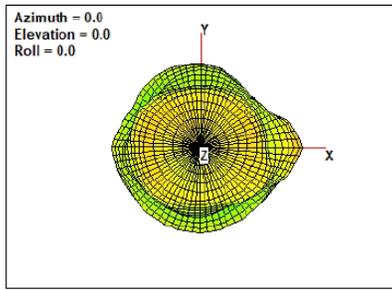
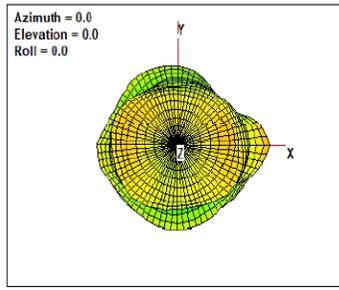


Figure 16: 2450 MHz radiation pattern

2402MHz



2440MHz



2480MHz

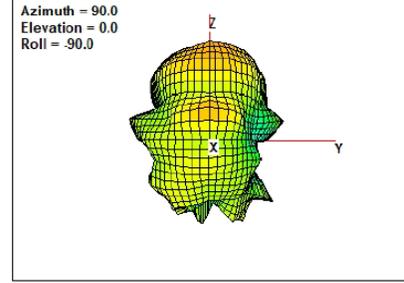
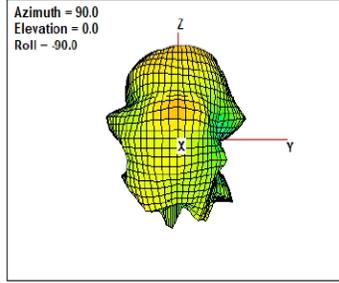
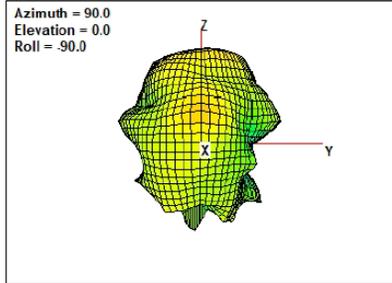
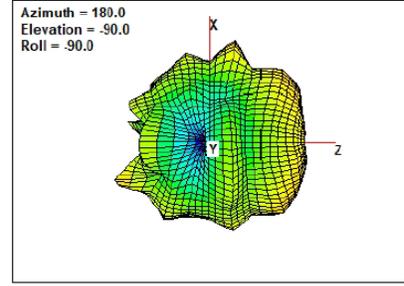
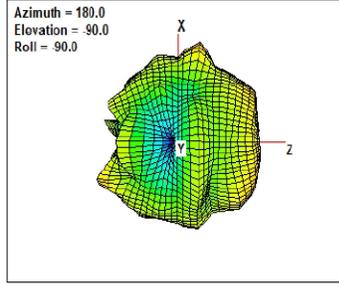
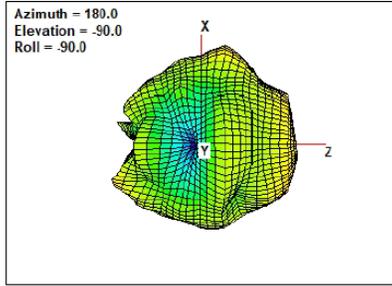
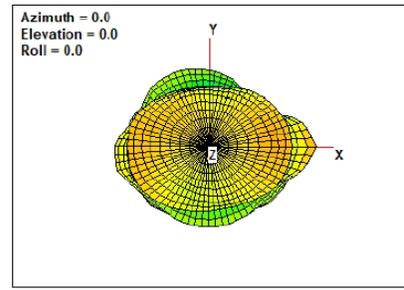


Figure 32: 2402 MHz 3D pattern

Figure 33: 2440 MHz 3D pattern

Figure 34: 2480 MHz 3D pattern

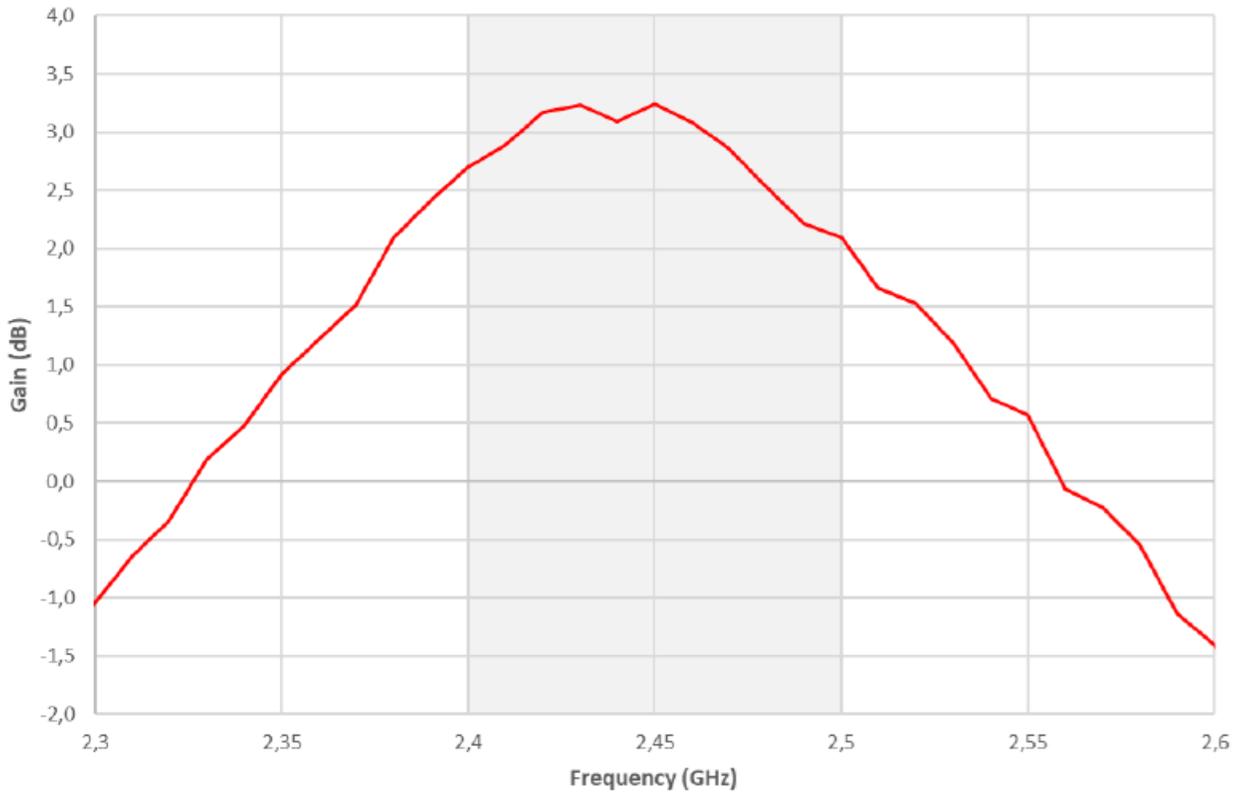


Figure 17: Peak Gain

PRELIMINARY

22 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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