TPS1686x 9V to 80V, 16mΩ, 10A Integrated Hotswap (eFuse) With Accurate And Fast Current Monitor

ADVANCE INFORMATION

1 Features

- Input operating voltage range: 9V to 80V
  - 92V absolute maximum
  - Withstands negative voltages up to –5V at output
- UIntegrated FET with low on resistance: R_{ON} = 16mΩ (typ)
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Adjustable overvoltage protection
- Adjustable output slew rate control (dVdt) for inrush current protection
- Precise load current monitoring
  - <3% error for >50% current
  - 1MHz bandwidth
- Robust overcurrent protection
  - Circuit-breaker response
  - Adjustable threshold: 1A to 10A
  - Overcurrent protection accuracy: ±3% (typ)
  - Adjustable transient overcurrent timer (ITIMER) to support peak currents
- Fast trip response to short-circuit events
- Overtemperature protection (OTP) with analog die temperature monitor output (TEMP)
  - FET SOA: 0.7W√s
- FET health monitoring and reporting
- Fault indication pin ($\overline{FLT}$)
- Power Good indication pin (PGOOD)
- UL 2367 recognition(planned)
- IEC 62368-1 CB certification (planned)
- Small footprint: QFN 6 × 5mm
  - IPC9592B clearance for 60V

2 Applications

- Fan loads in servers
- Input hotswap and hotplug
- Server and high performance computing
- Network interface cards
- Graphics and hardware accelerator cards
- Data center switches and routers
- Fire alarm control panel

3 Description

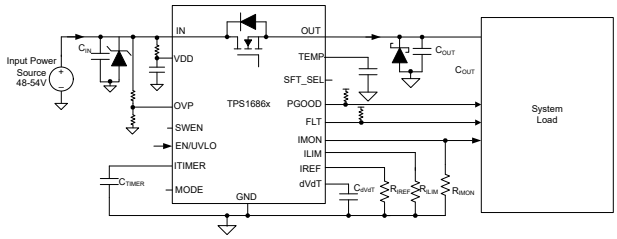
The TPS1686x is an integrated high current circuit protection and power management device. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short circuits and excessive inrush current. Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit level can be set by user as per system needs. A user adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse. An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management such as Intel PSYS and PROCHOT to optimize server and data-center performance.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS16860NLMR	NLM (VQFN, 23)	6.00mm × 5.00mm
TPS16861NLMR		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

PART NUMBER	FAULT BEHAVIOR
TPS16860	Auto-retry
TPS16861	Latch-off

5 Pin Configuration and Functions

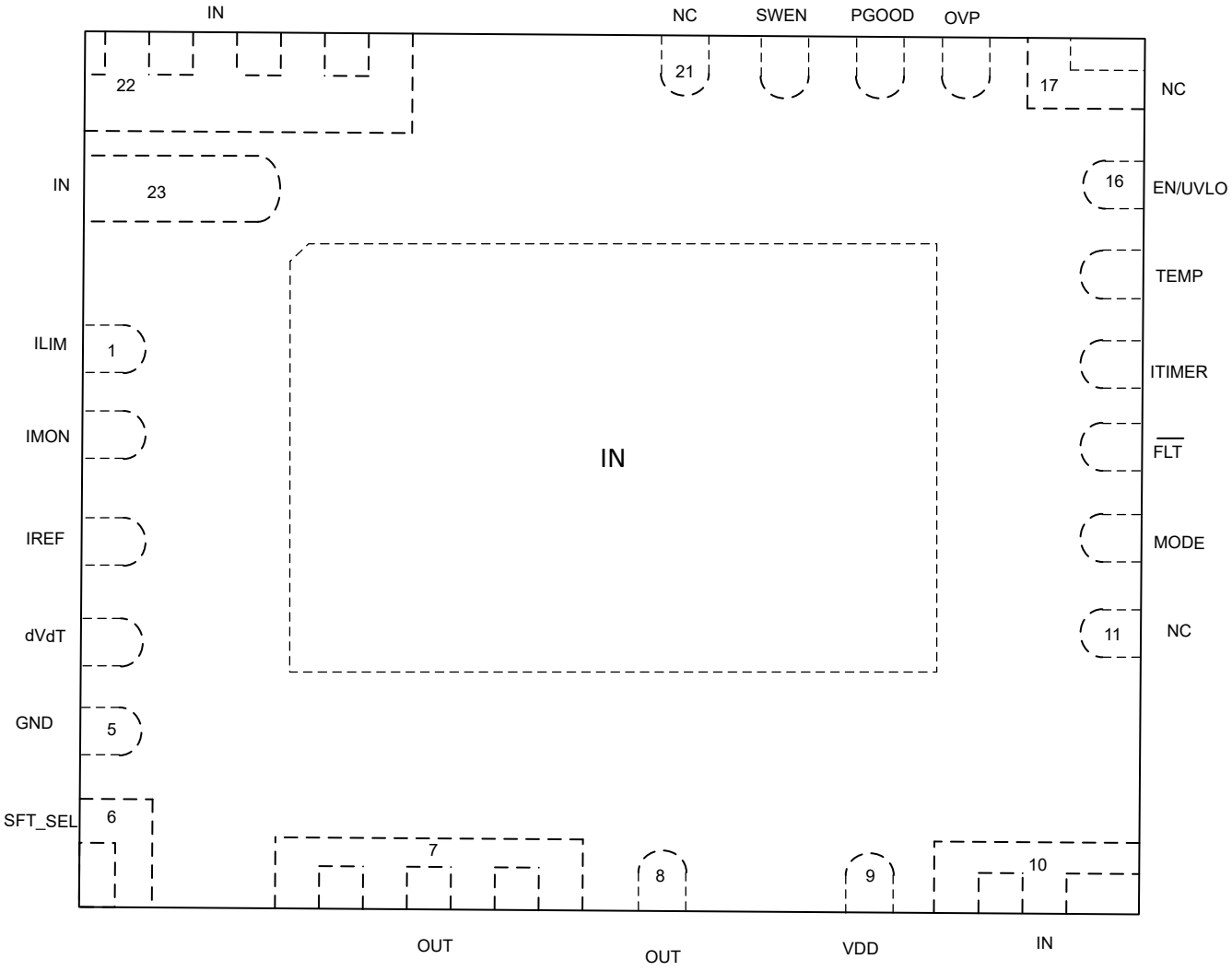

Figure 5-1. NLM Package, 23-Pin VQFN (top view)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ILIM	1	I/O	Outputs a proportional current to the load current. Connect an external resistor from this pin to GND to monitor the load current.
IMON	2	I/O	An external resistor from this pin to GND sets the overcurrent protection threshold and fast-trip threshold during steady-state. This pin also acts as a fast and accurate analog output load current monitor signal during steady-state. *Do not leave floating.*
IREF	3	I/O	Reference voltage for overcurrent, short-circuit protection and active current sharing blocks. Can be generated using internal current source and resistor on this pin, or can be driven from external voltage source. *Do not leave floating.*
dVdT	4	I/O	Start-up output slew rate control pin. Leave this pin open to allow fastest start-up. Connect capacitor to ground to slow down the slew rate to manage inrush current.
GND	5	G	Device ground reference pin. Connect to system ground.
SFT_SEL	6	I/O	Selects the Scalable fast trip threshold multiplier during steady state. Connect a resistor from this pin to GND to select the SFT multiplier.

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Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUT	7, 8	P	Power output. Must be soldered to the output power plane uniformly for proper heat dissipation.
VDD	9	P	Controller power input pin. Can be used to power the internal control circuitry with a filtered and stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.
IN	10, 22, 23	P	Power input. Must be soldered to the input power plane uniformly for proper heat dissipation.
NC	11, 17, 21	-	Do not connect anything to this pin.
MODE	12	I	NC
$\overline{FLT}$	13	O	Open drain active low fault output. Pull-up this pin to external supply voltage (≤ 5V) with a resistor.
ITIMER	14	I/O	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed the overcurrent threshold (but lower than fast-trip threshold) during steady-state operation before the device overcurrent response takes action.
TEMP	15	I/O	Analog voltage output for junction temperature. Voltage proportional to internal temperature of the device
EN/UVLO	16	I	Active high enable input. Connect resistor divider from input supply to set the undervoltage threshold. Do not leave floating.
OVP	18	I	Sets the over-voltage set-point. Connect a resistor divider from VIN to this pin. Do not leave floating.
PGOOD	19	O	Open-drain active high power good output. This pin has weak internal pull-up to internal supply voltage.
SWEN	20	I/O	Open-drain signal to indicate and control power switch ON/OFF status. This pin has weak internal pull-up to internal supply voltage.
IN	PowerPad™	P	Power input. Must be soldered to the input power plane uniformly for proper heat dissipation.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}, V_{DDMAX}	Maximum Input and Supply Voltage (-40°C ≤ T_J ≤ 125°C)	IN, VDD	–0.3	90	V
$V_{INMAX,25}$, $V_{DDMAX,25}$	Maximum Input and Supply Voltage (25°C ≤ T_J ≤ 125°C)	IN, VDD	–0.3	92	V
V_{OUTMAX}	Maximum Output Voltage	OUT	–5(2)	Min(92V, VIN + 0.3)	
V_{IN} - V_{OUT}	Maximum difference between IN and OUT	IN, OUT	-0.3	90	V
$V_{ILIMMAX}$	Maximum ILIM Pin Voltage	ILIM	–0.3	6	V
$V_{IMONMAX}$	Maximum IMON Pin Voltage	IMON	–0.3	6	V
V_{SFT_SELMAX}	Maximum SFT_SEL Pin Voltage	SFT_SEL	–0.3	6	V
V_{OVP}	Maximum OVP Pin Voltage	OVP	–0.3	6	V
V_{ITIMER}	Maximum ITIMER Pin Voltage	ITIMER	–0.3	6	V
$V_{IREFMAX}$	Maximum IREF Pin Voltage	IREF	–0.3	6	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage	DVDT	–0.3	6	V
$V_{MODEMAX}$	Maximum MODE Pin Voltage	MODE	–0.3	6	V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage	SWEN	–0.3	6	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink	SWEN		10	mA
V_{ENMAX}	Maximum EN/UVLO Pin Voltage	EN/UVLO	–0.3	6	V
$V_{FLTBMAX}$	Maximum $\overline{FLT}$ Pin Voltage	$\overline{FLT}$	–0.3	6	V
$I_{FLTBMAX}$	Maximum $\overline{FLT}$ Pin Sink Current	$\overline{FLT}$		10	mA
$V_{PGOODMAX}$	Maximum PGOOD Pin Voltage	PGOOD	–0.3	6	V
$I_{PGOODMAX}$	Maximum PGOOD Pin Sink Current	PGOOD		10	mA
V_{TEMP}	Maximum TEMP Pin Voltage	TEMP	–0.3	6	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) During FET OFF condition for negative transients.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	9	80	V
V_{DD}	Supply Voltage Range	VDD	9	80	V

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/ UVLO		5	V
V_{dVdT}	dVdT Pin Cap Voltage Rating	dVdT		4	V
V_{PGOOD}	PGOOD Pin Pull-up Voltage Range	PGOOD		5	V
$V_{SMBA/FLTb}$	SMBA/$\overline{FLT}$ Pin Pull-up Voltage Range	SMBA/ $\overline{FLT}$		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN		5	V
V_{TEMP}	TEMP/EECLK/GPIO1 Pin Voltage Rating	TEMP/ EECLK/ GPIO1		5	V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
C_{IN}	Capacitance on IN pins	IN	10		nF
C_{OUT}	Capacitance on OUT pins	OUT	10		µF
dV_{IN}/dt	Slew rate on IN pins	IN		500	V/µs
I_{MAX}	Continuous Switch Current	IN to OUT		10	A
$I_{MAX, Pulse}$	Peak Output Current for ≤10ms duration, T_A ≤ 70°C	IN to OUT		13	A
T_J	Junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS1686X LQFN PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.64	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.71	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.13	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Based on simulations conducted with the device mounted on a 3 x 4.5" PCB (2s2p) as JESD51-7

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 51V, OUT = Open, R_{IMON} = 5.55kΩ, V_{IREF} = 1V , $\overline{FLT}$ = 33kΩ pull-up to 3.3V, PGOOD = 33kΩ pull-up to 3.3V, C_{OUT} = 10µF, C_{IN} = 10nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2V, TEMP = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{IN}	Input voltage range		9		80	V
V_{DD}	Input voltage range		V_{IN}		80	V
$I_{QON(VDD)}$	V_{DD} ON state quiescent current	V_{DD} > V_{UVPR}, V_{EN} ≥ V_{UVLOR}, V_{OVP} < V_{OVPF}		600		µA
V_{UVPR}	V_{DD} Undervoltage Protection Threshold Rising	V_{DD} Rising		8.5		V
V_{UVPF}	V_{DD} Undervoltage Protection Threshold falling	V_{DD} Falling		7.05		V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVPHYS}	UVP Hysteresis VDD			1450		mV
INPUT SUPPLY (IN)						
$V_{UVPR(VIN)}$	VIN Undervoltage Protection Threshold	V_{IN} Rising		8.45		V
$V_{UVPF(VIN)}$	VIN Undervoltage Protection Threshold	V_{IN} Falling		7		V
$I_{QON(VIN)}$	V_{IN} ON state quiescent current	$V_{EN} \geq V_{UVLOR}$		1.53		mA
$I_{QOFF(VIN)}$	V_{IN} OFF state current	$V_{SDR} < V_{EN} < V_{UVLO}$		46		µA
$I_{SD(VIN)}$	V_{IN} shutdown current	$V_{EN} < V_{SDF}$		44		µA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
V_{UVLOR}	EN/UVLO pin voltage threshold for turning on, rising	EN/UVLO Rising		1.2		V
V_{UVLOF}	EN/UVLO pin voltage threshold for turning off and engaging QOD, falling	EN/UVLO Falling		1.12		V
$V_{UVLOHYS}$	UVLO Hysteresis			80		mV
V_{SDF}	Shutdown threshold	EN/UVLO Falling		0.45		V
V_{SDR}	Shutdown threshold	EN/UVLO Rising		0.5		V
I_{ENLKG}	EN/UVLO pin leakage current				0.1	µA
OVERVOLTAGE PROTECTION (IN)						
V_{OVPR}	Overvoltage protection threshold (rising)	OVP pin rising		1.17		V
V_{OVPF}	Overvoltage protection threshold (falling)	OVP pin falling		1.11		V
V_{OVPHYS}	Overvoltage protection threshold (Hysterisis)			60		mV
I_{OVPLKG}	OVP pin leakage current	V_{OVP} = 1.2V	–0.1		0.1	µA
$V_{OVPR(IN)}$	Internal Overvoltage protection threshold (rising)	VIN Rising	84	90.7	94.5	V
$V_{OVPF(IN)}$	Internal Overvoltage protection threshold (falling)	VIN falling	82	84.5	86	V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON state resistance	I_{OUT} = 3A, T_A = 25℃		16		mΩ
R_{ON}	ON state resistance	I_{OUT} = 3A, -40 < T_A < 125℃		25		mΩ
CURRENT LIMIT REFERENCE (IREF)						
V_{IREF}	IREF pin recommended voltage range		0.3		1.2	V
I_{IREF}	IREF internal sourcing current	V_{IREF} = 1V		25		µA
CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	Current Monitor Gain (ILIM:IOUT) vs. IOUT.	Device in steady state (PG asserted), I_{OUT} = 7A		18.9		uA/A
$I_{start\text{-}up\ peak}$	Peak current at Startup	V_{OUT}> V_{FB}, GHI de-asserted. VIN ≤60V		480		mA
V_{FB}	Foldback voltage			2		V
OUTPUT CURRENT MONITOR AND OVERCURRENT PROTECTION (IMON)						
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), I_{OUT} = 7A		18.19		µA/A
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), I_{OUT} = 4A		18.17		µA/A
I_{OCP}	IOUT Current limit trip (Circuit-Breaker) threshold	R_{IMON} = 5.5kΩ, V_{IREF} = 1V		10.85		A
CURRENT FAULT TIMER (ITIMER)						
I_{ITMR}	ITIMER pin internal discharge current	I_{OUT} > I_{TRIP}, ITIMER ↓		2.12		µA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ITMR}	ITIMER pin internal pull-up resistance			11.7		kΩ
V_{ITMR}	ITIMER pin internal pull-up voltage	I_{OUT} < I_{TRIP}		5		V
ΔV_{ITMR}	ITIMER discharge voltage	I_{OUT} > I_{TRIP}, ITIMER ↓		1.55		V
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast trip threshold in steady state	PG asserted High		45		A
I_{SFT}	Scalable fast trip current	R_{SFT_SEL} < 95kΩ, PG asserted High		I_{OC_BKP}		A
I_{SFT}	Scalable fast trip current	105kΩ < R_{SFT_SEL} < 195kΩ, PG asserted High		2.5 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	205kΩ < R_{SFT_SEL} < 295kΩ, PG asserted High		2 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	305kΩ < R_{SFT_SEL}, PG asserted High		1.5 × I_{OCP}		A
$I_{SFT(SAT)}$	Scalable fast trip Current (inrush)	During Powerup, PGOOD Low		2		A
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	dVdt Pin Charging Current			2		µA
G_{DVDT}	dVdt Gain	0.4V < V_{dVdt} < 2.4V		24.7		V/V
R_{DVDT}	dVdt Pin to GND Discharge Resistance			500		Ω
TEMP BALANCING						
GHI						
$V_{GS(GHI)}$ Rising	G-S Threshold when GHI/PG is asserted			7		V
$R_{ON(GHI)}$	Ron When GHI/PG is asserted			17.7		mΩ
QUICK OUTPUT DISCHARGE (QOD)						
I_{QOD}	Quick Output Discharge pull-down current	$V_{SD(R)}$ < V_{EN} < V_{UVLO}, 0℃ < Tj < 125℃, VIN = 51V		22		mA
TEMPERATURE SENSOR OUTPUT (TEMP)						
G_{TMP}	TEMP sensor gain	VIN = 51V		2.57		mV/℃
V_{TMP}	TEMP pin output voltage	T_J = 25 ℃, VIN = 51V		680		mV
I_{TMPSRC}	TEMP pin sourcing current	VIN = 51V		120		µA
I_{TMPSNK}	TEMP pin sinking current	VIN = 51V		10.5		µA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Absolute Thermal Shutdown Rising Threshold	T_J Rising, , VIN = 51V		150		°C
TSD_{HYS}	Absolute Thermal shutdown hysteresis	T_J Falling, VIN = 51V		13		°C
FET HEALTH MONITOR						
V_{DSFLT}	FET D-S Fault Threshold	SWEN = L, VIN = 51V		0.5		V
V_{DSOK}	FET D-S Fault Recovery Threshold	SWEN = L, VIN = 51V		0.64		V
SINGLE POINT FAILURE (ILIM, IMON, IREF, ITIMER)						
I_{OC_BKP}	Back-up overcurrent protection threshold	IMON short to GND		18		A

ADVANCE INFORMATION

6.6 Logic Interface

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45V to 60V, OUT = Open, R_{ILIM} = 931Ω R_{IMON} = 2.55kΩ, V_{IREF} = 1V , $\overline{FLT}$ = 33kΩ pull-up to 3.3V, PGOOD = 33kΩ pull-up to 3.3V, C_{OUT} = 10µF, C_{IN} = 10nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWEN						
R_{SWEN}	SWEN pin pull-down resistance	SWEN de-asserted Low		6.5		Ω
$I_{SWENLKG}$	SWEN pin leakage current	SWEN asserted high, pulled up to 5.5 V			1	µA
FAULT INDICATION (FLTB)						
R_{FLTB}	FLTB pin pull-down resistance	FLTB asserted Low		7.6		Ω
$I_{FLTBLKG}$	FLTB pin leakage current	FLTB de-asserted High, pulled up to 3.3 V through 33 kΩ			0.1	µA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low		7.9		Ω
I_{PGKG}	PG pin leakage current	PG asserted High,pulled up to 3.3 V through 33 kΩ			1	µA
Switching Characteristics						

6.7 Timing Requirements

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45V to 60V, OUT = Open, R_{ILIM} = 931Ω R_{IMON} = 2.55kΩ, V_{IREF} = 1V , $\overline{FLT}$ = 33kΩ pull-up to 3.3V, PGOOD = 33kΩ pull-up to 3.3V, C_{OUT} = 10µF, C_{IN} = 10nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{OVP} > V_{OVPR} V to SWEN↓		3		us
t_{Insdly}	Insertion delay	$V_{EN/UVLO}$ > $V_{UVLO(R)}$ to SWEN↑		18		ms
t_{FFT}	Fixed Fast-Trip response time Hard Short	V_{DS} > V_{DSCOMP} to SWEN↓		195		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 × I_{TRIP} to IOUT↓		418		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 × I_{TRIP}, C_{ITIMER} = Open		0		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 × I_{TRIP}, C_{ITIMER} = 4.7nF		2.75		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant		841		ms
$t_{EN(DG)}$	EN/UVLO de-glitch time			10		us
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		6.9		s
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}, C_{OUT} = 0.5 mF, V_{IN} = 51 V.		920		ms
t_{QOD}	QOD enable timer	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}		16		µs
$t_{FASTTEC}$	Fast recovery delay	SFT or FFT triggering to SWEN↑. Auto-retry device.		30		µs

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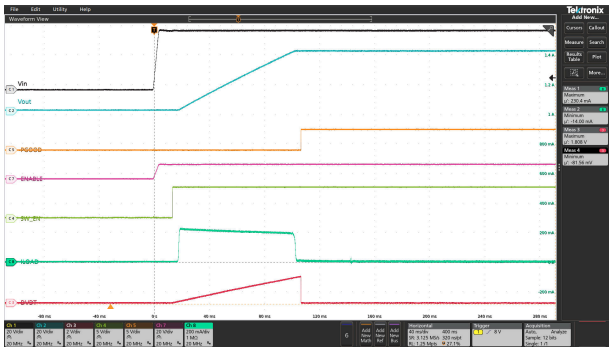
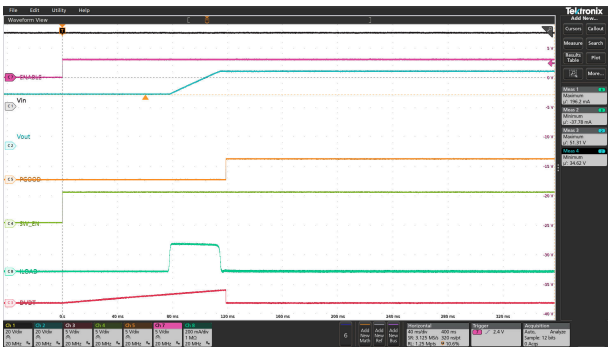
6.8 Typical Characteristics



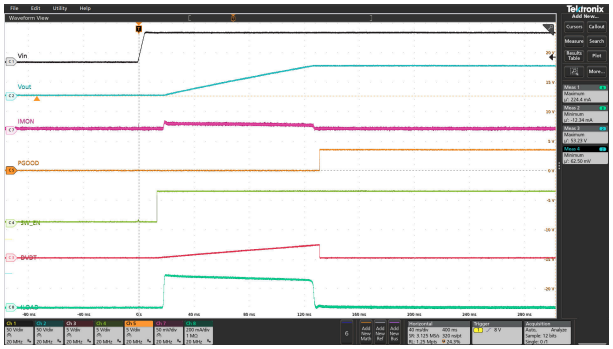
Input supply ramped up to 40V with appropriate resistor divider pulling EN high, C_{DVDT}=100nF, C_{OUT}=470µF

Figure 6-1. Power Up Sequencing Using Input Supply with EN connected to VIN via Resistor



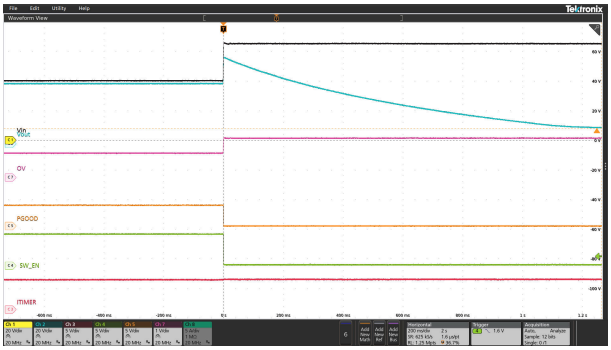
Input supply held steady at 54V, EN/UVLO pin toggled high. C_{DVDT}=100nF, C_{OUT}=470µF

Figure 6-2. Power Up Using EN/UVLO Pin



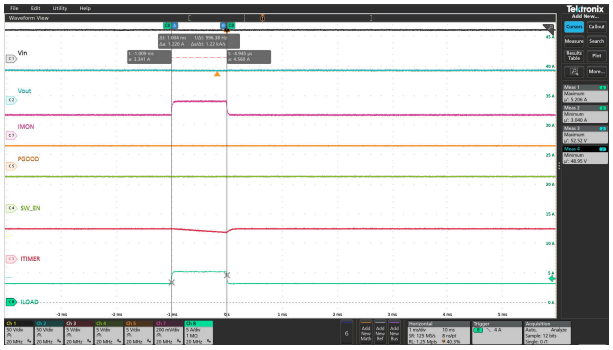
Input Supply of 51V, C_{OUT} = 470µF, C_{dVdt} = 100nF

Figure 6-3. Inrush Current Control with Capacitive Load



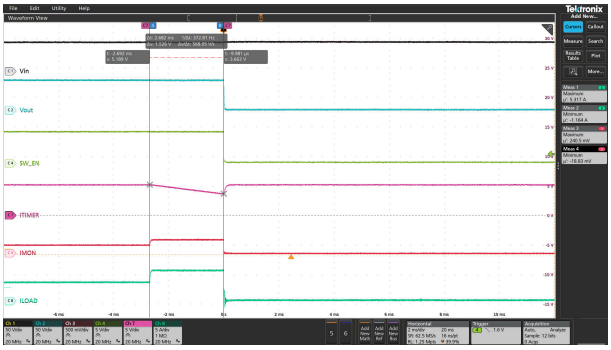
Input supply ramped up above OVP threshold of 58V to 66V

Figure 6-4. Input Overvoltage Protection Response



I_{OCP} = 5A, t_{ITIMER} = 2.6ms, I_{OUT} pulsed above the I_{OCP} threshold for short duration of 1ms which is than the T_{ITIMER} without triggering circuit-breaker response

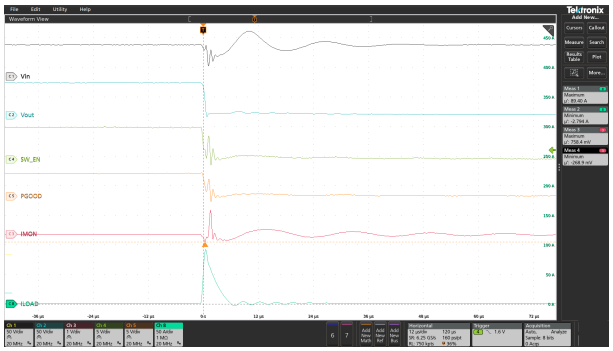
Figure 6-5. Peak Current Support Using Transient Overcurrent Blanking



I_{OCP} = 5A, t_{ITIMER} = 2.6ms, I_{OUT} stays above the I_{OCP} threshold persistently to trigger circuit-breaker response

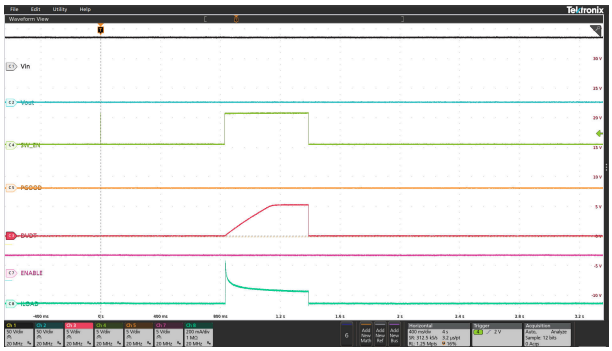
Figure 6-6. Overcurrent Protection Response (Circuit-Breaker)

6.8 Typical Characteristics (continued)



Output hard-short to GND while in steady. I_{OUT} rises above 2 × I_{OCP} triggers fast-trip response

Figure 6-7. Short-Circuit Protection Response



Device turned on with output hard-short to GND. Device limits the current with foldback.

Figure 6-8. Power Up into Short-Circuit

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7 Detailed Description

7.1 Overview

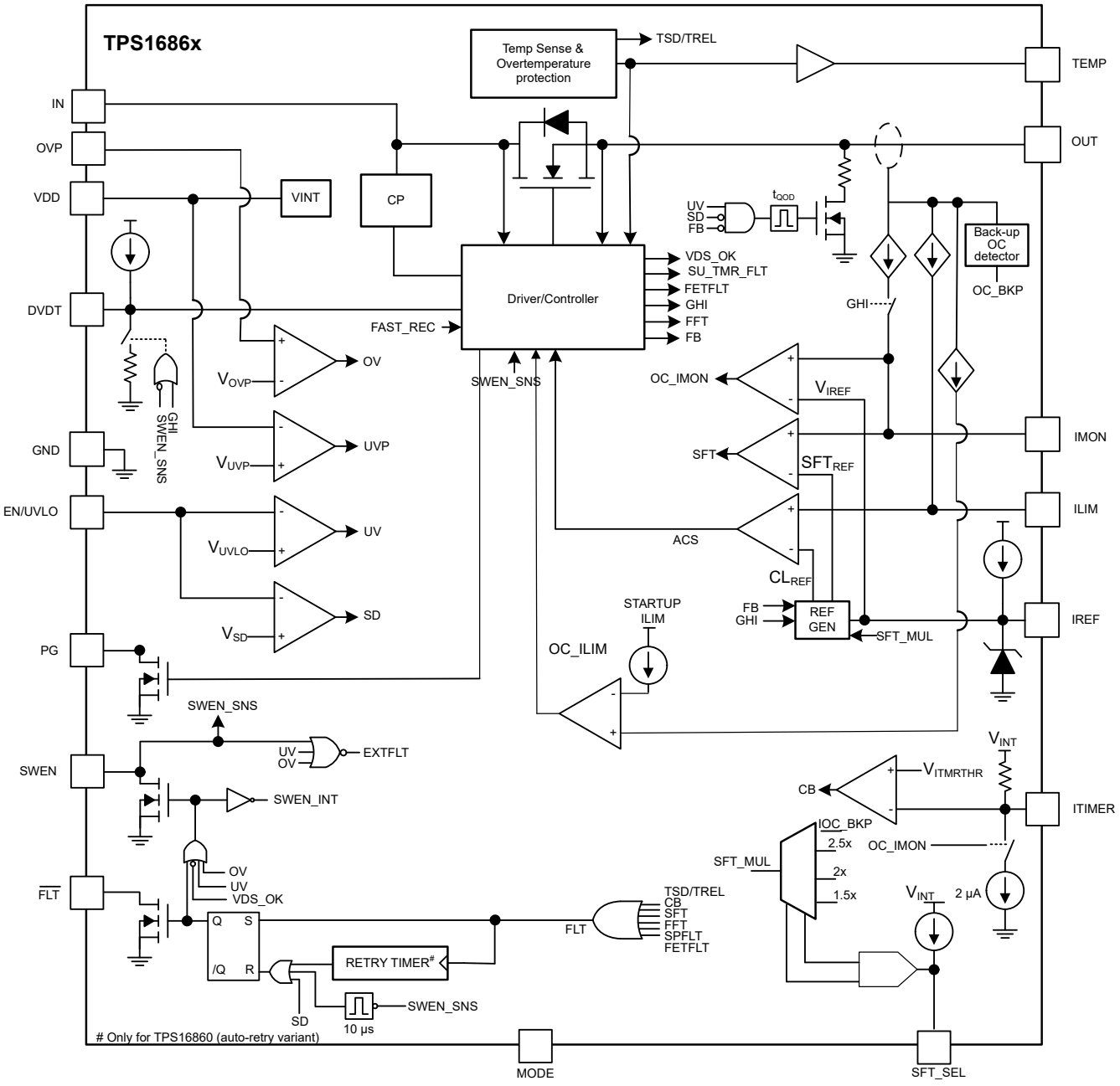
The TPS1686x is an eFuse with integrated power switch that is used to manage load voltage and load current. The device starts the operation by monitoring the VDD and IN bus. When V_{DD} & V_{IN} exceed the respective Undervoltage Protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next, the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low, the internal MOSFET is turned off.

After a successful start-up sequence, the TPS1686x device now actively monitors the load current and input voltage, and controls the internal FET to verify that the user adjustable overcurrent protection threshold limit I_{OCP} is not exceeded and overvoltage spikes on V_{IN} are cut-off. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This provides a robust protection design against real faults which is also immune to transients, thereby providing maximum system uptime.

The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This facilitates the implementation of advanced dynamic platform power management techniques to maximize system power utilization and throughput without sacrificing safety and reliability.

The device has integrated protection circuits to verify the device safety and reliability under recommended operating conditions. The internal FET is protected at all time using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (Tj) becomes too hot.

7.2 Functional Block Diagram



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7.3 Feature Description

The TPS1686x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Protection

The TPS1686x implements Undervoltage Lockout on VDD & VIN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage lockout has a default lockout threshold of V_{UVP} internally on VDD and V_{UVPIN} on V_{IN}. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The following figure and equation show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

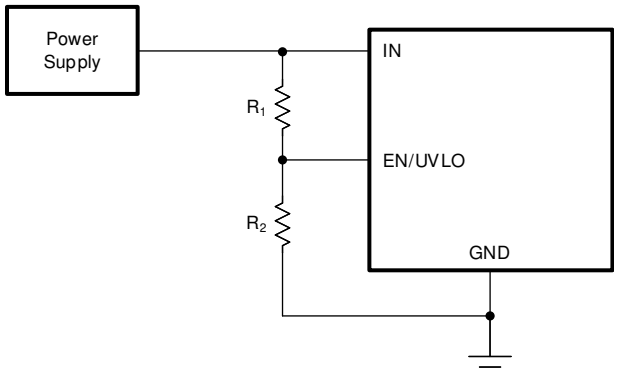

Figure 7-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = V_{UVLO(R)}\frac{R_1 + R_2}{R_2} \quad (1)$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for > t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and the device retains no digital state memory. The circuitry also resets any latched faults. In this condition, the device quiescent current consumption is minimal.

7.3.2 Insertion Delay

The TPS1686x implements insertion delay at start-up to let the supply stabilize before the device tries to turn on. This is to prevent any unexpected behavior in the system if the device tries to turn on while the card has not made firm contact with the backplane or if there's any supply ringing/oscillation during startup.

The device initially waits for the VDD supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, the device remains off for an additional delay of T_{Insdly} irrespective of the EN/UVLO pin condition.

7.3.3 Overvoltage Protection

The TPS1686x implements Overvoltage lockout to protect the load from input overvoltage conditions. A resistor divider needs to be connected on OVP pin to set the overvoltage set-point externally. The device also has a fixed internal OV protection on IN pin at $V_{OVPR(IN)}$ V.

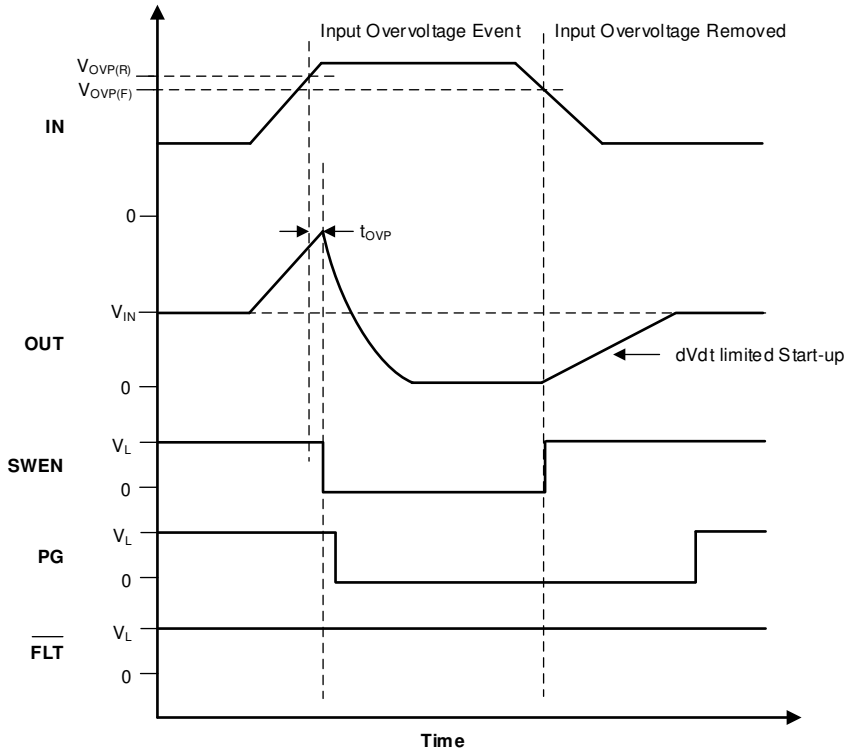

Figure 7-2. Input Overvoltage Protection Response

7.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS1686x incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control.
2. Fixed current limit ($I_{start-up}$) for overcurrent protection during start-up if the slew rate current is too high.
3. Foldback of current during Startup if device temperature starts rising to protect from Over Temperature.
4. Circuit-breaker with an adjustable threshold (I_{OCP}) and blanking timer (t_{ITIMER}) for overcurrent protection during steady-state.
5. Fast-trip response to severe overcurrent faults with an adjustable threshold (I_{SFT} = SFT_MUL × I_{OCP}) to quickly protect against severe short-circuits , as well as a fixed threshold (I_{FFT}) during steady state. Multiplier for SFT (SFT_MUL) is selected by resistor on SFT_SEL pin.

7.3.4.1 *Slew rate (dVdt) and Inrush Current Control*

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, the inrush current can damage the input connectors and cause the system power supply to droop. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (2)$$

A capacitor can be added to the DVDT pin to control the rising slew rate and lower the inrush current during turn-on. The required CdVdt capacitance to produce a given slew rate can be calculated using Equation 3.

$$C_{DVDT}(nF) = \frac{50}{SR(V/ms)} \quad (3)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

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Note

1. High input slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:
   a. Reduce the input inductance.
   b. Increase the capacitance on VIN pin.
   c. Increase the dVdt pin capacitance to reduce the slew rate or increase the start-up time.

7.3.4.1.1 Start-Up Time Out

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after SWEN is asserted, the device registers this condition as a fault. $\overline{FLT}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the device configuration.

7.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS1686x responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also provides robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 4.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (4)$$

Where G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT})

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- The internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage. Driving the IREF pin from an external low impedance reference voltage source as shown in Equation 5 is also possible.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (5)$$

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using Equation 6.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (6)$$

After an overcurrent condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (I_{SFT}), the device starts discharging the ITIMER pin capacitor using an internal pulldown current. If the load current drops below the current limit threshold before the ITIMER capacitor discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling the voltage up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor continues to discharge and after the capacitor falls by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the ITIMER capacitor is charged up to V_{INT} again so that the capacitor is at the default state before the next overcurrent event. This action verifies the full blanking timer interval is provided for every overcurrent event. Equation 7 can be used to calculate the R_{IMON} value for the desired overcurrent threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \quad (7)$$

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The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculated using Equation 8.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (8)$$

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay. However, this makes the circuit-breaker response extremely sensitive to noise and can cause false tripping during load transients.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the quiescent current – not a recommended mode of operation.
3. Increasing the ITIMER capacitor value extends the overcurrent blanking interval. However, this value also extends the time needed for the ITIMER capacitor to recharge up to V_{INT} before the next overcurrent event. If the next overcurrent event occurs before the ITIMER capacitor is recharged fully, less time is taken to discharge to the VITIMER threshold, thereby providing a shorter blanking interval than intended.

Figure 7-3 illustrates the overcurrent response for TPS1686x eFuse. After the part shuts down due to a circuit-breaker fault, the device either stays latched off (TPS16860 variant) or restarts automatically after a fixed delay (TPS16861 variant).

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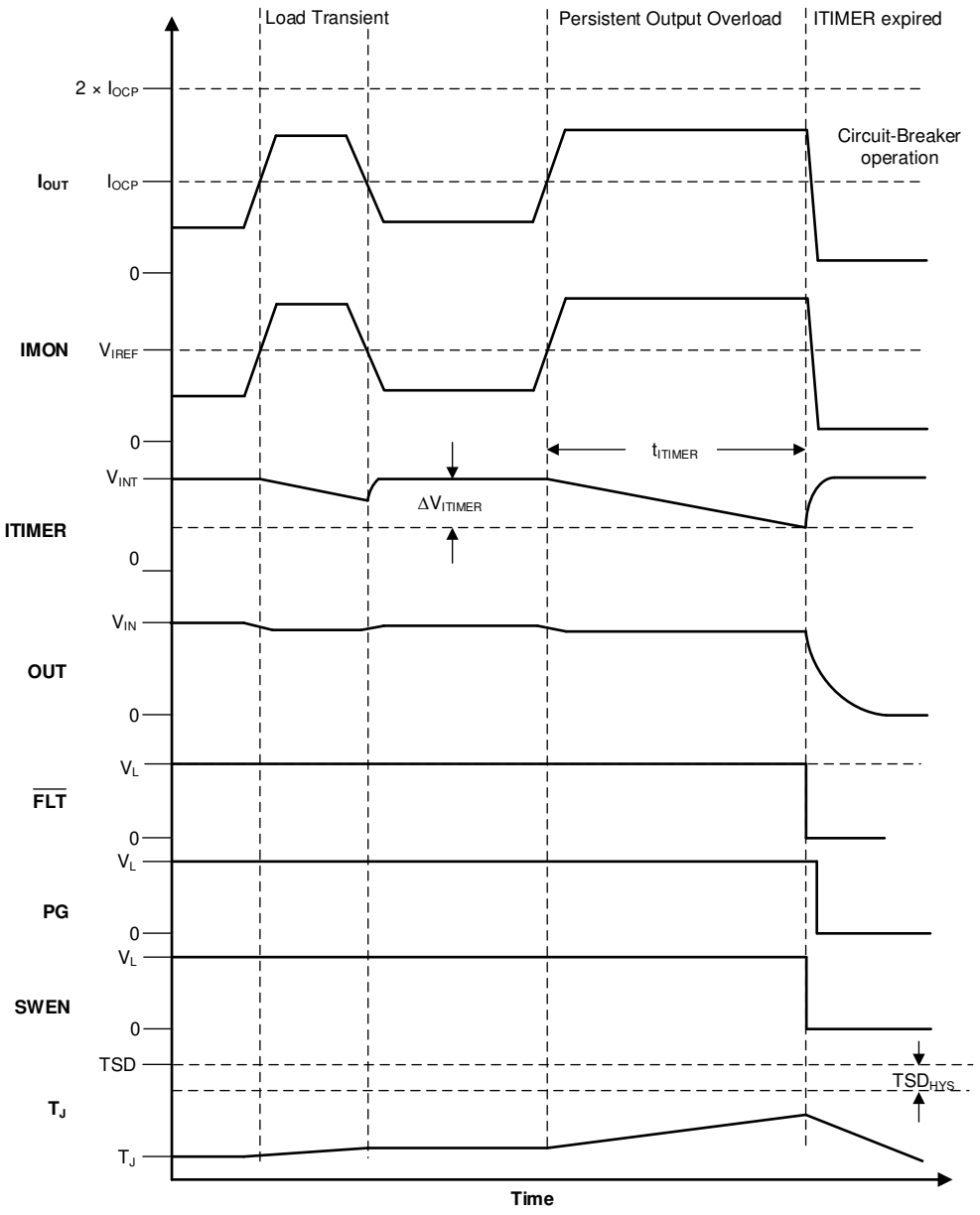

Figure 7-3. Steady-State Overcurrent (Circuit-Breaker) Response

7.3.4.3 Active Current Limiting During Start-Up

The TPS1686x responds to output overcurrent conditions during start-up by actively limiting the current. The startup current limit is internally fixed to $I_{start\text{-}up}$.

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to a TSD fault, the device either stays latched off (TPS16861 variants) or restarts automatically after a fixed delay (TPS16860 variants). See *Overtemperature protection* section for more details on device response to overtemperature.

Note

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

7.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. The fast-trip comparator employs a scalable threshold (I_{SFT}) during steady-state . I_{SFT} can be selected by resistor on SFT_SEL pin. This enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which is not always suitable for all systems. After the current exceeds the fast-trip threshold, the TPS1686x turns off the FET within t_{SFT}. The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}.

Table 7-1. Device Functional Modes Based on Resistor on SFT_SEL Pin

I_{SFT_SEL}	SFT_SEL pin
I_{OC_BKP}	R_{SFT_SEL} <95kΩ
2.5 x I_{OCP}	105kΩ < R_{SFT_SEL} < 195kΩ
2 xI_{OCP}	205kΩ < R_{SFT_SEL} < 295kΩ
1.5 xI_{OCP}	305kΩ < R_{SFT_SEL}

7.3.5 Analog Load Current Monitor (IMON)

The TPS1686x allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The IMON signal can be converted to a voltage by dropping the voltage across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using Equation 9.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \quad (9)$$

The TPS1686x IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as Intel PSYS or PROCHOT# to maximize system power usage and platform throughput without sacrificing safety or reliability.

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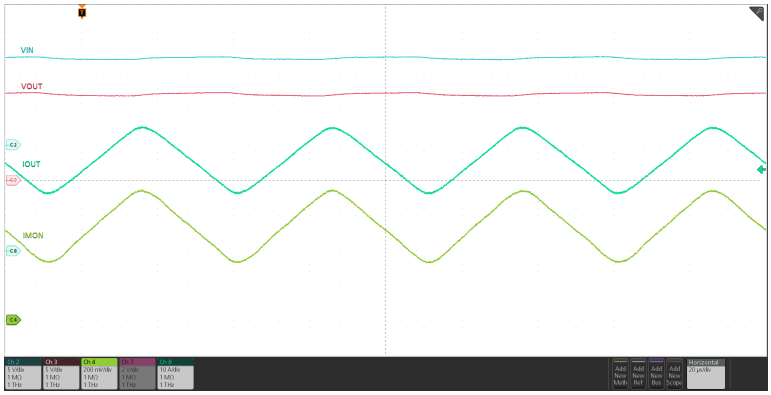

Figure 7-4. Analog Load Current Monitor Response

Note

1. The IMON pin provides load current monitoring information only during steady-state. During inrush, the IMON pin reports zero load current.
2. The ILIM pin reports the device load current at all times and can also be used as an analog load current monitor for the device.
3. Care must be taken to minimize parasitic capacitance on the IMON and ILIM pins to avoid any impact on the overcurrent and short-circuit protection timing.

7.3.6 Switch Enable Pin (SWEN)

The SWEN pin is a signal which is driven high when the FET must be turned ON. When the SWEN pin is driven low (internally or externally), the pin signals the driver circuit to turn OFF the FET.

Table 7-2. SWEN Summary

Device State	FET Driver Status	SWEN
Steady-state	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Undervoltage (VIN UVP)	OFF	L
Insertion delay	OFF	L
Overvoltage lockout (VIN OVP)	OFF	L
Transient overcurrent	ON	H
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L
Fast-trip	OFF	L
Fault response mono-shot running	OFF	L
Fault response mono-shot expired	ON	H
ILM pin open (start-up)	OFF	L
ILM pin short (start-up)	OFF	L
ILM pin open (steady-state)	OFF	L

Table 7-2. SWEN Summary (continued)

Device State	FET Driver Status	SWEN
ILM pin short (steady-state)	OFF	L
FET health fault	OFF	L

Note

1. The SWEN has a weak internal pullup but if needed can be pulled up to an external stable supply derived from the input of the eFuse using a resistor.

7.3.7 Analog Junction Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

7.3.8 Overtemperature Protection

The TPS1686x employs an internal thermal shutdown mechanism to protect the device when the internal FET becomes too hot to operate safely. When the TPS16860 detects thermal overload, the device shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS16861 detects thermal overload, the device remains off until the device has cooled down sufficiently. Thereafter, the device remains off for an additional delay of t_{RST} after which the device automatically retries to turn on if the shutdown mechanism is still enabled.

Table 7-3. Overtemperature Protection Summary

Device	Enter TSD	Exit TSD
TPS16861 (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} VDD cycled to 0V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$
TPS16860 (Auto-Retry)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} t_{RST} timer expired or VDD cycled to 0V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

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7.3.9 Fault Response and Indication ($\overline{FLT}$)

Table 7-4 summarizes the device response to various fault conditions.

Table 7-4. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Delay
Steady-state	None	N/A	H	
Inrush	None	N/A	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Undervoltage (VIN UVP)	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	H	
Transient overcurrent	None	N	H	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	L	
Short-circuit	Fast-trip	Y	L	t_{FT}
IMON pin open (steady-state)	Shutdown	Y	L	
IMON pin short (steady-state)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	50µs
IREF pin open (start-up)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y?	L?	
IREF pin open (steady-state)	Shutdown (if I_{OUT} > I_{OC_BKP})	Y	L	t_{ITIMER}
IREF pin short (steady-state)	Shutdown	Y	L	
IREF pin short (start-up)	Shutdown	Y	L	
ITIMER pin forced to high voltage	Shutdown (if I_{OUT} > I_{OCP} or I_{OUT} > I_{OC_BKP})	Y	L	t_{SPFAIL_TMR}
Start-up timeout	Shutdown	Y	L	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	10µs
FET health fault (G-D)	Shutdown	Y	L	
FET health fault (D-S)	Shutdown	N	L	t_{SU_TMR}
External fault (SWEN pulled low externally while device is not in UV or OV)	Shutdown	Y	L	

$\overline{FLT}$ is an open-drain pin and must be pulled up to an external supply.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the pin is de-asserted. This action also clears the t_{RST} timer (auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both latch-off and auto-retry variants.

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7.3.10 Power Good Indication (PG)

Power Good indication is an active high output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

Table 7-5. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Undervoltage (V_{EN} < V_{UVLO})	OFF	L	t_{PGD}
V_{IN} < V_{UVP}	OFF	L	
V_{DD} < V_{UVP}	OFF	L	
Overvoltage (V_{IN} > V_{OVP})	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L	t_{PGD} N/A
Fast-trip	OFF	L	t_{PGD} N/A
ILM pin open	OFF	L	t_{ITIMER} + t_{PGD} N/A
ILM pin short	OFF	L	t_{PGD} N/A
Overtemperature	Shutdown	L	t_{PGD} N/A

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted HIGH after a de-glitch time (t_{PGA}).

The PG is de-asserted if the FET is turned off at any time during normal operation. The PG de-assertion de-glitch time is t_{PGD}.

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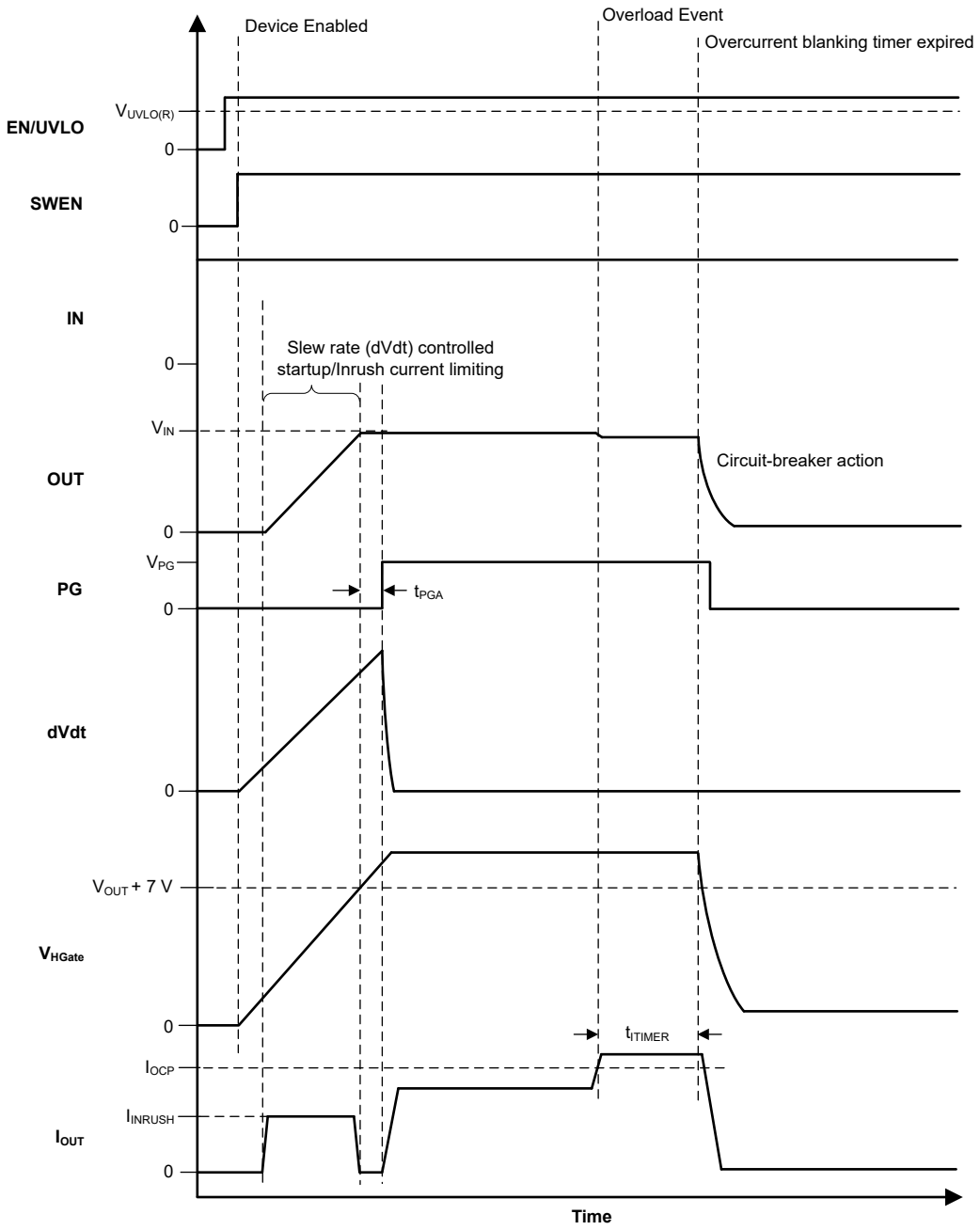

Figure 7-5. TPS1686x PG Timing Diagram

The PG is an open-drain pin and must be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.3.11 Output Discharge

The device has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)} < V_{EN} < V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly

remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when V_{OUT} < V_{FB} or if the device detects a fault.

The output discharge function can result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long-term degradation of the part.

7.3.12 FET Health Monitoring

The TPS1686x can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance by not providing power to the load correctly or by not providing the necessary level of protection. After a FET failure is detected, the TPS1686x tries to turn off the internal FET by pulling the gate low and asserts the $\overline{FLT}$ pin.

- **D-S short:** D-S short can result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at start-up by checking if V_{IN-OUT} < V_{DSFLT} before the FET is turned ON. If yes, the device engages the internal output discharge to try and discharge the output. If the V_{OUT} does not discharge below V_{FB} within a certain allowed interval, the device asserts the $\overline{FLT}$ pin.
- **G-D short:** The TPS1686x detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition.
- **G-S short:** The TPS1686x detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, this is latched as a G-S short fault.

7.3.13 Single Point Failure Mitigation

The TPS1686x relies on the proper component connections and biasing on the IMON, ILIM, IREF, and ITIMER pins to provide overcurrent and short-circuit protection under all circumstances. As an added safety measure, the device uses the following mechanisms to verify that the device provides some form of overcurrent protection even if any of these pins are not connected correctly in the system or the associated components have a failure in the field.

7.3.13.1 IMON Pin Single Point Failure

- **IMON pin open:** In this case, the IMON pin voltage is internally pulled up to a higher voltage and exceeds the threshold (V_{IREF}), causing the part to perform a circuit-breaker action even if there is no significant current flowing through the device.
- **IMON pin shorted to GND directly or through a very low resistance:** In this case, the IMON pin voltage is held at a low voltage and is not allowed to exceed the threshold (V_{IREF}) even if there is significant current flowing through the device, thereby rendering the primary overcurrent protection mechanism ineffective. The device relies on an internal overcurrent sense mechanism to provide some protection as a backup. If the device detects that the backup current sense threshold (I_{OC_BKP}) is exceeded but at the same time the primary overcurrent detection on IMON pin fails, the pin triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

7.3.13.2 IREF Pin Single Point Failure

- **IREF pin open or forced to higher voltage:** In this case, the IREF pin (V_{IREF}) is pulled up internally or externally to a voltage which is higher than the target value as per the recommended I_{OCP} or I_{LIM} calculations, preventing the primary circuit-breaker, active current limit, and short-circuit protection from getting triggered even if there is significant current flowing through the device. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold is exceeded but at the same the primary overcurrent or short-circuit detection on ILIM or IMON pin fails, the device triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

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- **IREF pin shorted to GND:** In this case, the V_{IREF} threshold is set to 0V, causing the part to perform active current limit or circuit-breaker action even if there is no significant current flowing through the device.

7.3.13.3 ITIMER Pin Single Point Failure

- **ITIMER pin open or short to GND:** In this case, the ITIMER pin is already discharged below $V_{ITIMERTHR}$ and hence indicates overcurrent blanking timer expiry instantaneously after an overcurrent event and triggers a circuit-breaker action without any delay.
- **ITIMER pin forced to some voltage higher than $V_{ITIMERTHR}$:** In this case, the ITIMER pin is unable to discharge below $V_{ITIMERTHR}$ and hence fails to indicate overcurrent blanking timer expiry, thereby rendering the circuit-breaker mechanism ineffective. The device relies on a backup overcurrent timer mechanism to provide some protection as a backup. If the device detects an overcurrent event on either the IMON pin or the backup overcurrent detection circuit, the device engages the internal backup time and after the timer expires ($t_{SPFLTMR}$), the device latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

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7.4 Device Functional Modes

The features of the device depend on the operating mode. Table 7-6 and Table 7-7 summarize the device functional modes.

Table 7-6. Device Functional Modes Based on EN/UVLO Pin

Pin: EN/UVLO	Device State	Output Discharge
> $V_{UVLO(R)}$	Fully ON	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (< t_{QOD})	FET OFF	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (> t_{QOD})	FET OFF	Enabled
< $V_{SD(F)}$	Shutdown	Disabled

Table 7-7. Device Functional Modes Based on Resistor at SFT_SEL Pin

I_{SFT_SEL}	SFT_SEL pin
I_{OC_BKP}	R_{SFT_SEL}< 95kΩ
2.5 x I_{OCP}	105kΩ < R_{SFT_SEL}< 195kΩ
2 x I_{OCP}	205kΩ < R_{SFT_SEL}< 295kΩ
1.5 x I_{OCP}	305kΩ < R_{SFT_SEL}

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS1686x is a high voltage and current eFuse that is typically used for power rail protection applications. The device operates from 9 V to 80 V with input overvoltage and adjustable undervoltage protection. The device provides ability to control inrush current and offers protection against overcurrent and short-circuit conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool,TPS1686x Design Calculator is available in the web product folder.

8.1.1 Single Device, Standalone Operation

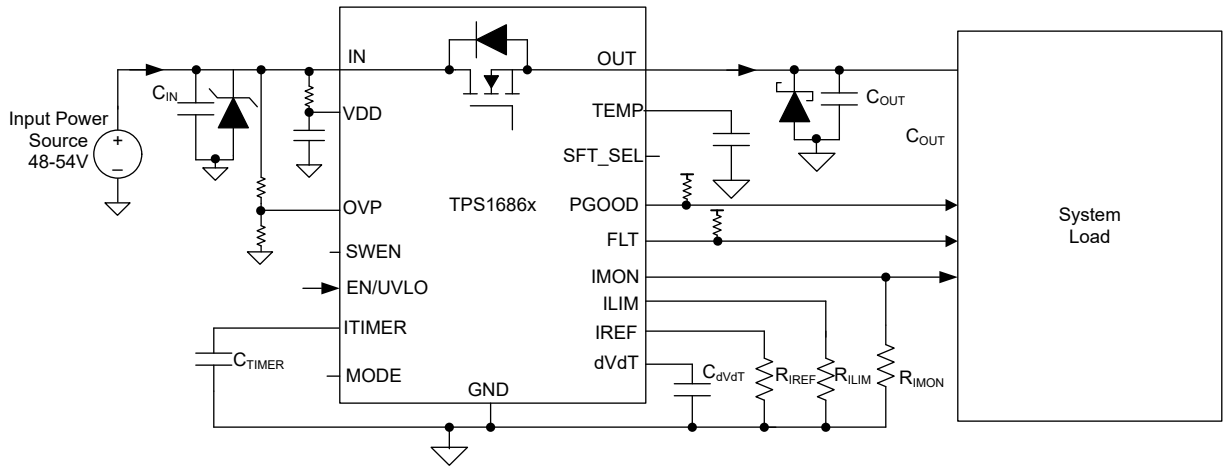

Figure 8-1. Single Device, Standalone Operation

Other variations:

1. The IREF pin can be driven from an external reference voltage source.
2. In a host MCU controlled system, EN/UVLO can be connected to a GPIO pin to control the device. IMON pin voltage can be monitored using an ADC. The host MCU can use a DAC to drive IREF to change the current limit threshold dynamically.
3. The device can be used as a simple high current load switch without adjustable overcurrent or fast-trip protection by tying the ILIM and IMON pins to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.

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8.2 Typical Application: 54V Fan Load Protection in Datacenter Servers

8.2.1 Application

This design example considers a 54V system operating voltage with a tolerance of ±10% for driving fan load. The maximum steady-state load current is 9A. If the load current exceeds 10A, the eFuse circuit must allow transient overload currents up to a 3ms interval. For persistent overloads lasting longer than that, the eFuse circuit must break the circuit and then latch-off. Figure 8-2 shows the application schematic for this design example.

TI recommends to short PG pin of TPS1686 with PWM signal from controller and connect this configuration to the PWM signal pin of fan. This helps to verify that fan load draws current after PG is high. This setup helps to verify that the TPS1686 starts successfully in less thermal stress by charging only bulk capacitor load and is not loaded by fan during startup.

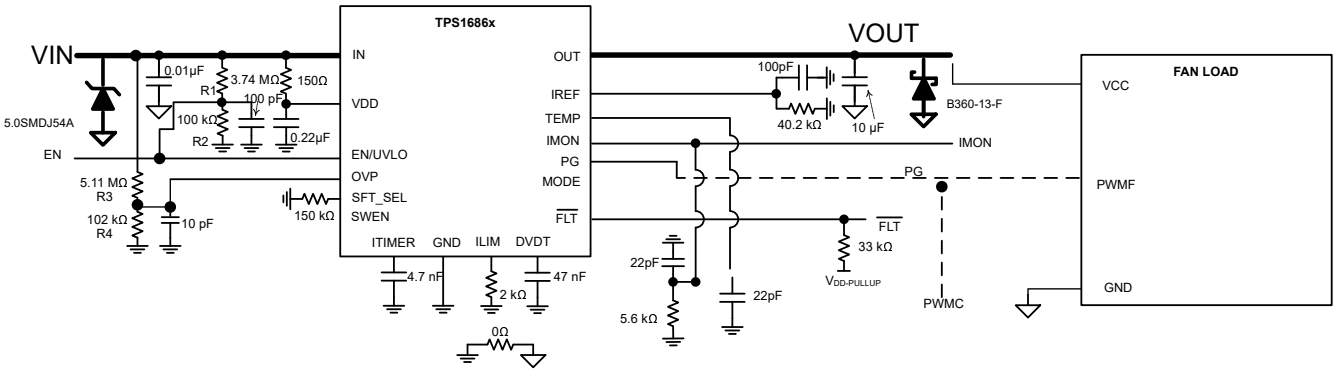

Figure 8-2. Application Schematic For a 54V, Fan Load Protection Circuit

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8.2.2 Design Requirements

Table 8-1 shows the design parameters for this application example.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	48.5V – 59.5V
Maximum DC load current ($I_{OUT(max)}$)	9A
Maximum output capacitance (C_{LOAD})	100uF
Are all the loads off until the PG is asserted?	Yes
Maximum ambient temperature	55°C
Transient overload blanking timer	3ms
Output voltage slew rate	1V/ms
Need to survive a “hot-short” on output condition ?	Yes
Need to survive a “power up into short” condition?	Yes
Fault response	Latch-off

8.2.3 Detailed Design Procedure

- **Selecting the C_{DVDT} capacitor to control the output slew rate and start-up time**

  A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of slew rate. Equation 10 is used to compute the value of C_{DVDT}.

$$C_{DVDT}(nF) = \frac{50}{V_{IN}(V)/T_{ss}(ms)} \quad (10)$$

  To get slew rate of 1V/ms , as per above equation we get C_{DVDT} as 50nF. We can keep nearby standard value of 47nF.

- **Selecting the R_{IREF} resistor to set the reference voltage for overcurrent protection.**

  . Equation 11 is used to calculate the value of R_{IREF}.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (11)$$

  In this design example, V_{IREF} is set at 1V. With I_{IREF} = 25µA (typical), we can calculate the target R_{IREF} to be 40kΩ. The closest standard value of R_{IREF} is 40.2kΩ with 0.1% tolerance and power rating of 100mW. For improved noise immunity, place a 100pF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to verify the proper operation of overcurrent detection circuit.

Selecting the R_{IMON} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady-state

TPS1686x eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 12.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (12)$$

G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.2µA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 13.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (13)$$

In this design example, I_{OCP} is considered as 10A, and R_{IMON} can be calculated to be 5.5 KΩ with G_{IMON} as 18.2µA/A and V_{IREF} as 1V. The nearest value of R_{IMON} is 5.6 KΩ with 0.1% tolerance and power rating of 100mW. For noise reduction, place a 22pF ceramic capacitor across the IMON pin and GND.

- **Selecting the C_{ITIMER} capacitor to set the overcurrent blanking timer**

An appropriate capacitor must be connected at the ITIMER pin to ground of the primary or standalone device to adjust the duration for which the load transients above the circuit-breaker threshold are allowed. The transient overcurrent blanking interval can be calculated using Equation 14.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (14)$$

Where t_{ITIMER} is the transient overcurrent blanking timer and C_{ITIMER} is the capacitor connected between ITIMER pin of the device and GND. I_{ITIMER} = 2µA (typical) and ΔV_{ITIMER} = 1..55V (typical). A 4.7nF capacitor with 10% tolerance and DC voltage rating of 25V is used as the C_{ITIMER} for the device in this design.

- **Selecting the resistors to set the undervoltage lockout threshold**

  The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in undervoltage protection section. The resistor values required for setting up the UVLO threshold are calculated using Equation 15.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (15)$$

  To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. From the device electrical specifications, UVLO rising threshold $V_{UVLO(R)}$ = 1.2V. From the design requirements, V_{INUVLO} = 46V. First choose the value of R_1 = 3.74MΩ and use Equation 15 to calculate R_2 = 100kΩ. Use the closest standard 1 % resistor values: R_1 = 3.74MΩ and R_2 = 100kΩ. For noise reduction, place a 100pF ceramic capacitor across the EN/UVLO pin and GND.

- **Selecting the resistors to set the overvoltage lockout threshold**

  The overvoltage lockout (OVLO) threshold is adjusted by employing the external voltage divider network of R_3 and R_4 connected between IN, OVLO, and GND pins of the device as described in the overvoltage protection section. The resistor values required for setting up the OVLO threshold are calculated using below equation.

$$V_{IN(OV)} = V_{OVLO(R)} \frac{R_3 + R_4}{R_4} \quad (16)$$

  To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_3 and R_4. From the device electrical specifications, OVLO rising threshold $V_{OVLO(R)}$ = 1.17V. From the design requirements, V_{INOVLO} = 60V. First choose the value of R_1 = 5.11MΩ and use Equation 15 to calculate R_3 = 101kΩ. Use the closest standard 1% resistor values: R_3 = 5.11MΩ and R_4 = 102kΩ. For noise reduction, place a 10pF ceramic capacitor across the OVLO pin and GND.

- **Selecting the R-C filter between VIN and VDD**

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VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (150Ω) – C (0.22µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short-circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

- **Selecting the pullup resistors and power supplies for $\overline{FLT}$,**

  $\overline{FLT}$ is the open drain output. If these logic signal is used, the signal must be pulled up to an appropriate supply rail voltage through 33kΩ pullup resistances.

- **Selection of TVS diode at input and Schottky diode at output**

  In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

  1. Minimize lead length and inductance into and out of the device.
  2. Use a large PCB GND plane.
  3. Addition of the Transient Voltage Suppressor (TVS) diodes to clamp the positive transient spike at the input.
  4. Using Schottky diodes across the output to absorb negative spikes.

  Refer to *TVS Clamping in Hot-Swap Circuits* , *Selecting TVS Diodes in Hot-Swap and ORing Applications*, TVS Diode recommendation tool for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (90V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. One(1) SMDJ54A is used in this design example.

  Note

  Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

  Selection of the Schottky diodes must be based on the following criteria:

  – The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 17 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

  $$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \quad (17)$$

  – Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. The negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (–5V).
  – DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
  – Leakage current (I_R) must be as small as possible.

  1 B360-13-F is used in this design example.

- **Selecting C_{IN} and C_{OUT}**

  TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.01µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 10µF can be used at the OUT pin of each device.

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8.2.4 Application Performance Plots

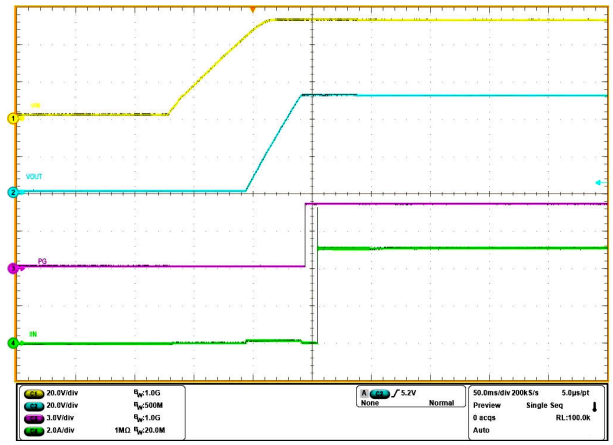

Figure 8-3. Supply ramped from 0V to 54V Startup

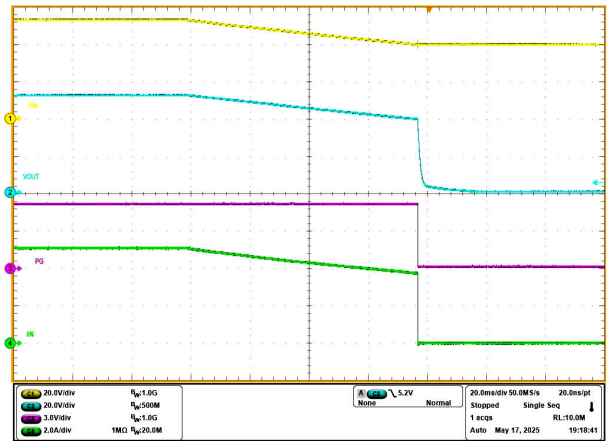

Figure 8-4. Supply turned off- UVLO

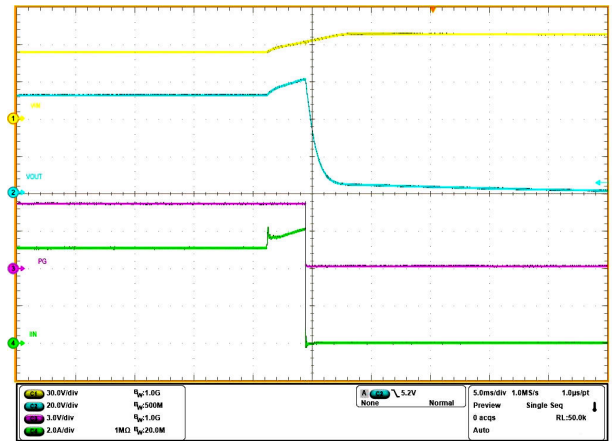

Figure 8-5. Supply ramped up beyond 54V- OVLO

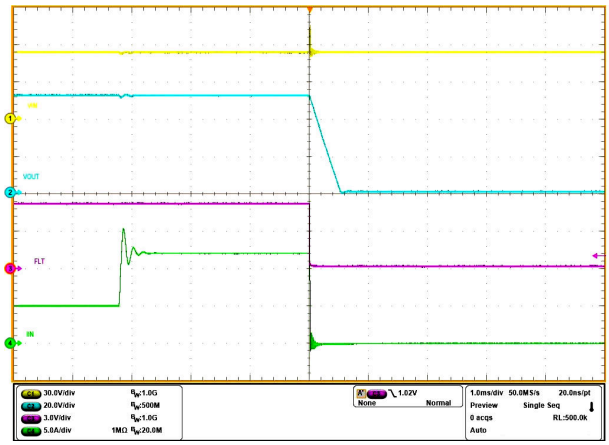

Figure 8-6. Load current goes above 10A- Overcurrent circuit-breaker response

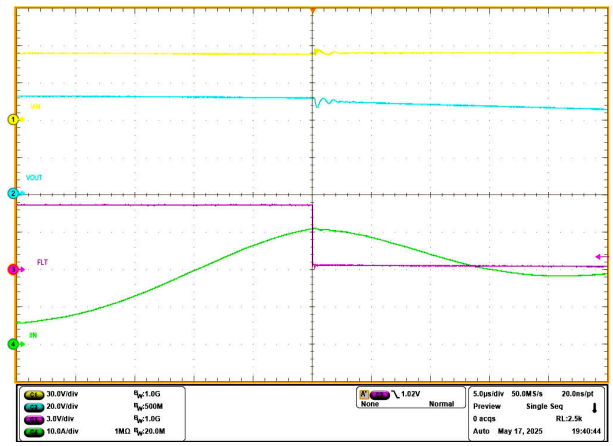

Figure 8-7. Output hot-short response

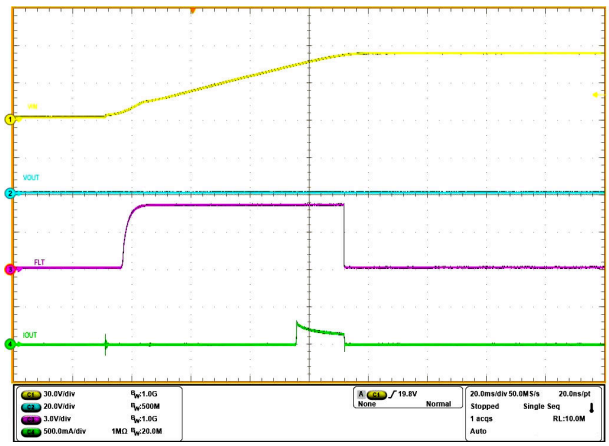

Figure 8-8. Power up into short

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8.3 Power Supply Recommendations

The TPS1686x devices are designed for a supply voltage in the range of 9V to 80V on the IN and VDD pins. TI recommends using a minimum capacitance of 0.01µF on the IN pin of each device to avoid coupling of high

slew rates during hot plug events. TI also recommends using an R-C filter from the input supply to the VDD pin on each device in parallel chain to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

8.3.1 Transient Protection

In the case of a short-circuit or circuit-breaker event when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 10µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.01µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 18.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (18)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent the device from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 8-9.

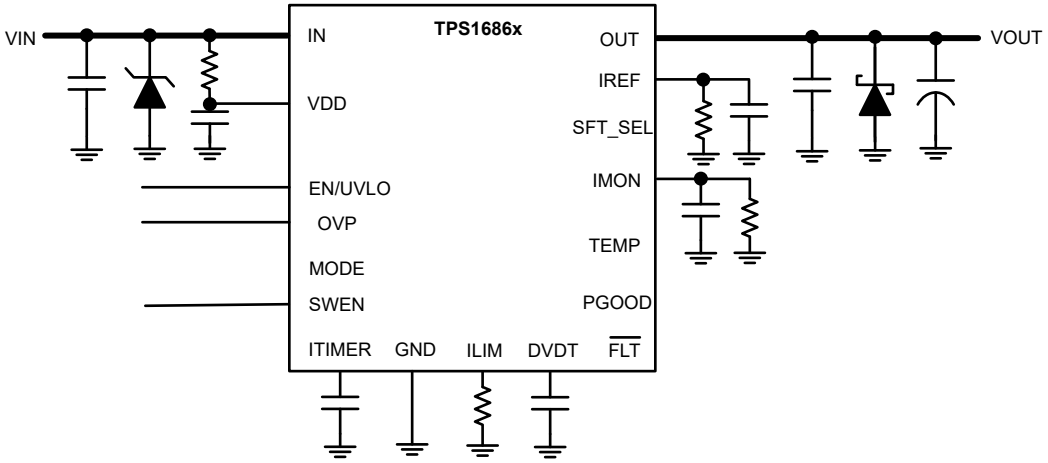

Figure 8-9. Circuit Implementation With Optional Protection Components

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8.3.2 Output Short-Circuit Measurements

Obtaining repeatable and similar short-circuit testing results is difficult. The following contributes to the variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because the device microscopically bounces and arcs. Verify that the configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.4 Layout

8.4.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.01µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 10µF or greater between the OUT terminal and GND terminal.
- The best placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See the following figure for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to the connection pins:
  - R_{ILIM}
  - R_{IMON}
  - C_{IMON}
  - C_{IREF}
  - C_{dVdT}
  - C_{ITIMER}
  - C_{IN}
  - C_{OUT}
  - C_{VDD}
  - Resistors for the EN/UVLO pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{IN}, C_{OUT}, C_{VDD}, R_{IREF}, C_{IREF}, R_{ILIM}, R_{IMON}, C_{IMON}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the IMON, IREF and ITIMER pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device the protection devices are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and the diode must be physically close to the OUT pins.

8.4.2 Layout Example

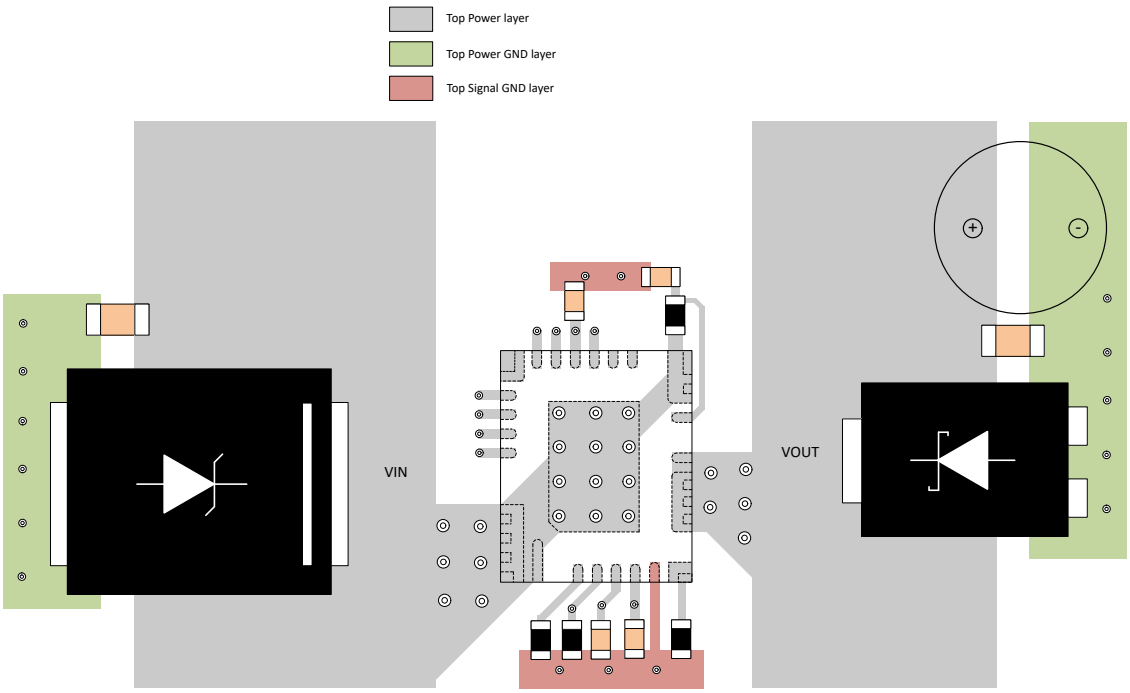

Figure 8-10. TPS1686x Device Layout Example

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TPS1686EVM eFuse Evaluation Board
- Texas Instruments, TPS1686x Design Calculator

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

PowerPad™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Advance Information Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGE OPTION ADDENDUM

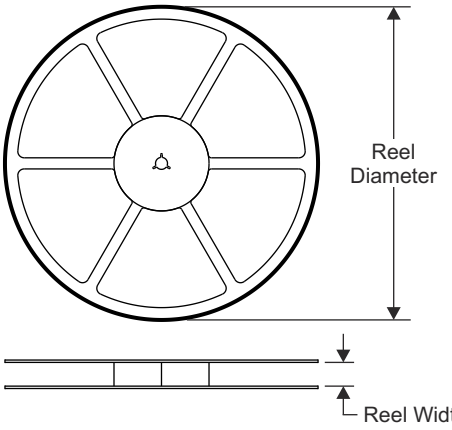
PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
PTS16860NLMR	Active	Preproduction	VQFN(NLM) | 23	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS16861NLMR	Active	Preproduction	VQFN(NLM) | 23	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

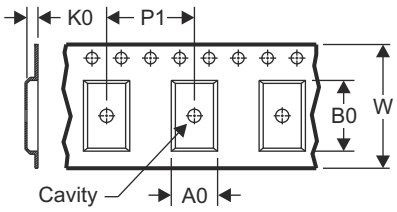
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

11.1 Tape and Reel Information

REEL DIMENSIONS

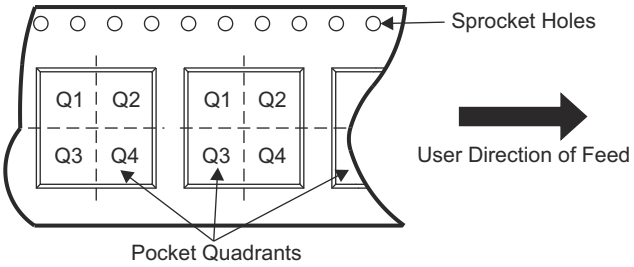


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

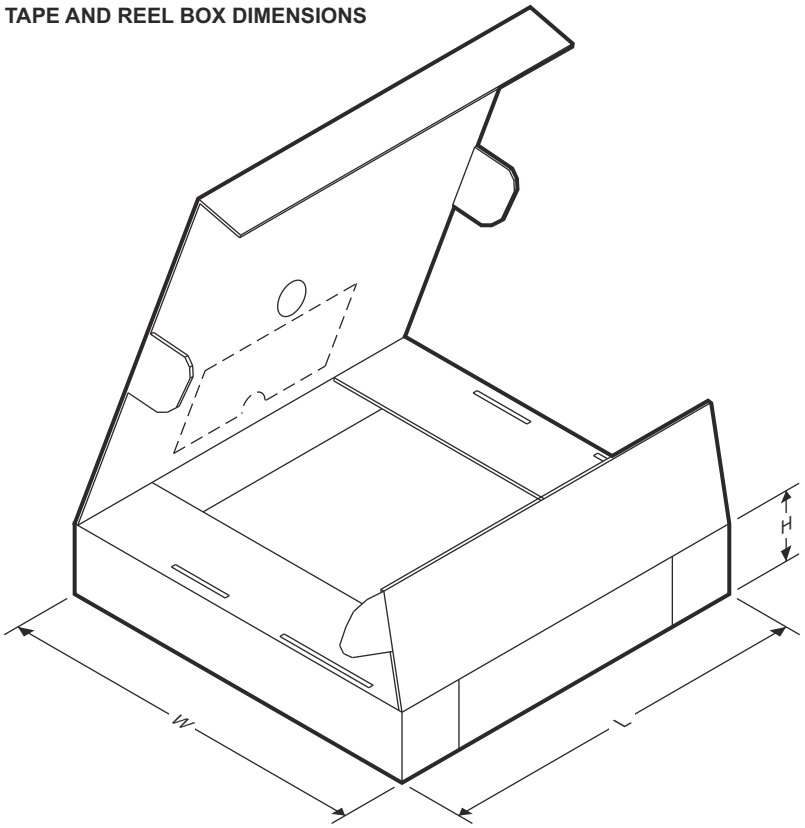


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS16860NLMR	VQFN	NLM	23	2500	330	12	5.3	6.3	1.2	8	12	Q2
PTPS16860NLMR	VQFN	NLM	23	2500	330	12	5.3	6.3	1.2	8	12	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS16860NLMR	VQFN	NLM	23	2500	367	367	38
PTPS16860NLMR	VQFN	NLM	23	2500	367	367	38

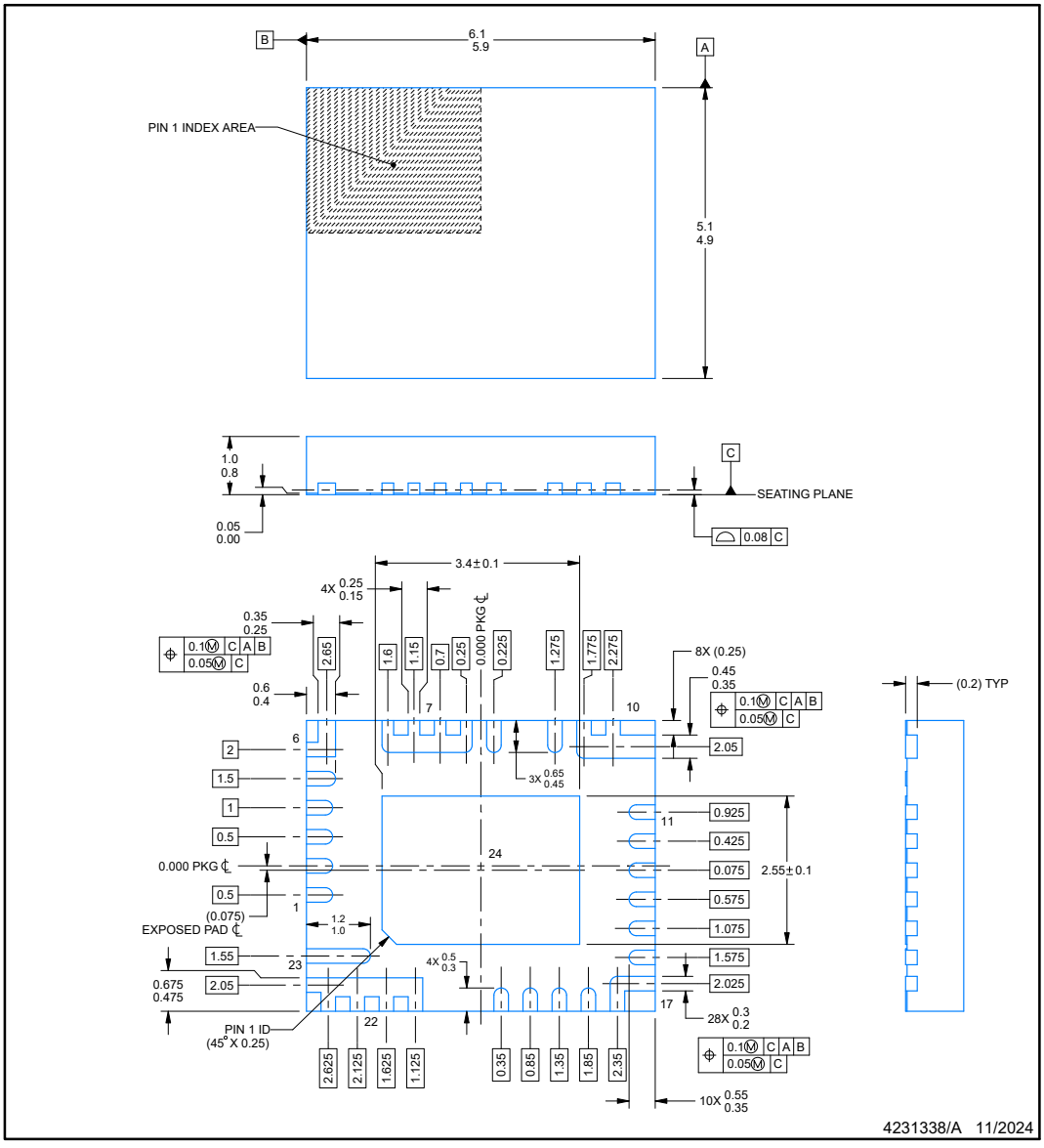
11.2 Mechanical Data

NLM0023A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

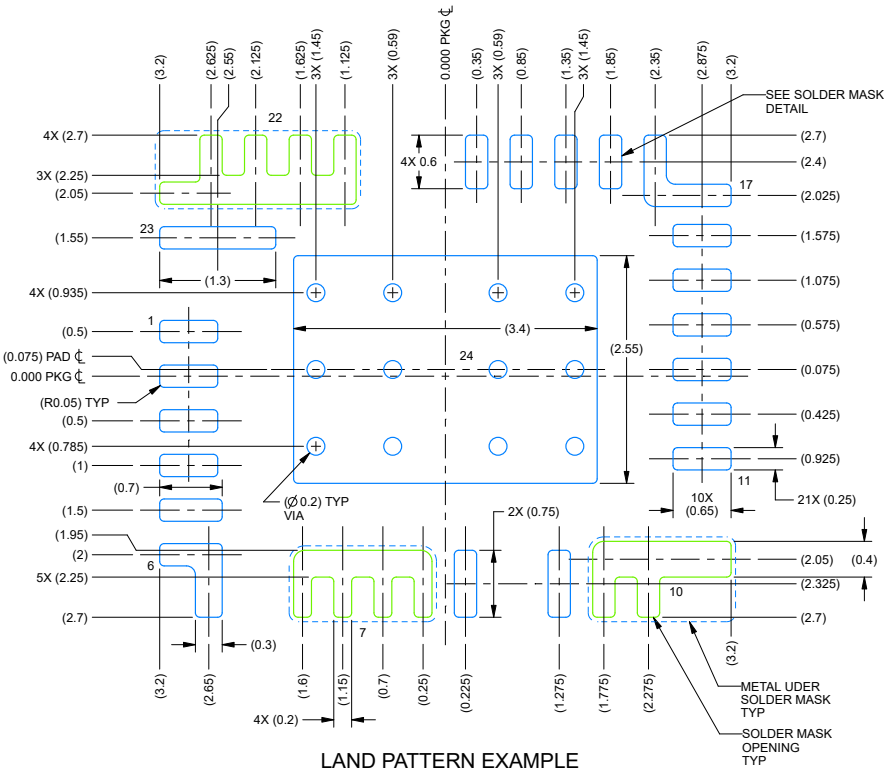
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

NLM0023A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



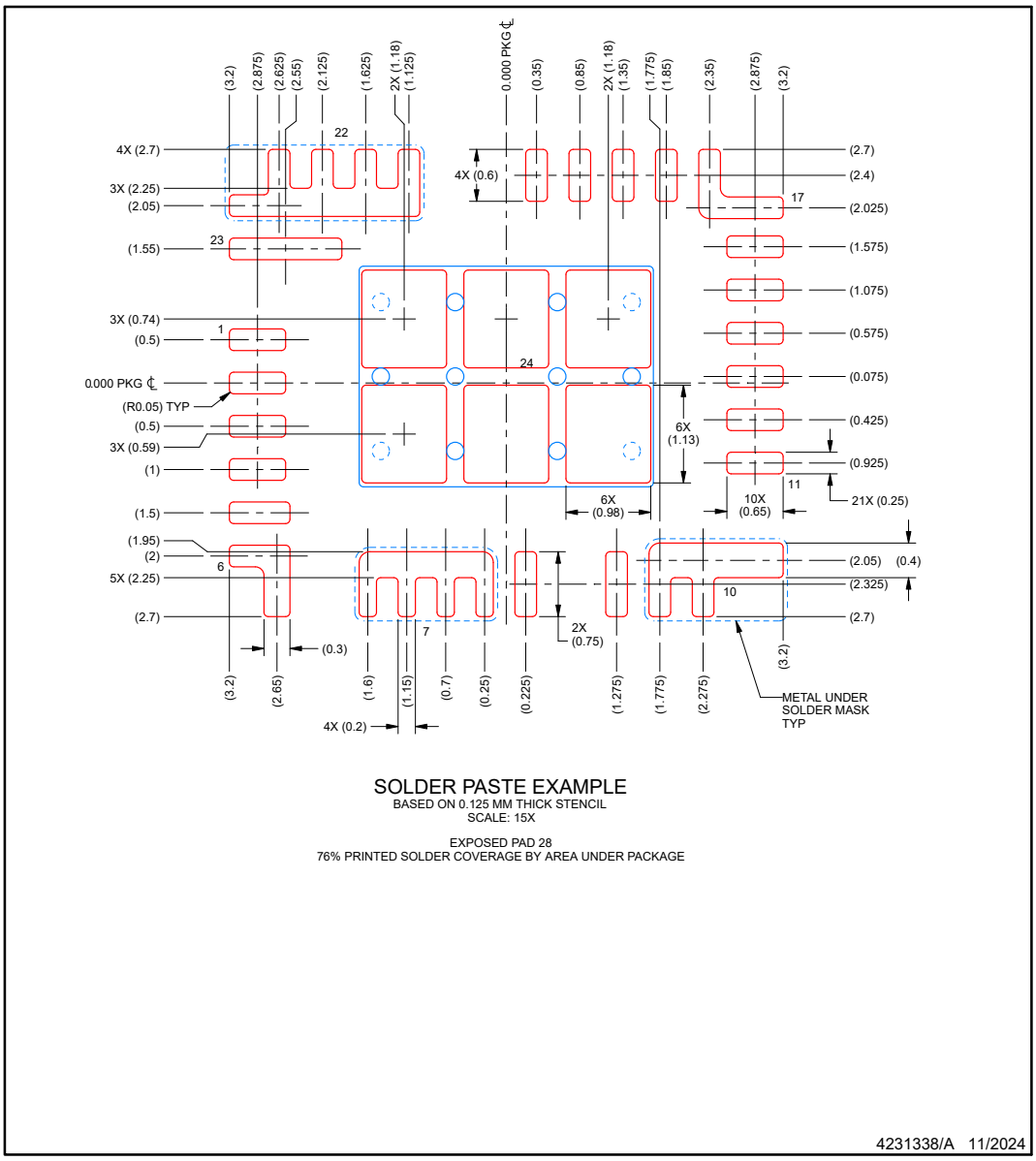
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

NLM0023A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 28
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231338/A 11/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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