IMX95CEC

i.MX 95 Applications Processors Data Sheet for Commercial Products

Rev. 2 — 11 November 2024 Preliminary Data Sheet

- For functional characteristics and the programming model, see i.*MX 95 Applications Processor Reference Manual* (IMX95RM).
- This datasheet contains information on a preproduction product. Specifications and information herein are subject to change without notice.

1 Introduction

i.MX 95 applications processors offer advanced graphics and video cores, powerful vision and machine learning acceleration, efficient CPU performance plus real-time processing and advanced security with integrated EdgeLock® secure enclave to support energy-efficient Edge Computing.

i.MX 95 applications processors integrate up to six Arm Cortex®-A55 cores and are the first i.MX devices to support functional safety with built-in Arm Cortex®-M33 which can be configured as a safety island. Optimizing performance and power efficiency for Industrial, IoT and Automotive devices, i.MX 95 processors are built with NXP's innovative Energy Flex architecture.

i.MX 95 applications processors offer a rich set of peripherals targeting automotive, industrial and commercial IoT market segments. Part of the EdgeVerse™ portfolio of intelligent edge solutions, i.MX 95 family will be offered in Commercial, Industrial, Extended Industrial and Automotive level qualification and backed by NXP's product longevity program.

Table 1. Feature summary

Subsystem	Features
Arm Cortex-A55 MPCore platform	• 6x Arm Cortex-A55, up to 2.0 GHz frequency • Arm v8.2 fully 64-bit capable • L1, L2, and L3 cache with ECC
Arm Cortex-M33 and Cortex-M7 platform	• 1x Arm Cortex-M33, up to 333 MHz frequency • 1x Cortex-M7, up to 800 MHz frequency • Arm v8-M supporting Trustzone-M • 16 kB + 16 kB / 32 kB + 32 kB cache (ECC) • 256 kB / 512 kB Tightly Coupled Memory (TCM) / on-chip SRAM (ECC)
Memory	• Up to 6.4 GT/s x 32 LPDDR5 (with Inline ECC) and 4267 MT/s x 32 LPDDR4x (with Inline ECC) • 3x uSDHC (SD3.0, SDIO3.0, eMMC5.1) • 8x LPI2C • 8x LPSPI • 2x I3C • 1x Octal SPI, including support for SPI NOR and SPI NAND memories • FlexSPI_FLR
Neural Processing Unit (NPU)	• 2.0 TOP/s Neural Network performance, up to 1.0 GHz (overdrive mode) and 800 MHz (nominal mode) • 1 MByte of SRAM embedded within the NPU, but it is available for other SoC usage when not using for ML purposes.
Graphics	• Arm Mali-G310 Graphic Processing Unit (GPU) — 3D GPU supporting 64 GFLOPs FP32 — OpenGL® ES 3.2 — Vulkan® 1.3 — OpenCL 3.0

Table continues on the next page...

Table 1. Feature summary*...continued*

Subsystem	Features
Video Processors	• 4Kp60 H.265 and H.264 encode and decode • 1x JPEG Encoder • 1x JPEG Decoder
Display Controller (up to 3 simultaneous displays)	• For 3 simultaneous displays (1x MIPI-DSI + 2x LVDS), both LVDS displays must have same resolution and timing. • 1x 350 MHz MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4kp30 or 3840 x 1440p60 • 2x 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane) • 16 kByte of SRAM, but it is available for other SoC usage when not using for 2D blitter purposes
Camera and ISP	• MIPI-CSI and ISP (2x 4-lane, 2.5 Gbps/lane) with PHY (one mux'd with DSI) • Up to 1x 4Kp60 fps (if one MIPI CSI is enabled), 2x 4Kp30, 4x 1080p60, or 8x 1080p30 • Up to 8x cameras with MIPI virtual channels • 96 kByte of SRAM, but it is available for other SoC usage when not using for ISP purposes.
Audio	• 5x Synchronous Audio Interfaces (SAI) • 17-lane I2S TDM (32-bit at 768 kHz frequency) • SPDIF Rx and SPDIF Tx • 8-channel PDM Microphone Interface (MICFIL) • 2 x Medium Quality Sound (MQS)
Connectivity	• 2x PCIe Gen 3.0 (1-lane) • 1x USB3.0 Type C with PHY • 1x USB2.0 with PHY • 2x 1 Gbps Ethernet ports with Time Sensitive Networking (TSN) capabilities • 1x 10 Gbps Ethernet port with Time Sensitive Networking (TSN) capabilities • IEEE 1588 for sync; and EEE • 5x CAN-FD • 2x 32-pin FLEXIO interfaces (bus or serial I/O)
Low Speed Communication Peripherals	• 8x UART
Timer and PWMs	• 2x Low Power Periodical Interrupt Timers (LPIT)

Table continues on the next page...

Table 1. Feature summary*...continued*

Subsystem	Features
	— 4-channel — 4 external trigger sources — Generic 32-bit resolution timer — Periodical interrupt generation • 6x Timer/PWM modules (TPM) — Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128 — 16-bit counter, support free-running counter or modulo counter mode, counting up or down — Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode • 2x Low-Power Timers (LPTMR) • 5x WatchDog modules (WDOG) • 1x System Counter (SYS_CTR) • 1x Timestamp Timer (TSTMR) • 1x General Purpose Timer (GPT)
GPIO and Pin Multiplexing	• General-purpose input/output (GPIO) modules with interrupt capability • Input/Output Multiplexing Controller (IOMUXC) to provide centralized pad control
Analog	• FRO Clock Generator (FRO_TUNER) • 2x Temperature Sensor (TEMPSENSE) • 16-channel, 12-bit Analog-to-Digital Converter (SAR_ADC) • 1x Trigger Mux (TRGMUX) to configure the trigger inputs for various peripherals
Clocking	• CCM • OSC • LPCG
Safety	• Integrated functional safety • Targeting ISO26262 ASIL-B and IEC61508 SIL2 compliance
Security	• Trusted Resource Domain Controller (TRDC) — Supports up to 16 resource domains • Arm TrustZone® (TZ) architecture • Secure and trusted access control • EdgeLock™ Secure Enclave

Table continues on the next page...

Table 1. Feature summary...*continued*

Subsystem	Features
	• Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, fine-grain key management augmented by extensive crypto services
System Debug	• Arm CoreSight® debug and trace architecture • Trace Port Interface Unit (TPIU) to support off-chip real-time trace • Support for 4-pin (JTAG) and SWD debug interfaces
Power management	• Supports PMIC integration to supply all power rails • Multiple power domains allow power gating of most digital and analog logic in low power mode • General Power Controller (GPC), several factors are involved in power management, not just a central controller
Package	• 15 x 15 mm FCBGA, 0.5 mm pitch • 19 x 19 mm FCBGA, 0.7 mm pitch

1.1 Ordering Information

Figure 1 describes the part number nomenclature, so the users can identify the characteristics of the specific part number.

Part Numbers : Not every combination of package, temperature qualification, core count, and feature enablement is available.

Part Type	i.MX Family	Segment	A-Core Qty.	Temp. Qual.	Package	Fab Source	A-Core Freq	Special	Silicon Revision
P	IMX95	9	6	A	VZ	X	N	A	B

Value	Short Description	A-Cores Qty	ISP	NPU	GPU	VPU	Display Controller	FuSa[1]	Temp. Qual.	Packages
9	Full Featured[4]	6 / 4 / 2[3]	✓	✓	✓	✓	✓	✓	A/C/D/X	VT/VY[2]/VZ
7	Vision[4]	6 / 4	✓	✓		✓		✓	A/C/D/X	VT/VY/VZ
5	HMI[4]	6 / 4		✓	✓	✓	✓	✓	A/C/D/X	VT/VY/VZ
3	Compute[4]	6 / 4 / 2[3]		✓				✓	A/C/D/X	VT/VY[2]/VZ
N	Networking[4]	6						✓	C/X	VZ

Cortex-A55 CPU Frequency	
Q[2]	2.0 GHz[2]
N	1.8 GHz
L	1.6 GHz
F	1.0 GHz

Special Fuse	
A	No special Fuse
C	Reserved
D	Reserved
M	ISP Tool Licensed
S	Reserved

Silicon Revision	
A	Rev 1.0 (A0)
B	Rev 2.0 (A1)
C	Rev 3.0 (B0)

Fab Source	
X	Single Source
Y	Multiple Source

Family	
IMX95	i.MX 95xx

Cortex-A Cores	
6	6 Cores
4	4 Cores
2	2 Cores

Part Type	
P	Sample
M	Mass Production
S	Special

Package Type	
VT	15 x 15 mm, 0.5 mm pitch, FCBGA (no lid)
VY	19 x 19 mm, 0.7 mm pitch, FCBGA (lidded)
VZ	19 x 19 mm, 0.7mm pitch, FCBGA (no lid)

Temperature Qualification	
A	Automotive: -40°C T_a to 125°C T_j
C	Industrial: -40°C T_a to 105°C T_j
D	Commercial: 0°C T_a to 95°C T_j
X	Extended Industrial: -40°C T_a to 125°C T_j

1. Functional Safety enablement via paid NXP Professional Services delivery of Safety Manager, Safety Manual, and Software (Safety Manager and SafeAssure packages).
2. 2.0GHz A-Core frequency available in i.MX 95 19x19 lidded package with Commercial Qualification only and requires suitable application and thermal solution to maintain operating environment between 0°C Ta and 95°C Tj in Super Overdrive mode.
3. 2x A-Core part available in Commercial temperature qualification only, with 1GHz A-core frequency.
4. 10Gb Ethernet is available on all VY/VZ (19 x 19) packages but not VT (15 x 15) due to pin-mux restrictions.
5. Special Fuse set to "M" denotes ISP tuning tools license. Only applicable on ISP enabled family segments.

Figure 1. Part number nomenclature - i.MX 95

Table 2 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers.

Table 2. Orderable part numbers

Product Part Number	Family	Number of Cortex®-A55 Cores	Qualification tier	Maximum speed	ISP	NPU	GPU	VPU	Display controller	10G	Package
MIMX9596DVTXQAA	95	6	Commercial	2.0 GHz	•	•	•	•	•	•	15 x 15 mm, 0.5 mm pitch
MIMX9594DVTXQAA	95	4	Commercial	2.0 GHz	•	•	•	•	•	•	15 x 15 mm, 0.5 mm pitch
MIMX9586DVTXQAA	95	6	Commercial	2.0 GHz		•	•	•	•		15 x 15 mm, 0.5 mm pitch
MIMX9584DVTXQAA	95	4	Commercial	2.0 GHz		•	•	•	•		15 x 15 mm, 0.5 mm pitch
MIMX9556DVTXQAA	95	6	Commercial	2.0 GHz	•		•	•	•		15 x 15 mm, 0.5 mm pitch
MIMX9554DVTXQAA	95	4	Commercial	2.0 GHz	•		•	•	•		15 x 15 mm, 0.5 mm pitch
MIMX9544DVTXQAA	95	4	Commercial	2.0 GHz	•	•		•			15 x 15 mm, 0.5 mm pitch
MIMX9542DVTXQAA	95	2	Commercial	2.0 GHz	•	•		•			15 x 15 mm, 0.5 mm pitch
MIMX9536DVTXQAA	95	6	Commercial	2.0 GHz		•				•	15 x 15 mm, 0.5 mm pitch
MIMX9534DVTXQAA	95	4	Commercial	2.0 GHz		•				•	15 x 15 mm, 0.5 mm pitch
MIMX9532DVTXQAA	95	2	Commercial	2.0 GHz		•				•	15 x 15 mm, 0.5 mm pitch
MIMX9516DVTXQAA	95	6	Commercial	2.0 GHz							15 x 15 mm, 0.5 mm pitch
MIMX9514DVTXQAA	95	4	Commercial	2.0 GHz							15 x 15 mm, 0.5 mm pitch
MIMX9512DVTXQAA	95	2	Commercial	2.0 GHz							15 x 15 mm, 0.5 mm pitch

Table continues on the next page...

Table 2. Orderable part numbers...*continued*

Product Part Number	Family	Number of Cortex®-A55 Cores	Qualification tier	Maximum speed	ISP	NPU	GPU	VPU	Display controller	10G	Package
MIMX9596DVZXQAA	95	6	Commercial	2.0 GHz	•	•	•	•	•	•	19 x 19 mm, 0.7 mm pitch (no lid)
MIMX9596DVYXQAA	95	6	Commercial	2.0 GHz	•	•	•	•	•	•	19 x 19 mm, 0.7 mm pitch (lid)

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/IMX or contact an NXP representative for details.

2 Block Diagram

Figure 2 shows the functional modules in the i.MX 95 processor system.

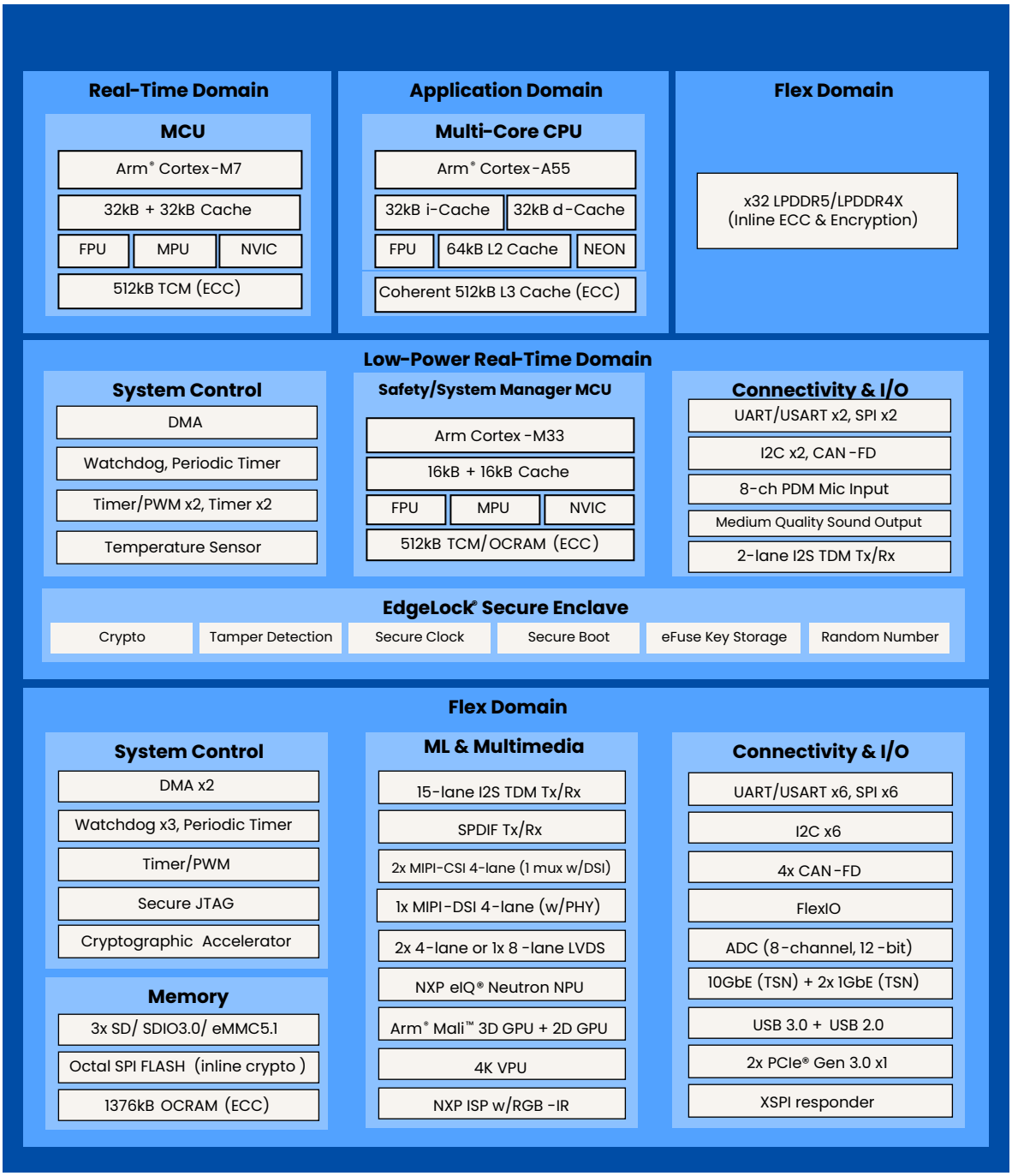


Figure 2. i.MX 95 system block diagram

NOTE

Some modules shown in this block diagram are not offered on all derivatives.

3 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 95 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section, "Package information and contact assignments". Signal descriptions are provided in the i.MX 95 Reference Manual (IMX95RM).

Table 3. Special signal considerations

Signal Name	Remarks
CLKIN1/CLKIN2	CLKIN1 and CLKIN2 are input pins without internal pull-up and pull-down.
NC	These signals are No Connect (NC) and should be unconnected in the application.
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
POR_B	POR_B has no internal pull-up/down resistor, and requires external pull-up resistor to NVCC_BBSM. It is recommended that POR_B is properly handled during power up/down. Please refer to the EVK design for details.
RTC_XTALI/ RTC_XTALO	RTC_XTALI and RTC_XTALO can be coupled to an external crystal element to generate 32.768K clock. Care must be taken to account parasitic capacitance of the pins in order to match the trimmed crystal assumptions for frequency accuracy. Care should also be taken to limit the parasitic leakage on or between RTC_XTALI and RTC_XTALO. This can debias the integrated amplifier resulting in reduced startup margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_ANA_1P8 level and the frequency shall be < 50 kHz under the typical conditions.
XTALI_24M/ XTALO_24M	The system requires a 24 MHz clock to operate. A 24 MHz crystal can be created by coupling an appropriately tuned quartz element to XTALI and XTALO. Care must be taken that the resulting oscillation frequency complies with the utilized serial interface standards such as PCIe and USB.

3.1 Unused input and output guidance

If a function of the i.MX 95 is not used, the I/Os and power rails of that function can be terminated to reduce overall board power.

Table 4. Unused function strapping recommendations for LVDS

Function	Pin name	Recommendations if unused
Single LVDS0	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N	Not connected
Single LVDS1	LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N	Not connected
Both LVDS0 and LVDS1	LVDS0_CLK_P, LVDS0_CLK_N, LVDS0_Dx_P, LVDS0_Dx_N, LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N,	Not connected
	VDD_LVDS_1P8	Tie to ground using a 10K resistor

Table 5. Unused function strapping recommendations for MIPI

Function	Pin name	Recommendations if unused
MIPI_DSICSI1	MIPI_DSICSI1_CLK_P, MIPI_DSICSI1_CLK_N, MIPI_DSICSI1_DX_P, MIPI_DSICSI1_DX_N,	Not connected
MIPI_CSI1	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_DX_P, MIPI_CSI1_DX_N,	Not connected
Both MIPI_CSI1 and MIPI_DSICSI1	MIPI_REXT, MIPI_DSICSI1_CLK_P, MIPI_DSICSI1_CLK_N, MIPI_DSICSI1_DX_P, MIPI_DSICSI1_DX_N, MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_DX_P, MIPI_CSI1_DX_N,	Not connected
	VDD_MIPI_1P8, VDD_MIPI_0P8,	Tie to ground using a 10K resistor

Table 6. Unused function strapping recommendations for USB

Function	Pin name	Recommendations if unused
USB1	USB1_VBUS, USB1_ID, USB1_D_P, USB1_D_N, USB1_TX0, USB1_RX0, USB1_TX1, USB1_RX1, USB1_TXRTUNE	Not connected
USB2	USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE	Not connected
Both USB1 and USB2	USB1_VBUS, USB1_ID, USB1_D_P, USB1_D_N, USB1_TX0, USB1_RX0, USB1_TX1, USB1_RX1, USB1_TXRTUNE, USB2_VBUS, USB2_ID, USB2_D_P, USB2_D_N, USB2_TXRTUNE,	Not connected
	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Tie to ground using a 10K resistor

Table 7. Unused function strapping recommendations for PCIe

Function	Pin name	Recommendations if unused
Single PCIE1	PCIE1_TX0_P, PCIE1_TX0_N, PCIE1_RX0_P, PCIE1_RX0_N,	Not connected
	PCIE1_REF_PAD_CLK_P, PCIE1_REF_PAD_CLK_N	Tie to ground using a 10K resistor
Single PCIE2	PCIE2_TX0_P, PCIE2_TX0_N, PCIE2_RX0_P, PCIE2_RX0_N,	Not connected
	PCIE2_REF_PAD_CLK_P, PCIE2_REF_PAD_CLK_N	Tie to ground uisng a 10K resistor

Table continues on the next page...

Table 7. Unused function strapping recommendations for PCIe...*continued*

Function	Pin name	Recommendations if unused
Both PCIE1 and PCIE2	PCIE1_TX0_P, PCIE1_TX0_N, PCIE1_RX0_P, PCIE1_RX0_N, PCIE2_TX0_P, PCIE2_TX0_N, PCIE2_RX0_P, PCIE2_RX0_N	Not connected
	VDD_PCI_1P8, VDD_PCI_0P8	Tie to ground uisng a 10K resistor
	PCIE1_REF_PAD_CLK_P, PCIE1_REF_PAD_CLK_N, PCIE2_REF_PAD_CLK_P, PCIE2_REF_PAD_CLK_N	Tie to ground using a 10K resistor
	PCIE_REF_OUT_CLK_P, PCIE_REF_OUT_CLK_N	Not connected

Table 8. Unused function strapping recommendations for Audio Transceiver

Function	Pin name	Recommendations if unused
Audio transceiver unused	AUD_AUX, AUD_P_UTIL, AUD_N_HPD	Not connected
	VDD_AUD_1P8	Should be supplied

Table 9. Unused function strapping recommendations for 10G ETH Serdes

Function	Pin name	Recommendations if unused
10G ETH Serdes	ETH_TX0_P, ETH_TX0_N, ETH_RX0_P, ETH_RX0_N, ETH_RESREF, ETH_REF_PAD_CLK_P, ETH_REF_PAD_CLK_N	Not connected
	VDD_ETH_1P8, VDD_ETH_0P8	Tie to ground using a 10K resistor

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 95 family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 10 for a quick reference to the individual tables and sections.

Table 10. i.MX 95 chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	See Absolute maximum ratings
Thermal resistance	See Thermal resistance

Table continues on the next page...

Table 10. i.MX 95 chip-level conditions...*continued*

For these characteristics, …	Topic appears …
Operating ranges	See Operating ranges
Clock sources	See Clock source
Power modes	See Power modes
Power supplies requirements and restrictions	See Power supplies requirements and restrictions

4.1.1 Absolute maximum ratings

CAUTION: Stresses beyond those listed in the following table may reduce the operating lifetime or cause immediate permanent damage to the device. The table below does not imply functional operation beyond those indicated in the operating ranges and parameters table.

Table 11. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ARM	Core supplies input voltages	-0.3	—	1.12	V	—
VDD_SOC	Core supplies input voltages	-0.3	—	1.08	V	—
NVCC_SD2	IO supply for SD2	-0.3	—	3.96	V	—
VDD2H_DDR	DDR PHY supply voltage	-0.3	—	1.32	V	—
VDDQ_DDR	DDR I/O supply voltage	-0.3	—	0.72	V	—
VDD_DDR_0P8	DDR I/O supply voltage	-0.3	—	0.96	V	—
NVCC_CCM_DAP	CCM supply voltage [1]	-0.3	—	3.96	V	—
NVCC_BBSM_1P8	IO supply and IO Pre-driver supply for BBSM bank	-0.3	—	2.16	V	—
USB1_VBUS, USB2_VBUS	USB VBUS input detected	-0.3	—	3.96	V	—
VDD_USB_0P8	Power for USB OTG PHY	-0.3	—	0.96	V	—
VDD_USB_1P8	Power for USB OTG PHY	-0.3	—	2.16	V	—
VDD_USB_3P3	Power for USB OTG PHY	-0.3	—	3.96	V	—
VDD_MIPI_0P8	MIPI PHY supply voltage	-0.3	—	0.96	V	—
VDD_MIPI_1P8	MIPI PHY supply voltage	-0.3	—	2.16	V	—
VDD_PCI_0P8	PCI PHY supply voltage	-0.3	—	0.96	V	—
VDD_PCI_1P8	PCI PHY supply voltage	-0.3	—	2.16	V	—
VDD_AUD_1P8	Audio transceiver supply voltage	-0.3	—	2.16	V	—
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON, NVCC_ENET	GPIO supply voltage	-0.3	—	3.96	V	—

Table continues on the next page...

Table 11. Absolute maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ETH_0P8	Digital supply for Ethernet PHY	-0.3	—	0.96	V	—
VDD_ETH_1P8	I/O voltage supply and analog high voltage power supply [1]	-0.3	—	2.16	V	—
VDD_LVDS_1P8	LVDS PHY supply voltage	-0.3	—	2.16	V	—
VDD_ANA_0P8	Analog core supply voltage	-0.3	—	0.96	V	—
VDD_ANA_1P8	Analog core supply voltage [1]	-0.3	—	2.16	V	—
VDD_ANAVDET_1P8	Analog core supply voltage	-0.3	—	2.16	V	—
TSTORAGE	Storage temperature range	-55	—	150	℃	—

1. This supply being incorrect can cause the IO pads to be misconfigured causing damage.

4.1.2 Electrostatic discharge and latch-up ratings

Table 12. Electrostatic discharge and latch-up ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VHBM	Electrostatic Discharge (ESD): Human Body Model (HBM) [1]	-1000	—	1000	V	—
VCDM	Electrostatic Discharge (ESD): Charged Device Model (CDM) [2]	-250	—	250	V	—
ILAT	Latch UP (LU) Immunity level: Class I at 25 °C ambient temperature [3]	-100	—	100	mA	—
ILAT	Latch UP (LU) Immunity level: Class II at 105 °C ambient [3]	-100	—	100	mA	—

1. Determined according to JEDEC Standard JS001, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
2. Determined according to JEDEC Standard JS002, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
3. Determined according to JEDEC Standard JESD78, IC Latch-up Test.

4.1.3 Thermal resistance

4.1.3.1 15 x 15 mm FCBGA package thermal characteristics

Table 13 displays the 15 x 15 mm FCBGA package thermal resistance data.

Table 13. 15 x 15 mm FCBGA thermal resistance data

Rating	Board Type[1]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	15.7	℃/W
Junction-to-Top of Package	JESD51-9, 2s2p	Ψ_{JT}	0.1	℃/W

Table continues on the next page...

Table 13. 15 x 15 mm FCBGA thermal resistance data...*continued*

Rating	Board Type[1]	Symbol	Value	Unit
Thermal Characterization parameter[2]				
Junction to Case Thermal Resistance[3]	N/A	$R_{\theta JC}$	0.2	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9). Test board has 40 vias under die shadow mapped according to BGA layout under die. Each vias is 0.2 mm in diameter and connects top layer with the first buried plane layer.
2. Determined in accordance to JEDEC JESD51-2A natural convection environment.
3. Junction-to-Case (top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface temperature.

4.1.3.2 19 x 19 mm FCBGA package thermal characteristics

Table 14 displays the 19 x 19 mm FCBGA package thermal resistance data.

Table 14. 19 x 19 mm FCBGA thermal resistance data

Rating	Board type[1]	Symbol	Value		Unit
			Bare die	Lidded	
Junction to Ambient thermal resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	13.4	12.3	°C/W
Junction-to-Top of package thermal characterization parameter[2]	JESD51-9, 2s2p	ψ_{JT}	0.1	0.4	°C/W
Junction to Case thermal resistance[3]	JESD51-9, 1s	$R_{\theta JC}$	0.2	0.6	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface.

4.1.4 Power architecture

The power architecture of i.MX 95 is defined based on the assumption that systems are constructed for the case where the PMIC is used to supply all the power rails to the processor. The SoC can be powered from discrete parts rather than a PMIC, but a discrete-based solution is not necessarily BOM cost-optimized.

NVCC_BBSM_1P8 must be powered first and stay until the last.

Majority of the digital logic is supplied with two supplies: VDD_ARM and VDD_SOC.

- VDD_ARM is for the CORTEXAMIX.
- VDD_SOC is for the rest of the modules in SoC.

The VDD_SOC has following modes:

- Overdrive mode
- Nominal mode
- Underdrive mode

- Suspend mode

GPIO interfaces functionally only need to operate at 1.8 V. One exception is the SD card interface, which must support both 1.8 V and 3.3 V (for compatibility with legacy 3.3 V SD cards), as well as the “GPIO” pins that may be connected to a RPi-like expansion connector (which for compatibility with components in the ecosystem need to be able to support 3.3 V, while also needing to support 1.8 V for 1.8 V-optimized designs).

The DRAM controller and PHY have multiple external power supplies:

Table 15. Power supplies of the DRAM controller and PHY

Power supplies	Modules
VDD_SOC	SoC synthesized DRAM controller digital logic
VDD_ANA_0P8/VDD_DDR_0P8	DRAM PLL and PHY digital logic
VDD_ANA_1P8	DRAM PLL and PHY analog circuitry
VDD2H_DDR	DRAM PHY I/O supply (1.1 V for LPDDR4X and 1.05 V for LPDDR5)
VDDQ_DDR	DRAM PHY I/O supply (0.6 V for LPDDR4X and 0.5 V for LPDDR5)

For all the integrated analog modules, their 1.8 V analog power will be supplied externally through power pads. These supplies are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For the integrated LVDS PHY, PCIe PHY, and USB PHYs, their 3.3 V (where supported), 1.8 V and their digital power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For BBSM/RTC, the 1.8 V IO pre-driver supply and 1.8 V IO pad supply will also be supplied externally. The BBSM_LP core digital domain logic is supplied by an internal LDO.

Figure 3 is the power architecture diagram for the whole chip. Note that it only shows power supplies and does not show capacitors that may be required for internal LDO regulators.

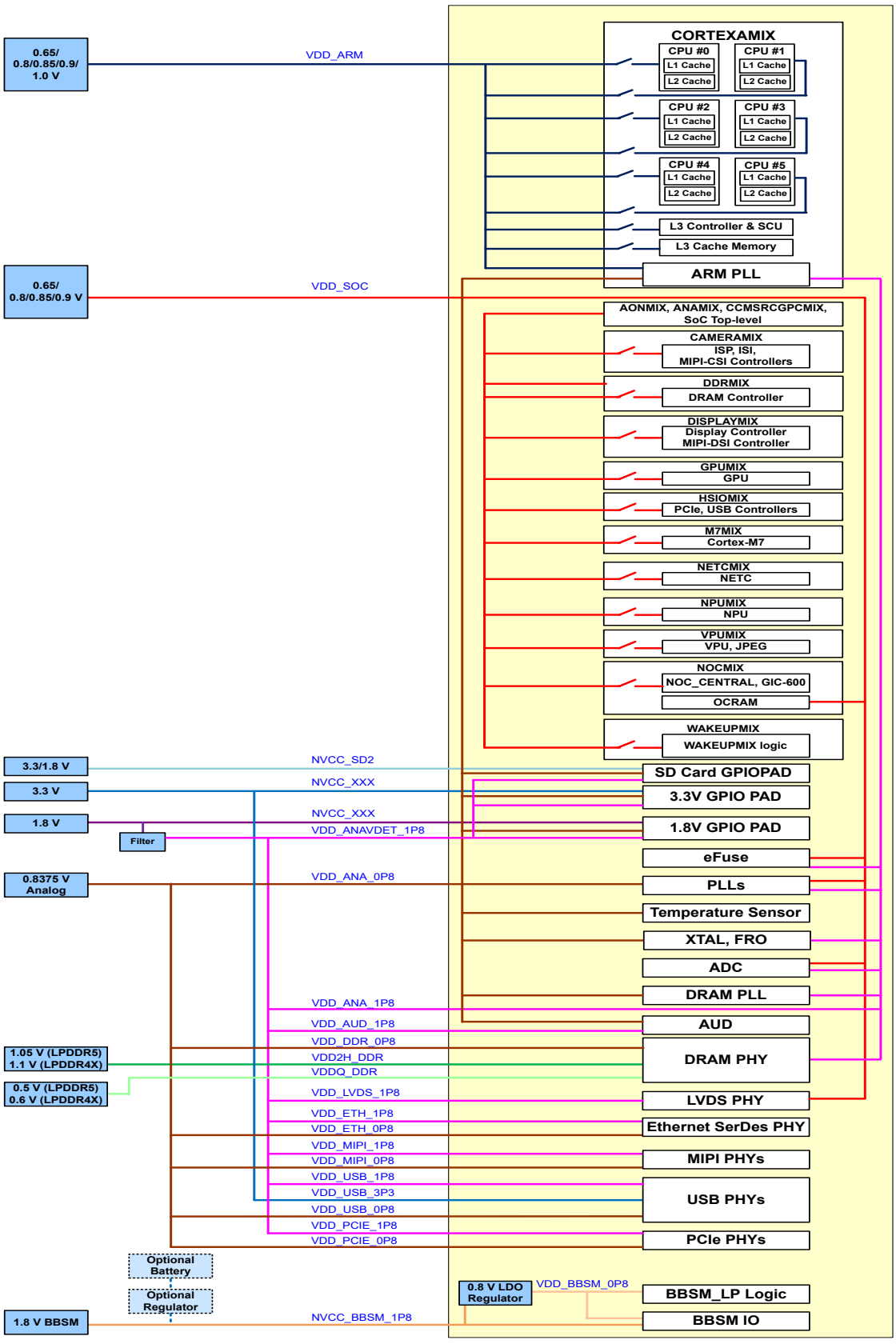


Figure 3. Power architecture of i.MX 95 family of processors

4.1.4.1 Ramp rate specifications

Table 16. Ramp rate specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD[VDD_SOC, VDD_ARM], VDD_ANA_0P8	Power supply for SoC logic, Cortext-A-55 core, PLLs, temperature sensor, and LVCMOS I/O	0.1	—	30	V/ms	Voltage level = 0.8 V
VDDQ_DDR / VDD2H_DDR	Voltage supply for LPDDR5/ LPDDR4X PHY, LPDDR5/ LPDDR4X mode	0.1	—	5	V/ms	Voltage level = 0.6 V / 1.1 V
VDD_ANA_1P8/ VDD_ANAVDET_1P8	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC, and 24 MHz XTAL	0.1	—	5	V/ms	Voltage level = 1.8 V
VDD_USB_3P3	3.3 V supply for USB PHY	0.1	—	30	V/ms	Voltage level = 3.3 V
NVCC_XXX	Power supply for GPIO	0.1	—	30	V/ms	Voltage level = 1.8 / 3.3 V
NVCC_BBSM_1P8	I/O supply for GPIO in BBSM bank	0.1	—	30	V/ms	Voltage level = 1.8 V

4.1.5 Power modes

This section introduces the power modes used in the i.MX 95.

4.1.5.1 Power mode definition

The i.MX 95 supports the following power modes:

- RUN Mode: All external power rails are on, the Cortex-A55 is active and running; other internal modules can be on/off based on application.
- Low Power RUN Mode: This mode is defined as a very low power run mode with all external power rails are on. In this mode, all the unnecessary power domain (MIX) can be off, except AONMIX and M7MIX. Cortex-M33 CPU in AONMIX runs System Manager and Cortex-M7 CPU in M7MIX handles all the computing and data processing. Cortex-A55 is power down and DRAM can be in self-refresh/retention mode. To use modules in other power domain, such as WAKEUPMIX, the user can turn on additional peripherals and related power as needed. Additional low power modes are also supported, but do not have power characterized in the Data Sheet. Refer to the Reference Manual for a full set of power management capabilities.
- IDLE Mode: This mode is defined as a mode, which the Cortex-A55 can automatically enter when there is no thread running and all high-speed devices are not active. The Cortex-A55 can be put into power gated state but with L3 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated, but still remains powered. Compared with RUN mode, all the external power rails from the PMIC remain the same and most of the modules still remain in their state, so the interrupt response in this mode is very small.
- SUSPEND Mode: This mode is defined as the most power saving mode where all the clocks are off (including the Cortex-M33 CPU, which is in AONMIX and cannot be power gated), all the unnecessary power supplies are off and all power gateable portions of the SoC are power gated. The Cortex-A55 CPUs and the Cortex-M7 CPU are fully power gated, all internal digital logic and analog circuit that can be powered down will be off, all PHYs are power gated. DRAM is set at self-refresh/retention mode. VDD_SOC (and related digital supply) voltage is reduced to the “Suspend mode” voltage. The exit time from this mode will be much longer than IDLE, but the power consumption will also be much lower.
- BBSM Mode: This mode is also called RTC mode. Only the power for the Battery Backed non-Secure Module (BBNSM) and Battery Backed Secure Module (BBSM) remain on to keep RTC, BBNSM and BBSM logic are alive.

- OFF Mode: All power rails are off.

NOTE

Beyond the modes defined here, additional options can be configured in software, such as to adjust clock frequencies or gate clocks through the CCM programming model, or to adjust on-die power-gating through the SRC or GPC programming model, or to adjust the voltage supplied to the VDD_SOC and VDD_ARM supplies as per Operating ranges in the Data Sheet.

NOTE

These power modes are different than the voltage mode ranges.

Table 17 summarizes the external power supply states in all the power modes.

Table 17. The power supply states

Power rail	OFF	BBSM	Low power SUSPEND (1.8 V Analog off)	SUSPEND	IDLE	RUN/LP RUN
NVCC_BBSM_1P8	OFF	ON	ON	ON	ON	ON
VDD_ARM	OFF	OFF	OFF or ON[1]	OFF or ON[1]	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON	ON
VDD2_DDR VDDQ_DDR	OFF	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON	ON
VDD_ANA_0P8 VDD_DDR_0P8 VDD_ETH_0P8 VDD_MIPI_0P8 VDD_PCI_0P8 VDD_USB_0P8	OFF	OFF	ON	ON	ON	ON
VDD_ANA_1P8/VDD_ANAVDET_1P8 VDD_AUD_1P8 VDD_ETH_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_PCI_1P8 VDD_USB_1P8 VDD_USB_3P3	OFF	OFF	OFF	ON	ON	ON

1. When SoC in a low power state, it can save more power when configuring PMIC to turn VDD_ARM off vs having the PMIC continue to supply VDD_ARM and rely on the on-die powergating around the CORTEXAMIX components.

4.1.5.2 Low power modes

The state of each module in the IDLE, SUSPEND, and BBSM modes are defined in the Table 18.

Table 18. Low power mode definition

	IDLE	SUSPEND	BBSM
CCM LPM mode	WAIT	STOP	N/A
Arm A55 CPU*	OFF	OFF	OFF
Shared L3 cache	ON	OFF	OFF
MEDIAMIX GPUMIX NPUMIX VPUMIX	OFF	OFF	OFF
DRAM controller and PHY	ON	OFF	OFF
ARM_PLL	OFF	OFF	OFF
DRAM_PLL	OFF	OFF	OFF
SYSTEM_PLL1	ON	OFF	OFF
XTAL	ON	OFF	OFF
RTC	ON	ON	ON
External DRAM device	Self-Refresh[1]	Self-Refresh [2]	OFF
USB PHY	In Low Power State	OFF	OFF
DRAM clock	266 MHz	OFF	OFF
AXI clock	133 MHz	OFF	OFF
Module clocks	ON as needed	OFF	OFF
EdgeLock	ON	ON	OFF
GPIO Wakeup	Yes	Yes	No
RTC Wakeup	Yes	Yes	Yes
USB remote wakeup[3]	Yes	No[4]	No
Other wakeup source	Yes	No	No

1. Automatic enter self-refresh when there is no DRAM access
2. Put into self-refresh mode by SW before entering low power mode

3. Remote wakeup can be supported if the USB PHY power is on in this mode.
4. Turn off externally by PMIC when PMIC_STBY_REQ signal is asserted.

4.1.6 Operating ranges

The following table provides the operating ranges of the i.MX 95 processors. For details about the power structure of processors, see the “Clock and Power Overview” chapter of the i.MX 95 Reference Manual (IMX95RM).

Table 19. Operating ranges

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_SOC	Power supply for SoC logic [1]	0.85	0.90	0.955	V	Power supply for SoC, overdrive mode
VDD_SOC	Power supply for SoC logic [1]	0.80	0.85	0.905	V	Power supply for SoC, nominal mode
VDD_SOC	Power supply for SoC logic [1]	0.76	0.80	0.85	V	Power supply for SoC, low drive mode
VDD_SOC	Power supply for SoC logic [1]	0.61	0.65	0.7	V	Power supply for SoC, suspend mode
VDD_ARM	Power supply for Cortex-A55 core [1]	0.95	1.00	1.05	V	Power supply for Cortex-A55, super overdrive mode
VDD_ARM	Power supply for Cortex-A55 core [1]	0.85	0.90	0.955	V	Power supply for Cortex-A55, overdrive mode
VDD_ARM	Power supply for Cortex-A55 core [1]	0.80	0.85	0.905	V	Power supply for Cortex-A55, nominal mode
VDD_ARM	Power supply for Cortex-A55 core [1]	0.76	0.80	0.85	V	Power supply for Cortex-A55, low drive mode
VDD_ARM	Power supply for Cortex-A55 core [1,2]	0	0	0	V	Power supply for Cortex-A55, suspend mode
NVCC_BBSM_1P8	IO supply for GPIO in BBSM bank	1.65	1.8	1.95	V	—
VDD_DDR_0P8	DDR supply for DDR PHY	0.795	0.8375	0.88	V	—
VDD_ETH_0P8	Digital supply for Ethernet PHY	0.795	0.8375	0.88	V	—
VDD_ETH_1P8	I/O voltage supply and analog high voltage power supply	1.71	1.8	1.89	V	—
VDD_ANA_0P8	Digital supply for PLLs, temperature sensor, and LVCMOS I/O	0.795	0.8375	0.88	V	—
VDD_ANA_1P8/ VDD_ANAVDET_ 1P8	1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC,	1.71	1.8	1.89	V	—

Table continues on the next page...

Table 19. Operating ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
	24 MHz XTAL, and supply voltage for voltage detect					
VDD_MIPI_0P8	Digital supply for MIPI PHY	0.795	0.8375	0.88	V	—
VDD_USB_0P8	Digital supply for USB PHYs	0.795	0.8375	0.88	V	—
VDD_USB_1P8	1.8 V supply for USB PHYs	1.71	1.8	1.89	V	—
VDD_USB_3P3	3.3 V supply for USB PHY (Vmax consistent with Vmax supported by NVCC GPIO supplies)	3.069	3.3	3.45	V	—
VDD_PCI_0P8	Digital supply for PCIe PHY	0.795	0.8375	0.88	V	—
VDD_PCI_1P8	1.8 V supply for PCIe PHY	1.71	1.8	1.89	V	—
VDD_LVDS_1P8	1.8 V supply for LVDS	1.71	1.8	1.89	V	—
VDD_MIPI_1P8	1.8 V supply for MIPI PHYs	1.71	1.8	1.89	V	—
VDD_AUD_1P8	1.8 V supply for audio transceiver	1.71	1.8	1.89	V	—
VDD2H_DDR	Voltage supply for LPDDR5/ LPDDR4X PHY, LPDDR5 mode	1.01	1.05	1.12	V	—
VDD2H_DDR	Voltage supply for LPDDR5/ LPDDR4X PHY, LPDDR4X mode	1.06	1.1	1.17	V	—
VDDQ_DDR	Voltage supply for LPDDR5/4X PHY, LPDDR5 Mode, ODT enabled or disabled	0.47	0.5	0.57	V	—
VDDQ_DDR	Voltage supply for LPDDR5/4X PHY, LPDDR4X Mode	0.57	0.6	0.65	V	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 1.8 V mode	1.65	1.8	1.95	V	—
NVCC_AON, NVCC_SD2, NVCC_GPIO, NVCC_WAKEUP, NVCC_CCM_DAP, NVCC_ENET	Power supply for GPIO when it is in 3.3 V mode	3	3.3	3.45	V	—

1. Voltages > Vtyp x 1.05 but < Vmax are only supported if using a PMIC supporting Automatic Voltage Positioning (AVP).
2. When SoC in a low power state, it can save more power when configuring PMIC to turn VDD_ARM off vs having the PMIC continue to supply VDD_ARM and rely on the on-die powergating around the CORTEXAMIX components.

4.1.7 Temperature ranges specifications

Table 20. Temperature ranges specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Tj	Junction temperature—Commercial [1,2]	0	—	95	°C	—
Ta	Ambient temperature—Commercial [1]	0	—	—	°C	—

1. See the application note, i.MX 95 Product Lifetime Usage Estimates for information on product lifetime (power-on hours) for this processor.
2. Tj minimum temperature supported at startup where Tj = Ta.

4.1.8 Maximum frequency of modules

The following table provides the maximum frequency of modules in the i.MX 95 family of processors.

Table 21. Maximum frequency of modules

Symbol	Description	Frequency (Low Drive mode)	Frequency (Nominal Drive mode)	Frequency (Overdrive mode)	Frequency (Super-Overdrive mode)	Unit
Cortex-A55 cores	CORTEXMIX	900	1404	1800	2004	MHz
DynamIQ Shared Unit (DSU)	CORTEXMIX	750	1170	1500	1670	MHz
Cortex-M33 core	AONMIX	166.67	250	333.33	—	MHz
Cortex-M7 core	M7MIX	400	667	800	—	MHz
EdgeLock® Secure Enclave	AONMIX	133.33	200	250	—	MHz
NPU	NPUMIX	500	800	1000	—	MHz
DRAM (LPDDR5/LPDDR4X)	DRAMMIX	3200/1866	4800/2880	6400/4266	—	MT/s
ISP	CAMERAMIX	400	666.67	800	—	MHz
ISI	CAMERAMIX	333.33	500	667	—	MHz
3D GPU	GPUMIX	500	800	1000	—	MHz
Display controller	DISPLAYMIX	400	667	800	—	MHz
VPU	VPUMIX	333.33	500	666.67	—	MHz
JPEG	VPUMIX	250	400	500	—	MHz

4.1.9 Clock source

This section introduces on-chip oscillator and external clock sources.

4.1.9.1 External input clock sources

The i.MX 95 processor is designed to function with quartz crystals to generate the frequencies necessary for operation. 24 MHz for the main clock source and 32.768 kHz for the real time clock. External clock can be injected into RTC_XTALI if the frequency precision and jitter precision are sufficient.

The XTAL input is used to synthesize all of the clocks in the system with the RTC_XTAL input contributing to time keeping and low frequency operations.

Table 22. External input clock sources

Symbol	Description	Min	Typ	Max	Unit	Condition
fckil	RTC_XTALI Oscillator [1]	—	32.768	—	kHz	—

1. External clock source or a crystal with the integrated oscillator amplifier. Recommended nominal frequency is 32.768 kHz.

4.1.9.1.1 Audio external clock frequency

Table 23 shows the maximum frequency of external clock.

Table 23. Audio external clock frequency

Symbol	Description	Frequency (Low drive mode)	Frequency (Nominal mode)	Frequency (Overdrive mode)	Unit
fext_clk	EXT_CLK maximum frequency[1]	133	200	200	MHz

1. Audio EXT_CLK signal muxed on either pin SD2_VSELECT or PDM_BIT_STREAM1.

4.1.9.2 RTC_OSC

The following table shows the external input clock case for the RTC_XTAL oscillator.

Table 24. RTC_OSC

Symbol	Description	Min	Typ	Max	Unit	Condition
f	Frequency	—	32.768	—	kHz	—
VIH	RTC_XTALI	0.9 x NVCC_BBSM_1P8	—	NVCC_BBSM_1P8	V	—
VIL	RTC_XTALI	0	—	0.1 x NVCC_BBSM_1P8	V	—
—	Duty cycle	45	—	55	%	—

For the case where an external clock is desired to be the source of the 32.768 kHz clock, the RTC_XTALI pin may be driven with the RTC_XTALO pin disconnected.

4.1.9.3 24 MHz quartz specification

An external 24 MHz crystal is used in conjunction with the integrated amplifier to form a crystal oscillator that is used as the reference clock for all frequency synthesis on the processor.

Table 25. 24 MHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition
fXTAL	Frequency [1]	—	24	—	MHz	—
CLOAD	Cload	—	12	—	pF	—
DL	Drive level	—	—	100	µW	—
ESR	ESR	—	—	120	Ω	—

1. Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

4.1.9.4 32.768 kHz quartz specification

An external 32.768 kHz oscillator is necessary.

Table 26. 32.768 kHz quartz specification

Symbol	Description	Min	Typ	Max	Unit	Condition
fXTAL	Frequency (crystal mode) [1]	—	32.768	—	kHz	—
CLOAD	Cload	—	12.5	—	pF	—
ESR	ESR	—	—	90	KΩ	—

1. Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

4.1.9.5 Free Running Oscillator (FRO) specifications

The FRO is a trimmable 200 to 400 MHz low power, high accuracy internal oscillator, that can be used as a clock source for some i.MX 95 modules.

Table 27. Free Running Oscillator (FRO) specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
FCLK	Clock Frequency	200	—	400	MHz	Depending upon trim / VDDCORE > 0.7 V
FACC	Frequency Accuracy [1]	—	± 2.0	± 4.0	%	VDDCORE > 0.7 V / FCLK = 400 MHz / Open Loop
TSU	Startup Time	—	50	—	µs	Fast startup disabled

1. Accuracy over temperature at lower frequencies may be worse.

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

Figure 4 illustrates the power-up and power-down sequence of i.MX 95 processors.

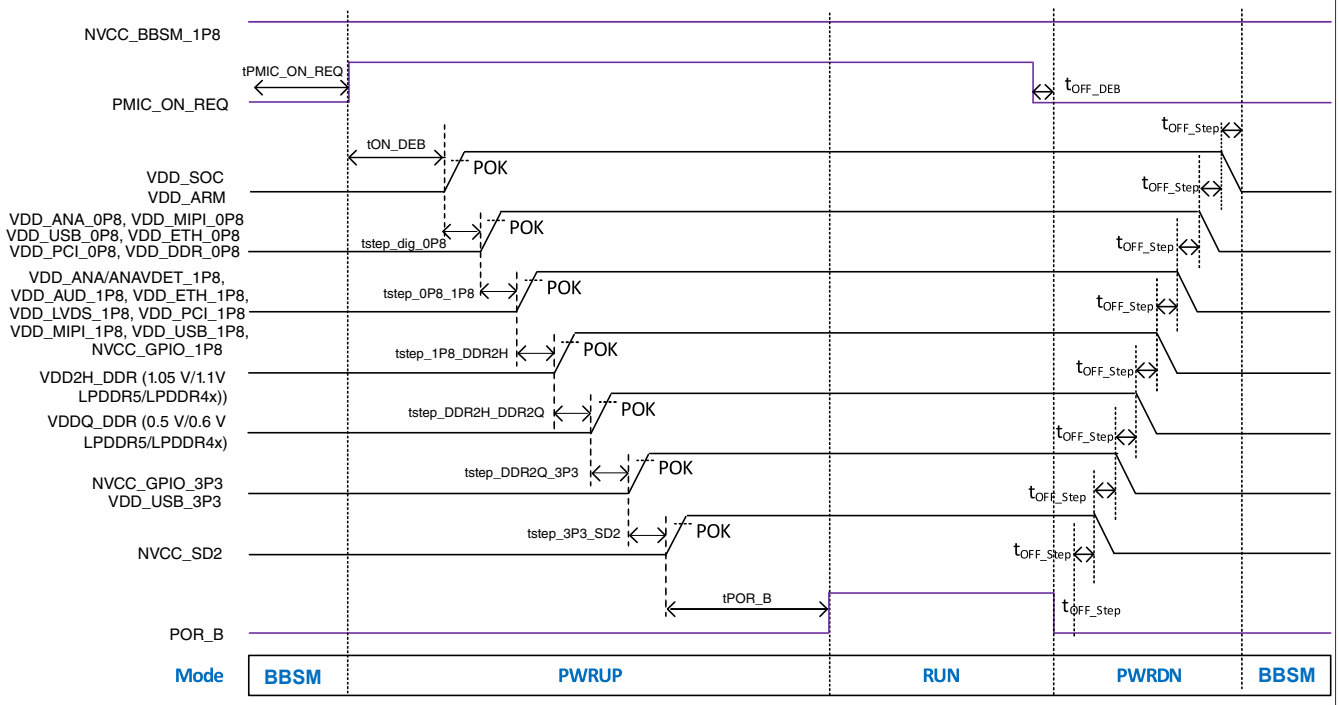


Figure 4. The power sequence of i.MX 95 processors

NOTE

POR_B must be asserted whenever VDD_SOC is powered down, but NVCC_BBSM_1P8 is powered up (when the processor is in BBSM mode).

Power sequencing

1. Turn on NVCC_BBSM_1P8
2. [The SoC asserts PMIC_ON_REQ at this point in time.]
3. Turn on VDD_SOC digital voltage supplies.
4. Turn on VDD_ARM, either together with VDD_SOC or after VDD_SOC is stable.

NOTE

There is no sequence requirement between VDD_ARM and VDD_SOC.

5. Turn on all VDD_*_0P8 analog, DDR, PHY, and PLL supplies.

NOTE

This step may be simultaneous with etither of the VDD_SOC and/or VDD_ARM supplies if desired.

6. Turn on all remaining 1.8 V supplies. This includes VDD_*_1P8 analog, PHY and PLL supplies, and any NVCC_XXX I/O supplies that are being operated at 1.8 V.
7. Turn on DDR VDD2H supply.
8. Turn on DDR VDDQ supply.

NOTE

The i.MX SoC has no VDD2H vs VDDQ sequencing requirements, but generally VDDQ must come up after VDD2H to meet DRAM memory component specification.

9. Turn on any 3.3 V supplies. This includes NVCC_XX I/O supplies that being operated at 3.3 V and VDD_USB_3P3.

NOTE

This 3.3 V supply step may be simultaneous with the DDR VDD2H or DDR VDDQ supplies if desired.

10. Turn on NVCC_SD2, if NVCC_SD2 is being used for a dynamically switchable 1.8/3.3 V SD card voltage (booting initially at 3.3 V).

NOTE

If NVCC_SD2 is operating at a fixed 1.8 V-only or 3.3 V-only voltlage in a give system, then it may power up at the same time as other supplies of the same voltage.

11. POR_B release (it should be asserted during the entire power-up sequence).

4.2.1 Power-up sequence

The power-up sequence is defined as follows:

Table 28. Power-up sequence

Symbol	Description	Min	Typ	Max	Unit	Condition
tPMIC_ON_Req	The time from when NVCC_BBSM_1P8 reaches its minimum operating range to when the SoC begins to assert PMIC_ON_REQ.	0	2	—	ms	—
tON_DEB	The time from when PMIC_ON_REQ reaches its high-level output voltage (VOH) to when VDD_SOC begins to power-up.	0	1	—	ms	—
(not shown in timing diagram)	The time from when VDD_SOC begins to power-up to when VDD_ARM begins to power-up.	0	0.5	—	ms	—
tstep_dig_0p8	The time from when the latter of VDD_SOC or VDD_ARM begins to power-up to when all VDD_*_0P8 analog, PHY and PLL supplies begin to power-up.	0	0.5	—	ms	—
tstep_0p8_1p8	The time from when the final VDD_*_0P8 analog, PHY and PLL supply begins to power-up to when 1.8 V supplies begin to power-up.	0.2	0.25	—	ms	—
tstep_1p8_ddr2h	The time from when the final 1.8V supply begins to power-up to when the DDR VDD2H supply begins to power-up.	0.4	0.5	—	ms	—

Table continues on the next page...

Table 28. Power-up sequence...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tstep_ddr2h_ddrq	The time from when the DDR VDD2H supply begins to power-up to when the DDR VDDQ supply begins to power-up.	0	0.3	—	ms	—
tstep_ddrq_3p3	The time from when the DDR VDDQ supply begins to power-up to when any 3.3 V supply begins to power-up.	0	0.1	—	ms	—
tstep_3p3_sd2	If NVCC_SD2 is being used for a dynamically switchable 1.8/3.3 V SD card voltage (booting initially at 3.3 V), then this represents the time from when the final 3.3 V supply begins to power-up to when NVCC_SD2 begins to power-up.	0	1	—	ms	—
tPOR_B	The time from when all supplies reach their minimum operating range to when POR_B may be released.	0.4	0.5	—	ms	—

4.2.2 Power-down sequence

The power-down sequence is defined as follows:

-Turn off NVCC_BBSM_1P8 last

-Turn off VDD_SOC after the other (non-BBSM) power rails or at the same time as other (non-BBSM) rails.

-No sequence for other power rails during power-down.

4.3 PLL electrical characteristics

Following sections introduce the Fractional-N (FracN) Phase-Locked Loops (PLL) and Low Noise PLL electrical characteristics.

4.3.1 Fracn PLL

Table 29. Fracn PLL

Symbol	Description	Min	Typ	Max	Unit	Condition
TLock	PLL lock time	-	-	100	µS	—
Fout	Output Clock Frequency	9.8M	—	2.5G	Hz	—
FPLL_MOD	SSCG modulation frequency	30	-	64	kHz	at less than 40MHz ref clk
ΔFPLL_MOD	SSCG modulation depth	-4*Fref*pfd	—	—	Hz	Down Spread

4.3.2 Low Noise PLL

Table 30. Low Noise PLL

Symbol	Description	Min	Typ	Max	Unit	Condition
TLock	PLL lock time	—	—	100	µs	—
FPLL_MOD	SSCG modulation frequency	30	—	64	KHz	at Fref_pfd < 40 MHz
ΔFPLL_MOD	SSCG modulation depth	-4*Fref*pfd	—	—	Hz	Down Spread

4.4 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

4.4.1 General purpose I/O (GPIO) DC parameters

The following tables show the DC parameters for GPIO pads. The parameters are guaranteed per the operating ranges table, unless otherwise noted.

Table 31. General purpose I/O (GPIO) DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH (1.8V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DS = 1, IOH = 1.1 mA DS = 6, IOH = 6.6 mA
VOL (1.8 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DS = 1, IOL = 1.1 mA DS = 6, IOL = 6.6 mA
VOH (3.3 V)	High-level output voltage	0.8 x NVCC_xxx	—	NVCC_xxx	V	DS = 1, IOH = 2 mA DS = 6, IOH = 12 mA
VOL (3.3 V)	Low-level output voltage	0	—	0.2 x NVCC_xxx	V	DS = 1, IOL = 2 mA DS = 6, IOL = 12 mA
VIL	Low-level input voltage	0	—	0.3 x NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C
VIH	High-level input voltage	0.7 x NVCC_xxx	—	NVCC_xxx	V	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C
Rpd3.3v	Pull-down resistor	24	43	87	KΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125°C

Table continues on the next page...

Table 31. General purpose I/O (GPIO) DC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Rpu3.3v	Pull-up resistor	18	37	72	KΩ	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125°C
Rpd1.8v	Pull-down resistor	13	23	48	KΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125°C
Rpu1.8v	Pull-up resistor	12	22	49	KΩ	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125°C

Note: For GPIO pads, when the supplies are ramp-up or/and below operating level, the pad state values are undefined.

Note: For PHY pads, the PAD state values are undefined before POR_B is asserted.

4.4.1.1 Additional leakage parameters

Table 32. Additional leakage parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
IIH	Leakage high	-5	—	5	µA	Non-PHY IO, 1.65 V -3.465 V, Temp = -40°C to 125°C | pad = VDDIO
IIL	Leakage low	-5	—	5	µA	Non-PHY IO, 1.65 V to 3.465 V, Temp = -40°C to 125°C | pad = VDDIO

4.4.2 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX95 application processors.

4.4.3 DDR pin I/O leakage DC parameters

Table 33. DDR pin I/O leakage DC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
IOz	I/O leakage current [1,2]	—	—	±180	µA	—

1. Refer to IBIS model for complete IV curve characteristics
2. Output leakage is measured with all outputs disabled, 0 V ≤ Vout ≤ VddQ

4.4.4 LVDS DC electrical characteristics

Table 34. LVDS DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
Vod	Differential Voltage Output Voltage	0.25	—	0.45	V	Rload = 100 Ω
Voh	Output Voltage High	1.25	—	1.6	V	Rload = 100 Ω
Vol	Output Voltage Low	0.9	—	1.25	V	Rload = 100 Ω
Vos	Offset Static Voltage (i.e. Common mode voltage)	1.125	—	1.375	V	Rload = 100 Ω
Vosdiff	VOS (Ripple peak to peak)	—	—	25	mV	Rload = 100 Ω
ISA ISB	Output short-circuited to GND [1]	—	—	4.2	mA	—
ISAB	Output short current [1]	—	—	4.2	mA	—

1. This value is base on test.

4.5 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR5 and LPDDR4X modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

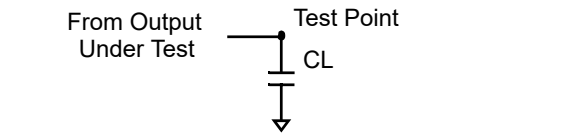


Figure 5. Load circuit for output

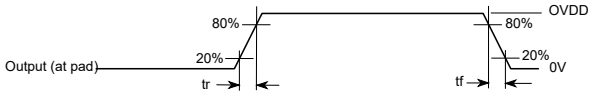


Figure 6. Output transition time waveform

4.5.1 General purpose I/O (GPIO) AC parameters

Table 35. General purpose I/O (GPIO) AC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
tR	TX rise time	3950	—	5950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x1
tF	TX fall time	4140	—	5600	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x1
tR	TX rise time	1890	—	2820	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tF	TX fall time	1790	—	2560	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tR	TX rise time	675	—	1950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x3
tF	TX fall time	584	—	1730	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x3
tR	TX rise time	521	—	1320	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x4
tF	TX fall time	442	—	748	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x4
tR	TX rise time	454	—	742	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x5
tF	TX fall time	380	—	554	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x5
tR	TX rise time	419	—	639	ps	Slew rate FSEL1 = 11b, Fast Slew Rate

Table continues on the next page...

Table 35. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						(1.62 V, 1.8 V, 1.98 V), Drive strength x6
tF	TX fall time	349	—	506	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x6
tR	TX rise time	4030	—	5790	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x1
tF	TX fall time	4410	—	6290	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x1
tR	TX rise time	1870	—	2950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tF	TX fall time	1900	—	3310	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x2
tR	TX rise time	774	—	1930	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x3
tF	TX fall time	719	—	2070	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x3
tR	TX rise time	598	—	1360	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x4
tF	TX fall time	490	—	1590	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x4
tR	TX rise time	543	—	1040	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x5
tF	TX fall time	401	—	1160	ps	Slew rate FSEL1 = 11b, Fast Slew Rate

Table continues on the next page...

Table 35. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						(3 V, 3.3 V, 3.465 V), Drive strength x5
tR	TX rise time	505	—	887	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x6
tF	TX fall time	356	—	747	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x6

4.5.2 DDR I/O AC electrical characteristics

The DDR I/O pads support LPDDR4X/LPDDR5 operational modes. The DDR Memory Controller (DDRMC) is compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX95 application processors.

4.5.3 LVDS AC timing specifications

Table 36. LVDS AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
f	Operating data rate	—	—	1155	Mbps	Rload = 100 Ω Vload = 2 pF Note: This is the maximum work condition of operating data rate.
Tfall	Vod fall time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.
Trise	Vod rise time, 20 - 80%	—	—	0.3	UI (Unit Interval)	Rload = 100 Ω Vload = 2 pF Note: Measurement levels are 20% - 80% from output voltage.
Tskew	Lane skew [1,2]	—	250	—	ps	Rload = 100 Ω, Cload = 2 pF

1. Tskew is the differential time at Vod = 0 voltage between different channel.
2. This value is absolute value and base on test.

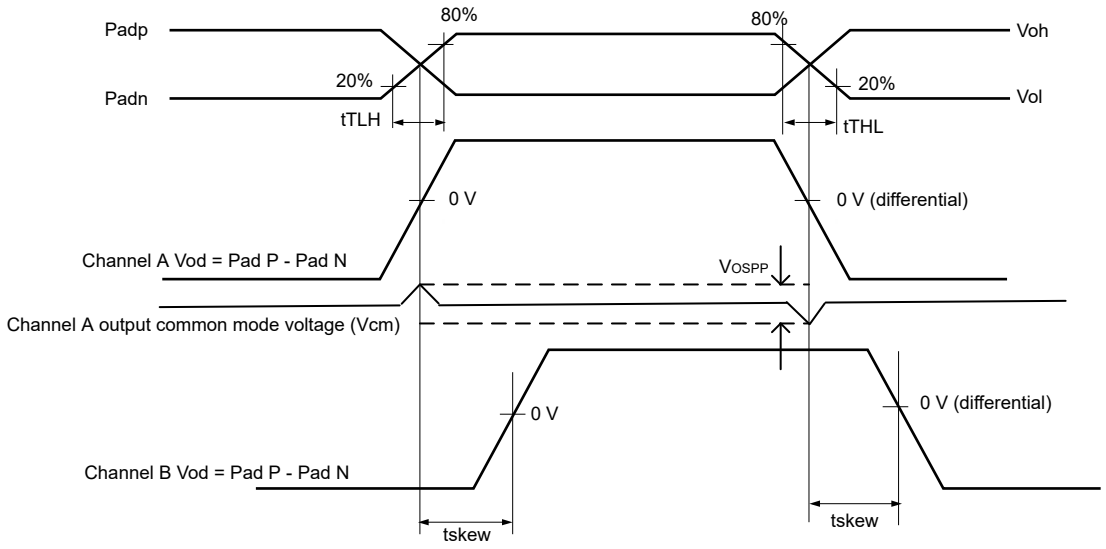


Figure 7. Output transition time waveform

4.6 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See *TIA/EIA STANDARD 644-A, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (2001)* for details.

4.6.1 DDR I/O output buffer impedance

The DDR output driver and ODT impedances are controlled across PVT using ZQ calibration procedure with a 120 Ω ±1% resistor connected to ground. Programmable drive strength and ODT impedance targets available in the NXP DDR tool are detailed in the device's IBIS model. Impedance deviation (calibration accuracy) is about approximately ±10% (maximum/minimum impedance) across PVT.

4.7 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 95 processor.

4.7.1 Reset timings parameters

The following figure shows the reset timing and table lists the timing parameters.

Table 37. Reset timings parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
CC1	Duration of POR_B to be qualified as valid. Note: POR_B rise/fall times must be 5 ns or less.	1	—	—	RTC_XTALI cycle	—

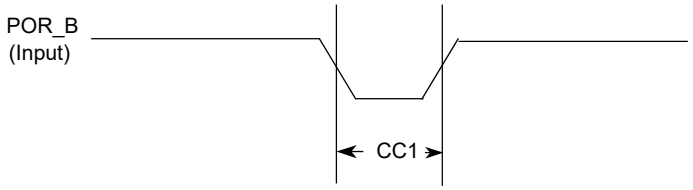


Figure 8. Reset timing diagram

4.7.2 JTAG timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table lists signal parameters.

Table 38. JTAG timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
SJ0	JTAG_TCK frequency of operation [1,2,3,4]	—	—	50	MHz	—
SJ1	JTAG_TCK cycle time in crystal mode [1,2]	20	—	—	ns	—
SJ2	JTAG_TCK clock pulse width measured at VM [1,2,5]	10	—	—	ns	—
SJ3	JTAG_TCK rise and fall times [1,2]	—	—	3	ns	—
SJ4	Boundary scan input data set-up time [1,2]	15	—	—	ns	—
SJ5	Boundary scan input data hold time [1,2]	15	—	—	ns	—
SJ6	JTAG_TCK low to output data valid [1,2]	—	—	600	ns	—
SJ7	JTAG_TCK low to output high impedance [1,2]	—	—	600	ns	—
SJ8	JTAG_TMS, JTAG_TDI data set-up time [1,2]	5	—	—	ns	—
SJ9	JTAG_TMS, JTAG_TDI data hold time [1,2]	5	—	—	ns	—
SJ10	JTAG_TCK low to JTAG_TDO data valid [1,2]	—	—	14	ns	—
SJ11	JTAG_TCK low to JTAG_TDO high impedance [1,2]	—	—	14	ns	—
SJ14	JTAG_TCK low to JTAG_TDO data invalid [1,2]	1	—	—	ns	—

1. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance of the transmission line can be equal to the selected RDSON of the I/O pad output driver.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. 50 MHz frequency is for the JTAG debug interface. For boundary scan, the maximum TCK frequency is 10 MHz.
4. TDC = target frequency of JTAG
5. VM = mid-point voltage

Following figure depicts the JTAG test clock imput timing.

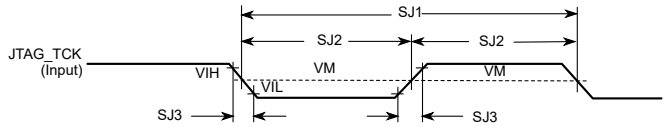


Figure 9. Test Clock Input Timing Diagram

Following figure depicts the JTAG boundary scan timing.

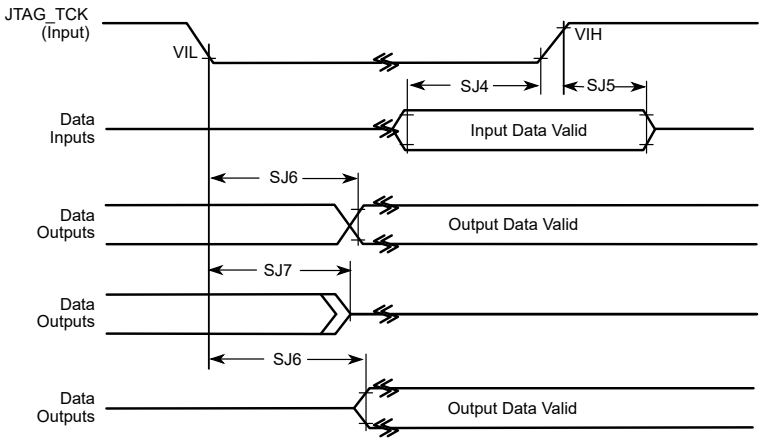


Figure 10. Boundary system (JTAG) timing diagram

Following figure depicts the JTAG test access port.

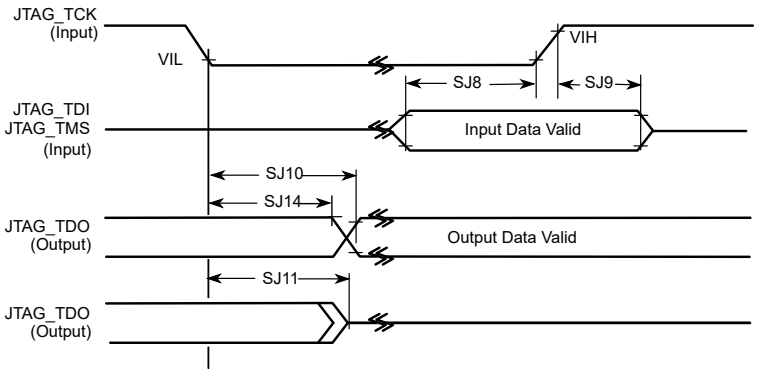


Figure 11. Test Access Port Timing Diagram

4.7.3 SWD timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Following table shows SWD timing.

Table 39. SWD timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
S0	SWD_CLK frequency	—	—	50	MHz	—
S1	SWD_CLK cycle time	20	—	—	ns	—
S2	SWD_CLK pulse width	10	—	—	ns	—
S3	Input data setup time	5	—	—	ns	—
S4	Input data hold time	5	—	—	ns	—
S5	Output data valid time	—	—	14	ns	—
S6	Output high impedance time	—	—	14	ns	—
S7	Output data invalid time	0	—	—	ns	—

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ω , unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line can be equal to the selected RDSON of the I/O pad output.

Following figure depicts the SWD timing.

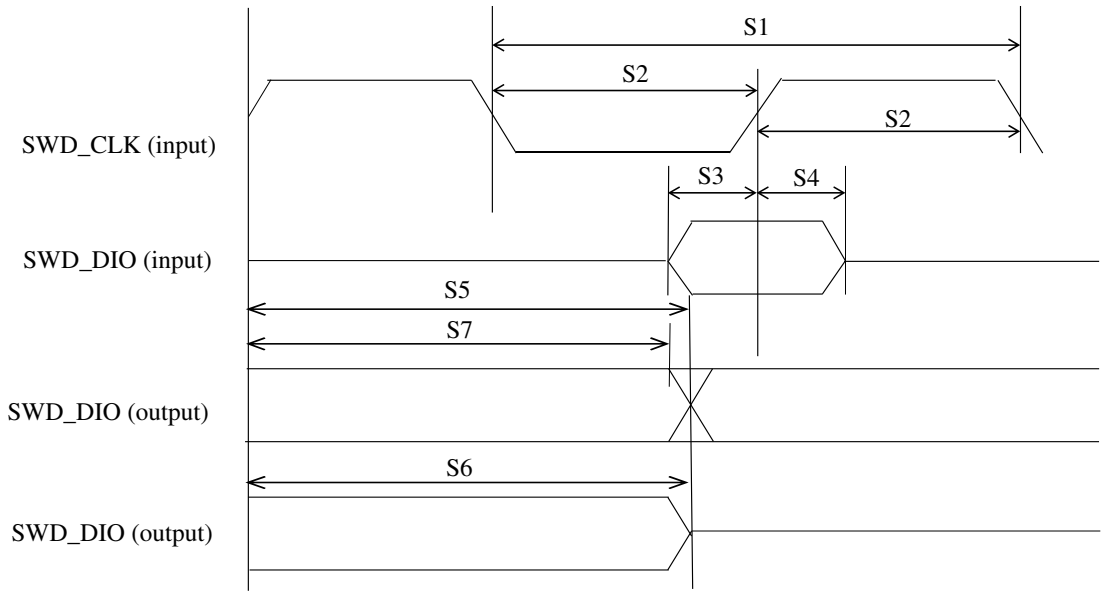


Figure 12. SWD timing

4.7.4 DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

The i.MX95 Family of processors have been designed and tested to work with JEDEC JESD209—compliant LPDDR5/LPDDR4X memory.

JEDEC LPDDR4X Specification JESD209-4C, November 2019

JEDEC LPDDR5 Specification JESD209-5A, January 2020

Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND, and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors:IMX9-PROCESSORS .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 40. DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Number of controllers (LPDDR4X)	—	—	1	—	—
—	Number of controllers (LPDDR5)	—	—	1	—	—
—	Number of channels (LPDDR4X)	—	—	2	—	—
—	Number of Chip Selects (LPDDR4X)	—	—	2	—	—
—	Bus Width	—	—	32	bit	—
—	Maximum Clock Frequency (LPDDR4X)	—	—	4266	MT/s	—
—	Maximum Clock Frequency (LPDDR5)	—	—	6400	MT/s	—

4.7.4.1 Clock/data/command/address pin allocations

These processors use generic names for clock, data, and command address bus (DCF—DRAM controller functions).

4.8 Analog interfaces

This section introduces the timing and electrical parameters about analog interfaces of i.MX 95 processors.

4.8.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

4.8.1.1 SAR ADC

Table 41. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition
VADIN	ADC Input Voltage	VGND	—	VDDA	V	on or off channels
fADCK	ADC Conversion Clock Frequency	20	—	66	MHz	—
Csample	Sample cycles	5.5	—	—	ns	—
Ccompare	Fixed compare cycles	—	58	131.5	ns	—
Cconversion	Clock conversion cycles	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	Cconversion = Csample + Ccompare	number of cycles	—
CAD_INPUT	ADC Input Capacitance	—	—	7	pF	ADC component plus pad capacitance (~2pF)
RAD_INPUT	ADC Input Series Resistance	—	—	1.25	kΩ	—
DNL	ADC Differential Non-linearity	—	±2	—	LSB	after calibration
INL	ADC Integral Non-linearity	—	±6	—	LSB	after calibration
RAS	Analog source resistance	—	—	5	KΩ	—
Bandgap	Output voltage ready time for bandgap	—	1	—	µs	—

4.9 Audio

This section introduces the timing and electrical parameters about audio subsystem of I.MX 95 processor.

4.9.1 SAI switching specifications

This section provides the AC timings for the SAI in Controller (clocks driven) and Target (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR2[BCP] = 0, SAI_RCR2[BCP] = 0) and non inverted frame sync (SAI_TCR4[FSP] = 0, SAI_RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The SAI4 pins muxed with ENET2 and the SAI4 pins muxed with XSPI1 are mutually exclusive. It does not support a use case where some SAI4 pins are connected to ENET2 and other SAI4 pins are simultaneously connected to XSPI1.

SAI5 is supported entirely on SD3 or entirely on XSPI1 (but not multiplexed across both XSPI1 and SD3 pins). SAI5 is also supported with some pins on SD3 and others on XSPI1, as long as the non-data signals (SYNCs and/or BCLKs) are on the one interface (SD3 or XSPI1), and all TX_DATA pins are on the one interface (SD3 or XSPI1), and all RX_DATA pins are on the one interface (SD3 or XSPI1).

SAI2 is supported entirely on ENET pins (at up to maximum supported speeds). However, the SAI2 on XSPI1 pins are limited to no more than 25 MHz – the faster 50 MHz Controller Tx and 66.67 MHz Target Rx modes are supported by the SAI2 only on ENET2 pins.

4.9.1.1 SAI/I2S Controller mode timing (50 MHz)

To achieve 50 MHz for BCLK operation, clock must be set in feedback mode and TCR2[BCI] = 1 must be configured to enable it for the transmitter.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 42. SAI/I2S Controller mode timing (50 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition
S1	SAI_MCLK cycle time	20	—	—	ns	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—
S3	SAI_BCLK cycle time	20	—	—	ns	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	3	—	—	ns	—
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	2	—	—	ns	—

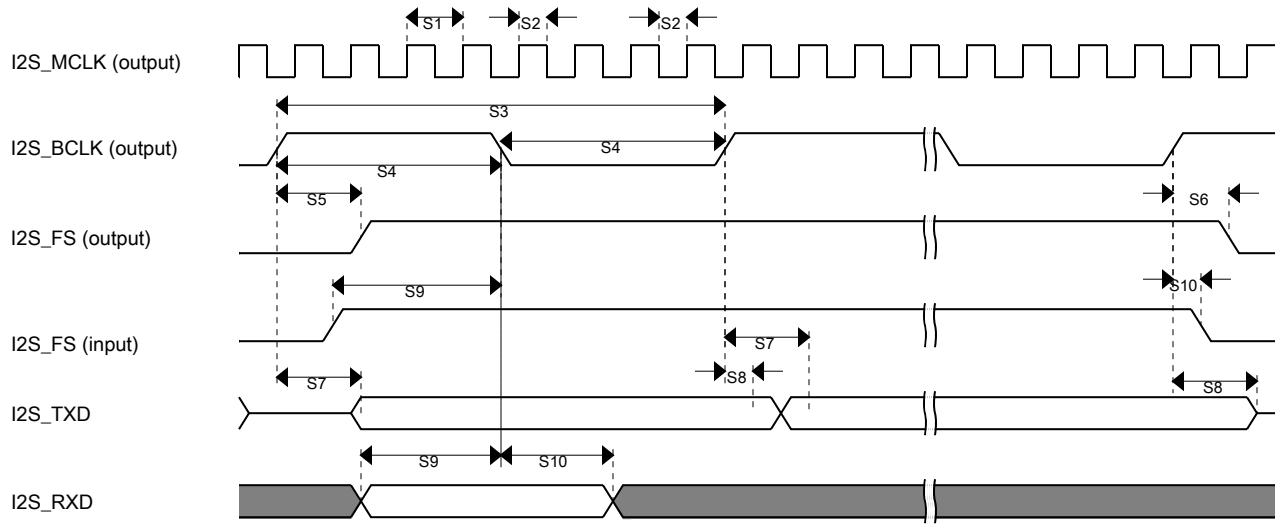


Figure 13. SAI timing-Controller modes

4.9.1.2 SAI/I2S Controller mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 43. SAI/I2S Controller mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition
S1	SAI_MCLK cycle time	40	—	—	ns	—
S2	SAI_MCLK pulse width high/low	40%	—	60%	MCLK period	—
S3	SAI_BCLK cycle time	40	—	—	ns	—
S4	SAI_BCLK pulse width high/low	40%	—	60%	BCLK period	—
S5	SAI_BCLK to SAI_FS output valid	—	—	3	ns	—
S6	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—
S7	SAI_BCLK to SAI_TXD valid	—	—	3	ns	—
S8	SAI_BCLK to SAI_TXD invalid	-2	—	—	ns	—
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK [1]	9.5	—	—	ns	—
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	—	ns	—

1. SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.

4.9.1.3 SAI/I2S Target mode timing (66 MHz)

To support 66 MHz for SAI Rx Target mode (input SAI Rx Clk, input SAI Rx Frame Sync, and input SAI Rx Data) for the following pins:

SAI2.RX_* pins multiplexed over ENET2

SAI5.RX_* pins multiplexed over SD3

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Table 44. SAI/I2S Target mode timing (66 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition
S11	SAI_BCLK cycle time (input)	15	—	—	ns	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—
S14	SAI_FA input hold after SAI_BCLK	2	—	—	ns	—
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—

4.9.1.4 SAI/I2S Target mode timing (25 MHz)

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10-pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 45. SAI/I2S Target mode timing (25 MHz)

Symbol	Description	Min	Typ	Max	Unit	Condition
S11	SAI_BCLK cycle time (input)	40	—	—	ns	—
S12	SAI_BCLK pulse width high/low (input)	40%	—	60%	BCLK period	—
S13	SAI_FS input setup before SAI_BCLK	3	—	—	ns	—
S14	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid [1]	—	—	9.5	ns	—
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	—	ns	—
S17	SAI_RXD setup before SAI_BCLK	3	—	—	ns	—
S18	SAI_RXD hold after SAI_BCLK	2	—	—	ns	—

Table continues on the next page...

Table 45. SAI/I2S Target mode timing (25 MHz)...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
S19	SAI_FS input assertion to SAI_TXD output valid3 [2]	—	—	15	ns	—

1. SAI4 pins multiplexed over ENET2 when operating at 3.3 V I/O supply, this parameter value is 9.75 ns.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear.

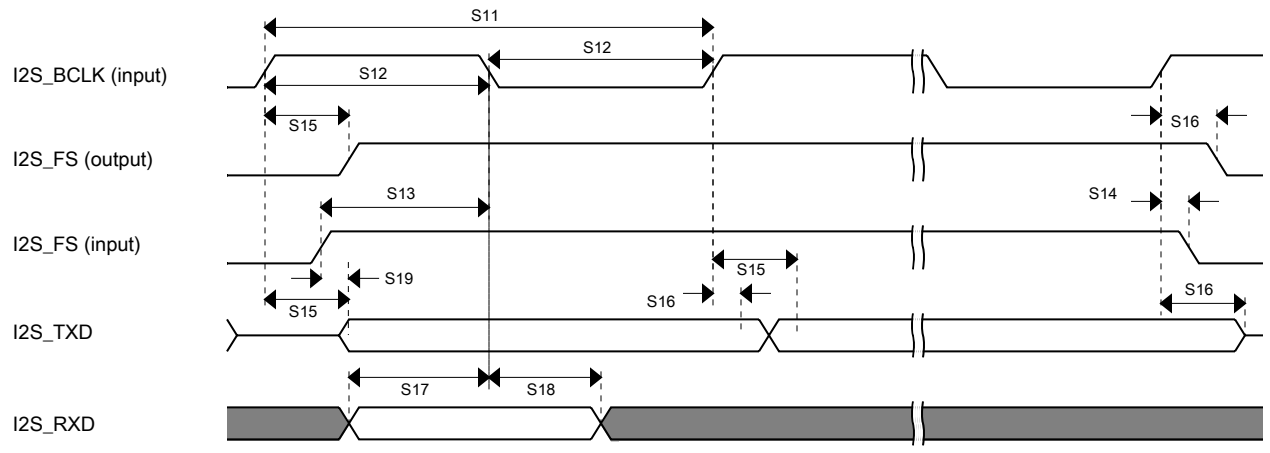


Figure 14. SAI timing-Target mode

4.9.1.5 SAI I/O specifications

Table 46. SAI I/O specifications

Mode	Pins	Clock	Frequency	Output	Input
Controller Tx	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX. Any SAI interface does not multiplex over ENET pins for a SAI instance is not in NETCMIX.	TXC	50 MHz	TXD	—
		TXC	50 MHz	TXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is not in NETCMIX.	TXC	25 MHz	TXD	—
	Any SAI interface does not multiplex over ENET pins for a SAI instance is in NETCMIX.	TXC	25 MHz	TXFS	—
	Any	TXC	25 MHz	—	TXFS
Controller Rx	Any	RXC	25 MHz	—	RXD

Table continues on the next page...

Table 46. SAI I/O specifications...*continued*

Mode	Pins	Clock	Frequency	Output	Input
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI interface multiplexes over ENET pins for a SAI instance is in NETCMIX.	RXC Loopback Mode	50 MHz	—	RXD
	Any SAI interface does not multiplex over ENET pins for a SAI instance is not in NETCMIX.	RXC Loopback Mode	50 MHz	—	RXFS
Target Tx	Any	TXC	25 MHz	TXD	—
		TXC	25 MHz	TXFS	—
		TXC	25 MHz	—	TXFS
Target Rx	SAI2 multiplexes over Ethernet pins, or (for SoCs supporting SAI5 and SD3), SAI5 multiplexes over SD3 pins.	RXC	66.7 MHz	—	RXD
		RXC	66.7 MHz	—	RXFS
		RXC	25 MHz	RXFS	—
	Any SAI instance or pinmux location is not mentioned above.	RXC	25 MHz	—	RXD
		RXC	25 MHz	—	RXFS
		RXC	25 MHz	RXFS	—

4.9.2 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

The following table and figures show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Table 47. SPDIF timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
—	SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns	—
—	Skew	—	—	1.5	ns	SPDIF_OUT output (Load = 50 pf)
—	Transition rising	—	—	24.2	ns	SPDIF_OUT output (Load = 50 pf)
—	Transition falling	—	—	31.3	ns	SPDIF_OUT output (Load = 50 pf)

Table continues on the next page...

Table 47. SPDIF timing parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Skew	—	—	1.5	ns	SPDIF_OUT output (Load = 30 pf)
—	Transition rising	—	—	13.6	ns	SPDIF_OUT output (Load = 30 pf)
—	Transition falling	—	—	18	ns	SPDIF_OUT output (Load = 30 pf)
srckp	Modulating Rx clock (SPDIF_SR_CLK) period	40	—	—	ns	—
srckph	SPDIF_SR_CLK high period	16	—	—	ns	—
srckpl	SPDIF_SR_CLK low period	16	—	—	ns	—
stclkp	Modulating Tx clock (SPDIF_ST_CLK) period	40	—	—	ns	—
stclkph	SPDIF_ST_CLK high period	16	—	—	ns	—
stclkpl	SPDIF_ST_CLK low period	16	—	—	ns	—

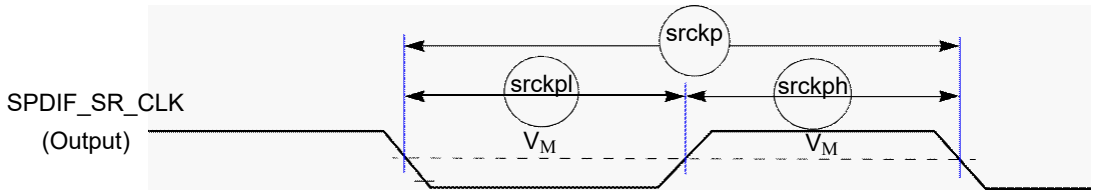


Figure 15. SPDIF_SR_CLK timing diagram

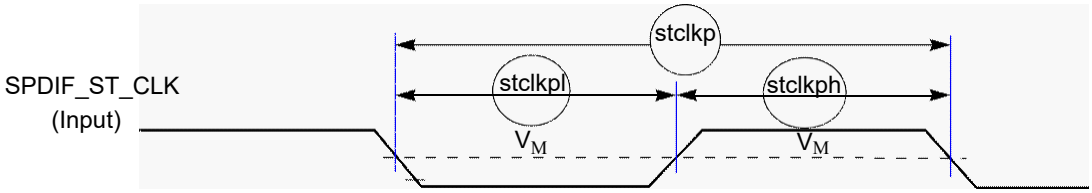


Figure 16. SPDIF_ST_CLK timing diagram

4.9.3 Timer/PDM Microphone interface timing parameters

NOTE

These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIV] = 0), otherwise there are no special timing requirements.

The PDM microphones must meet the setup and hold timing requirements shown in the following table. The "k" factor value in Table 48 depends on the selected quality mode as shown in Table 49.

Table 48. PDM timing parameters

Parameter	Value
trs, tfs	≤ floor (k x CLKDIV) -1 / PDM_CLK_ROOT rate [1]
trh, tfh	≥ 0

1. Depending on K value, user must make sure floor (K x CLKDIV) > 1 to avoid timing problems.

Table 49. K factor value

Quality factor	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

Figure 17 illustrates the timing requirements for the PDM.

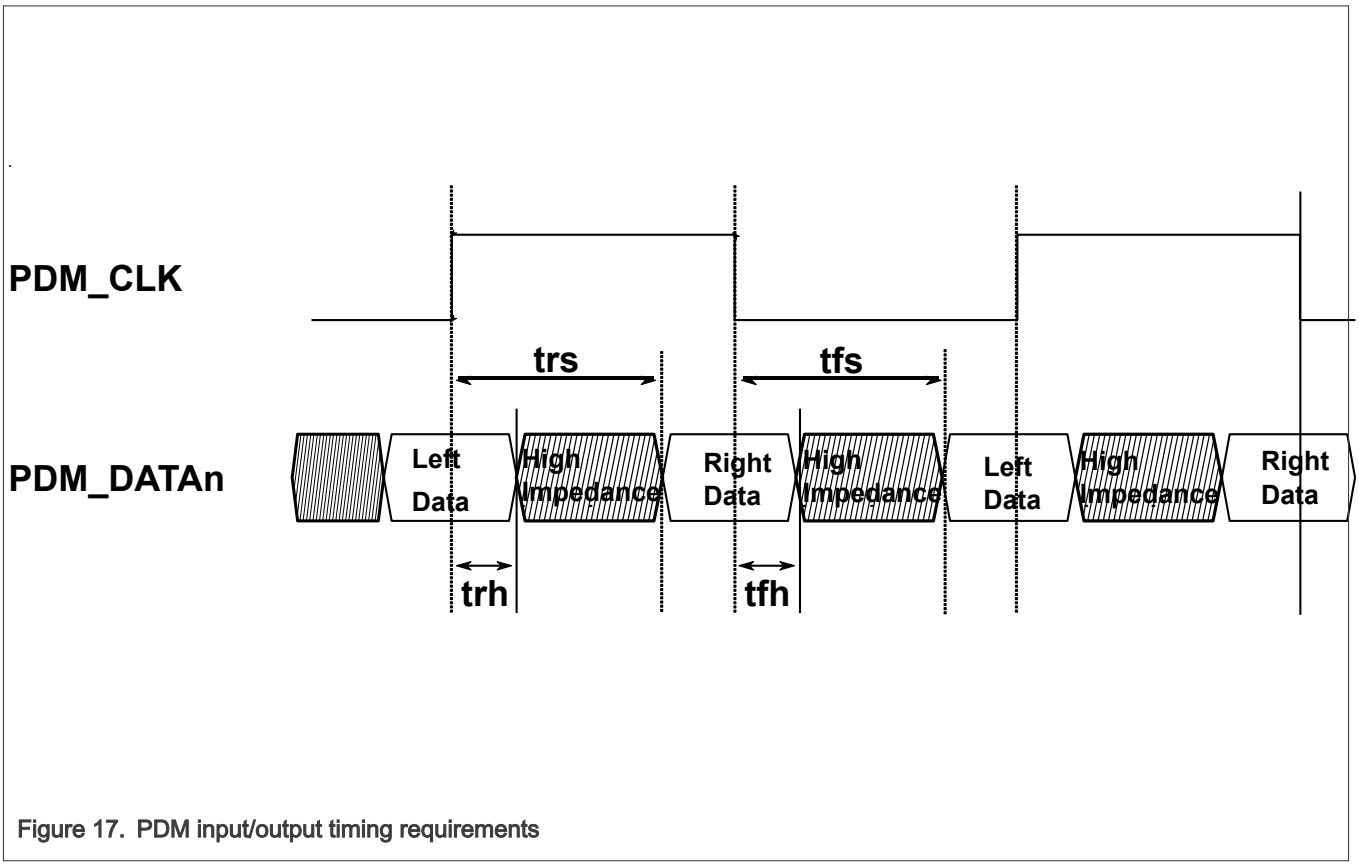


Figure 17. PDM input/output timing requirements

4.9.4 Medium Quality Sound (MQS) electrical specifications

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. Two outputs are asynchronous PWM pulses and their maximum frequency is 1/32 x mclk_frequency.

Table 50. Medium Quality Sound (MQS) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fmclk	Bit clock is used to generate the mclk.	—	24.576	66.5	MHz	—

Frequency of mclk depends on software settings.

See Section, General purpose I/O AC parameters for other electrical specifications.

4.10 Display and graphics

This section introduces the timing and electrical parameters about display and graphic interfaces.

4.10.1 MIPI D-PHY electrical characteristics

The i.MX 95 processors conform to the MIPI CSI-2 and D-PHY standards for protocol and electrical specifications.

Compatible with standards:

- MIPI Alliance Specification for Display Serial Interface Version 1.2 (MIPI DSI controller)
- MIPI Standard 1.2 for D-PHY (MIPI DSI D-PHY)
- Compatible with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 2.1

4.10.1.1 MIPI CSI-2

Table 51. MIPI CSI-2

Symbol	Description	Min	Typ	Max	Unit	Condition
ILEAK	Input pin leakage current	-100	—	100	uA	—
UIINST	HS UI Instantaneous	0.4	—	12.5	ns	—
VIL-LP	Input low voltage	—	—	550	mV	—
VIH-LP	Input high voltage	740	—	—	mV	Data rate > 1.5Gbps
VIH-LP	Input high voltage	880	—	—	mV	Data rate <= 1.5Gbps
VHYST	Input hysteresis	25	—	—	mV	—
VOL	Output low voltage level	-50	—	50	mV	—
VOH	Output high voltage level	1.1	—	1.3	V	Data rate <= 1.5Gbps
VOH	Output high voltage level	0.95	—	1.3	V	Data rate > 1.5Gbps
VIDTH	Differential input high voltage	—	—	70	mV	Data rate <= 1.5Gbps
VIDTH	Differential input high voltage	—	—	40	mV	Data rate > 1.5Gbps
VIDTL	Differential input low voltage	-70	—	—	mV	Data rate <= 1.5Gbps
VIDTL	Differential input low voltage	-40	—	—	mV	Data rate > 1.5Gbps

Table continues on the next page...

Table 51. MIPI CSI-2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VIHHS	Single-ended input high voltage	—	—	460	mV	—
VILHS	Single-ended input low voltage	-40	—	—	mV	—
VCMRX_DC	Input common-mode voltage	70	—	330	mV	—
ZID	Differential input impedance	80	100	125	Ohm	—
VCMTX	HS transmitter static common-mode voltage	150	200	250	mV	(VP-VN)/2; Value when driven into a load impedance in the Zid range.
VOHHS	HS output high voltage	—	—	360	mV	Value when driven into a load impedance in the Zid range.
VOD	HS transmit absolute differential voltage	150	200	250	mV	—
eSPIKE	LP input pulse rejection	—	—	300	V.ps	Time-voltage integration of a voltage spike above VIL in LP-0 state, or below VIH in LP-1 state. Receiver does not change state if maximum pulse specification is met.
TMIN_RX	LP minimum input pulse	20	—	—	ns	Minimum pulse width recognized by the receiver.
VINT	LP peak interference voltage	—	—	200	mV	—
fINT	LP interference frequency	450	—	—	MHz	—
Tflp, Tflp	LP 15%-85% signal rise/fall time	—	—	25	ns	—
tslew	Output slew rate	—	—	150	mV/ns	@CLOAD = 70pF
tslew_fall	Output slew rate (falling edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF
tslew_rise	Output slew rate (rising edge)	25	—	—	mV/ns	@CLOAD = 0pF - 70pF
CLOAD	Output load capacitance	—	—	70	pF	—
TSETUP	Data to clock setup time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps
TSETUP	Data to clock setup time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps
THOLD	Clock to data hold time	0.15	—	—	UIINST	> 0.08Gbps, <= 1Gbps
THOLD	Clock to data hold time	0.2	—	—	UIINST	> 1Gbps, <= 1.5Gbps

Table continues on the next page...

Table 51. MIPI CSI-2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
ΔVCMRX(HF)	HS common mode interference beyond 450 MHz	—	—	50	mV	Data rate > 1.5Gbps
ΔVCMRX(LF)	HS common mode interference between 50MHz and 450 MHz	-25	—	25	mV	Data rate > 1.5Gbps
RATE[RX]	Receive Serial Data Rate [1]	80	—	2500	Mbps	80 Ω ≤ RL ≤ 125 Ω
RATE[TX]	Transmit Serial Data Rate	80	—	2500	Mbps	per lane, 80 Ω ≤ RL ≤ 125 Ω
RATE[TX]	Transmit Serial Data Rate - Tx Reverse Mode	80	—	625	Mbps	per lane, 80 Ω ≤ RL ≤ 125 Ω
TCLKP	HS Clock Period	0.8	—	25	ns	80 Ω ≤ RL ≤ 125 Ω
TSKEW[TX]	Data to clock skew	-0.15	—	0.15	Ulinst	> 0.08Gbps, < 1Gbps
TSKEW[TX]	Data to clock skew	-0.2	—	0.2	Ulinst	> 1Gbps, < 1.5Gbps
TSKEW[TLIS]	Data to clock skew	-0.2	—	0.2	Ulinst	> 0.08Gbps, < 1Gbps
TSKEW[TLIS]	Data to clock skew	-0.1	—	0.1	Ulinst	> 1Gbps, < 1.5Gbps
TSKEW[TX] static	Static data to clock skew (TX)	-0.2	—	0.2	Ulinst	> 1.5Gbps
TSKEW[TLIS] static	Static data to clock skew (channel)	-0.1	—	0.1	Ulinst	> 1.5Gbps
TSKEW[RX] static	Static data to clock skew (RX) tolerance	-0.3	—	0.3	Ulinst	> 1.5Gbps, < 2.5Gbps
TSKEW[TX] dynamic	Dynamic data to clock skew	-0.15	—	0.15	Ulinst	> 1.5Gbps
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	—	—	100	us	> 1.5Gbps
TSKEWCAL initial	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode	2^15	—	—	Ulinst	> 1.5Gbps
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	—	—	10	us	> 1.5Gbps
TSKEWCAL periodic	Time that the transmitter drives the deskew-calibration pattern in the periodic skew-calibration mode	2^15	—	—	Ulinst	> 1.5Gbps
ΔVCMTX(HF)	Common mode variations above 450 MHz	—	—	15	mV(RMS)	—
ΔVCMTX(LF)	Common mode variations between 50MHz - 450 MHz	—	—	25	mV(RMS)	—

Table continues on the next page...

Table 51. MIPI CSI-2...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
trise_fall	20% - 80% rise and fall time	100	—	—	ps	Data rate <= 1.5Gbps
trise_fall	20% - 80% rise and fall time	—	—	0.4	UI	Data rate > 1.5Gbps
trise_fall	20% - 80% rise and fall time	50	—	—	ps	Data rate > 1.5Gbps

1. Maximum total rate for all lanes is 3.2Gbps.

4.11 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC5.1 (single data rate) timing, eMMC5.1/SD3.0 (dual data rate) timing and SDR50/SDR104 AC timing.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.11.1.1 uSDHC SDR electrical specifications

Table 52. uSDHC SDR electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fpp	Clock frequency [1,2]	—	—	400	kHz	Low speed
fpp	Clock frequency [2,3]	—	—	25/50	MHz	SD/SDIO Full Speed/ High Speed
fpp	Clock frequency [2,4]	—	—	25/52	MHz	MMC Full Speed/High Speed
fOD	Clock frequency [2]	100	—	400	kHz	Identification Mode
tWL	Clock low time	7	—	—	ns	—
tWH	Clock high time	7	—	—	ns	—
tTLH	Clock rise time [2]	—	—	3	ns	—
tTHL	Clock fall time [2]	—	—	3	ns	—
tOD	uSDHC output delay [2]	-6.6	—	3.6	ns	uSDHC Output/Card Inputs SD_CMD, SDx_DATAx
tISU	uSDHC Input setup time [5]	2.5	—	—	ns	uSDHC Input/Card Outputs SD_CMD, SDx_DATAx
tIH	uSDHC Input hold time [5,6]	1.5	—	—	ns	uSDHC Input/Card Outputs SD_CMD, SDx_DATAx

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V.
2. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 3.5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).
3. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

4. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
5. Input timing assumes an input signal slew rate of 3ns (20%/80%).
6. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.

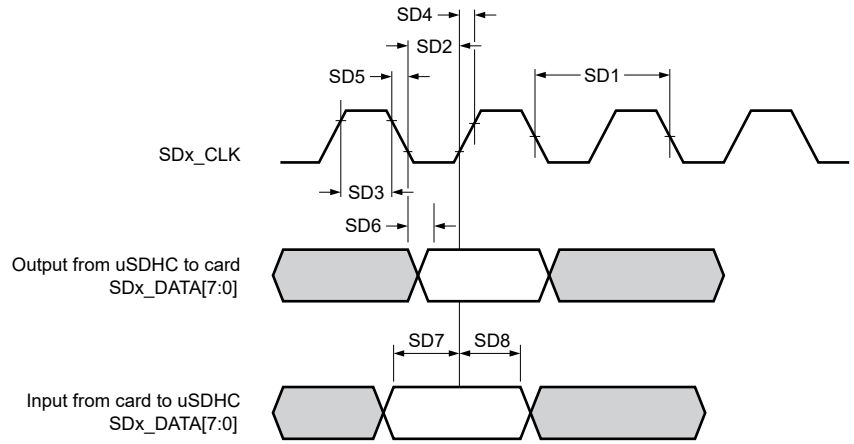


Figure 18. SD/eMMC4.3 High Speed Mode Interface Timing

4.11.1.2 uSDHC Dual Data Rate (DDR) electrical specifications

Table 53. uSDHC Dual Data Rate (DDR) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fpp	Clock frequency (eMMC5.1 DDR) [1]	—	—	52	MHz	—
fpp	Clock frequency (SD3.0 DDR) [1]	—	—	50	MHz	—
tOD	uSDHC output delay (output valid) [1]	2.8	—	6.8	ns	—
tISU	uSDHC Input setup time [2]	2.4	—	—	ns	—
tIH	uSDHC Input hold time [2]	1.5	—	—	ns	—

1. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 3.5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin).
2. Input timing assumes an input signal slew rate of 3ns (20%/80%).

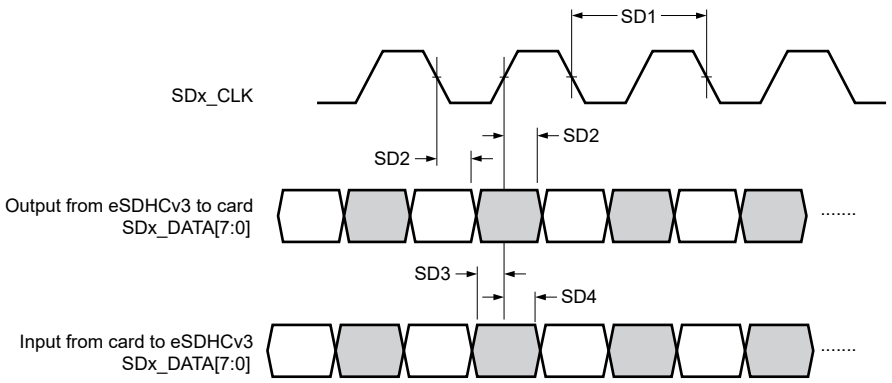


Figure 19. SD/eMMC4.4/4.41 DDR50 Mode Interface Timing

4.11.1.3 uSDHC DDR-HS400

Following table lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

Table 54. uSDHC DDR-HS400

Symbol	Description	Min	Typ	Max	Unit	Condition
fPP	Clock frequency [1]	—	—	200	MHz	Nominal and Overdrive mode
tCL	Clock low time	2.2	—	—	ns	Nominal and Overdrive mode
tCH	Clock high time	2.2	—	—	ns	Nominal and Overdrive mode
tOD1	Output skew from Data of Edge to SCK [1]	0.45	—	—	ns	Nominal and Overdrive mode
tOD2	Output skew from Edge of Data to SCK [1]	0.45	—	—	ns	Nominal and Overdrive mode
tRQ	Input skew [2]	—	—	0.45	ns	Nominal and Overdrive mode
tRQH	Hold skew [2]	—	—	0.45	ns	Nominal and Overdrive mode
fPP	Clock frequency [1]	—	—	133	MHz	Low drive mode
tCL	Clock low time	3.3	—	—	ns	Low drive mode
tCH	Clock high time	3.3	—	—	ns	Low drive mode
tOD1	Output skew from Data of Edge to SCK [1]	0.45	—	—	ns	Low drive mode
tOD2	Output skew from Edge of Data to SCK [1]	0.45	—	—	ns	Low drive mode
tRQ	Input skew [2]	—	—	0.45	ns	Low drive mode
tRQH	Hold skew [2]	—	—	0.45	ns	Low drive mode

1. Output timing valid for maximum external load CL = 15 pF, which is assumed to be an 8 pF load at the end of a 50 Ohm, un-terminated, 2-inch microstrip trace on standard FR4 (1.5 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
2. Input timing assumes an input signal slew rate of 1ns (20%/80%).

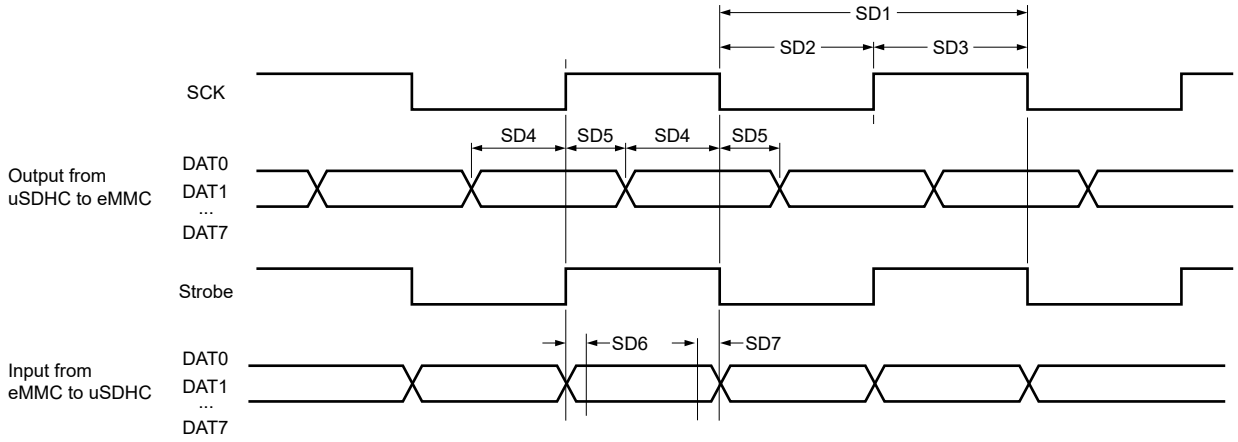


Figure 20. HS400 Mode Interface Timing

4.11.1.4 uSDHC SDR-HS200

Table 55. uSDHC SDR-HS200

Symbol	Description	Min	Typ	Max	Unit	Condition
tCLK	Clock frequency period [1]	5.0	—	—	ns	Nominal and Overdrive mode
tCL	Clock low time	2.2	—	—	ns	Nominal and Overdrive mode
tCH	Clock high time	2.2	—	—	ns	Nominal and Overdrive mode
tOD	uSDHC Output Delay [1]	-1.6	—	1	ns	Nominal and Overdrive mode
tODW	Input data window [2,3]	0.475 x tCLK	—	—	ns	Nominal and Overdrive mode
tCLK	Clock frequency period [1]	7.5	—	—	ns	Low drive mode
tCL	Clock low time	3.3	—	—	ns	Low drive mode
tCH	Clock high time	3.3	—	—	ns	Low drive mode
tOD	uSDHC Output Delay [1]	-1.6	—	1	ns	Low drive mode
tODW	Input data window [2,3]	0.475 x tCLK	—	—	ns	Low drive mode

1. Output timing valid for maximum external load CL = 15 pF, which is assumed to be an 8 pF load at the end of a 50 Ohm, un-terminated, 2-inch microstrip trace on standard FR4 (1.5 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
2. HS200 is for 8 bits while SDR104 is for 4 bits.
3. Input timing assumes an input signal slew rate of 1ns (20%/80%).

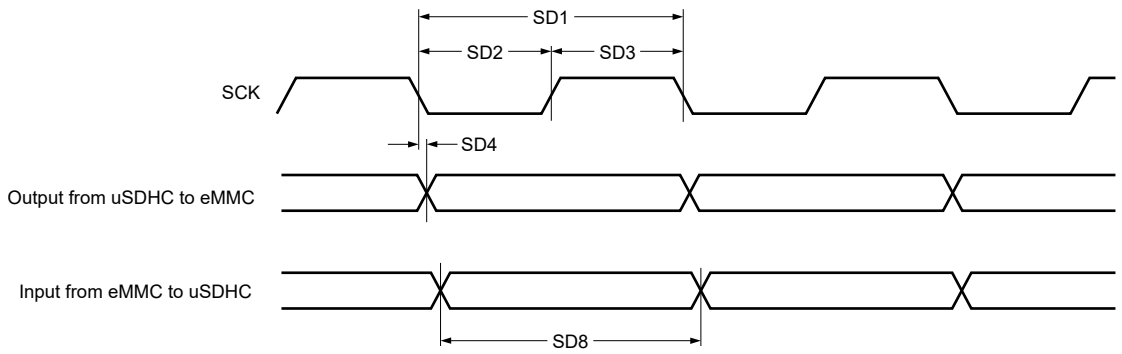


Figure 21. HS200 Mode Interface Timing

4.11.1.5 SDR50/SDR104 AC timing

Table 56. SDR50/SDR104 AC timing

Symbol	Description	Min	Typ	Max	Unit	Condition
tCLK	Clock Frequency Period (Card input clock) [1]	5	—	—	ns	Nominal and Overdrive mode
tCLK	Clock Frequency Period (Card input clock) [1]	7.5	—	—	ns	Low drive mode
tCH	Clock High Time (Card input clock)	2.2	—	—	ns	Nominal and Overdrive mode
tCH	Clock High Time (Card input clock)	3.3	—	—	ns	Low drive mode
tCL	Clock Low Time (Card input clock)	2.2	—	—	ns	Nominal and Overdrive mode
tCL	Clock Low Time (Card input clock)	3.3	—	—	ns	Low drive mode
tOD	uSDHC Output Delay (uSDHC output / card inputs SD_CMD, SDx_DATAx in SDR50) [2]	-3	—	1	ns	Nominal and Overdrive mode
tOD	uSDHC Output Delay (uSDHC output / card inputs SD_CMD, SDx_DATAx in SDR50) [2]	-3	—	1	ns	Low drive mode
tOD	uSDHC Output Delay (uSDHC output / card inputs SD_CMD, SDx_DATAx in SDR104) [2]	-1.6	—	1	ns	Nominal and Overdrive mode
tOD	uSDHC Output Delay (uSDHC output / card inputs SD_CMD, SDx_DATAx in SDR104) [2]	-1.6	—	1	ns	Low drive mode
tODW	uSDHC Input Data Window (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR104) [1,3]	0.5 x tCLK	—	—	ns	Nominal and Overdrive mode

Table continues on the next page...

Table 56. SDR50/SDR104 AC timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tODW	uSDHC Input Data Window (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR104) [1,3]	0.5 x tCLK	—	—	ns	Low drive mode
tISU	uSDHC Input Setup Time (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR50) [1]	2.4	—	—	ns	Nominal and Overdrive mode
tISU	uSDHC Input Setup Time (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR50) [1]	2.4	—	—	ns	Low drive mode
tIH	uSDHC Input Hold Time (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR50) [1]	1.5	—	—	ns	Nominal and Overdrive mode
tIH	uSDHC Input Hold Time (uSDHC input / card outputs SD_CMD, SDx_DATAx in SDR50) [1]	1.5	—	—	ns	Low drive mode

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be 8 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (1.5 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. Data window in SDR100 mode is variable.

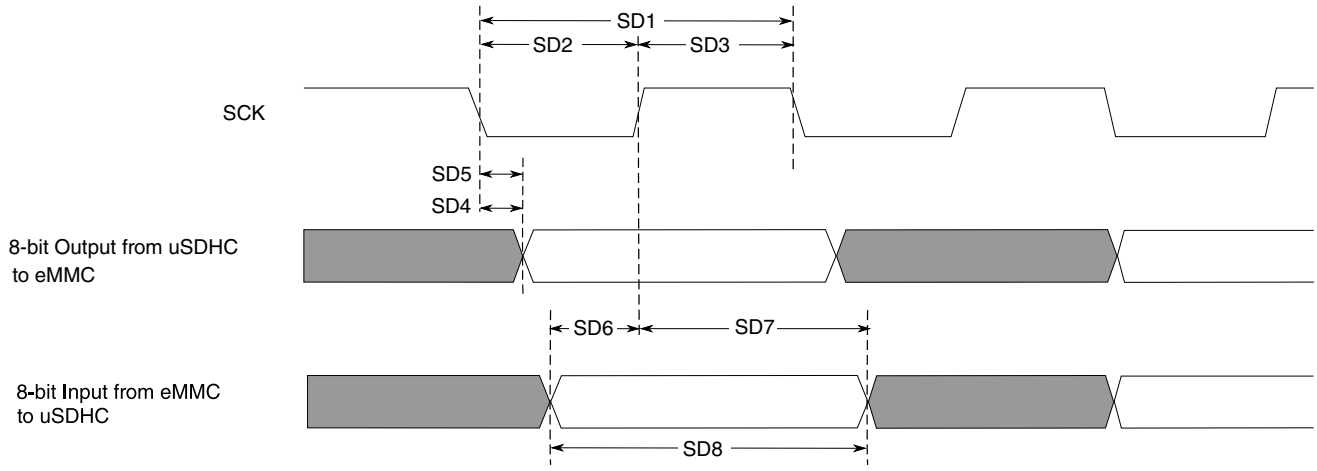


Figure 22. SDR50/SDR104 timing

4.11.1.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for the related I/O power supplies are identical to those shown in GPIO DC parameters table.

4.11.1.7 uSDHC supported modes

For SD:

- All SD 3.0 protocols are supported at full speeds on all three SDHC interfaces. This includes DS, HS, SDR12, SDR25, SDR50, SDR104, and DDR50.
- The maximum supported SDR frequency is 200 MHz which is covered in SDR104 mode, and maximum DDR frequency is 50 MHz as a part of DDR50 mode.

For eMMC:

- eMMC HS400 is only supported on SDHC1 as that is the only one with 8-bit interface.
- eMMC HS200 is supported on all three SDHC interfaces because this protocol supports both 4-bit mode and 8-bit mode, which can work on SDHC2 and SDHC3.
- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are also supported on all three SDHC interfaces.
- The maximum supported SDR frequency is 200 MHz which is covered in HS200 mode, and the maximum DDR frequency is 200 MHz as a part of HS400 mode.

uSDHC3 is multiplexing on GPIO_IO[27:22], below are the modes which are targeted:

- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are supported.
- SDR50 (100 MHz) and SDR104 (200 MHz) modes are NOT supported.
- eMMC HS400 and HS200 modes are NOT supported
- The maximum supported SDR and DDR frequency is 50 and 52 MHz

If I/O is supplied by 3.3 V, the maximum supported SDR/DDR frequency is 50/52 MHz

4.11.2 Ethernet controller (ENET)

Ethernet supports the following key features:

- Support ENET AVB
- Support IEEE 1588
- Support Energy Efficient Ethernet (EEE)
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation
- SGMII (1G and 2.5G), USXGMI, and XFI

The following sections describe the DC and AC electrical characteristics for the EMI, RMII, RGMII, and IEEE standard 1588 interfaces.

4.11.2.1 Ethernet Management Interface (EMI)

This section describes the electrical characteristics for the EMI interface.

4.11.2.1.1 Ethernet management interface AC Timing specifications

This table describes the EMI AC timing specifications

Table 57. Ethernet management interface AC Timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fMDC	Clock frequency [1]	2.5	5	10	MHz	—
tMGCH	MDC clock pulse width high	40	—	60	%	—

Table continues on the next page...

Table 57. Ethernet management interface AC Timing specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tMGCL	MDC clock pulse width low	40	—	40	%	—
tMDKHDX	MDC to MDIO output delay [2,3,4]	Y x tenet_clk - 3	—	Y x tenet_clk + 3	—	NEG=0
tMDKHDX	MDC to MDIO output delay [2,3,4]	Y -tenet_clk	—	Y + tenet_clk	—	NEG=1
tMDDVKH	MDIO to MDC input setup time [5]	8	—	—	ns	—
tMDDXKH	MDIO to MDC input hold time	0	—	—	ns	—
tRGTR	Rise time (20%-80%)	—	—	TBD	ns	—
tRGTF	Fall time (20%-80%)	—	—	TBD	ns	—

1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the MDC clock frequency.
2. For NEG=0: Y = (1+(2+6*EHOLD)*MDIO_HOLD) For NEG=1: Y=MDIO_CLK_DIV even: MDC clk / 2 Y=MDIO_CLK_DIV odd: (MDC clk / 2) +/- tENET_CLK
3. tENET_CLK = 333 Mhz max. How to program ???
4. MDIO timing is configurable by programming the EMDIO_CFG register fields. The default value of Y = 5. Y is the value determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD], and MDIO[EHOLD]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time requirement of Ethernet PHY.
5. The setup time tMDDVKH is measured at a) 470pf load @ 1.8V in open-drain mode b) 300pf load @ 1.8V in push-pull mode

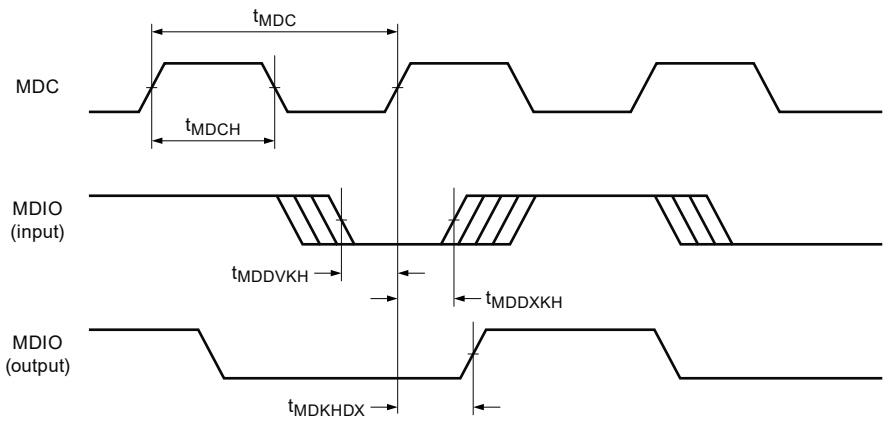


Figure 23. Ethernet management interface timing diagram

4.11.2.1.2 Ethernet management interface DC electrical characteristics at voltage rail =1.8V

This table provides the EMI DC electrical characteristics

Table 58. Ethernet management interface DC electrical characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—

Table continues on the next page...

Table 58. Ethernet management interface DC electrical characteristics at voltage rail =1.8V*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	µA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—

4.11.2.2 RGMII inteface

This section describes the electrical characteristics for the RGMII interface.

4.11.2.2.1 RGMII DC Electrical Characteristics at (voltage rail) ≥ 1.8V

The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11. Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver. RGMII timing specifications are only valid for 1.8 V nominal I/O pad supply voltage. The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver device

Table 59. RGMII DC Electrical Characteristics at (voltage rail) ≥ 1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage [1]	0.7 x SUPPLY	—	—	V	—
VIL	Input low voltage [1]	—	—	0.3 x SUPPLY	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN) [2]	—	—	±50	µA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA) [2]	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA) [2]	—	—	0.2	V	—

1. The min VIL and max VIH values are based on the respective min and max (supply) values found in Recommended Operating Conditions.
2. The symbol (supply) represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4.11.2.2.2 RGMII AC Timing Specifications

Table 60. RGMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
tSKRGTTX	Data to clock output skew (at transmitter) [1]	-500	0	500	ps	—
tSKRGTRX	Data to clock input skew (at receiver) [2]	1	—	2.6	ns	—
tRGT	Clock period duration [3]	7.2	8	8.8	ns	—
tRGTHtRGT	Duty cycle for 10BASE-T and 100BASE-TX [3,4]	40	50	60	%	—
tRGTHtRGTgig	Duty cycle for Gigabit	45	60	55	%	—
tRGTR-HP	Rise time (20%-80%) SUPPLY = 1.8V [5,6]	—	—	0.75	ns	—
tRGTR-OpenAlliance	Rise time (20%-80%) SUPPLY = 1.8V [5,6]	—	—	1	ns	—
tRGTF-HP	Fall time (20%-80%) SUPPLY = 1.8V [5,6]	—	—	0.75	ns	—
tRGTF-OpenAlliance	Fall time (20%-80%) SUPPLY = 1.8V [5,6]	—	—	1	ns	—

1. The frequency of RGMII input clk should not exceed the frequency of RGMII output clk by more than 300 ppm.
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, tRGT scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.
5. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
6. Applies to inputs and outputs.

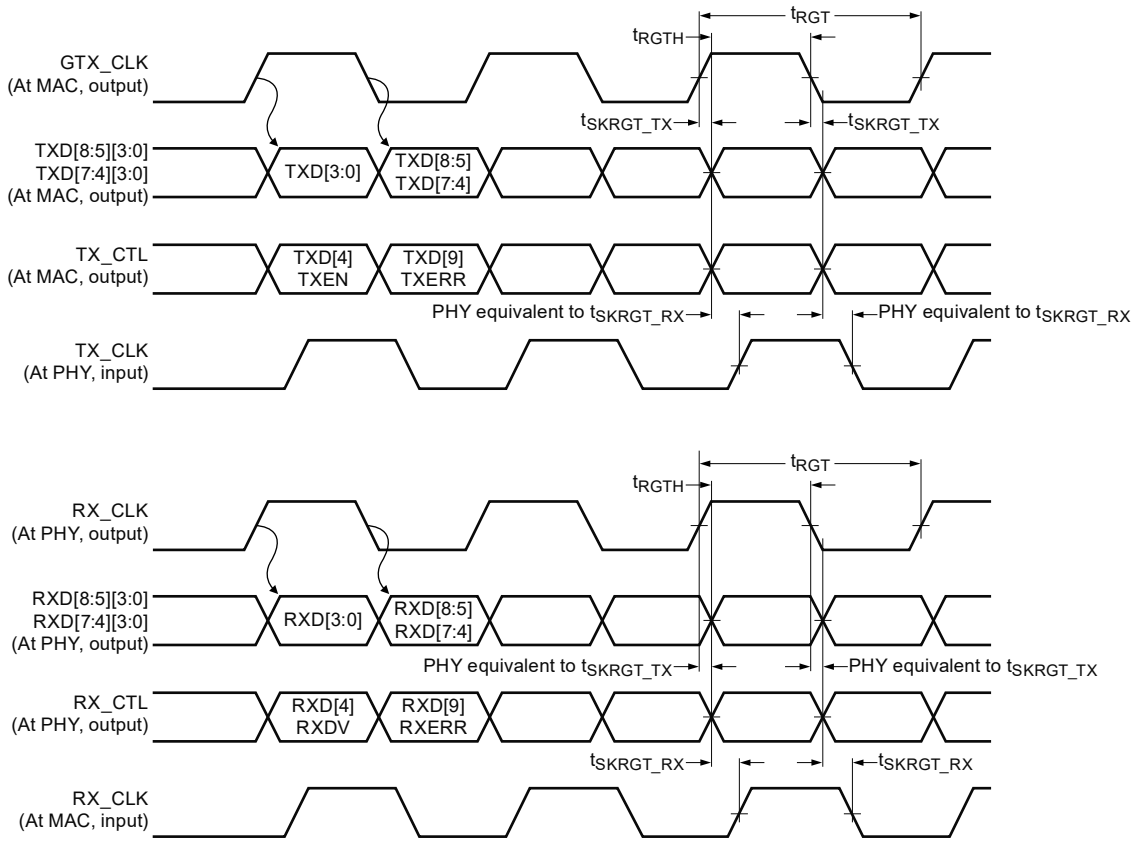


Figure 24. RGMII AC timing and Multiplexing diagram

4.11.2.3 RMII interface

This section describes the electrical characteristics for the RMII interface.

4.11.2.3.1 RMII DC Electrical Characteristics at voltage rail = 3.3V

Table 61. RMII DC Electrical Characteristics at voltage rail = 3.3V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	2	—	—	V	—
VIL	Input low voltage	—	—	0.8	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±5	μA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—

4.11.2.3.2 RMII DC Electrical Characteristics at voltage rail =1.8V

Table 62. RMII DC Electrical Characteristics at voltage rail =1.8V

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	0.7 x SUPPLY	—	—	V	—
VIL	Input low voltage	—	—	0.3 x SUPPLY	V	—
IIN	Input current (VIN=0 or VIN = SUPPLY_IN)	—	—	±50	µA	—
VOH	Output high voltage (SUPPLY = min, IOH = -0.1 mA)	SUPPLY - 0.2	—	—	V	—
VOL	Output low voltage (SUPPLY = min, IOL = 0.1 mA)	—	—	0.2	V	—

4.11.2.3.3 RMII AC Timing Specifications

Table 63. RMII AC Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
tRMT	TX Clock period duration	15	20	25	ns	—
tRMTH	TX Clock Duty cycle for 10BASE-T and 100BASE-TX	35	50	65	%	—
tRMTR	TX Rise time (20%-80%)	1	—	5	ns	—
tRGTF	TX Fall time (20%-80%)	1	—	5	ns	—
tRMTJ	TX Clock peak-to-peak jitter	—	—	250	ps	—
tRMTDX	TX Clock to Data/TX_EN Delay	2	—	14	ns	—
tRMRDV	RXD/CRS_DV/RXER to Clock rising edge, setup time	4	—	—	ns	—
tRMRDX	Clock rising edge to RXD/ CRS_DV/RXER, hold time	2	—	—	ns	—

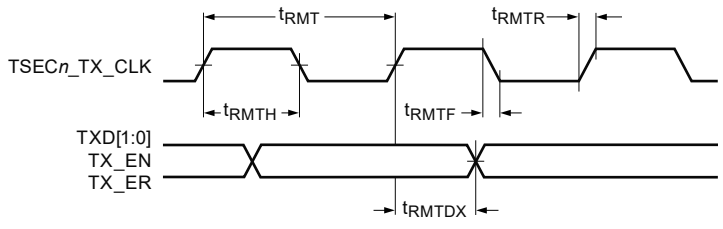


Figure 25. RMII Transmit AC timing diagram

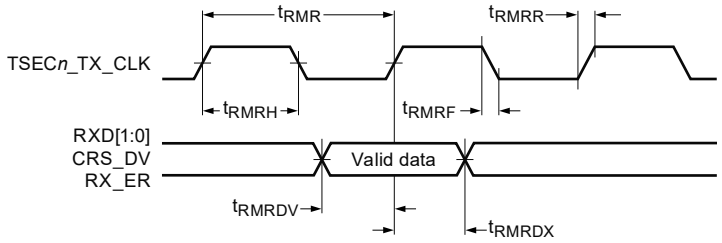


Figure 26. RMII Receive AC timing diagram

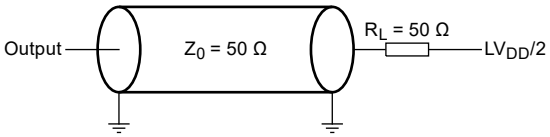


Figure 27. eTSEC AC Test Load

4.11.2.4 NETC 1588 interface

The following table describes the Ethernet 1588 electrical characteristics.

Table 64. NETC 1588 interface

Symbol	Description	Min	Typ	Max	Unit	Condition
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKH/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	2 x t1588CLK	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11

Table continues on the next page...

Table 64. NETC 1588 interface...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tT1588OV	TMR_1588_CLK_OUT to TMR_1588_PULSE_OUT1/2,TMR_1588_ALARM_OUT1/2 valid	0.5	—	4.0	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11
tT1588TRIGH	TMR_1588_TRIG_IN1/2 pulse width	2 x t1588CLK	—	—	ns	CLOAD = 25 pF; DSE[5:0] = 001111 and FSEL1[1:0] = 11

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (1.5 pF/inch). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

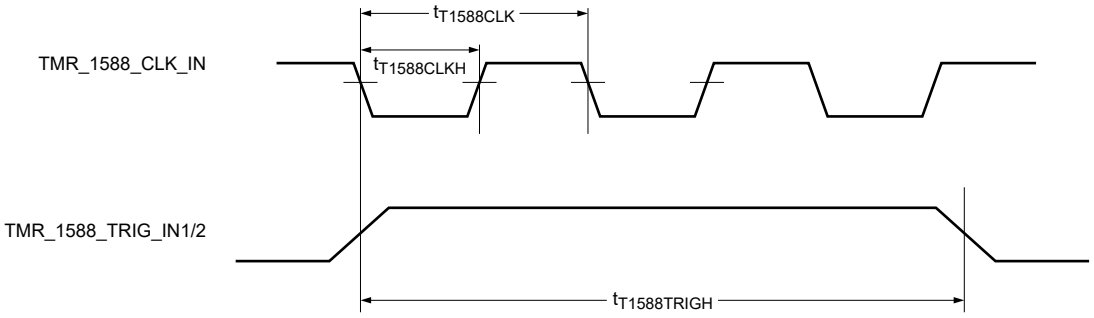
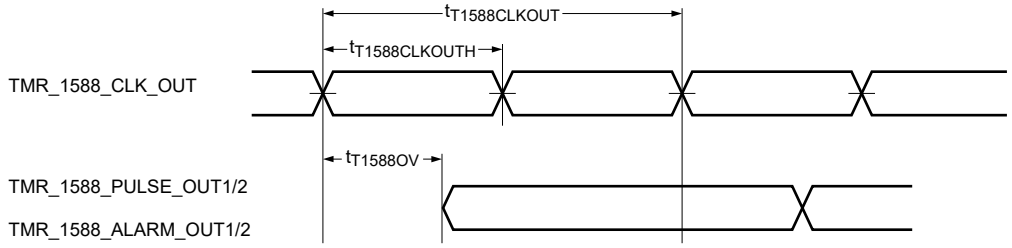


Figure 28. IEEE 1588 input AC timing



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 29. IEEE 1588 output AC timing

4.11.2.5 Ethernet SGMII

This section describes the electrical characteristics for the SGMII interface.

4.11.2.5.1 SGMII 1G and 2.5G differential transmitter output AC timing characteristics

Table 65. SGMII 1G and 2.5G differential transmitter output AC timing characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval for 1G (3.125 Gbps bit rate)	—	320	—	UI	—

Table continues on the next page...

Table 65. SGMII 1G and 2.5G differential transmitter output AC timing characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval for 1G (1.25 Gbps bit rate)	—	800	—	UI	—
Trise	Transmit Vod rise time (20-80%)	100	—	200	ps	—
Tfall	Transmit Vod fall time (20-80%)	100	—	200	ps	—
Dj	Transmit Deterministic Jitter	—	—	0.17	UI	—
—	Transmit Total Jitter	—	—	0.35	UI	—

4.11.2.5.2 SGMII 1G and 2.5G differential transmitter output DC electrical characteristics

Table 66. SGMII 1G and 2.5G differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VOD	Transmit Output Differential Voltage	1000	—	1400	mV	—
Voh	Output voltage high	—	—	1525	mv	—
Vol	Output voltage low	875	—	—	—	—
Vos	Output offset voltage	1075	—	1325	mV	—
RDOUT	Transmit Differential Output Impedance	80	—	100	Ω	Rload = 100 Ω ±1%
Δ|Vod|	Change in Vod between “0” and “1”	—	—	25	mV	—
ΔVos	Change in Vos between “0” and “1”	—	—	25	mV	—
Is	Output current on Short to GND	—	—	40	mA	—

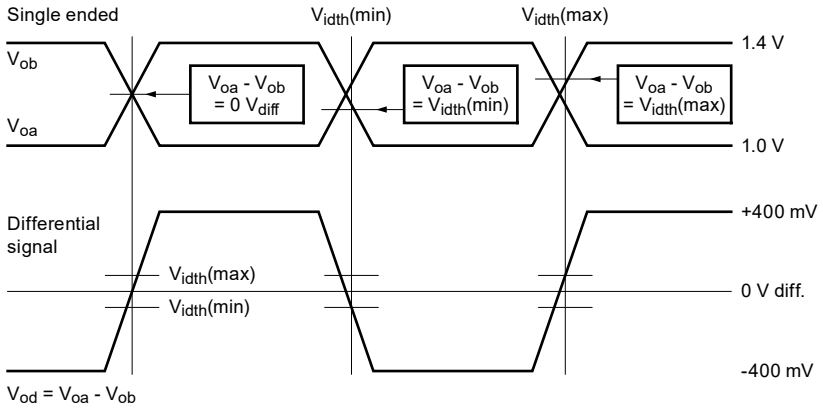


Figure 30. Maximum driver signal levels shown for 1.2 Vos

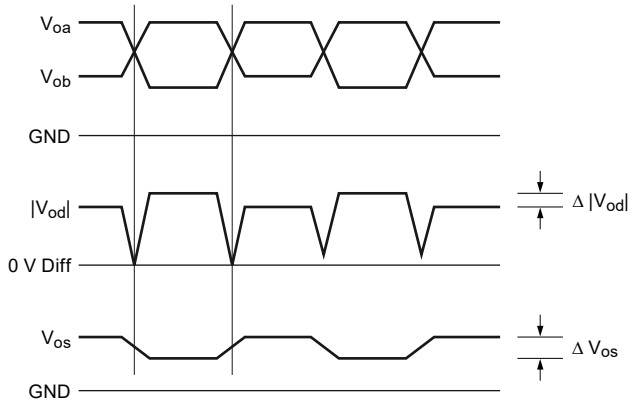


Figure 31. Driver signal levels

4.11.2.5.3 SGMII 1G and 2.5G differential receiver input AC timing characteristics

Table 67. SGMII 1G and 2.5G differential receiver input AC timing characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval for 1G (3.125 Gbps bit rate)	—	320	—	UI	—
UI	Unit Interval for 1G (1.25 Gbps bit rate)	—	800	—	UI	—
Sjt	Receiver deterministic jitter tolerance with sinusoidal noise	—	0.37	UI	—	—
DRjt	Receiver combined random and deterministic jitter tolerance with sinusoidal noise	—	0.55	UI	—	—
Tjt	Receiver total jitter tolerance	—	0.65	UI	—	—
BER	Bit Error Rate	—	10^12	—	—	—

4.11.2.5.4 SGMII 1G and 2.5G differential receiver input DC electrical characteristics

Table 68. SGMII 1G and 2.5G differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
Vin	Input Voltage range	-400	—	400	mV	—
Vidth	Input differential threshold	-50	—	50	mV	—
Rin	Receiver differential input impedance	80	—	120	Ω	—

4.11.2.6 USXGMII interface

This section describes the electrical characteristics for the USXGMII interface.

4.11.2.6.1 USXGMII differential transmitter output DC electrical characteristics

Table 69. USXGMII differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
TX_Diff_PP	Differential peak-to-peak output voltage	—	—	1200	mV	—
TX_DIFF_PP_OFF	Differential peak-to-peak output voltage with TX disabled	—	—	30	mV	—
VCM	Common-mode voltage limits	0	—	1.9	V	—
—	Common-mode voltage deviation during LPI	—	—	150	mV	—
RLDIFF	Differential output return loss (min.)	9	—	—	dB	50 MHz - 2500 MHz
RLDIFF	Differential output return loss (min.)	9 - 12 * log (f/ 2500M)	—	—	dB	2500 MHz - 7500 MHz
RLCM	Common-mode output return loss (min.)	6	—	—	dB	50 MHz - 2500 MHz
RLCM	Common-mode output return loss (min.)	6 - 12 * log (f/ 2500M)	—	—	dB	2500 MHz - 7500 MHz

4.11.2.6.2 USXGMII differential receiver input DC electrical characteristics

Table 70. USXGMII differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
BER	Bit error ratio	—	10e-12	—	—	—
RX_Diff_PP	Differential input peak-to-peak amplitude	—	—	1200	mV	—
—	Receiver coupling	—	—	100	nF	—
SDD11	Differential input return loss	9	—	—	dB	50 MHz - 2500 MHz
SDD11	Differential input return loss	9 - 12 * log (f/ 2500M)	—	—	dB	2500 MHz - 7500 MHz
—	Amplitude of broadband noise (interference tolerance) [1]	5.2/12	—	—	mV	Channel Loss 15 dB

1. This parameter is tested with PRBS31 test pattern.

4.11.2.6.3 USXGMII differential transmitter output AC timing specifications

Table 71. USXGMII differential transmitter output AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Signal speed	10.3125 - 10%	—	10.3125 +10%	GBd	—
Tr/Tf	Transition time (20%–80%)	24	—	47	ps	—
RJ	Random jitter [1]	—	—	0.15	UI	—
DJ	Deterministic jitter	—	—	0.15	UI	—
DCD	Duty Cycle Distortion [2]	—	—	0.035	UI	—
TJ	Total jitter	—	—	0.28	UI	—

1. Jitter is specified at BER 10-12.
2. Duty Cycle Distortion is considered part of the deterministic jitter distribution.

4.11.2.6.4 USXGMII differential receiver input AC timing specifications

Table 72. USXGMII differential receiver input AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Signal speed	10.3125 - 100 ppm	—	10.3125 +100 ppm	GBd	—
Tr/Tf	Transition time (20%–80%)	—	—	47	ps	—
SJ	Sinusoidal jitter (peak-to-peak)	—	—	0.115	UI	—
RJ	Random jitter (peak-to-peak)	—	—	0.13	UI	—
DCD	Duty cycle distortion (peak-to-peak)	—	—	0.035	UI	—

4.11.2.7 XFI

4.11.2.7.1 XFI differential transmitter output DC electrical characteristics

Table 73. XFI differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
Zd	Reference differential impedance	—	100	—	Ω	—
Vcm	DC Common Mode Voltage	0	—	3.6	V	—
Vcmac	Output AC Common Mode Voltage	—	—	15	mV (RMS)	—
SDD22	Differential Output Return Loss	20	—	—	dB	For frequency range from 0.05 to 0.1 GHz
SDD22	Differential Output Return Loss	10	—	—	dB	For frequency range from 0.1 to 7.5 GHz

Table continues on the next page...

Table 73. XFI differential transmitter output DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
SDD22	Differential Output Return Loss	10-16.6 x log(f/7.5)	—	—	dB	For frequency range from 7.5 to 15 GHz
SCC22	Common mode output return loss [1]	6	—	—	dB	For frequency range from 0.05 to 15 GHz
Y1	Eye Mask [2]	180	—	—	mV	—
Y2	Eye Mask [2]	—	—	385	mV	—
Rd	Differential resistance	80	100	120	Ω	—
T_Vdiff	Output differential voltage	360	—	770	mV	—

1. Common mode reference impedance is 25 Ω. Common Mode Return Loss helps absorb reflections and noise for EMI.
2. See Figure, XFI SerDes Transmitter differential output

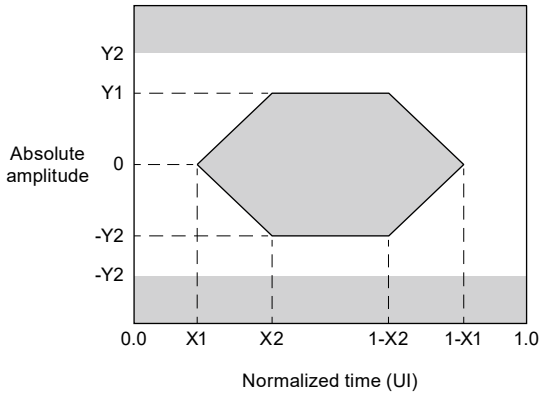


Figure 32. XFI SerDes Transmitter differential output

4.11.2.7.2 XFI differential transmitter output AC timing specifications

Table 74. XFI differential transmitter output AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
T_BAUD	TX baud rate	10.3115	10.3125	10.3135	Gb/s	—
UI	Unit Interval	—	96.96	—	ps	—
Dj	Deterministic Jitter	—	—	0.15	UI	—
Tj	Total Jitter	—	—	0.3	UI	—
Tr/Tf	Rise/fall time (20%–80%)	24	—	—	ps	—
X1	Eye Mask [1]	—	—	0.15	UI	—
X2	Eye Mask [1]	—	—	0.4	UI	—

1. See Figure, XFI SerDes Transmitter differential output

4.11.2.7.3 XFI differential receiver input DC electrical characteristics

Table 75. XFI differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
R_Vdiff	Input differential voltage	110	—	1050	mV	—
R_Rd	Differential Resistance	80	100	120	Ω	—
SDD11	Differential Input Return Loss	20	—	—	dB	For frequency range from 0.05 to 0.1 GHz
SDD11	Differential Input Return Loss	10	—	—	dB	For frequency range from 0.1 to 7.5 GHz
SDD11	Differential Input Return Loss	9 - 12 x log (f / 2500 M)	—	—	dB	For frequency range from 2.5 to 7.5 GHz
SDD11	Differential Input Return Loss	10-16.6*log(f/7.5)	—	—	dB	For frequency range from 7.5 to 15 GHz
SCC11	Common Mode Input Return Loss [1]	6	—	—	dB	For frequency range from 0.1 to 15 GHz
SCD11	Differential to Common Mode Input Conversion [1]	12	—	—	dB	For frequency range from 0.1 to 15 GHz
Y1	Eye Mask [2]	55	—	—	mV	—
Y2	Eye Mask [2]	—	—	525	mV	—
Zd	Reference Differential Impedance	—	100	—	Ω	—
—	AC Common Mode Voltage	—	—	25	mV (RMS)	—

1. Common mode reference impedance is 25 Ω. SCD11 relates to conversion of differential to common mode and the associated generation of EMI.
2. See Figure, XFI SerDes Receiver differential input compliance mask

Out of 525 mV, 100 mV is allocated for multiple reflection.

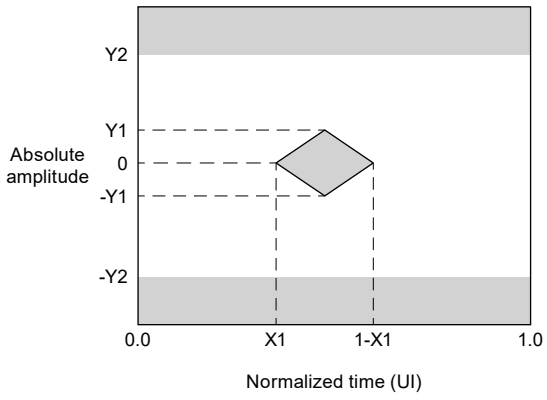


Figure 33. XFI SerDes Receiver differential input compliance mask

4.11.2.7.4 XFI differential receiver input AC timing specifications

Table 76. XFI differential receiver input AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Tj	Total jitter [1,2]	—	—	0.65	UI (p-p)	—
Non-EQJ	Total non-EQJ jitter [2]	—	—	0.45	UI (p-p)	—
X1	Eye Mask [3,4]	—	—	0.325	UI	—

1. The XFI channel has a loss budget of 9.6 dB at 5.5 GHz. The channel loss including connector at 5.5 GHz is 6 dB. The channel crosstalk and reflection margin is 3.6 dB.
2. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.
3. Mask coordinate X1 = 0.225 if total non-EQJ jitter is measured.
4. See Figure, XFI SerDes Receiver differential input compliance mask

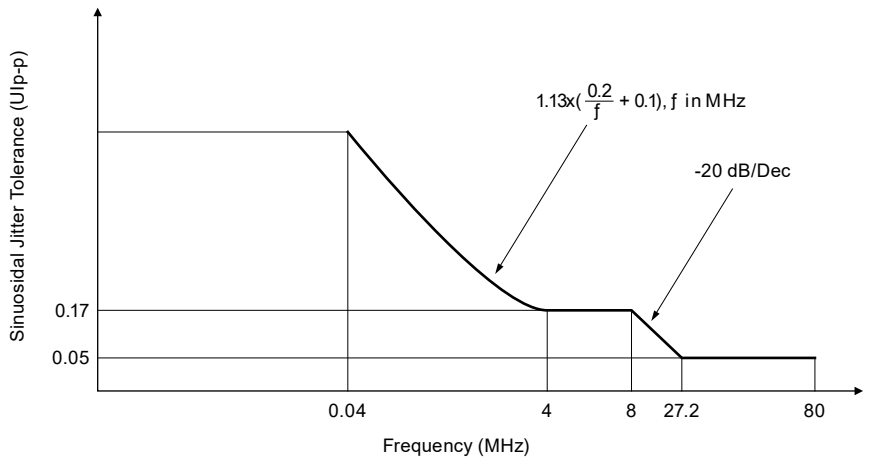


Figure 34. Sinusoidal jitter tolerance

4.11.3 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with Controller and Peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% VDD and 80% VDD thresholds, unless noted, as well as input signal transitions of 3 ns and a 25 pF maximum load on all LPSPI pins.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.11.3.1 LPSPI DC electrical characteristics

Table 77. LPSPI DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage [1,2]	0.7 x VDDO	—	—	V	—

Table continues on the next page...

Table 77. LPSPI DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VIL	Input low voltage [1,2]	—	—	0.3 x VDDO	V	—
IIN/IOZ	Input/Output leakage current [2]	-5	—	5	µA	—
VOH	Output high voltage [2]	VDDO - 0.45	—	—	V	IOH = -2 mA at VDDO min
VOL	Output lowvoltage [2]	—	—	0.45	V	IOL = 2 mA at VDDO min

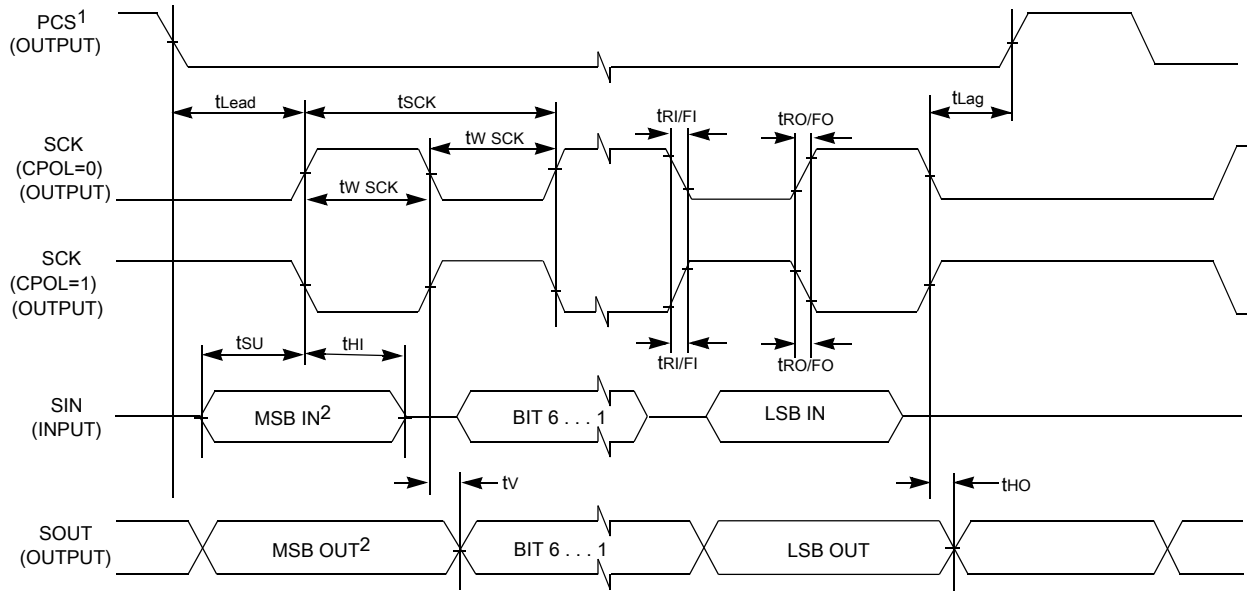
1. The minimum VIL and maximum VI values are based on the respective minimum and maximum VDD values found in Recommended Operating Conditions.
2. For recommended operating conditions, see Recommended Operating Conditions.

4.11.3.2 LPSPI Controller mode AC timing specifications

Table 78. LPSPI Controller mode AC timing specifications

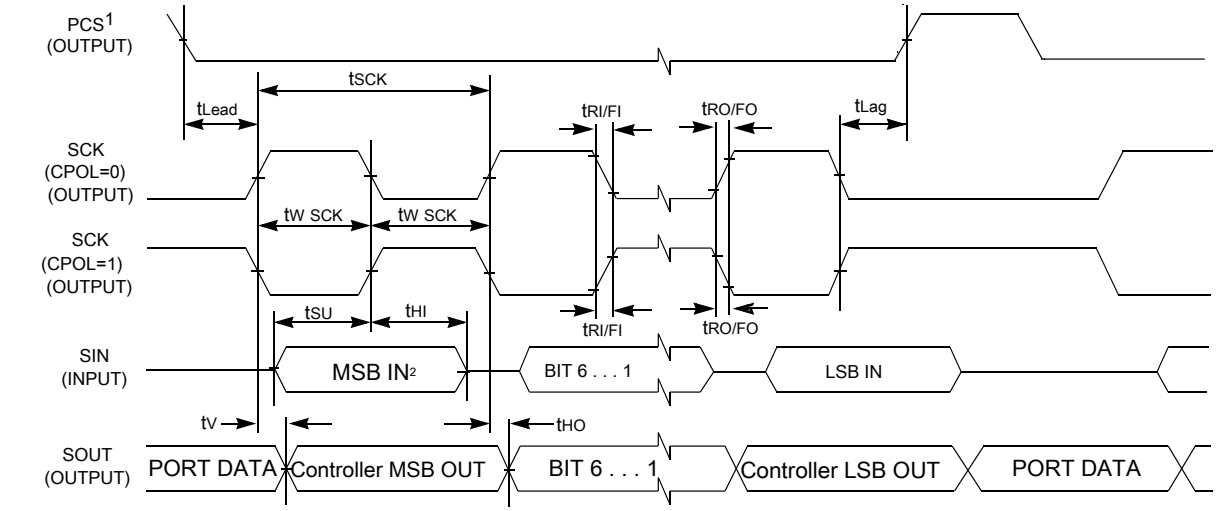
Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	Frequency of LPSPI clock root [1,2,3]	—	—	30	MHz	—
fSCK	Frequency of LPSPI clock root [4]	—	—	60	MHz	—
tSCK	SCK period [5]	2 x tperiph	—	—	ns	—
tLead	Enable lead time	1	—	—	tperiph	—
tLag	Enable lag time	1	—	—	tperiph	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 3	—	tSCK / 2 + 3	ns	—
tSU	Data setup time (inputs) [6]	8	—	—	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.
tHI	Data hold time (inputs) [6]	0	—	—	ns	—
tV	Data valid (after SCK edge)	—	—	2.5	ns	—
tHO	Data hold time (outputs)	-2.5	—	—	ns	—
tRI/FI	Rise/Fall time input	—	—	3	ns	—
tRO/FO	Rise/Fall time output	—	—	3	ns	—

1. The clock driver in the LPSPI module for fperiph must guaranteed this limit is not exceeded.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
4. In controller loopback mode when LPSPI_CFGR1[SAMPLE] bit is 1.
5. tperiph = 1000 / fperiph
6. If LPSPI_CFGR1[SAMPLE] bit is 1, the data setup time (inputs) / data hold time (inputs) specifications are same with the one in Peripheral mode.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI Controller mode timing (CPHA = 1)

4.11.3.3 LPSPI Target mode AC timing specifications

Table 79. LPSPI Target mode AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCK	Frequency of LPSPI clock root [1,2]	—	—	30	MHz	—

Table continues on the next page...

Table 79. LPSPI Target mode AC timing specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tSCK	SCK period [3]	2 x tperiph	—	—	ns	—
tLead	Enable lead time	1	—	—	tperiph	—
tLag	Enable lag time	1	—	—	tperiph	—
tWSCK	Clock (SCK) high or low time	tSCK / 2 - 5	—	tSCK / 2 + 5	ns	—
tSU	Data setup time (inputs)	3	—	—	ns	—
tHI	Data hold time (inputs)	3	—	—	ns	—
ta	Slave access time [4]	—	—	20	ns	—
tdis	Slave MISO disable time [5]	—	—	20	ns	—
tV	Data valid (after SCK edge)	—	—	8	ns	When operating at 3.3 V I/O supply, this parameter value is 9 ns.
tHO	Data hold time (outputs)	0	—	—	ns	—

1. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. tperiph = 1000 / fperiph
4. Time to data active from high-impedance state
5. Hold time to high-impedance state

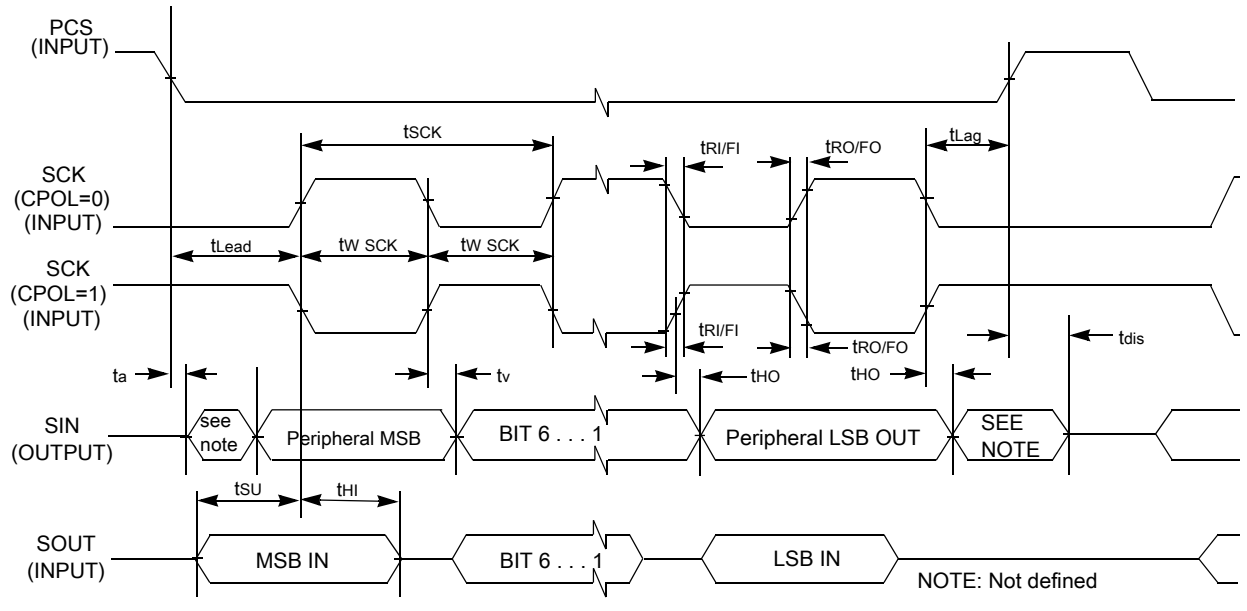


Figure 37. LPSPI Target mode timing (CPHA = 0)

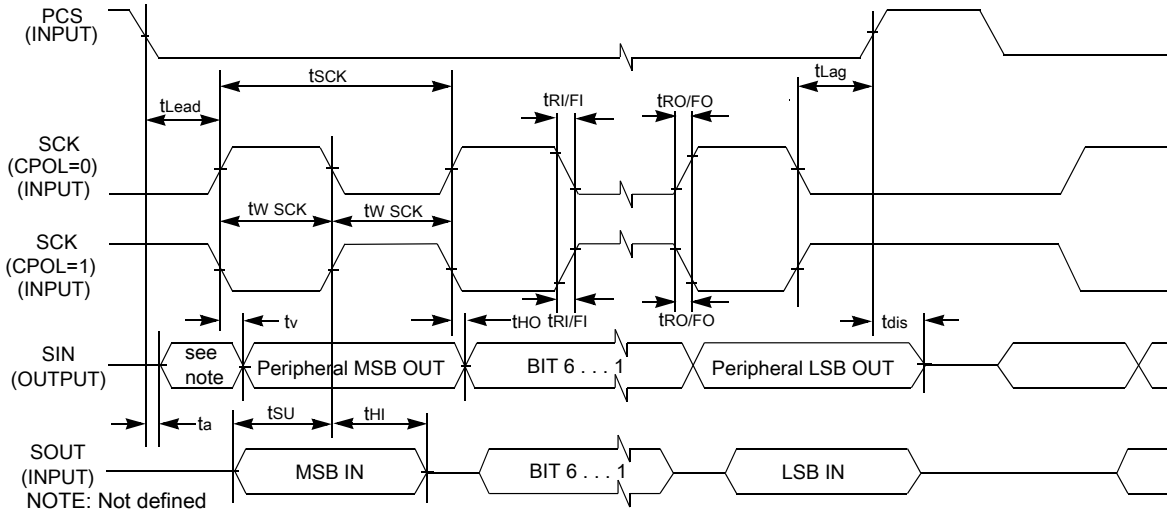


Figure 38. LPSPI Target mode timing (CPHA = 1)

4.11.4 LPI2C timing parameters

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target.

Table 80. LPI2C timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
tIH_SC	Input Start condition hold time	2	—	—	MODULE_CLK cycle	—
tCL	Input Clock low time	8	—	—	MODULE_CLK cycle	—
tIH	Input Data hold time	0	—	—	ns	SDA transitions after SCL falling edge
tCH	Input Clock high time	4	—	—	MODULE_CLK cycle	—
tISU	Input Data setup time (standard mode)	250	—	—	ns	SDA transitions before SCL rising edge
tISU_F	Input Data setup time (fast mode)	100	—	—	ns	SDA transitions before SCL rising edge
tISU_RSC	Input Start condition setup time (repeated start condition)	2	—	—	MODULE_CLK cycle	—
tISU_SC	Input Start condition setup time	2	—	—	MODULE_CLK cycle	—

Table continues on the next page...

Table 80. LPI2C timing parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tOH_SC	Output Start condition hold time	6	—	—	MODULE_CLK cycle	—
tCL	Output Clock low time	10	—	—	MODULE_CLK cycle	—
tRISE	SDA/SCL rise time	—	—	100	ns	SRE[2:0] = 110
tOH	Output Data hold time	7	—	—	MODULE_CLK cycle	SRE[2:0] = 110
tFALL	SDA/SCL fall time	—	—	100	ns	SRE[2:0] = 110
tCH	Output Clock high time	10	—	—	MODULE_CLK cycle	SRE[2:0] = 110
tOSU	Output Data setup time	2	—	—	MODULE_CLK cycle	SRE[2:0] = 110
tOSU_RSC	Output repeated start condition setup time	20	—	—	MODULE_CLK cycle	SRE[2:0] = 110
tOSU_SC	Output start condition setup time	11	—	—	MODULE_CLK cycle	SRE[2:0] = 110
fSCL	SCL clock frequency: Standard mode (Sm) [1,2]	0	—	100	kHz	—
fSCL	SCL clock frequency: Fast mode (Fm) [1,2]	0	—	400	kHz	—
fSCL	SCL clock frequency: Fast mode Plus (Fm++) [1,2]	0	—	1000	kHz	—
fSCL	SCL clock frequency: High speed mode (Hs-mode) [1,2]	0	—	3400	kHz	—
fSCL	SCL clock frequency: Ultra Fast mode (Ufm) [1,2]	0	—	5000	kHz	—

1. For more details, see UM10204 I2C-bus specification and user manual.
2. Standard, Fast, Fast+, and Ultra Fast modes are supported; High speed mode (HS) in slave mode.

4.11.5 Improved Inter-Integrated Circuit Interface (I3C) specifications

Unless otherwise specified, I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

4.11.5.1 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns.

Table 81. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1,2]	32	—	—	ns	—
tDIG_H	SCL Clock High Period [2]	32	—	—	ns	—
tSCO	Clock in to Data Out for Target [3,4]	—	—	12	ns	—
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Target [6,7]	0	—	—	—	Applicable for target and controller loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for target and controller loopback modes

1. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
2. tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
3. Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Controller may be a Target in a multi-Controller system, and thus shall also adhere to this requirement
4. Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Controller to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
6. SDA Input Hold time in Target mode is 1 ns.
7. tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Controller mode vs. Target mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

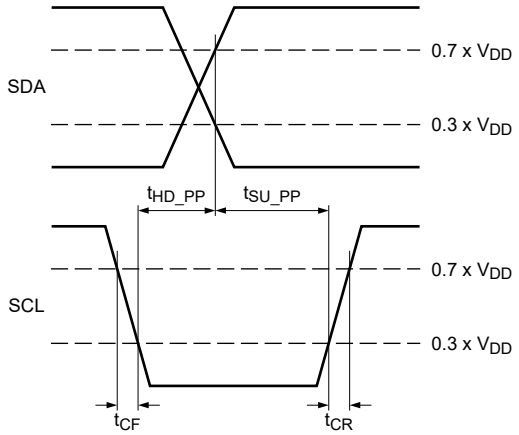


Figure 39. Controller out timing

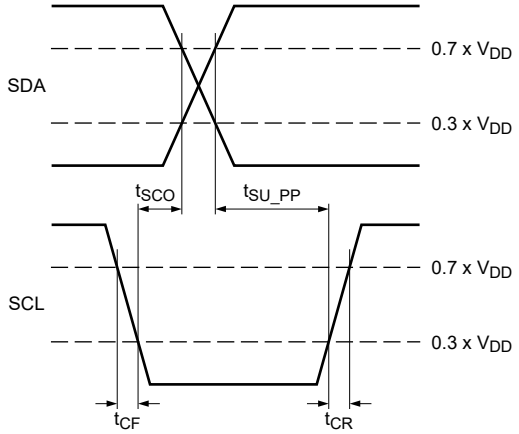


Figure 40. Target out timing

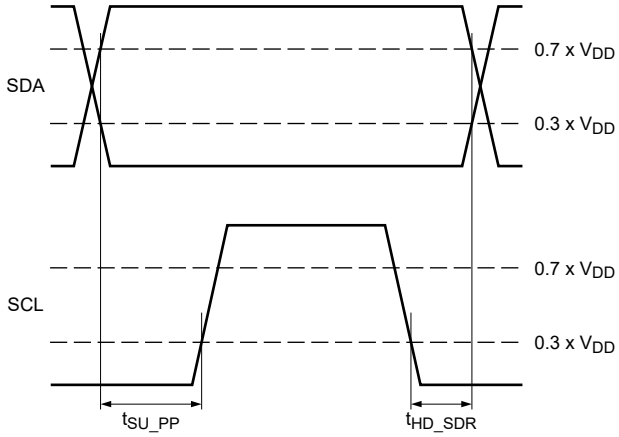


Figure 41. Controller SDR timing

4.11.6 CAN network AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has two CAN modules

available. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Please see General purpose I/O (GPIO) AC parameters for timing parameters.

Table 82. CAN-FD electrical specifications

Parameters	BCAN (Classical and FD)	FlexCAN (Classical and FD)	BCANXL (Classical, FD, and XL)	Unit
Minimum operating frequency	20/40	20/40	40/160	MHz
Maximum Baud Rate	8/8	8/8	20/20	Mbps
TXD Rise time wcs	4/4	4/4	4/4	ns
TXD Fall time wcs	4/4	4/4	4/4	ns
RXD Rise time wcs	4/4	4/4	4/4	ns
RXD Fall time wcs	4/4	4/4	4/4	ns
TXD	3.3/3.3	3.3/3.3	3.3/3.3	V
RXD	3.3/3.3	3.3/3.3	3.3/3.3	V
Internal delay wcs	100/50	100/50	50/12.5	ns
TX PAD delay wcs	25/25	25/25	25/25	ns
RX PAD delay wcs	10/10	10/10	10/10	ns
TX routing delay wcs	5/5	5/5	5/5	ns
RX routing delay wcs	5/5	5/5	5/5	ns
Transceiver loop delay wcs	250/250	250/250	190/190	ns
Total loop delay	395/345	395/345	285/247.5	ns

4.11.7 Pulse Width (PWM) timing parameters

This section describes the output timing parameters of the TPM.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

The following table lists the PWM timing parameters.

Table 83. Pulse Width (PWM) timing parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
—	PWM Module Clock Frequency	0	—	83.3	MHz	—
P1	PWM output pulse width high	12	—	—	ns	—
P2	PWM output pulse width low	12	—	—	ns	—

The following figure depicts the timing of the PWM.

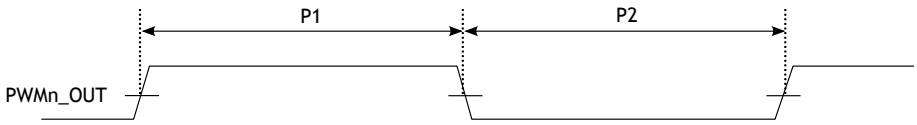


Figure 42. TPM timing

4.11.8 FlexSPI timing parameters

The FlexSPI interface can work in SDR or DDR modes.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. CLock transition measured at mid-supply.

Input timing assumes an input signal slew rate of 1 ns (20%/80%) and Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, un-terminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.11.8.1 FlexSPI PADs grouping

See Table 115 for SPI1_* PAD muxing.

See Table 84 for SD1/SD3_* PAD muxing.

Table 84. SD1/SD3_* PAD muxing

Signal name	Pad name
FlexSPIA_SS1_B	SD1_DATA3
FlexSPIA_DATA4	SD1_DATA4
FlexSPIA_DATA5	SD1_DATA5
FlexSPIA_DATA6	SD1_DATA6
FlexSPIA_DATA7	SD1_DATA7
FlexSPIA_DQS	SD1_STROBE
FlexSPIA_SCLK	SD3_CLK
FlexSPIA_SS0_B	SD3_CMD
FlexSPIA_DATA0	SD3_DATA0

Table continues on the next page...

Table 84. SD1/SD3_* PAD muxing...*continued*

Signal name	Pad name
FlexSPIA_DATA1	SD3_DATA1
FlexSPIA_DATA2	SD3_DATA2
FlexSPIA_DATA3	SD3_DATA3
SCLK PAD loopback	SD3_SLCK_DUMMY
DQS PAD loopback	XSPI1_DQS_DUMMY

4.11.8.2 FlexSPI DC electrical characteristics

Table 85. FlexSPI DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	0.7 x OVDD	—	—	V	The min VIL and max VIH values are based on the respective min and max OVIN values found in Recommended Operating Conditions.
VIL	Input low voltage	—	—	0.3 x OVDD	V	The min VIL and max VIH values are based on the respective min and max OVIN values found in Recommended Operating Conditions.
VOH	Output low voltage (IOH = 100 µA)	0.85 x OVDD	—	—	V	—
VOL	Output high voltage (IOH = -100 µA)	—	—	0.15 x OVDD	V	—
IIN	Input current	—	—	±50	µA	(0V ≤ VIN ≤ OVDD) The symbol OVIN represents the input voltage of the supply referenced in Recommended Operating Conditions

4.11.8.3 FlexSPI input/read timing

There are four sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)

- Dummy read strobe generated by FlexSPI controller and looped back through the SCK pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x2)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

4.11.8.3.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC]

4.11.8.3.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Figure 43 depicts the FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2.

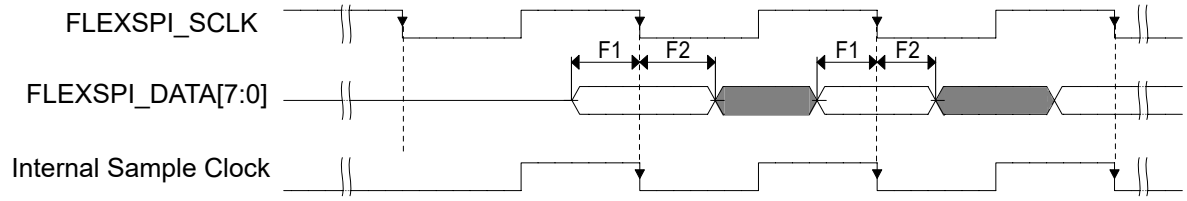


Figure 43. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X0, 0X1, 0x2

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.11.8.3.1.2 FlexSPI input timing in SDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Table 86. FlexSPI input timing in SDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	66	MHz	Nominal and Overdrive mode
F1	Setup time for incoming data	6	—	—	ns	Nominal and Overdrive mode
F2	Hold time for incoming data	0	—	—	ns	Nominal and Overdrive mode
—	Frequency of operation	—	—	50	MHz	Low drive mode
F1	Setup time for incoming data	7	—	—	ns	Low drive mode
F2	Hold time for incoming data	0	—	—	ns	Low drive mode

4.11.8.3.1.3 FlexSPI input timing in SDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Table 87. FlexSPI input timing in SDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	166	MHz	Nominal and Overdrive mode
F1	Setup time for incoming data	1.2	—	—	ns	Nominal and Overdrive mode

Table continues on the next page...

Table 87. FlexSPI input timing in SDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
F2	Hold time for incoming data	1	—	—	ns	Nominal and Overdrive mode
—	Frequency of operation	—	—	100	MHz	Low drive mode
F1	Setup time for incoming data	2	—	—	ns	Low drive mode
F2	Hold time for incoming data	1	—	—	ns	Low drive mode

4.11.8.3.2 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC]

4.11.8.3.2.1 FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Table 88. FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	33	MHz	Nominal, Overdrive, and Low drive mode
F1	Setup time for incoming data	6	—	—	ns	Nominal, Overdrive, and Low drive mode
F2	Hold time for incoming data	0	—	—	ns	Nominal, Overdrive, and Low drive mode

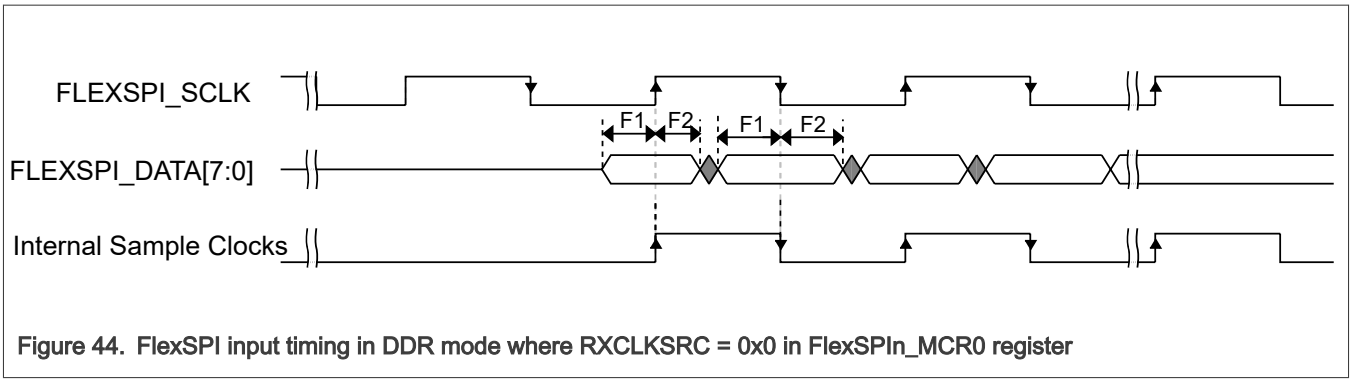


Figure 44. FlexSPI input timing in DDR mode where RXCLKSRC = 0x0 in FlexSPIn_MCR0 register

4.11.8.3.2.2 FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Table 89. FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	83	MHz	Nominal and Overdrive mode
F1	Setup time for incoming data	1.2	—	—	ns	Nominal and Overdrive mode
F2	Hold time for incoming data	1	—	—	ns	Nominal and Overdrive mode
—	Frequency of operation	—	—	66	MHz	Low drive mode

Table continues on the next page...

Table 89. FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
F1	Setup time for incoming data	1.7	—	—	ns	Low drive mode
F2	Hold time for incoming data	1	—	—	ns	Low drive mode

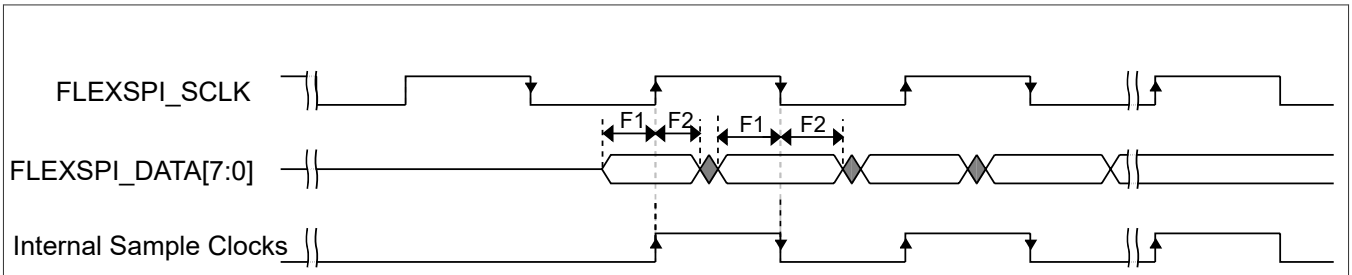


Figure 45. FlexSPI input timing in DDR mode where RXCLKSRC = 0x1 or 0x2 in FlexSPIn_MCR0 register

4.11.8.3.2.3 DDR mode with RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

Table 90. DDR mode with RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation [1]	—	—	200	MHz	Nominal and Overdrive mode
tIH_DQS	Input hold time (w.r.t DQS) [1]	1.725	—	—	ns	Nominal and Overdrive mode
tISU_DQS	Input setup time (w.r.t DQS) [1]	-0.525	—	—	ns	Nominal and Overdrive mode
—	Frequency of operation [1]	—	—	133	MHz	Low drive mode
tIH_DQS	Setup time for incoming data [1]	2.65	—	—	ns	Low drive mode
tISU_DQS	Hold time for incoming data [1]	-0.75	—	—	ns	Low drive mode

1. These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage. For 3.3 V I/O supply, see the FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (Low drive mode).

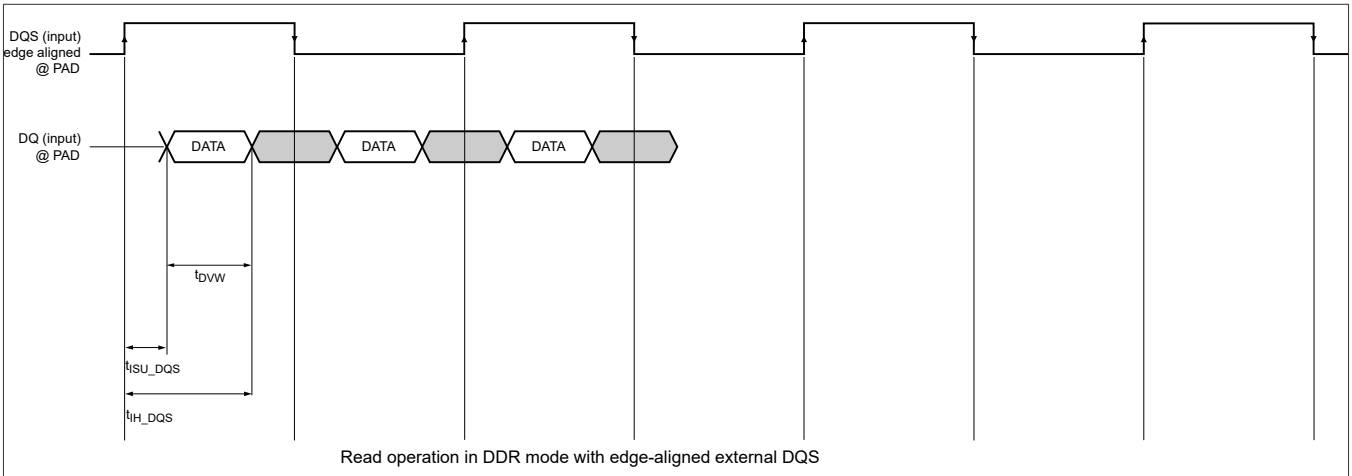


Figure 46. FlexSPI input timing in DDR mode where RXCLKSRC = 0x3 in FlexSPIn_MCR0 register

4.11.8.4 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.11.8.4.1 FlexSPI output timing in SDR mode

Table 91. FlexSPI output timing in SDR mode

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation [1,2]	—	—	200	MHz	Nominal and Overdrive mode
Tck	SCK clock period [1]	5	—	—	ns	Nominal and Overdrive mode
TDVO	Output data valid time [1]	—	—	0.6	ns	Nominal and Overdrive mode
TDHO	Output data hold time [1]	-0.6	—	—	ns	Nominal and Overdrive mode
TCSS	Chip select output setup time [1]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode
TCSH	Chip select output hold time [1]	(TCSH x Tck) - 0.6	—	—	SCLK	Nominal and Overdrive mode
—	Frequency of operation	—	—	133	MHz	Low drive mode
Tck	SCK clock period	7.5	—	—	ns	Low drive mode
TDVO	Output data valid time	—	—	2	ns	Low drive mode
TDHO	Output data hold time	-2	—	—	ns	Low drive mode
TCSS	Chip select output setup time [3]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Low drive mode
TCSH	Chip select output hold time [3]	(TCSH x Tck) -2	—	—	SCLK	Low drive mode

1. These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage. For 3.3 V I/O supply, see the FlexSPI SDR output timing in SDR mode (Low drive mode).
2. The actual maximum frequency supported is limited by the FlexSPIn _MCR0[RXCLKSRC] configuration used, see the FlexSPI SDR input timing specifications.
3. TCSS and TCSH are configured by the FlexSPI n _FLSHAxCR1 register. See i.MX 95 Applications Processor Reference Manual (IMX95RM) for more details.

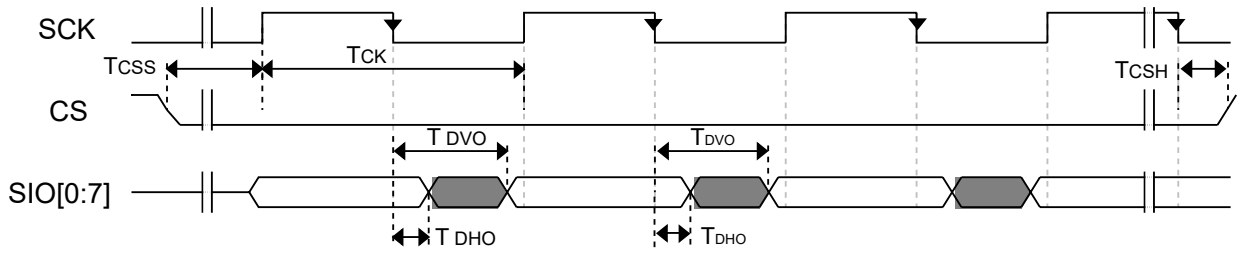


Figure 47. FlexSPI output timing in SDR mode

4.11.8.4.2 FlexSPI output timing in DDR mode

Table 92. FlexSPI output timing in DDR mode

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation [1,2]	—	—	200	MHz	Nominal and Overdrive mode
Tck	SCK clock period [1]	5	—	—	ns	Nominal and Overdrive mode
TDVO	Output data valid time [1]	—	—	1.815	ns	Nominal and Overdrive mode
TDHO	Output data hold time [1]	0.615	—	—	ns	Nominal and Overdrive mode
TCSS	Chip select output setup time [1,3]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode
TCSH	Chip select output hold time [1,3]	(TCSS + 0.5) x Tck - 0.6	—	—	SCLK	Nominal and Overdrive mode
—	Frequency of operation [2]	—	—	133	MHz	Low drive mode
Tck	SCK clock period	7.5	—	—	ns	Low drive mode
TDVO	Output data valid time	—	—	2.75	ns	Low drive mode
TDHO	Output data hold time	0.9	—	—	ns	Low drive mode
TCSS	Chip select output setup time [3]	(TCSS + 0.5) x Tck - 0.9	—	—	SCLK	Low drive mode
TCSH	Chip select output hold time [3]	(TCSS + 0.5) x Tck - 0.9	—	—	SCLK	Low drive mode

1. These timing specifications are valid only for 1.8 V nominal IO pad supply voltage. For 3.3 V I/O supply, see Table. FlexSPI output timing in DDR mode (Low drive mode).
2. The actual maximum frequency supported is limited by the FlexSPIn_MCR0[RXCLKSRC] configuration used, see the FlexSPI DDR input timing specifications.
3. TCSS and TCSH are configured by the FlexSPIn_FLSHAxCR1 register. See i.MX 95 Applications Processor Reference Manual (IMX95RM) for more details.

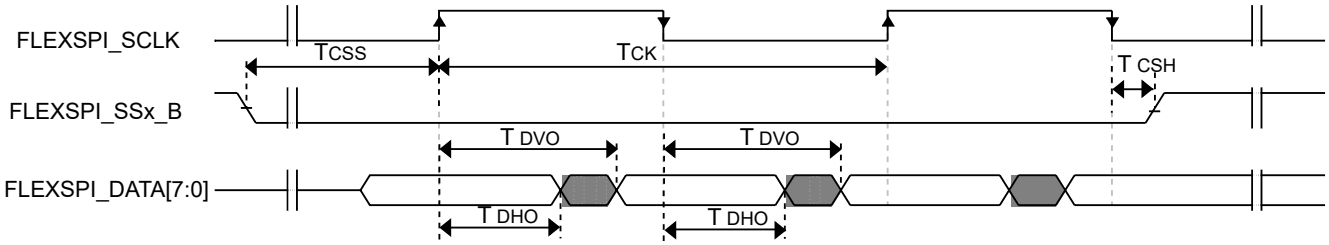


Figure 48. FlexSPI output timing in DDR mode

4.11.9 FlexSPI_FLR Specifications

Tested on samples basis and specified through design and characterization data. TA = 25 ℃, VCC = 3.0 V.

4-byte address alignment for Quad Read: read address start from A1, A 0 = 0,0

For details about FlexSPI Follower specifications, please refer to https://www.winbond.com.

4.11.10 LPUART I/O configuration and timing parameters

Please refer to General purpose I/O (GPIO) AC parameters.

4.11.11 Flexible I/O controller (FLEXIO) specifications

4.11.11.1 Flexible I/O controller (FlexIO) DC electrical characteristics

Table 93. Flexible I/O controller (FlexIO) DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VIH	Input high voltage [1,2]	0.7 x VDDO	—	—	V	—
VIL	Input low voltage [1,2]	—	—	0.3 x VDDO	V	—
IIN/IOZ	Input/output leakage current	—	—	-250/+50	µA	—
VOH	Output high voltage (IOH = -2mA at VDDO min)	VDDO-0.45	—	—	V	—
VOL	Output high voltage (IOL = 2mA at VDDO min)	—	—	0.45	V	—

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min VIL and max VIH values are based on the respective min and max VDD values found in Recommended Operating Conditions.

4.11.11.2 Flexible I/O controller (FlexIO) AC timing characteristics

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Input timing assumes an input signal slew rate of 3 ns (20%/80%).

Output timing valid for maximum external load CL = 25 pF, which is assumed to be a load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25-pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

The following table shows FlexIO timing specifications.

Table 94. Flexible I/O controller (FlexIO) AC timing characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle [1]	0	—	12	ns	—
tIDS	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle [1]	0	—	12	ns	—

1. Assume pinx muxed on same VDD_IO domain with the load

4.11.12 USB PHY parameters

Implemented PHYs are compatible with following standards.

- *Universal Serial Bus Revision 3.0 Specification (including ECNs and errata)*
- *Universal Serial Bus Revision 2.0 Specification (including ECNs and errata)*

4.11.12.1 USB2.0 specifications

4.11.12.1.1 USB 2.0 DC electrical characteristics

Table 95. USB 2.0 DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output High voltage	2.8	—	—	V	VDD ≥3.0 V
VOL	Output Low voltage	—	—	0.8	V	VDD ≥3.0 V
VCRS	Output Crossover Point	1.3	—	2	V	—
ZDRV	Output impedance	28	36	44	Ω	Driving High
ZDRV	Output impedance	28	36	44	Ω	Driving Low
RPU	Pull-up resistance	1.425	1.5	1.575	kΩ	Full speed (D + Pull-up)
TR	Output Rise time	4	—	20	ns	Full speed
TF	Output Fall time	4	—	20	ns	Full speed
VDI	Differential Input Sensitivity	0.2	—	—	V	| (D+) - (D-) |
VCM	Differential Input Common mode range	0.8	—	2.5	V	—
IL	Input leakage current	—	< 1.0	—	µA	Pullups Disabled

4.11.12.1.2 USB 2.0 AC timing specifications

Table 96. USB 2.0 AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
FREF_OFFSET	Reference clock frequency offset	-300	—	300	ppm	—
JRMSREF_CLK	Reference clock random jitter (RMS) [1,2]	—	—	3	ps	—
DJREF_CLK	Reference clock cycle-to-cycle jitter [3]	—	—	150	ps	—
tKHK/tSYSCLK	Reference clock duty cycle	40	—	60	%	—
fSYSCLK	Reference clock frequency	—	24	—	MHz	—

1. The peak-to-peak Rj specification is calculated at 14.069 times the RJRMS for 10 - 12 BER.
2. 1.5 MHz to Nyquist frequency. For example, 100 MHz reference clock, the Nyquist frequency is 50 MHz.
3. DJ across all frequencies.

4.11.12.2 USB 3.0 spcifications

4.11.12.2.1 USB 3.0 DC electrical characteristics

Table 97. USB 3.0 DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
Vtx-diff-pp	Differential output voltage [1]	800.0	1000.0	1200.0	mVp-p	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
Vtx-diff-pp-low	Low power differential output voltage [1]	400.0	—	1200.0	mVp-p	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
Vtx-de_ratio	Transmit de-emphasis [1]	3.0	—	4.0	dB	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
ZdiffTX	Differential impedance [1]	72.0	100.0	120.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
RTX-DC	Transmit common mode impedance [1]	18.0	—	30.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
TTX-CM-DCACTIVEIDLEDELTA	Absolute DC common mode voltage bteween U1 and U0 [1]	—	—	200.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
VTX-IDLEDIFF-DC	DC electrical idle differential output voltage [1]	0	0	10.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
RRX-DIFF-DC	Differential receiver input impedance [1]	72.0	100.0	120.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
RRX-DC	Receiver DC common mode impedance [1]	18.0	—	30.0	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V
ZRX-HIGHIMP-dc	DC input CM input impedance for V > 0 during reset or power down [1,2,3]	25000.0	—	—	Ω	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V

Table continues on the next page...

Table 97. USB 3.0 DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VTRXIDLE-IDLE-DET-DIFFpp	LPFS detect threshold [1]	100.0	—	300.0	mV	USB_HVDD = 3.3 V, USB_SVDD = 0.8 V

1. For operating conditions, see Recommended Operating Conditions.
2. Below the minimum is noise. Must wake up above the maximum.
3. Each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor.

4.11.12.2.2 USB 3.0 AC timing specifications

Table 98. USB 3.0 AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fUSB	Speed	—	5.0	—	Gb/s	—
TTX-EYE	Transmitter eye	0.625	—	—	UI	—
UI_TX	Unit interval (Transmitter)	199.94	200.0	200.06	ps	—
AC CAP	AC coupling capacitor	75.0	—	200.0	nF	—
UI_RX	Unit interval (Receiver)	199.94	200.0	200.06	ps	—
tPeriod	Period (LFPS)	20.0	—	100.0	ns	—
Vtx-diff-pp-lfps	Peak-to-peak differential amplitude (LFPS)	800.0	—	1200.0	mV	—
trise/fall	Rise and fall time (LFPS)	—	—	4.0	ns	—
DC LFPS	Duty cycle (LFPS)	40.0	—	60.0	%	—

UI does not account for SSC-caused variations.

Measured at compliance TP1. See the Figure. Transmit normative setup for details.

See the Figure. Transmit normative setup.

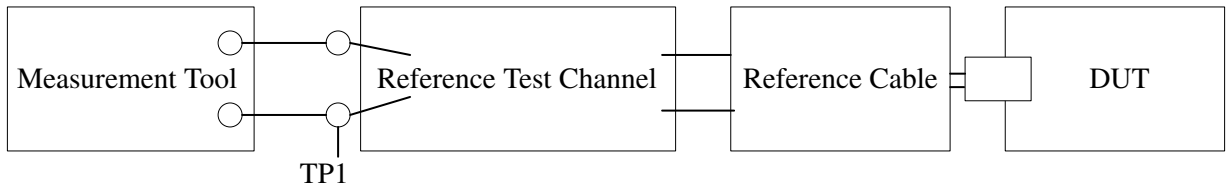


Figure 49. Transmit normative setup

4.11.12.3 Pad/Package/Board connections

The USBx_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

Each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor.

The USB 2.0 PHY uses USBx_TXRTUNE and an external resistor to calibrate the USBx_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on each of USBx_TXRTUNE pad to ground.

4.11.13 PCIe 3.0 PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen3 x1 lane and supports the *PCI Express Base Specification, Revision 3.1, November 2013, PCI-SIG*.

4.11.13.1 PCI Express 8 GT/s differential transmitter output DC electrical characteristics

Table 99. PCI Express 8 GT/s differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VVTX-FS-NO-EQ	Full swing transmitter voltage with no TX Eq [1]	800.0	—	1300.0	mVPP	—
VVTX-RS-NO-EQ	Reduced swing transmitter voltage with no TX Eq [1]	400.0	—	1300.0	mVPP	—
VTX- EIEOS-FS	Minimum swing during EIEOS for full swing [2]	250.0	—	—	mVPP	—
VTX- EIEOS-RS	Minimum swing during EIEOS for reduced swing [2]	232.0	—	—	mVPP	—
VTX- BOOST-FS	Maximum nominal Tx boost ratio for full swing [3]	8.0	—	—	dB	—
VTX- BOOST-RS	Maximum nominal Tx boost ratio for reduced swing	2.5	—	—	dB	—
VTX-AC-CM-PP	Tx AC peakpeak common mode voltage [4]	—	—	150.0	mVPP	—
VTX-DC-CM	Transmitter DC common-mode voltage [5]	0	—	3.6	V	—
VTX-CM-DC-ACTIVEIDLE-DELTA	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle [6]	0	—	100.0	mV	—
VTX-CM-DC-LINEDELTA	Absolute Delta of DC Common Mode Voltage between D+ and D- [6]	0	—	25.0	mV	—
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage [7]	0	—	20.0	mV	—
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage [8]	0	—	5.0	mV	—
VTX-RCV-DETECT	The amount of voltage change allowed during Receiver Detection [9]	—	—	600.0	mV	—
ZTX-DIFF- DC	DC differential transmitter impedance [10]	—	—	120.0	Ω	—
ITX-SHORT	Tx short circuit current [11]	—	—	90	mA	—

1. Voltage measurements for VTX-FS-NO-EQ and VTX-RS-NO-EQ are made using the 64-zeroes / 64-ones pattern in the compliance pattern.
2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the V TX-FS-NO-EQ measurement which represents the maximum peak voltage the transmitter can drive. The V TX-EIEOS-FS and V TX-EIEOS-RS voltage limits are imposed to

guarantee the EIEOS threshold of 175 mV P-P at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.
3. For full swing signaling VTX-EIEOS-FS is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space.
4. VTX-AC-CM-PP = max(VTX0_P + VTX0_N) / 2 - min(VTX0_P + VTX0_N) / 2 No more than 50 mVPP in 30 kHz to 500 MHz range.
5. The allowed DC common-mode voltage at a transmitter pin under any conditions.
6. |VTX-CM-DC [during L0] – VTX-CM-Idle-DC [during Electrical Idle]| ≤ 100 mV VTX-CM-DC = DC(avg) of |VTX-D+ + VTX-D-| / 2 VTX-CM-Idle-DC= DC(avg) of |VTX-D+ + VTX-D-| / 2 [Electrical Idle]
7. VTX-IDLE-DIFF-AC-p = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 20 mV. Voltage must be band pass filtered to remove any DC component and HF noise. The bandpass is constructed from two first-order filters, the high pass and low pass 3 dB bandwidths are 10 kHz and 1.25 GHz, respectively.
8. VTX-IDLE-DIFF-DC = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 5 mV. Voltage must be low pass filtered to remove any AC component. The low pass filter is first-order with a 3 dB bandwidth of 10 kHz.
9. The total amount of voltage change in a positive direction that a Transmitter can apply to sense whether a low impedance Receiver is present.
10. Transmitter DC differential mode low impedance
11. The total single-ended current a transmitter can supply when shorted to ground

4.11.13.2 PCI Express 8 GT/s differential transmitter output AC timing specifications

Table 100. PCI Express 8 GT/s differential transmitter output AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	124.9625	—	125.0375	ps	—
TTX-UTJ	Transmitter uncorrelated total jitter	—	—	31.25	ps p-p at 10^-12	—
TTX-UDJDD	Transmitter uncorrelated deterministic jitter	—	—	12.0	ps p-p	—
TTX-UPW- TJ	Total uncorrelated pulse width jitter (PWJ) [2]	—	—	24.0	ps p-p at 10^-12	—
TTX-UPW- DJDD	Deterministic DjDD uncorrelated PWJ [2]	—	—	10.0	ps p-p	—
TTX-DDJ	Data dependent jitter [3]	—	—	18	ps p-p	—
CTX	AC Coupling Capacitor [4]	176	—	265	nF	—

1. Each UI is 125 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. PWJ parameters shall be measured after data dependent jitter (DDJ) separation. Measured with optimized preset value after de-embedding to transmitter pin.
3. Measured with optimized preset value after de-embedding to transmitter pin.
4. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

4.11.13.3 PCI Express 8 GT/s differential receiver input DC electrical characteristics

Table 101. PCI Express 8 GT/s differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VRX-CM-AC-P	Rx AC common Mode Voltage [1]	—	—	75 (EH < 100 mVPP) 125 (EH	mVPP	—

Table continues on the next page...

Table 101. PCI Express 8 GT/s differential receiver input DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
				≥ 100 mVPP)		
VRX- LAUNCH-8 G	Generator launch voltage [2]	—	800.0	—	mVPP	—
VRX-MAX-SE-SW	Max single-ended swing	-300.00	—	300.00	mVPP	—
VRX-SV-8G	Eye height [3]	25.00	—	—	mVPP	—

1. Measured at Rx pins into a pair of 50 Ω terminations into ground.
2. Measured at TP1 per PCI Express base spec. rev 3.1
3. Measured at TP2P per PCI Express base spec. rev 3.1 .

4.11.13.4 PCI Express 8 GT/s differential receiver input AC timing specifications

Table 102. PCI Express 8 GT/s differential receiver input AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	124.9625	125	125.0375	ps	—
TRX-SV-8G	Eye width at TP2P [2]	0.300	—	0.350	UI	—
TRX-SV-SJ-8G	Sinusoidal jitter at 100 MHz [3]	—	—	0.10	UI p-p	—
TRX-SV-RJ-8G	Random jitter [4]	—	—	2.00	ps RMS	—

1. Each UI is 125 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. TRX-SV-8G is referenced to TP2P and obtained after post processing data captured at TP2. TRX-SV-8G includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
3. Fixed at 100 MHz. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency.
4. Random jitter spectrally flat before filtering. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.

4.11.13.5 PCI Express 5 GT/s differential transmitter output DC electrical characteristics

Table 103. PCI Express 5 GT/s differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VTX-DIFF-PP	Full swing transmitter voltage with no TX Eq [1]	800.0	—	1200.0	mVPP	—
VTX-DIFF-PP-LOW	Reduced swing transmitter voltage with no TX Eq [1]	400.0	—	1200.0	mVPP	—
VTX-DE-RATIO-3.5dB	Tx de-emphasis ratio at 3.5 dB [2]	3.0	—	4.0	dB	—
VTX-DE-RATIO-6dB	Tx de-emphasis ratio at 6 dB [2]	5.5	—	6.5	dB	—
VTX-AC-CM-PP	Tx AC peak-peak common mode voltage [3]	—	—	150.0	mVPP	—
VTX-DC-CM	Tx DC peak-peak common mode voltage [4]	0	—	3.6	V	—

Table continues on the next page...

Table 103. PCI Express 5 GT/s differential transmitter output DC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
ZTX-DIFF- DC	DC differential transmitter impedance [5]	—	—	120.0	Ω	—
ITX-SHORT	Tx short circuit current [6]	—	—	90	mA	—

1. VTX_DIFFp-p = 2 x | VTX0_P - VTX0_N |
2. Ratio of VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
3. VTX-AC-CM-PP = max(VTX0_P + VTX0_N) / 2 - min(VTX0_P + VTX0_N) / 2 No more than 100 mVPP in 30 kHz to 500 MHz range.
4. The allowed DC common-mode voltage at a transmitter pin under any conditions.
5. Transmitter DC differential mode low impedance
6. The total single-ended current a transmitter can supply when shorted to ground.

4.11.13.6 PCI Express 5 GT/s differential transmitter output AC timing specifications

Table 104. PCI Express 5 GT/s differential transmitter output AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	199.94	—	200.0600	ps	—
TTX-HF-DJ-DD	Tx deterministic jitter > 1.5 MHz	—	—	0.15	UI	—
TTX-LF-RMS	Tx RMS jitter < 1.5 MHz [2]	—	3.00	—	ps RMS	—
TTTX-EYE	Transmitter Eye including all jitter sources [3]	0.75	—	—	UI	—
CTX	AC Coupling Capacitor [4]	75	—	265	nF	—

1. Each UI is 200 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
3. The maximum transmitter jitter can be derived as: TTX-MAX-JITTER = 1 - TTX-EYE =0.25 UI. Specified at the measurement point into a timing and voltage test load as shown in Figure and measured over any 250 consecutive transmitter UIs.
4. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

4.11.13.7 PCI Express 5 GT/s differential receiver input DC electrical characteristics

Table 105. PCI Express 5 GT/s differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VRX-CM-AC-P	Rx AC common Mode Voltage [1]	—	—	150	mVP	—
ZRX-DC	Receiver DC single ended impedance [2]	40	—	60	Ω	—
VRX- IS-DIFF	Differential input swing	0.3	—	—	VPP	—
VRX-EYE	Receive eye voltage opening	—	120	—	mVPP	—

1. Measured at Rx pins into a pair of 50 Ω terminations into ground.
2. Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

4.11.13.8 PCI Express 5 GT/s differential receiver input AC timing specifications

Table 106. PCI Express 5 GT/s differential receiver input AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	199.940	200.00	200.060	ps	—
TRX-EYE	Receiver eye time opening	0.3	—	—	UI	—
TRX-HF-DJ-DD	Max Dj impinging on Rx under test	—	—	88	ps	—
TRX-SSC-RES	33 kHz Refclk residual	—	—	75	ps	—
TRX-LF-RMS	10 kHz to 1.5 MHz RMS jitter	—	—	4.2	ps RMS	—
TRX-TJ-CC	Max Rx inherent timing error	—	—	0.4	UI	—
TRX-DJ-DD_CC	Max Rx deterministic timing error	—	—	0.3	UI	—
TRX-MIN-PULSE	Minimum width pulse at Rx	0.6	—	—	UI	—

1. Each UI is 200 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.

4.11.13.9 PCI Express 2.5 GT/s differential transmitter output DC electrical characteristics

Table 107. PCI Express 2.5 GT/s differential transmitter output DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VTX-DIFF-PP	Full swing transmitter voltage with no TX Eq [1]	800.0	—	1200.0	mVPP	—
VTX-DIFF-PP-LOW	Reduced swing transmitter voltage with no TX Eq [2]	400.0	—	1200.0	mVPP	—
VTX-DE-RATIO-3.5dB	Tx de-emphasis ratio at 3.5dB [3]	3.0	—	4.0	dB	—
VTX-DC-CM	Tx DC peak-peak common mode voltage [4]	0	—	3.6	V	—
ZTX-DIFF- DC	DC differential transmitter impedance [5]	80.0	—	120.0	Ω	—
ITX-SHORT	Tx short circuit current [6]	—	—	90	mA	—
VTX-CM-AC-P	Tx AC peak common mode voltage [7]	—	20	—	mVPP	—

1. VTX_DIFFp-p = 2 x | VTX0_P - VTX0_N |
2. VTX_DIFFp-p-LOW = 2 x | VTX0_P - VTX0_N |
3. Ratio of VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
4. The allowed DC common-mode voltage at a transmitter pin under any conditions.
5. Transmitter DC differential mode low impedance
6. The total single-ended current a transmitter can supply when shorted to ground.
7. VTX-CM-AC-P = RMS[(VTX0_P + VTX0_N) / 2 - DCAVG(VTX0_P + VTX0_N) / 2]

4.11.13.10 PCI Express 2.5 GT/s differential transmitter output AC timing specifications

Table 108. PCI Express 2.5 GT/s differential transmitter output AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	399.88	—	400.1200	ps	—
TTTX-EYE	Transmitter Eye including all jitter sources [2]	0.75	—	—	UI	—
CTX	AC Coupling Capacitor [3]	75	—	265	nF	—
TTX-EYE-MEDIAN-to-MAX-JITTER	Maximum time between the jitter median and max deviation from the median [4]	—	—	0.1250	UI	—

1. Each UI is 400 ps ±300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. The maximum transmitter jitter can be derived as TTX-MAX-JITTER = 1 -TTX-EYE = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10 -12. A TTX-EYE - 0.75 UI provides for a total sum of deterministic and random jitter budget of T TX-JITTER-MAX = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The TTX-EYE-MEDIAN-to-MAX-JITTER median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
4. Jitter is defined as the measurement variation of the crossing points (VTX-DIFFp-p = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI.

4.11.13.11 PCI Express 2.5 GT/s differential receiver input DC electrical characteristics

Table 109. PCI Express 2.5 GT/s differential receiver input DC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
VRX-CM-AC-P	Rx AC common Mode Voltage [1]	—	—	150	mVPP	—
ZRX-DC	Receiver DC single ended impedance [2]	40	—	60	Ω	—
VRX- IS-DIFF	Differential input swing	0.3	—	—	VPP	—
VRX-ST	Eye height	0.175	—	—	VPP	—

1. Measured at Rx pins into a pair of 50 Ω terminations into ground.
2. Required receiver D+ as well as D-DC Impedance (50 ± 20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

4.11.13.12 PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications

Table 110. PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
UI	Unit Interval [1]	399.880	400.000	400.120	ps	—
TRX-EYE	Receiver eye time opening	0.4	—	—	UI	—

1. Each UI is 400 ps ± 300ppm. UI does not account for spread-spectrum clock dictated variations.

4.11.13.13 REFCLK IN DC characteristics

Table 111. REFCLK IN DC characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
TCLK_DUTY	Reference clock duty cycle [1]	40	—	60	%	—
SWREF_CLK	Rising/Falling Edge Rate [2]	0.6	—	4	V/ns	—
VMAX	Absolute maximum voltage at pinincluding overshoot [3]	—	—	1.15	V	—
VMIN	Absolute minimum voltage at pinincluding overshoot [3]	-0.3	—	—	V	—
VMAX	Maximum input voltage level [3]	—	—	0.88	V	—
VMIN	Minimum input voltage level [3]	-0.15	—	—	V	—
Viswing	Single-ended input swing	0.3	—	0.88	VPP	—
Vidiff	Differential input swing	0.3	—	1.76	VPPdiff	—

1. Measurement taken from differential waveform.
2. Measured from -150 mV to +150 mV on the differential waveform (derived from REF_PAD_CLK_P minus REF_PAD_CLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.
3. Measurement taken from single ended waveform.

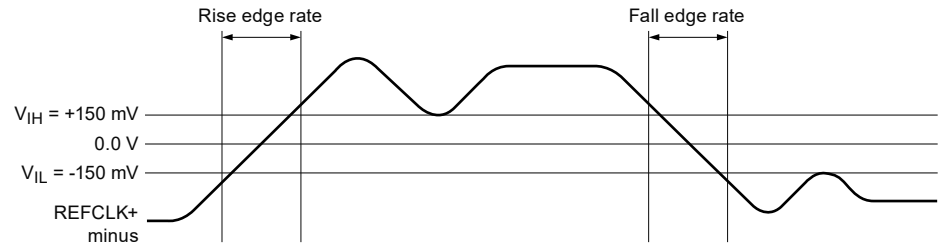


Figure 50. Differential measurement points for Rise and Fall time

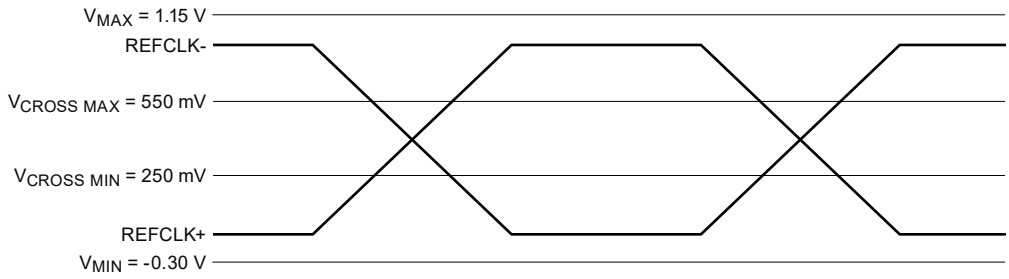


Figure 51. Single-Ended measurement points for absolute cross point and swing

4.11.13.14 REFCLK IN AC specifications in common clocked architecture

Table 112. REFCLK IN AC specifications in common clocked architecture

Symbol	Description	Min	Typ	Max	Unit	Condition
FREFCLK	Refclk frequency without SSC (SRNS)	99.97	100	100.03	MHz	—
FREF_OFFSET	Reference clock frequency offset without SSC	-300	—	300	ppm	—
FREF_OFFSET	Reference clock frequency offset with SSC	-300	—	2800	ppm	—
FREFCLK-RMS-CC	RMS Refclk jitter for common Refclk Rx architecture for 8GT/s	—	—	1	ps RMS	—
FREFCLK-HF-RMS	RMS Refclk jitter for common Refclk Rx architecture > 1.5 MHz for 5 GT/s	—	—	3.1	ps RMS	—
FREFCLK-LF-RMS	RMS Refclk jitter for common Refclk Rx architecture 10 kHz - 1.5 MHz for 5 GT/s	—	—	3	ps RMS	—
FSSC	SSC frequency range	30	—	33	kHZ	—
TSSC-FREQ-DEVIATION	SSC deviation	—	—	±0.5	%	—
TTRANSPORT-DELAY	Tx-Rx transport delay	12	—	—	ns	—

4.11.13.15 REFCLK IN AC specifications in separate clocked architecture

Table 113. REFCLK IN AC specifications in separate clocked architecture

Symbol	Description	Min	Typ	Max	Unit	Condition
FREFCLK	Refclk frequency without SSC (SRNS)	99.97	100	100.03	MHz	—
FREF_OFFSET	Reference clock frequency offset without SSC	-300	—	300	ppm	—
FREF_OFFSET	Reference clock frequency offset with SSC (SRIS)	-300	—	2800	ppm	—
TREFCLK-RMS-SRIS	RMS Refclk jitter for separate Refclk independent SSC architecture	—	—	0.5	ps RMS	8 GT/s
TREFCLK-RMS-SRIS	RMS Refclk jitter for separate Refclk independent SSC architecture	—	—	2.0	ps RMS	5 GT/s
FSSC	SSC frequency range	30	—	33	kHZ	—
TSSC-FREQ-DEVIATION	SSC deviation	—	—	±0.5	%	—

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

i.MX 95 supports three different boot modes:

- Normal Boot Mode
- Boot from Internal Fuse Mode
- Serial Download Boot Mode

Three different boot modes can be selected via different boot mode pins or overridden by fuses.

i.MX 95 has one kind of boot type:

- Low Power Boot (LPB): only M33 core is running after POR.

For detailed boot mode configuration, see the "Fusemap" and the "System Boot" chapter in i.MX 95 Reference Manual (IMX95RM).

5.1 Boot mode configuration pins

There are four boot mode pins used to select boot mode.

Table 114. Fuses and associated pins used for boot

BOOT_MODE [3:0]	Functions
X000	Boot from Internal Fueses
X001	Serial Download (USB1)
X010	uSDHC1 8-bit eMMC5.1
X011	uSDHC2 4-bit SD3.0
X100	FlexSPI Serial NOR
X101	FlexSPI Serial NAND
X110	Reserved
X111	Reserved

- HW samples the boot CFG pins before ROM starts, these pins should be mapped to Boot CFG pins by default.
- Once HW samples the boot CFG pins and stores the boot CFG in CMC register, the register should be latched and reflecting the pins status.

Additional boot options are also supported for both Normal Boot Mode and Internal Fuse mode:

- All boot modes support for a range of speeds, timings, and protocol formats;
- eMMC boot can be supported from any USDHC1 only, while SD boot can be supported from any USDHC instance 1 or 2;
- Serial NOR boot supports 1-bit, 4-bit, and 8-bit mode;
- Serial NAND boot supports 1-bit, 4-bit, and 8-bit mode (8-bit Serial NAND)

BOOT_MODE pins are multiplexed over other functional pins. The functional I/O that multiplexed with these pins must be selected subject to two criteria:

- Functional I/O must not be used if they are inputs to the SoC, which could potentially be constantly driven by external components. Such functional mode driving may interfere with the need for the board to pull these pins a certain way while POR is asserted.
- Functional I/O must not be used if they are outputs of the SoC, which will be connected to components on the board that may misinterpret the signals as valid signals if they are toggled (such as, the board drives them while POR is asserted).

5.2 Boot devices interfaces allocation

i.MX 95 supports three kinds of boot devices:

- Primary Boot Device

  The Primary boot device is selected by Boot Mode fuses if boot mode is boot from Internal Fuses. Otherwise, it can be selected by Boot Mode pins. The valid primary boot device options are SD/eMMC/FlexSPI NOR/SPI NAND. The valid options also depend on the Boot Type and other fuses configuration.

- Recovery Boot Device

  After failure of booting from Primary Boot Device, i.MX 95 tries to boot from another boot source. The recovery boot device is only from SPI1 or SPI2.

- Serial Download Boot Device

  Cortex-M33 supports serial download mode via USB1.

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 115. Boot through FlexSPI

Signal name	Pad name	Alt
FlexSPIA_DATA0	XSPI1_DATA0	ALT0
FlexSPIA_DATA1	XSPI1_DATA1	ALT0
FlexSPIA_DATA2	XSPI1_DATA2	ALT0
FlexSPIA_DATA3	XSPI1_DATA3	ALT0
FlexSPIA_DQS	XSPI1_DQS	ALT0
FlexSPIA_SS0_B	XSPI1_SS0_B	ALT0
FlexSPIA_SS1_B	XSPI1_SS1_B	ALT0
FlexSPIA_SCLK	XSPI1_DATA0	ALT0
FlexSPIA_DATA4	XSPI1_DATA4	ALT0
FlexSPIA_DATA5	XSPI1_DATA5	ALT0
FlexSPIA_DATA6	XSPI1_DATA6	ALT0
FlexSPIA_DATA7	XSPI1_DATA7	ALT0

Table 116. Boot through uSDHC1

Signal name	PAD name	ALT
USDHC1_CMD	SD1_CMD	ALT0
USDHC1_CLK	SD1_CLK	ALT0
USDHC1_DATA0	SD1_DATA0	ALT0
USDHC1_DATA1	SD1_DATA1	ALT0
USDHC1_DATA2	SD1_DATA2	ALT0
USDHC1_DATA3	SD1_DATA3	ALT0
USDHC1_DATA4	SD1_DATA4	ALT0
USDHC1_DATA5	SD1_DATA5	ALT0
USDHC1_DATA6	SD1_DATA6	ALT0
USDHC1_DATA7	SD1_DATA7	ALT0
USDHC1_RESET	SD1_DATA5	ALT2

Table 117. Boot through uSDHC2

Signal name	PAD name	ALT
USDHC2_CMD	SD2_CMD	ALT0
USDHC2_CLK	SD2_CLK	ALT0
USDHC2_DATA0	SD2_DATA0	ALT0
USDHC2_DATA1	SD2_DATA1	ALT0
USDHC2_DATA2	SD2_DATA2	ALT0
USDHC2_DATA3	SD2_DATA3	ALT0
USDHC2_RESET	SD2_RESET_B	ALT0
USDHC2_VSELECT	SD2_VSELECT	ALT0

Table 118. Boot through SPI1

Signal name	PAD name	ALT
SPI1_PCS1	PDM_BIT_STREAM0	ALT2
SP11_SIN	SAI1_TXC	ALT2

Table continues on the next page...

Table 118. Boot through SPI1*...continued*

SPI1_SOUT	SAI1_RXD0	ALT2
SPI1_SCK	SAI1_TXD0	ALT2
SPI1_PCS0	SAI1_TXFS	ALT2

Table 119. Boot through SPI2

Signal name	PAD name	ALT
SPI2_PCS1	PDM_BIT_STREAM1	ALT2
SP12_SIN	UART1_RXD	ALT2
SPI2_SOUT	UART2_RXD	ALT2
SPI2_SCK	UART2_TXD	ALT2
SPI2_PCS0	UART1_TXD	ALT2

NOTE

USB1 interfaces are dedicated pins, thus no IOMUX options.

6 Package information and functional contact assignments

This section includes the contact assignment information and mechanical package drawing.

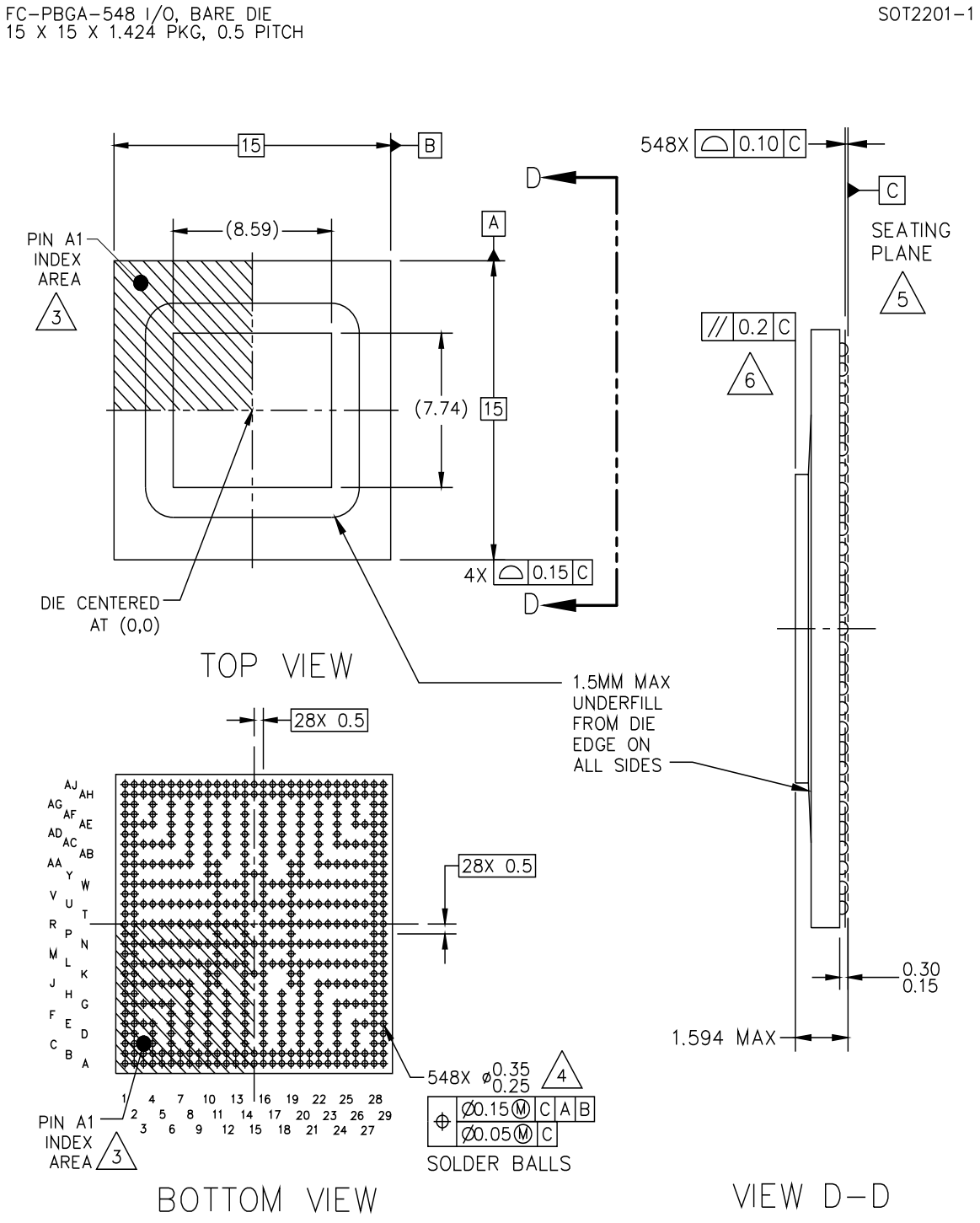
6.1 15 x 15 mm package information

This section includes the 15 x 15 mm package contact assignment information and mechanical package drawing.

6.1.1 15 x 15 mm, 0.5 mm pitch, ball matrix

Figure 52 shows the top, bottom, and side views of the 15 x 15 mm FCBGA package.

Figure 52. 15 x 15 mm FCBGA, case x package Top, Bottom, and Side Views



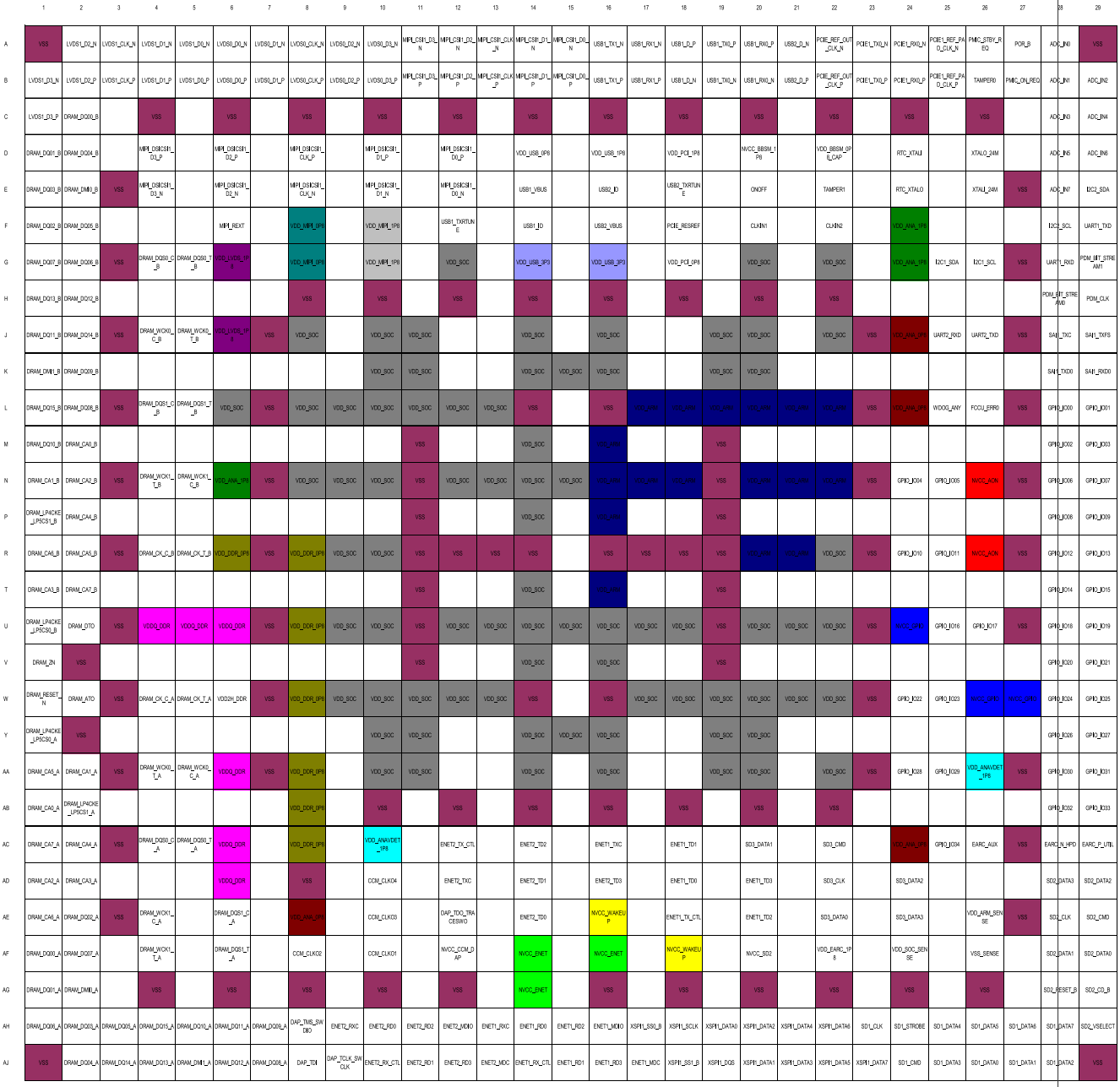
6.1.2 15 x 15 mm supplies contact assignments and functional contact assignments

See the attached excel file for details.

6.1.3 15 x 15 mm, 0.5 mm pitch, ball map

Figure 53 shows the 15 x 15 mm, 0.5 mm pitch, ball map for i.MX 95

Figure 53. 15 x 15 mm FCBGA ball map



6.2 19 x 19 mm package information

This section includes the 19 x 19 mm package contact assignment information and mechanical package drawing.

6.2.1 19 x 19 mm, 0.7 mm pitch, ball matrix

Figure 54 and Figure 55 shows the top, bottom, and side views of the 19 x 19 mm FCBGA package.

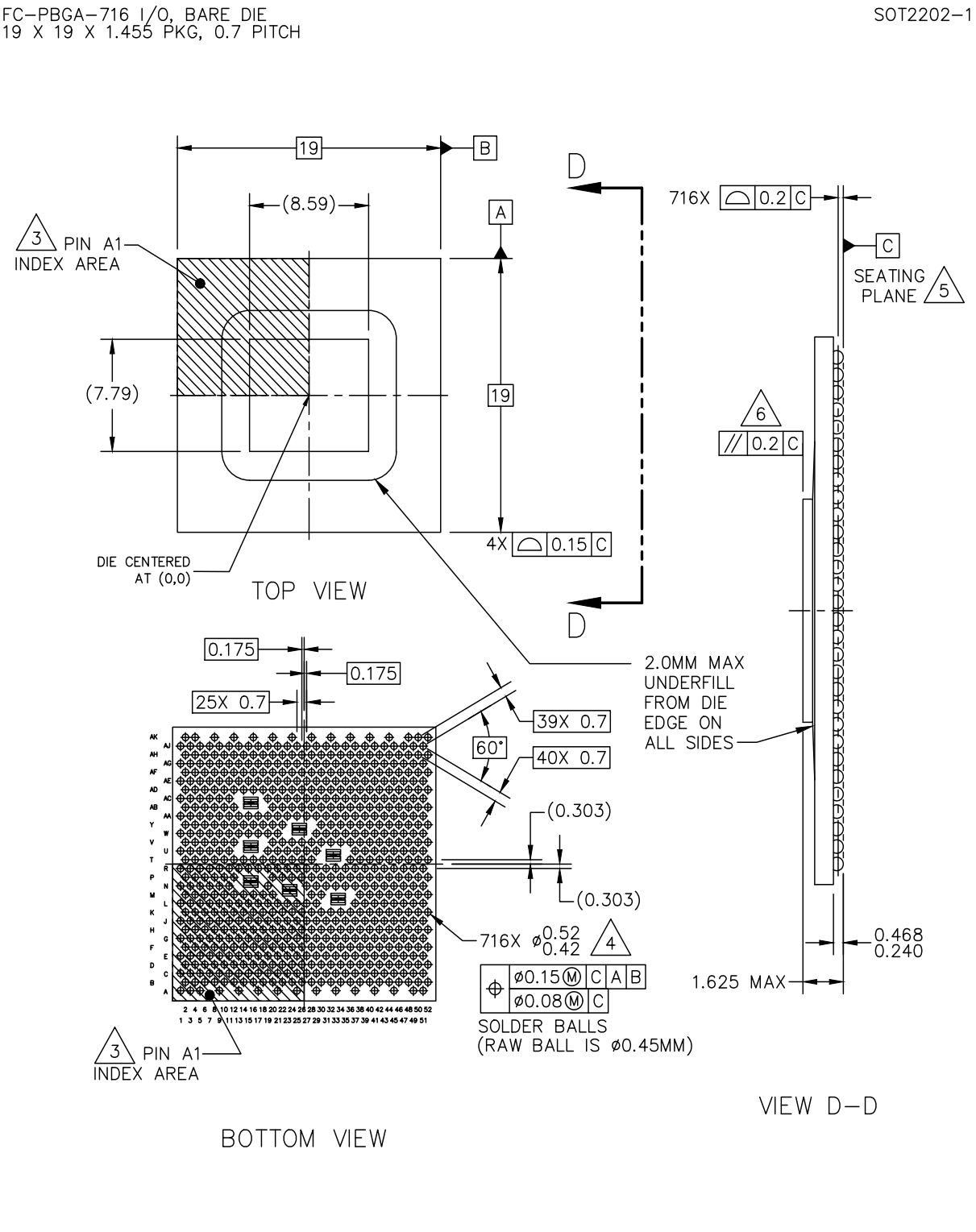
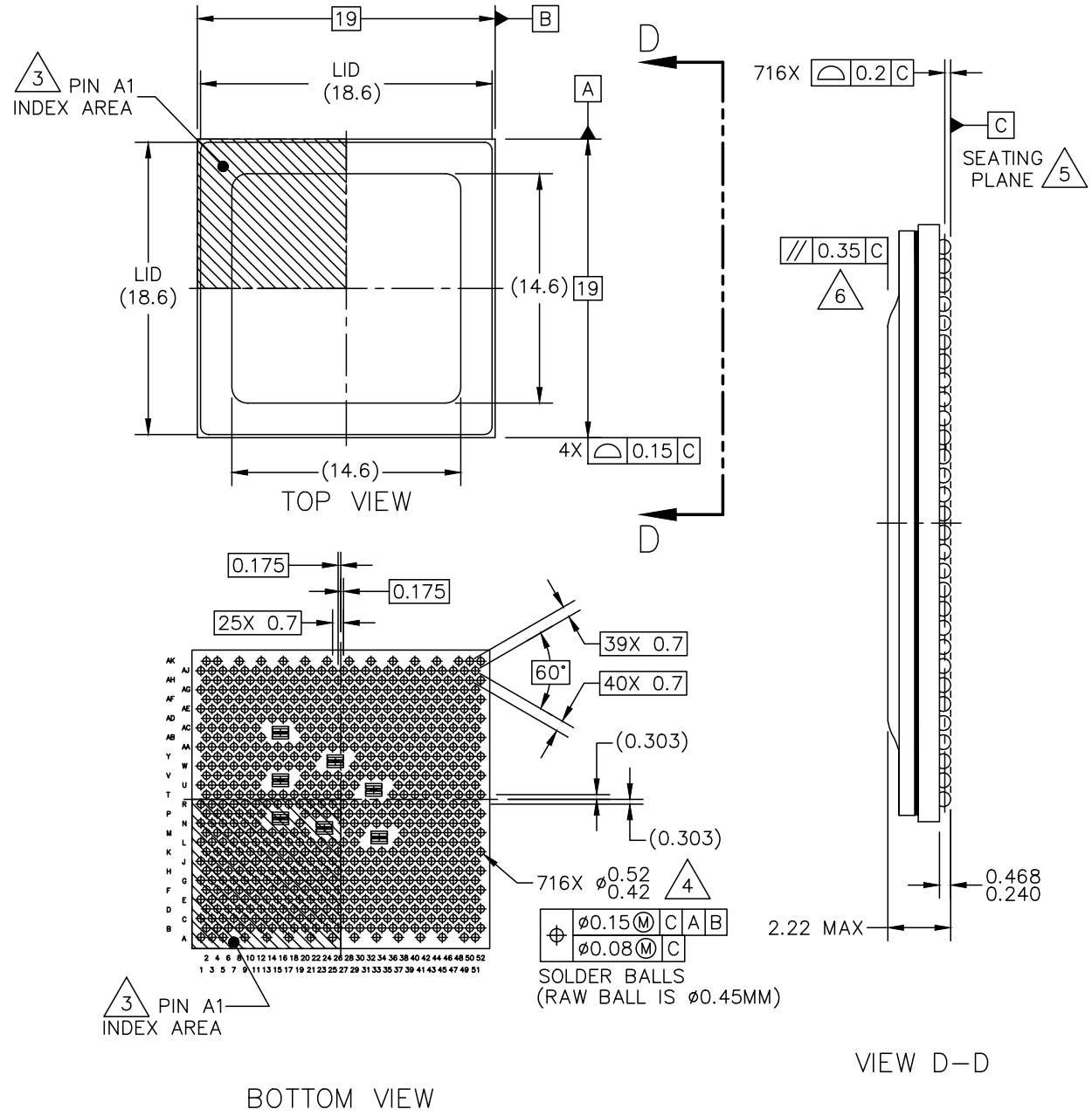


Figure 54. 19 x 19 mm FCBGA, case x package Top, Bottom, and Side Views

H–FC–PBGA–716 I/O, LIDDED
19 X 19 X 2.0 PKG, 0.7 PITCH

SOT2204–1



DATE: 13 JUL 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA02037D	REVISION: O	PAGE: 1 OF 6

Figure 55. 19 x 19 mm FCBGA (Lidded), case x package Top, Bottom, and Side Views

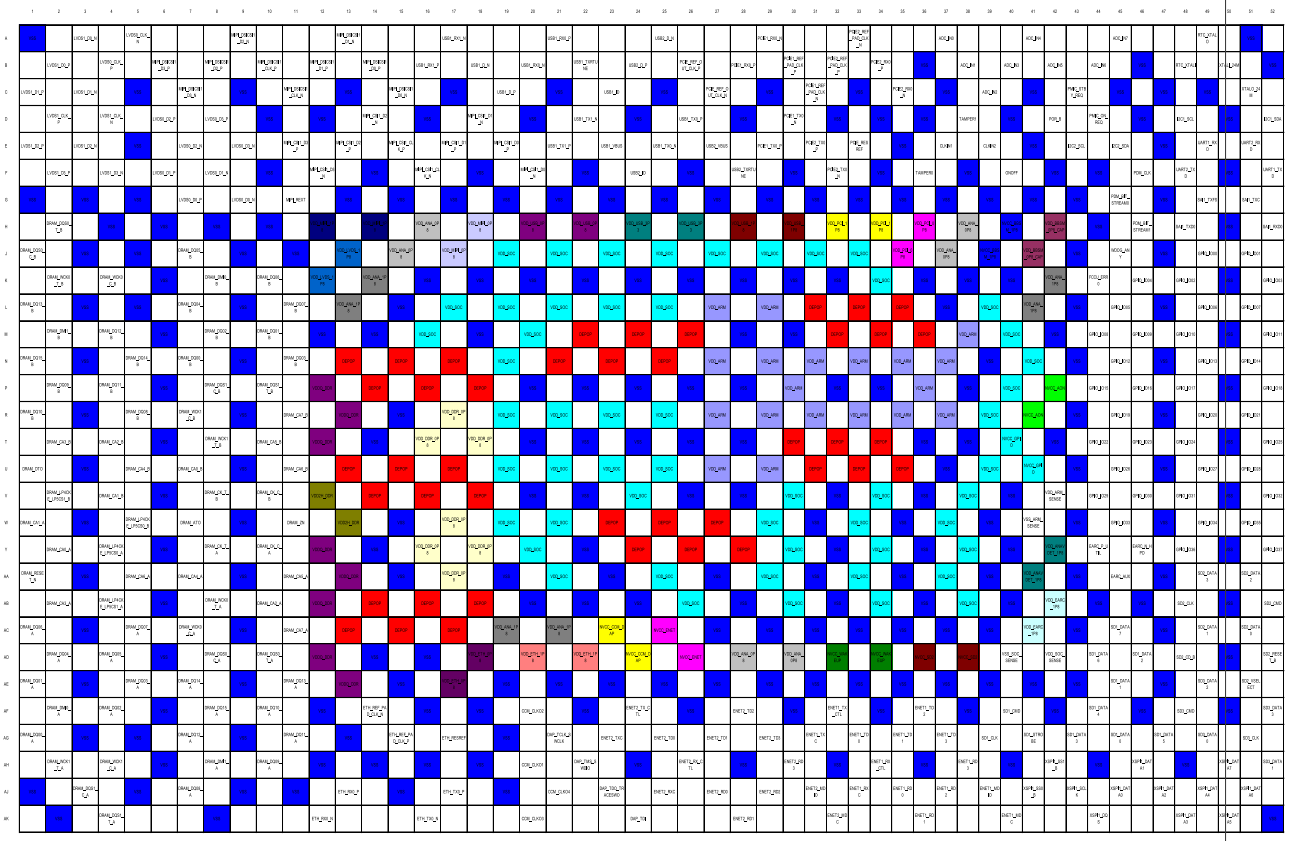
6.2.2 19 x 19 mm supplies contact assignments and functional contact assignments

See the attached excel file for details.

6.2.3 19 x 19 mm, 0.7 mm pitch, ball map

Figure 56 shows the 19 x 19 mm, 0.7 mm pitch, ball map for i.MX 95

Figure 56. 19 x 19 mm FCBGA ball map



7 Revision History

Table 120 provides a revision history for this data sheet.

Table 120. Data Sheet document revision history

Rev. Number	Date	Substantive Change(s)
Rev. 2	11/2024	• Updated Table 1 • Updated Ordering Information

Table continues on the next page...

Table 120. Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated Table 2 • Updated Figure 2 • Removed I.MX 95 module list • Updated Table 11 • Updated Power architecture • Updated Ramp rate specifications • Updated Table 17 • Updated Table 19 • Updated Maximum frequency of modules • Updated Clock source • Updated Power supplies requirements and restrictions • Updated General purpose I/O (GPIO) DC parameters • Added DDR pin I/O leakage DC parameters • Updated LVDS DC electrical characteristics • Updated Table 35 • Updated LVDS AC timing specifications • Updated SAI switching specifications • Updated DDR SDRAM–specific parameters (LPDDR5/LPDDR4X) • Removed WDOG Reset timing parameters • Updated Improved Inter-Integrated Circuit Interface (I3C) specifications • Updated Ethernet controller (ENET) • Updated FlexSPI timing parameters • Updated Flexible I/O controller (FLEXIO) specifications • Updated USB PHY parameters • Updated Table 114 • Updated Boot mode configuration pins • Updated Boot devices interfaces allocation
Rev. 1	02/2024	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

Contents

1 Introduction....2
1.1 Ordering Information....5
2 Block Diagram....7
3 Special Signal Considerations....8
3.1 Unused input and output guidance....9
4 Electrical characteristics....11
4.1 Chip-level conditions....11
4.1.1 Absolute maximum ratings....12
4.1.2 Electrostatic discharge and latch-up ratings....13
4.1.3 Thermal resistance....13
4.1.4 Power architecture....14
4.1.5 Power modes....17
4.1.6 Operating ranges....20
4.1.7 Temperature ranges specifications....22
4.1.8 Maximum frequency of modules....22
4.1.9 Clock source....22
4.2 Power supplies requirements and restrictions....24
4.2.1 Power-up sequence....26
4.2.2 Power-down sequence....27
4.3 PLL electrical characteristics....27
4.3.1 Fracn PLL....27
4.3.2 Low Noise PLL....28
4.4 I/O DC parameters....28
4.4.1 General purpose I/O (GPIO) DC parameters....28
4.4.2 DDR I/O DC electrical characteristics....29
4.4.3 DDR pin I/O leakage DC parameters....29
4.4.4 LVDS DC electrical characteristics....30
4.5 I/O AC parameters....30
4.5.1 General purpose I/O (GPIO) AC parameters....31
4.5.2 DDR I/O AC electrical characteristics....33
4.5.3 LVDS AC timing specifications....33
4.6 Differential I/O output buffer impedance....34
4.6.1 DDR I/O output buffer impedance....34
4.7 System modules timing....34
4.7.1 Reset timings parameters....34
4.7.2 JTAG timing parameters....35
4.7.3 SWD timing parameters....37
4.7.4 DDR SDRAM–specific parameters (LPDDR5/LPDDR4X)....38
4.8 Analog interfaces....38
4.8.1 12-bit ADC electrical specifications....39
4.9 Audio....39
4.9.1 SAI switching specifications....39
4.9.2 SPDIF timing parameters....44
4.9.3 Timer/PDM Microphone interface timing parameters....45
4.9.4 Medium Quality Sound (MQS) electrical specifications....47
4.10 Display and graphics....47
4.10.1 MIPI D-PHY electrical characteristics....47
4.11 External peripheral interface parameters....50
4.11.1 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing....50
4.11.2 Ethernet controller (ENET)....56
4.11.3 LPSPI timing parameters....70
4.11.4 LPI2C timing parameters....74
4.11.5 Improved Inter-Integrated Circuit Interface (I3C) specifications....75
4.11.6 CAN network AC electrical specifications....77
4.11.7 Pulse Width (PWM) timing parameters....78
4.11.8 FlexSPI timing parameters....79
4.11.9 FlexSPI_FLR Specifications....86
4.11.10 LPUART I/O configuration and timing parameters....86
4.11.11 Flexible I/O controller (FLEXIO) specifications....86
4.11.12 USB PHY parameters....87
4.11.13 PCIe 3.0 PHY parameters....90
5 Boot mode configuration....98
5.1 Boot mode configuration pins....98
5.2 Boot devices interfaces allocation....99
6 Package information and functional contact assignments....101
6.1 15 x 15 mm package information....101
6.1.1 15 x 15 mm, 0.5 mm pitch, ball matrix....102
6.1.2 15 x 15 mm supplies contact assignments and functional contact assignments....103
6.1.3 15 x 15 mm, 0.5 mm pitch, ball map....103
6.2 19 x 19 mm package information....104
6.2.1 19 x 19 mm, 0.7 mm pitch, ball matrix....104
6.2.2 19 x 19 mm supplies contact assignments and functional contact assignments....107
6.2.3 19 x 19 mm, 0.7 mm pitch, ball map....107
7 Revision History....107
Legal information....109

For more information, please visit: https://www.nxp.com

Date of release: 11 November 2024
Document identifier: IMX95CEC