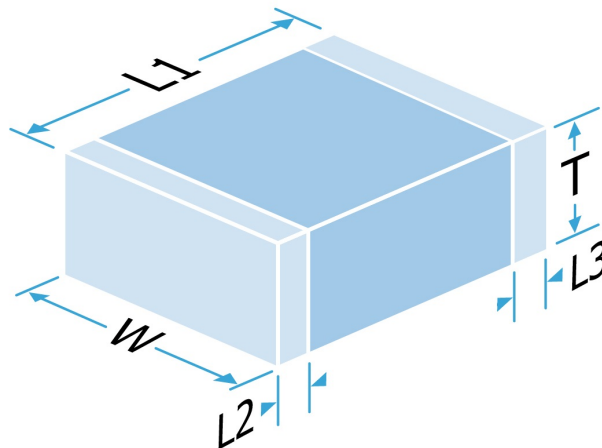


Multilayer Ceramic Chip Capacitor

Part Number: 2225Y0630392GKT

Description: 2225 63Vdc 3.9nF $\pm 2\%$ C0G/NP0 (1B) to AEC-Q200 (CTI ≥ 600)

A range of C0G MLC capacitors fully tested and approved to automotive specification AEC-Q200. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.



Mechanical Specification

Size Code	2225
Length (L1) in mm (")	5.7 +0.50/-0.40 (0.225 +0.02/-0.016)
Width (W) in mm (")	6.30 $\pm$ 0.40 (0.252 $\pm$ 0.016)
Thickness (T) in mm (")	2.5 Max (0.1 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	1.143 (0.045)
Termination Material	FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 500 per reel
Conformal Coating	Not normally required

General Electrical Specification

Rated Voltage	63Vdc
Nominal Capacitance Value	3.9nF
Capacitance Tolerance	$\pm 2\%$
Tangent of Loss Angle (Tan δ)	≤ 0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof	158Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	
Min Insulation Resistance (IR)	100.00GOhm @ 63Vdc
Dielectric Classification	C0G/NP0 (1B) to AEC-Q200 (CTI ≥ 600)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0 $\pm$ 30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Monday, July 21, 2025

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Part Number: 2225Y0630392GKT

Description: 2225 63Vdc 3.9nF $\pm 2\%$ C0G/NP0 (1B) to AEC-Q200 (CTI ≥ 600)

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

247 compliant

California Proposition 65

No exposure risk

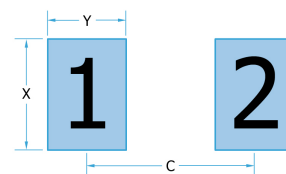
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

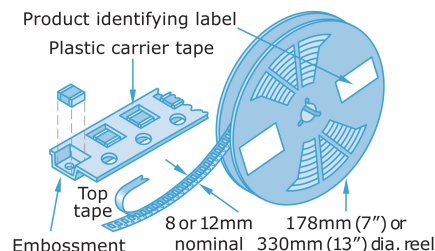
	2225	
C	5.20mm	0.205"
Y	1.65mm	0.065"
X	6.70mm	0.264"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

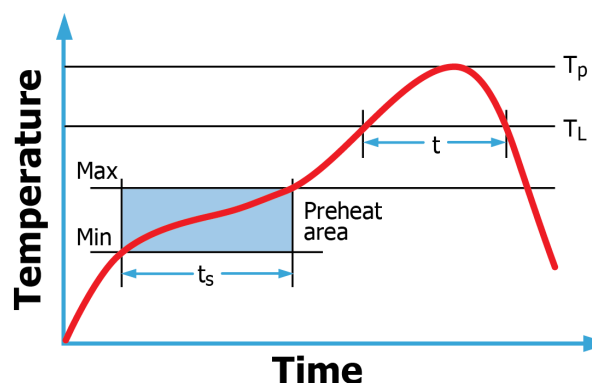
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness $> 1.0\text{mm}$. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Complex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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