

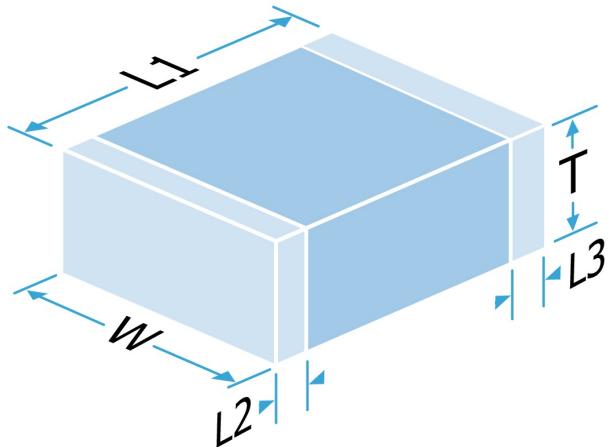


Multilayer Ceramic Chip Capacitor

Part Number: 3640J5000470GAR

Description: 3640 500Vdc 47pF $\pm 2\%$ C0G/NP0 (1B) to AEC-Q200

A range of C0G MLC capacitors fully tested and approved to automotive specification AEC-Q200. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.



Mechanical Specification

Size Code	3640
Length (L1) in mm (")	9.2 ± 0.50 (0.36 ± 0.02)
Width (W) in mm (")	10.16 ± 0.50 (0.40 ± 0.02)
Thickness (T) in mm (")	2.5 Max (0.1 Max)
Minimum Termination Band (L2,L3) in mm (")	0.50 (0.020)
Maximum Termination Band (L2,L3) in mm (")	1.50 (0.060)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	13" Reel, 500 per reel
Conformal Coating	Not normally required

General Electrical Specification

Rated Voltage	500Vdc
Nominal Capacitance Value	47pF
Capacitance Tolerance	$\pm 2\%$
Tangent of Loss Angle (Tan δ)	≤ 0.00153
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof	750Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (1B) to AEC-Q200
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0 ± 30 ppm/°C
Climatic Category (IEC)	Rated DC Voltage -
Ageing Characteristic	55/125/56
	Zero

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at <http://www.knowlescapacitors.com> or by contacting us.

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Date: Monday, July 21, 2025

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Multilayer Ceramic Chip Capacitor

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Description: 3640 500Vdc 47pF $\pm 2\%$ C0G/NP0 (1B) to AEC-Q200

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

247 compliant

California Proposition 65

No exposure risk

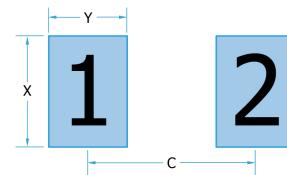
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

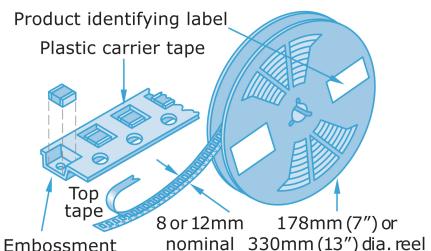
IPC-7351 pad design

3640		
C	8.40mm	0.331"
Y	2.05mm	0.081"
X	10.65mm	0.419"



Packaging

Tape packaging information for tape-and-reel parts:



Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.

Soldering

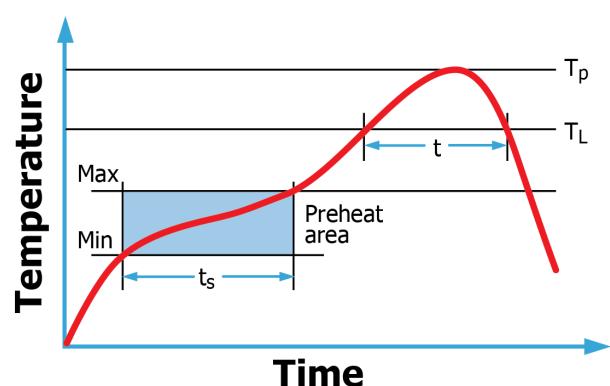
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Compex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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