

# Multilayer Ceramic Chip Capacitor

**Part Number:** 1206J6300473KXT

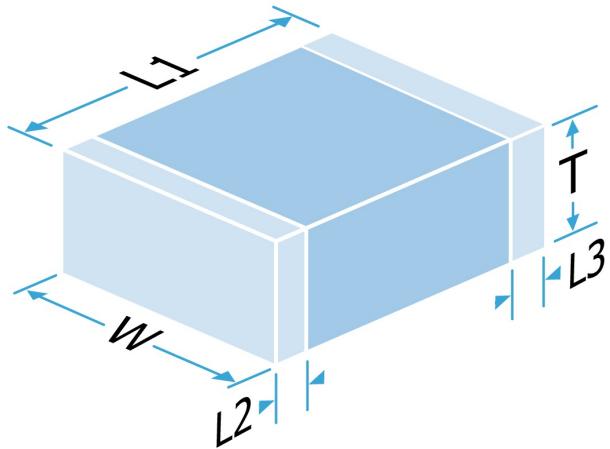
**Description:** 1206 630Vdc 47nF  $\pm 10\%$  X7R (2R1) (CTI  $\geq 600$ )

A range of X7R MLC capacitors to suit a variety of applications. In a wide selection of chip sizes, rated voltages and terminations, including FlexiCap™, the world's first commercially available flexible termination.

WS2, WR2, WS3 and WR3 parts use StackiCap™ patented construction technology.

DR1, WR2 and WR3 parts have a voltage de-rating above 105°C.

Suffix code PXX or PX mandates the use of precious metal electrode (PME) materials. This may incur additional costs.



## Mechanical Specification

Size Code	1206
Length (L1) in mm (")	3.2 $\pm 0.20$ (0.126 $\pm 0.008$ )
Width (W) in mm (")	1.6 $\pm 0.20$ (0.063 $\pm 0.008$ )
Thickness (T) in mm (")	1.7 Max (0.068 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	0.75 (0.030)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 2500 per reel
Conformal Coating	Not normally required

## General Electrical Specification

Rated Voltage	630Vdc
Nominal Capacitance Value	47nF
Capacitance Tolerance	$\pm 10\%$
Tangent of Loss Angle (Tan $\delta$ )	$\leq 0.025$
Capacitance and Tan $\delta$ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof	945Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	21.28GOhm @ 100Vdc
Min Insulation Resistance (IR)	X7R (2R1) (CTI $\geq 600$ )
Dielectric Classification	-55°C / +125°C
Rated Temperature Range	No DC Voltage $\pm 15\%$
Maximum Capacitance Change over Temperature Range	Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	<2% per decade (nominal capacitance is 1000 hour value)

## Knowles Precision Devices - Sales

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Date: Sunday, July 20, 2025

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## Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

247 compliant

California Proposition 65

No exposure risk

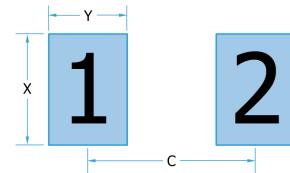
## Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

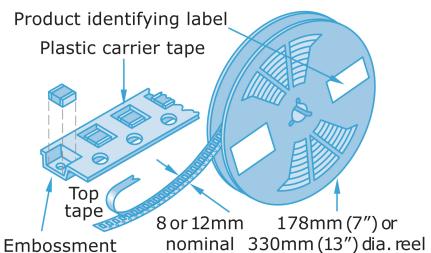
IPC-7351 pad design

1206		
C	3.00mm	0.118"
Y	1.15mm	0.045"
X	1.80mm	0.071"



## Packaging

Tape packaging information for tape-and-reel parts:



Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.

## Soldering

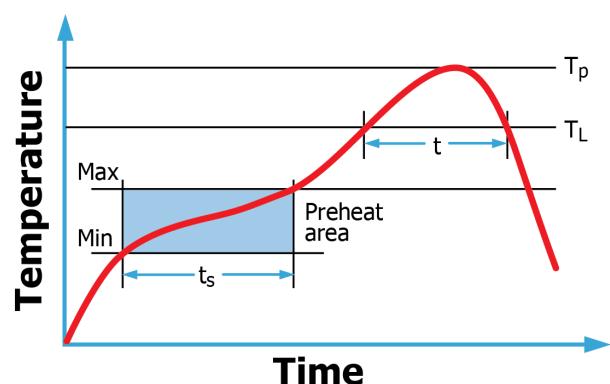
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness  $>1.0\text{mm}$ . Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



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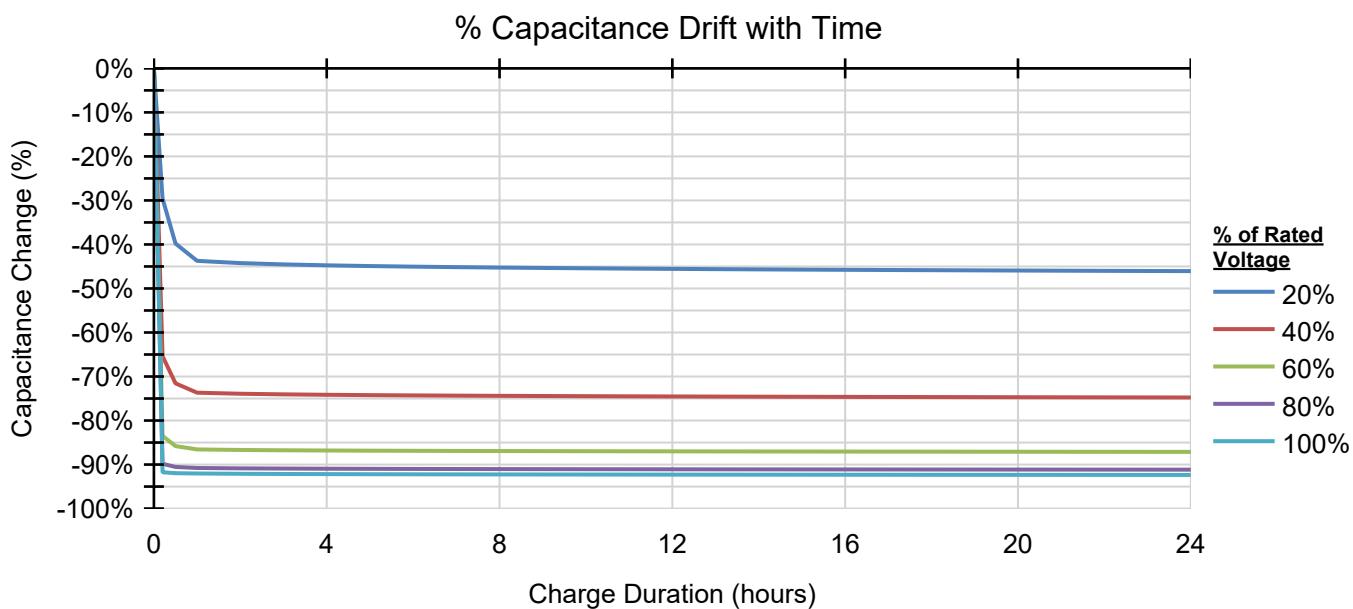
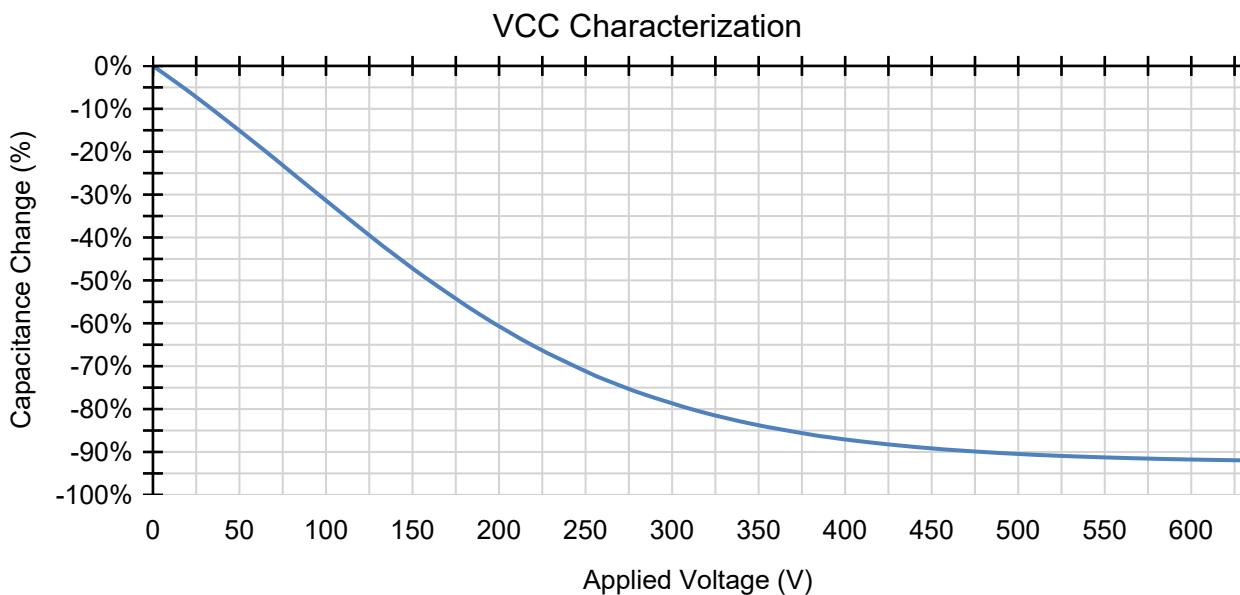


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## DC Bias Characteristics



The curves represent the 'typical worst case' curve – i.e. the typical curve of a 'worst case' component having the most capacitance loss delivered against the specification.

Knowles Precision Devices reserve the right to substitute any component with a similar component of the same or higher specification. In some cases this may mean that the capacitance drop with applied voltage is, in practice, less than the curve shown

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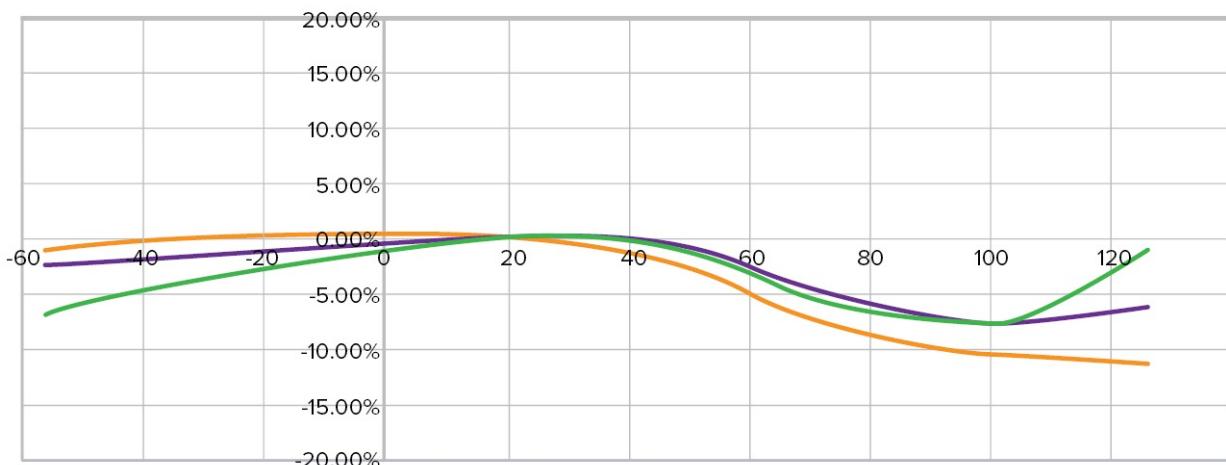
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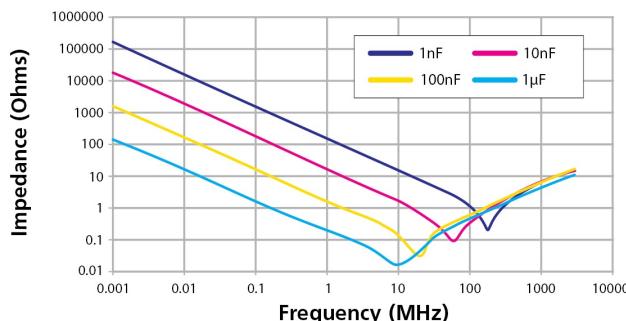
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## Typical Capacitance Change vs Temperature

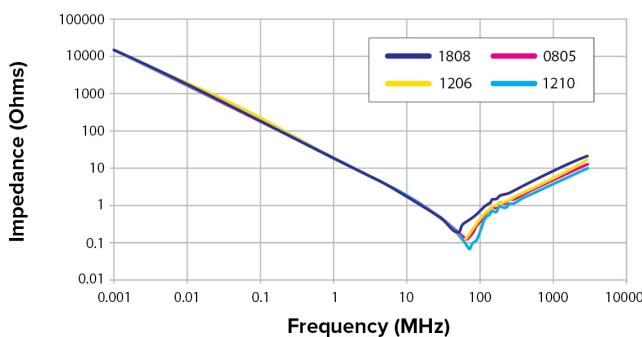


Typical TC Curves for X7R capacitors showing different dielectric types

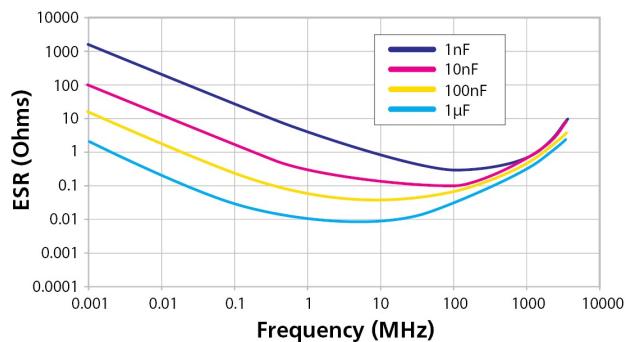
### Stable X7R Dielectric



### Stable X7R Dielectric — 10nF



### Stable X7R Dielectric



Typical Performance Data - X7R

For part specific data, please contact your local sales office

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