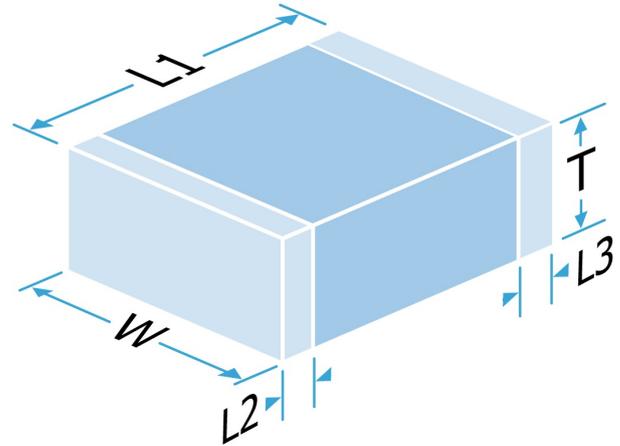


# Multilayer Ceramic Chip Capacitor

**Part Number:** 0805J5005P60DGTH20

**Description:** 0805 500Vdc 5.6pF  $\pm 0.50$ pF C0G/NP0 (200°C) (CTI  $\geq 600$ )

A range of MLC capacitors with defined capacitance variation and rated for reliable operation at temperatures up to +200°C. These components suit a variety of applications where increased temperature operation is required. Available 100% lead free RoHS compliant.



## Mechanical Specification

Size Code	0805
Length (L1) in mm (")	2.0 $\pm$ 0.20 (0.079 $\pm$ 0.008)
Width (W) in mm (")	1.25 $\pm$ 0.20 (0.049 $\pm$ 0.008)
Thickness (T) in mm (")	1.3 Max (0.051 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	0.75 (0.030)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 3000 per reel

## General Electrical Specification

Rated Voltage	500Vdc
Nominal Capacitance Value	5.6pF
Capacitance Tolerance	$\pm 0.50$ pF
Tangent of Loss Angle (Tan $\delta$ )	$\leq 0.00507$
Capacitance and Tan $\delta$ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof	750Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (200°C) (CTI $\geq 600$ )
Rated Temperature Range	-55°C / +200°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0 $\pm$ 30ppm/°C to 125°C (Typ 33ppm/°C at 200°C) Rated DC Voltage -
Climatic Category (IEC)	-
Ageing Characteristic	Zero

### Knowles Precision Devices - Sales

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Date: Sunday, July 20, 2025

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# Multilayer Ceramic Chip Capacitor

**Part Number:** 0805J5005P60DGTH20

**Description:** 0805 500Vdc 5.6pF  $\pm 0.50\text{pF}$  COG/NP0 (200°C) (CTI  $\geq 600$ )

## Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	247 compliant
California Proposition 65	No exposure risk

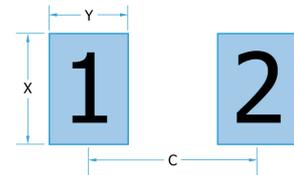
## Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

### IPC-7351 pad design

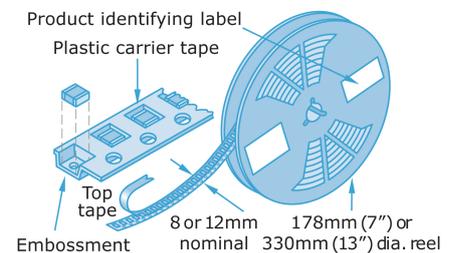
	0805	
C	1.80mm	0.071"
Y	1.15mm	0.045"
X	1.45mm	0.057"



## Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



## Soldering

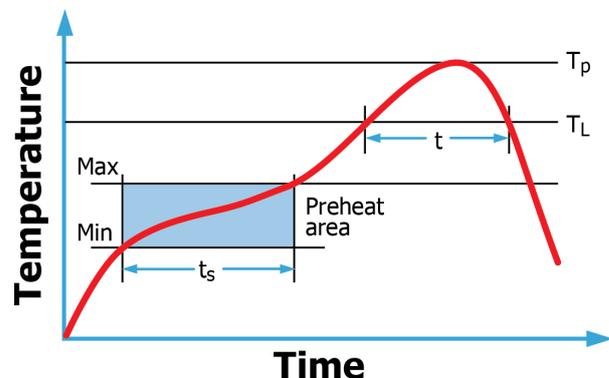
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness  $>1.0\text{mm}$ . Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Compex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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