UFS Memory

MTFC128GBCAVTC-AAT, MTFC128GBCAVTC-AIT, MTFC256GBCAVTC-AAT, MTFC256GBCAVTC-AIT

Features

- Universal flash storage (UFS) controller and NAND flash
- V_{CC}: 2.4–2.7V; 2.7–3.6V
- V_{CCQ}: 1.14 –1.26V
- JEDEC/UFS specification version 3.1-compliant[1]
  - Advanced 6-signal interface
  - Differential I/O pins
  - 2 lanes supported
  - High speed: Gear 1/2/3/4 supported
  - Permanent and power-on write protection
  - Boot operation (high-speed boot)
  - Sleep mode
  - Replay-protected memory block (RPMB)
  - Background operation
  - Reliable write
  - Discard/erase
  - Command queuing
  - FFU
  - Cache
- Production state awareness
- HPB
- Write booster
- REFRESH operation
- Temperature event notification
- Performance throttling notification
- Package compliance:
  - RoHS certification
  - BGA

Options	Marking
• Density	
– 128GB	128G
– 256GB	256G
• NAND component	
– 512Gb	BC
• Controller	AV
• Packages	
– 153-ball LFBGA JEDEC UFS Ball Assignment 2	TC
• Automotive and Functional Safety	A[3, 4]
– AEC-Q104	
– PPAP	
– FMEDA (ISO 26262-5:2018, cl. 8, 9)	
– Safety Application Note	
• Operating and storage temperature ranges[2]	
– From –40°C to +95°C	IT
– From –40°C to +115°C	AT

Notes: 1. The JEDEC specification is available at http://www.jedec.org/standards-documents/focus/flash/universal-flash-storage-ufs
2. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.
3. For functional safety documentation contact your Micron sales representative.
4. Automotive SPICE, contact your Micron sales representative

Part Numbering Information

Micron® UFS memory devices are available in different configurations and densities.

Figure 1: UFS Part Numbering

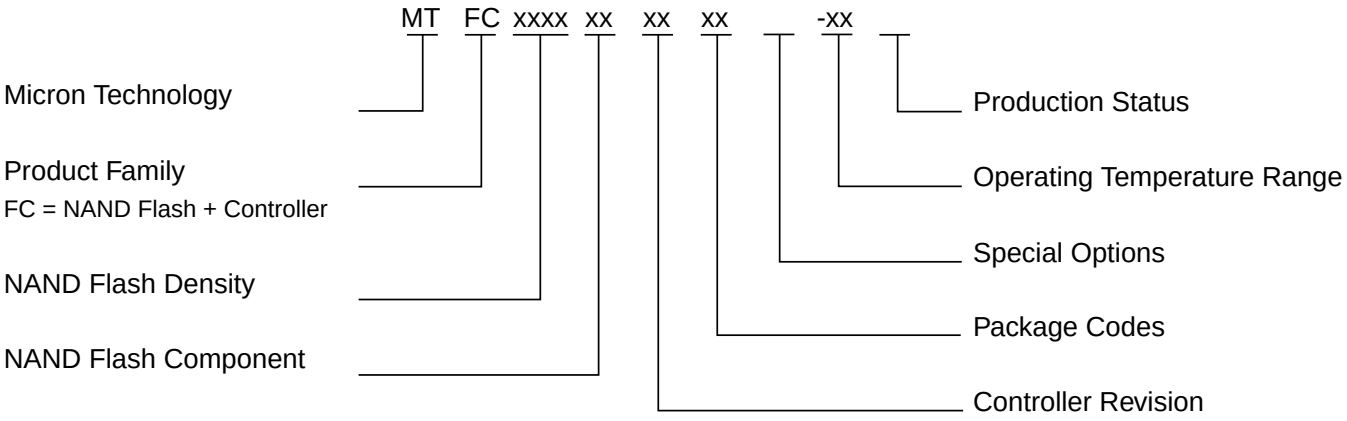

Table 1: Ordering Information

Base Part Number	Density	Package	Notes
MTFC128GBCAVTC-AIT, MTFC128GBCAVTC-AAT	128GB	153-ball LFBGA - JEDEC UFS Ball Assignment 2 11.5mm × 13mm × 1.3mm	1, 2
MTFC256GBCAVTC-AIT, MTFC256GBCAVTC-AAT	256GB	153-ball LFBGA - JEDEC UFS Ball Assignment 2 11.5mm × 13mm × 1.3mm	1, 2

Notes: 1. All the above MPNs can be ordered in the shipping form of tray and tape and reel.
2. Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.

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Functional Safety Notes

This automotive UFS product family has been developed under an IATF 16949-compliant Quality Management System (QMS) to provide a level of systematic fault coverage as per ISO 26262 QM definition. Additional support may be available to customers who need to integrate Micron's products in their functional safety-related applications. This support may include Safety Analysis Report, reporting FMEDA results and metrics, Safety Application Note and Pin FMEA Report, providing guidelines and instructions for using Micron products in safety-related applications. Contact a Micron sales representative to initiate the process required to obtain the functional safety documentation.

General Description

Micron universal flash storage (UFS) is a communication and mass data storage device that includes an M-PHY interface, one or more NAND Flash components, and a controller on an advanced 6-signal bus, which is compliant with the UFS system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for automotive applications, including information and entertainment, navigation tools, advanced driving assistance systems, and a variety of other industrial and portable products.

Performance/Current Consumption – Product Revision Level 010x

Table 2: Performance

Condition[1]		Typical Values		Unit
		128GB	256GB	
Sequential	Write	450	810	MB/s
	Read	1900	2000	MB/s
Random	Write	75,000	100,000	IOPS
	Read	170,000	205,000	IOPS

Note: 1. Two lanes, high-speed mode gear 4; sequential access of 512KB chunk; random access of 4KB chunk; command queue depth = 32, write booster enabled, burst performance, room temperature. Performance is temperature dependent and subject to thermal throttling for current consumption as shown in the Active Current Consumption table. Stable performance requires disabling thermal throttling and extended current consumption capability.

Additional performance data, such as sustained and system performance on a specific application board, will be provided in a separate document upon customer request.

Table 3: Active Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})[1, 3]		Peak Values (I_{CC}/I_{CCQ})[2, 3]		Unit
	128GB	256GB	128GB	256GB	
Write	120/530	210/540	800/1000	800/1000	mA
Read	140/740	150/740	800/1000	800/1000	mA

Notes: 1. Two lanes, high-speed mode gear 4; V_{CC} = 2.5V; V_{CCQ} = 1.2V; T_{OPER} = 25°C; Measurements done as average RMS current consumption.
2. Measurement bandwidth of 1 MHz. Thermal throttling is enabled by default, but extended current consumption capability is required to keep performance stable, for which thermal throttling must be disabled.
3. Refer to electrical addendum for additional measurements results and conditions. Refer to Power Parameter descriptor for maximum current value in line to JEDEC specification.

Table 4: Low-Power Mode

Condition[1,2]	Typical Values (I_{CC}/I_{CCQ})		Maximum Values (I_{CC}/I_{CCQ})		Unit
	128GB	256GB	128GB	256GB	
Sleep	25/440	45/440	35/550	75/550	µA
Idle	25/440	45/440	35/550	75/550	µA

Notes: 1. Two lanes, low-speed mode PWM gear 4, M-PHY in Hibernate; V_{CC} = 2.5V; V_{CCQ} = 1.2V; T_{OPER} = 25°C.
2. Refer to electrical addendum for additional measurements results and conditions.

Performance/Current Consumption – Product Revision Level 030x

Engineering samples may have a PRL equal to 000x.

Table 5: Performance

Condition[1]		Typical Values				Unit
		128GB		256GB		
		AIT	AAT	AIT	AAT	
Sequential	Write	500	510	900	950	MB/s
	Read	1700	2000	1750	2000	MB/s
Random	Write	85,000	90,000	110,000	125,000	IOPS
	Read	165,000	170,000	190,000	200,000	IOPS

Note: 1. Two lanes, high-speed mode gear 4; sequential access of 512KB chunk; random access of 4KB chunk; command queue depth = 32, write booster enabled, burst performance. Higher performance is achieveable, and it requires extended current consumption capability with respect to the Active Current Consumption table.

Additional performance data, such as sustained and system performance on a specific application board, will be provided in a separate document upon customer request.

Table 6: Active Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})[1, 3]				Peak Values (I_{CC}/I_{CCQ})[2, 3]				Unit
	128GB		256GB		128GB		256GB		
	AIT	AAT	AIT	AAT	AIT	AAT	AIT	AAT	
Write	115/485	115/530	220/475	220/515	800 / 1000	800 / 1200	800 / 1000	800 / 1200	mA
Read	125/700	125/735	130/670	130/710	800 / 1000	800 / 1200	800 / 1000	800 / 1200	mA

Notes: 1. Two lanes, high-speed mode gear 4; V_{CC} = 2.5V; V_{CCQ} = 1.2V; T_{OPER} = 25°C; Measurements done as average RMS current consumption.
2. Measurement bandwidth of 1 MHz. A host may choose a different power profile with related performance and current consumption.
3. Refer to electrical addendum for additional measurements results and conditions. Refer to Power Parameter descriptor for maximum current value in line to JEDEC specification.

Table 7: Low-Power Mode

Condition[1, 2]	Typical Values (I_{CC}/I_{CCQ})		Maximum Values (I_{CC}/I_{CCQ})		Unit
	128GB	256GB	128GB	256GB	
Sleep	25/440	45/440	35/550	75/550	µA
Idle	25/440	45/440	35/550	75/550	µA

Notes: 1. Two lanes, low-speed mode PWM gear 4, M-PHY in Hibernate; V_{CC} = 2.5V; V_{CCQ} = 1.2V; T_{OPER} = 25°C.
2. Refer to electrical addendum for additional measurements results and conditions.

Signal Descriptions

Table 8: Signal Descriptions

Symbol	Type	Description
REF_CLK	Input	Reference clock: When not active, this signal should be pull-down or driven low by the host SoC.
RST_n	Input	Hardware reset signal
D_{IN0}_t, D_{IN0}_c	Input	Downstream data lane 0: Differential input signals into UFS device from the host
D_{IN1}_t, D_{IN1}_c	Input	Downstream data lane 1: Differential input signals into UFS device from the host
D_{OUT0}_t, D_{OUT0}_c	Output	Upstream data lane 0: Differential output signals from the UFS device to the host
D_{OUT1}_t, D_{OUT1}_c	Output	Upstream data lane 1: Differential output signals from the UFS device to the host
VSF[9:1]	Input/ Output	Vendor specific function: VSF[9:1] must be left floating
VDDi	Input	Input terminal to provide bypass capacitor for internal regulator related to the NAND memory device
VDDiQ	Input	Input terminal to provide bypass capacitor for internal regulator related to the memory controller (core)
VDDiQ2	Input	Input terminal to provide bypass capacitor for internal regulator related to the memory controller (interface)
V_{CC}	Supply	Supply voltage for the NAND memory device
V_{CCQ}	Supply	Supply voltage used for the memory controller and the M-PHY interface
V_{SS}	Supply	Ground
NC	–	No connect: NC pins must be connected to ground or left floating.
RFU	–	Reserved for future use: RFU pins must be left floating.

Signal Assignments

Figure 2: 153-ball LFBGA – JEDEC UFS Ball Assignment 2 (Top View, Ball Down)

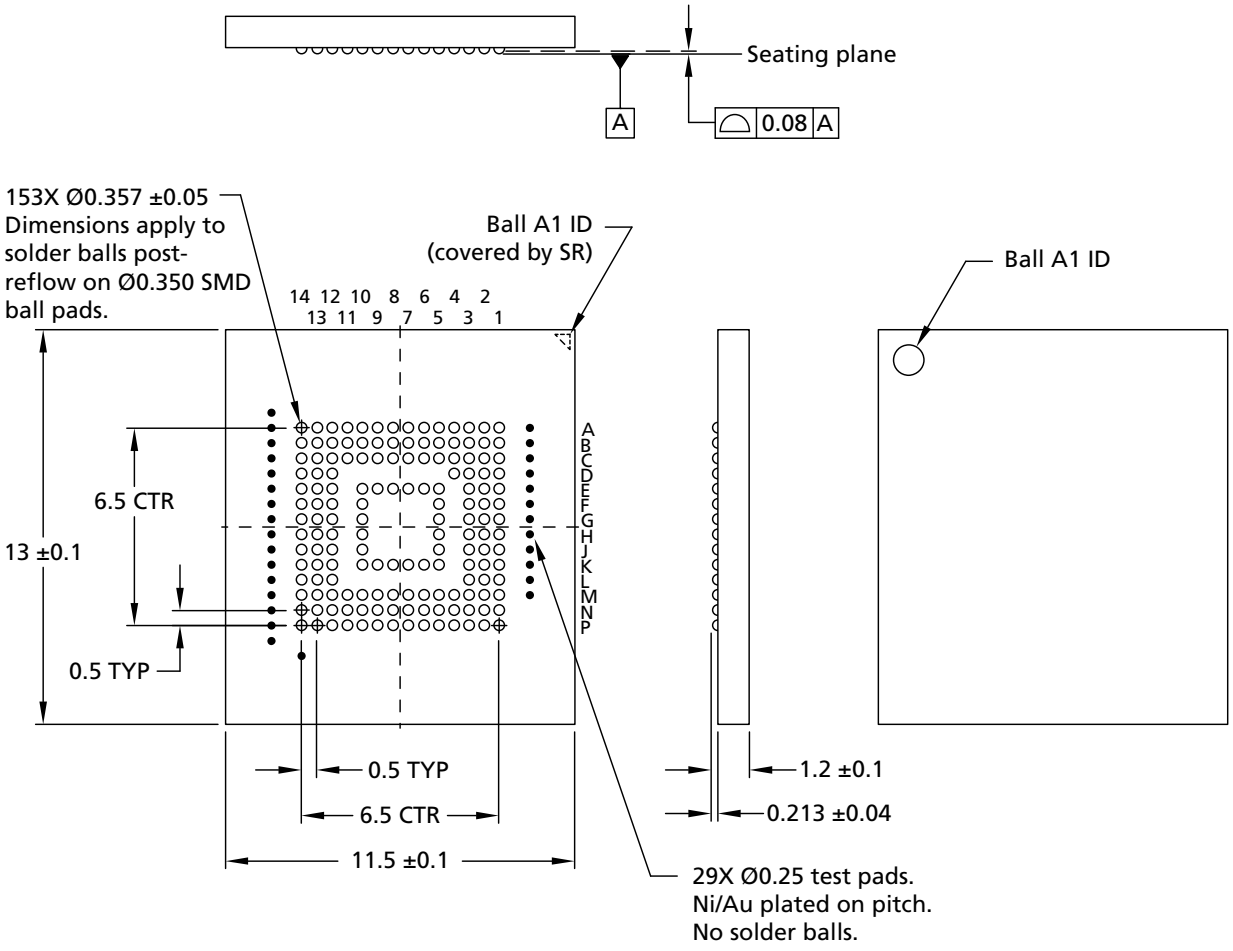
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNC	DNC	VDDiQ	V_{CCQ}	V_{CCQ}	NC	NC	VDDiQ2	VDDi	NC	NC	NC	DNC	DNC	A
B	DNC	V_{SS}	RFU	V_{CCQ}	V_{CCQ}	NC	NC	V_{CC}	V_{CC}	NC	V_{SS}	V_{SS}	RFU	DNC	B
C	NC	V_{SS}	V_{SS}	V_{CCQ}	V_{CCQ}	NC	NC	V_{CC}	V_{CC}	RFU	V_{SS}	V_{SS}	RFU	RFU	C
D	$D_{IN1\_}t$	$D_{IN1\_}c$	V_{SS}	NC								V_{SS}	V_{SS}	V_{SS}	D
E	NC	V_{SS}	V_{SS}		V_{CCQ}	VSF1	VSF2	V_{CC}	VSF3	VSF4		V_{SS}	RFU	RFU	E
F	$D_{IN0\_}t$	$D_{IN0\_}c$	V_{SS}		V_{CCQ}					VSF5		V_{SS}	V_{SS}	V_{SS}	F
G	NC	V_{SS}	V_{SS}		VSF6					V_{SS}		V_{SS}	RFU	RFU	G
H	REF_ CLK	RST_n	V_{SS}		V_{SS}					V_{SS}		V_{SS}	V_{SS}	V_{SS}	H
J	NC	V_{SS}	V_{SS}		V_{SS}					VSF7		V_{SS}	RFU	RFU	J
K	$D_{OUT0\_}c$	$D_{OUT0\_}t$	V_{SS}		V_{SS}	NC	NC	V_{CC}	NC	VSF8		V_{SS}	V_{SS}	V_{SS}	K
L	NC	V_{SS}	V_{SS}									V_{SS}	RFU	RFU	L
M	$D_{OUT1\_}c$	$D_{OUT1\_}t$	V_{SS}	V_{SS}	V_{SS}	RFU	RFU	NC	NC	RFU	NC	V_{SS}	V_{SS}	V_{SS}	M
N	DNC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	RFU	RFU	V_{CC}	V_{CC}	RFU	V_{SS}	V_{SS}	RFU	DNC	N
P	DNC	DNC	RFU	V_{SS}	V_{SS}	RFU	RFU	V_{CC}	V_{CC}	VSF9	V_{SS}	V_{SS}	DNC	DNC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top View (ball down)

Notes: 1. The following balls are not connected in this product family, although specified by JEDEC Standard No. 21-C: A[7:6],B[7:6], C[7:6], and K[7:6].
2. The corner pins (A1, A2, B1; A13, A14, B14; N1, P1, P2; and N14, P13, P14) are internally connected. Do not route through these pins.

Package Dimensions

Figure 3: 153-Ball LFBGA – 11.5mm × 13.0mm × 1.3mm (Package Code: TC)



Notes: 1. Dimensions are in millimeters.
2. For optimal Solder Joint Reliability (SJR) performance refer to CSN33 for recommended PCB pad dimension to align to the SMD ball pad size of the package.
3. In the entire UFS package area, solder mask is recommended to cover the via pad in the PCB to avoid possible contact with Ni/Au plated test pads on the UFS package. The Ni/Au plated test pads are reserved for Micron internal use only.
4. Solder ball composition: SACQ with CuOSP pads (Sn, 4.0% Ag, 0.5% Cu, 3% Bi, 0.05% Ni).

Architecture

Figure 4: UFS Functional Block Diagram

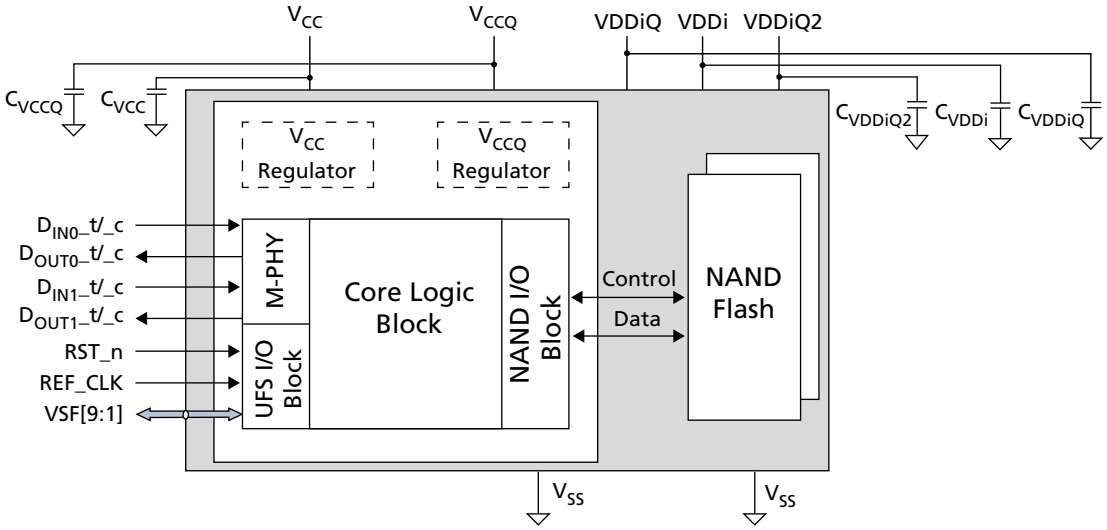


Table 9: Recommended Capacitor Values[1]

Parameters	Symbol	Min	Typ	Max	Unit
V_{CC} capacitor	C_{VCC}	4.7	10.0	–	µF
			0.1		
V_{CCQ} capacitor	C_{VCCQ}	4.7	10.0	–	µF
			0.1		
VDDi capacitor	C_{VDDi}	0	2.2	–	µF
VDDiQ capacitor	C_{VDDiQ}	0	2.2	–	µF
VDDiQ2 capacitor	C_{VDDiQ2}	0	2.2	–	µF

Note: 1. VDDi, VDDiQ and VDDiQ2 capacitors are optional.

UFS M-PHY Attributes

Micron device supports 2 lanes configuration.

Table 10: PHY M-TX Capability Attributes

Name	ID	Value Lane 0 Lane 1	Type	Notes
TX_HSMODE_Capability	01h	01h	R	FALSE = 0, TRUE = 1
TX_HSGEAR_Capability	02h	04h	R	HS_G1_TO_G4 = 4
TX_PWMG0_Capability	03h	00h	R	0 = NO, 1 = YES
TX_PWMGEAR_Capability	04h	04h	R	Range from PWM_G1 to PWM_G7
TX_Amplitude_Capability	05h	02h	R	SA = 1, LA = 2, BOTH = 3
TX_ExternalSYNC_Capability	06h	00h	R	FALSE = 0, TRUE = 1
TX_HS_Unterminated_LINE_Drive_Capability	07h	00h	R	0 = N0, 1 = YES
TX_LS_Terminated_LINE_Drive_Capability	08h	00h	R	0 = N0, 1 = YES
TX_Min_SLEEP_NoConfig_Time_Capability	09h	0Fh	R	1 to 15
TX_Min_STALL_NoConfig_Time_Capability	0Ah	FFh	R	1 to 255
TX_Min_SAVE_Config_Time_Capability	0Bh	FAh	R	1 to 250
TX_REF_CLOCK_SHARED_Capability	0Ch	01h	R	0 = N0, 1 = YES
TX_PHY_MajorMinor_Release_Capability	0Dh	41h	R	Bit[7:4]: Major version number Bit[3:0]: Minor version number
TX_PHY_Editorial_Release_Capability	0Eh	01h	R	Bit[7:0] = 1 to 99
TX_Hibern8Time_Capability	0Fh	01h	R/W	1 to 128
TX_Advanced_Granularity_Capability	10h	00h	R/W	Bit[2:1]: Step size Bit[0]: Supports fine granularity steps
TX_Advanced_Hibern8Time_Capability	11h	01h	R/W	1 to 128
TX_HS_Equalizer_Setting_Capability	12h	03h	R	Bit[1:0]

Table 11: PHY M-RX Capability Attributes

Name	ID	Value Lane 0 Lane 1	Type	Notes
RX_HSMODE_Capability	81h	01h	R	0 = NO, 1 = YES
RX_HSGEAR_Capability	82h	04h	R	HS_G1_TO_G4 = 4
RX_PWMG0_Capability	83h	00h	R	0 = NO, 1 = YES
RX_PWMGEAR_Capability	84h	04h	R	Range from PWM_G1 to PWM_G7
RX_HS_Unterminated_LINE_Drive_Capability	85h	00h	R	0 = NO, 1 = YES
RX_LS_Terminated_LINE_Drive_Capability	86h	00h	R	0 = NO, 1 = YES
RX_Min_SLEEP_NoConfig_Time_Capability	87h	0Fh	R	1–15
RX_Min_STALL_NoConfig_Time_Capability	88h	FFh	R	1–255
RX_Min_SAVE_Config_Time_Capability	89h	FAh	R	1–250
RX_REF_CLOCK_SHARED_Capability	8Ah	01h	R/W	0 = NO, 1 = YES

Table 11: PHY M-RX Capability Attributes (Continued)

Name	ID	Value Lane 0 Lane 1	Type	Notes
RX_HS_G1_SYNC_LENGTH_Capability	8Bh	48h	R/W	Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE
RX_HS_G1_PREPARE_LENGTH_Capability	8Ch	0Fh	R	0–15
RX_LS_PREPARE_LENGTH_Capability	8Dh	0Ah	R	0–15
RX_PWM_Burst_Closure_Length_Capability	8Eh	1Fh	R/W	0–31
RX_Min_ActivateTime_Capability	8Fh	05h	R/W	1–9
RX_PHY_MajorMinor_Release_Capability	90h	41h	R	Bit[7:4]: Major version number Bit[3:0]: Minor version number
RX_PHY_Editorial_Release_Capability	91h	01h	R	1–99
RX_Hibern8Time_Capability	92h	03h	R/W	1–128
RX_PWM_G6_G7_SYNC_LENGTH_Capability	93h	00h	R/W	Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 0 to 15
RX_HS_G2_SYNC_LENGTH_Capability	94h	48h	R/W	Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE
RX_HS_G3_SYNC_LENGTH_Capability	95h	48h	R/W	Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE
RX_HS_G2_PREPARE_LENGTH_Capability	96h	0Fh	R/W	Bit[3:0]: 0 to 15
RX_HS_G3_PREPARE_LENGTH_Capability	97h	0Fh	R/W	Bit[3:0]: 0 to 15
RX_Advanced_Granularity_Capability	98h	00h	R/W	Bit[2:1]: Step size Bit[0]: Supports fine granularity steps
RX_Advanced_Hibern8Time_Capability	99h	01h	R/W	1–128
RX_Advanced_Min_ActivateTime_Capability	9Ah	01h	R/W	Bit[3:0]: 1–14
RX_HS_G4_SYNC_LENGTH_Capability	9Bh	48h	R/W	Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE
RX_HS_G4_PREPARE_LENGTH_Capability	9Ch	0Fh	R/W	Bit[3:0]: 0–15
RX_HS_Equalizer_Setting_Capability	9Dh	01h	R/W	Bit[0] =0: No equalization Bit[0] =1: Yes equalization
RX_HS_ADAPT_LENGTH_FINE_Capability	9Eh	8Fh	R/W	Bit[6:0]: 0 to 127
RX_HS_ADAPT_LENGTH_COARSE_Capability	9Fh	8Fh	R/W	Bit[6:0]: 0 to 17

UPIU Transaction Codes

Micron devices support the following UPIU transaction codes. For detailed information, refer to JEDEC UFS 3.1 specification.

Table 12: UPIU Transaction Codes

Initiator to Target	Transaction Code	Target to Initiator	Transaction Code
NOP OUT	00h	NOP IN	20h
COMMAND	01h	RESPONSE	21h
DATA OUT	02h	DATA IN	22h
TASK MANAGEMENT REQUEST	04h	TASK MANAGEMENT RESPONSE	24h
Reserved	11h	READY TO TRANSFER	31h
QUERY REQUEST	16h	QUERY RESPONSE	36h

UFS Descriptors

Descriptors are blocks or pages of parameters that describe something about the device. Descriptors are classified into types: device descriptors, configuration descriptors, unit descriptors, and so forth. Micron devices support the following UFS descriptors. For detailed information, refer to the JEDEC UFS specification.

Table 13: Descriptor Identification Values

Descriptor Type	Descriptor IDN
Device	00h
Configuration	01h
Unit	02h
Reserved	03h
Interconnect	04h
String	05h
Reserved	06h
Geometry	07h
Power	08h
Reserved	09h...FFh

Table 14: Configuration Descriptor

Offset	Size	Name	Default Value	Description
00h	1	bLength	E6h	Size of this descriptor
01h	1	bDescriptorIDN	01h	Configuration descriptor type identifier
02h	1	bConfDescContinue	00h	00h: This value indicates that this is the last configuration descriptor in a sequence of write descriptor query requests. Device shall perform internal configuration based on received configuration descriptor(s). 01h: This value indicates that this is not the last configuration descriptor in a sequence of write descriptor query requests. Other configuration descriptors will be sent by host. Therefore, the device should not perform the internal configuration yet.
03h	1	bBootEnable	00h	Enables to boot feature.
04h	1	bDescrAccessEn	00h	Enables access to the device descriptor after the partial initialization phase of the boot sequence.
05h	1	bInitPowerMode	01h	Configures the power mode after device initialization or hardware reset.
06h	1	bHighPriorityLUN	7Fh	Configures the high priority logical unit.
07h	1	bSecureRemovalType	00h	Configures the secure removal type.
08h	1	bInitActiveICCLevel	00h	Configures the I_{CC} level in active mode after device initialization or hardware reset.
09h	2	wPeriodicRTCUpdate	00h	Frequency and method of real-time clock update (see Device Descriptor).
0Bh	1	bHPBControl	01h	HPB Control Mode Configures the Control Mode of HPB

Table 14: Configuration Descriptor (Continued)

Offset	Size	Name	Default Value	Description
0Ch	1	bRPMBRegionEnable	00h	RPMB Region Enable Configures which RPMB regions are enabled in RPMB well-known logical unit
0Dh	1	bRPMBRegion1Size	00h	RPMB Region 1 Size Configures the size of RPMB region 1 if RPMB region 1 is enabled
0Eh	1	bRPMBRegion2Size	00h	RPMB Region 2 Size Configures the size of RPMB region 2 if RPMB region 2 is enabled
0Fh	1	bRPMBRegion3Size	00h	RPMB Region 3 Size Configures the size of RPMB region 3 if RPMB region 3 is enabled
10h	1	bWriteBoosterBufferNo UserSpaceReductionEn	00h	Enables the User Space reduction when Write Booster Buffer is configured
11h	1	bWriteBoosterBufferType	00h	Configures the Write Booster Buffer type
12h	4	dNumSharedWrite BoosterBufferAllocUnits	00h	Configures the Write Booster Buffer size for a shared Write Booster Buffer configuration

Table 15: Device Descriptor

Offset	Size	Name	Default Value	Description
00h	1	bLength	59h	Size of this descriptor
01h	1	bDescriptorIDN	00h	Device descriptor type identifier
02h	1	bDevice	00h	Device type: 00h Others: Reserved
03h	1	bDeviceClass	00h	UFS device class: Mass storage: 00h
04h	1	bDeviceSubClass	00h	UFS mass storage subclass: Bits (0/1) specify as follows: Bit 0: Bootable/non-bootable Bit 1: Embedded/removable Bit 2: Reserved (for unified memory extension specification) Others: Reserved
05h	1	bProtocol	00h	Protocol supported by UFS device: SCSI: 00h
06h	1	bNumberLU	00h	Number of logical units (user configurable): bNumberLU does not include well known logical units
07h	1	bNumberWLU	04h	Number of well-known logical units
08h	1	bBootEnable	00h	Boot enable indicates whether the device is enabled for boot (user configurable): 00h: Boot feature disabled 01h: Bootable feature enabled
09h	1	bDescrAccessEN	00h	Descriptor access enable indicates whether the device descriptor can be read after the partial initialization phase of the boot sequence (user configurable): 00h: Device descriptor access disabled 01h: Device descriptor access enabled

Table 15: Device Descriptor (Continued)

Offset	Size	Name	Default Value	Description
0Ah	1	bInitPowerMode	01h	Initial power mode defines the power mode after device initialization or hardware reset (user configurable): 00h: UFS-sleep mode 01h: Active mode
0Bh	1	bHighPriorityLUN	7Fh	High priority LUN defines the high-priority logical unit (user configurable): Valid values are from 0 to the number of logical units specified by bMaxNumberLU, and 7Fh. If the value is 7Fh, all logical units have the same priority.
0Ch	1	bSecureRemovalType	00h	Secure removal type (user configurable): 00h: Information removed by an erase of the physical memory 01h: Information removed by overwriting the addressed locations with a single character followed by an erase 02h: Information removed by overwriting the addressed locations with a character, its complement, then a random character 03h: Information removed using a vendor define mechanism Others: Reserved
0Dh	1	bSecurityLU	01h	Support for security LU: 00h: Not supported 01h: RPMB Others: Reserved
0Eh	1	bBackgroundOpsTermLat	05h	Background operations termination latency defines the maximum latency for the termination of ongoing background operations. When the device receives a COMMAND UPIU with a transfer request, the device shall start the data transfer and send a DATA IN UPIU or an RTT UPIU within the latency declared in bBackgroundOpsTermLat. The latency is expressed in units of 10ms (for example, 01h = 10ms, FFh = 2550ms). The latency is undefined if the value of this parameter is 0.
0Fh	1	bInitActiveICCLevel	00h	Initial active I_{CC} level defines the bActiveICCLevel value after power-on or reset (user configurable): Valid range from 00h to 0Fh
10h	2	wSpecVersion	0310h	Specification version: Bits[15:8] = major version in BCD format Bits[7:4] = minor version in BCD format Bits[3:0] = version suffix in BCD format Example: 3.21 = 0321h
12h	2	wManufactureDate	–	Manufacturing date: BCD version of the device manufacturing date Example: August 2010 = 0810h
14h	1	iManufactureName	00h	Manufacturer name: Index to the string which contains the manufacturer name
15h	1	iProductName	01h	Product name: Index to the string which contains the product name

Table 15: Device Descriptor (Continued)

Offset	Size	Name	Default Value	Description
16h	1	iSerialNumber	02h	Serial number: Index to the string which contains the serial number
17h	1	iOEMID	03h	OEM ID: Index to the string which contains the OEM ID
18h	2	wManufactureID	12Ch	Manufacturer ID: Manufacturer ID as defined in JEDEC standard JEP106 "Standard Manufacturer's Identification Code"
1Ah	1	bUD0BaseOffset	16h	Unit descriptor 0 base offset
1Bh	1	bUDConfigPLength	1Ah	Unit descriptor configuration parameter length: Total size of the configurable unit descriptor parameters
1Ch	1	bDeviceRTTCap	02h	RTT capability of device: Maximum number of outstanding RTTs supported by device. The minimum value is 2.
1Dh	2	wPeriodicRTCUpdate	00h	Frequency and method of real-time clock update (user configurable): Bits[15:10]: Reserved Bit[9]: TIME_BASELINE 0h: Time elapsed from the previous dSecondsPassed update 1h: Absolute time elapsed from January 1st 2010 00:00 NOTE if the host device has a real-time clock, it should use TIME BASELINE = "1." If the host device has no real-time clock, it should use TIME BASELINE = "0." Bits[8:6]: TIME_UNIT 0h = Undefined 1h = Months 2h = Weeks 3h = Days 4h = Hours 5h = Minutes 6h = Reserved 7h = Reserved Bits[5:0]: TIME_PERIOD If TIME_UNIT is 0, TIME_PERIOD is ignored and the period between RTC update is not defined. All fields are configurable by the host.
1Fh	1	bUFSFeaturesSupport[2]	FFh	UFS features support: This field indicates which features are supported by the device. A feature is supported if the related bit is set to 1. Bit[0]: Field firmware update (FFU) Bit[1]: Production state awareness (PSA)[4] Bit[2]: Device life span Bit[3]: Refresh operation Bit[4]: TOO_HIGH_TEMPERATURE Bit[5]: TOO_LOW_TEMPERATURE Bit[6]: Extended Temperature Bit[7]: Host Performance Booster (HPB) Others: Reserved Bit 0 shall be set to 1

Table 15: Device Descriptor (Continued)

Offset	Size	Name		Default Value	Description
20h	1	bFFUTimeout		0Ah	Field firmware update timeout: The maximum time, in seconds, that access to the device is limited or not possible through any ports associated due to execution of a WRITE BUFFER command. A value of 0 indicates that no timeout is provided.
21h	1	bQueueDepth		20h	Queue depth: 0: The device implements the per-LU queuing architecture 1.. 255: The device implements the shared queuing architecture. This parameter indicates the depth of the shared queue. If bLUQueueDepth > 0 for any LU (except RPMB LU), then bQueueDepth shall be 0.
22h	2	wDeviceVersion		–	Device version: This field provides the device version.
24h	1	bNumSecureWPArea		20h	Number of secure write protect areas: This value specifies the total number of secure write protect areas supported by the device. The value shall be equal to or greater than bNumberLU and shall not exceed 32 (bNumberLU ≤ bNumSecureWPArea ≤ 32).
25h	4	dPSAMaxDataSize [3]	128 GB	PRL 010x: 9EED55h PRL 030x: 1AD1A6Ah	PSA maximum data size: This parameter specifies the maximum amount of data that may be written during the pre-soldering phase of the PSA flow. The value indicates the total amount of data for all logical units with bPSASensitive = 01h. Value expressed in units of 4KB.
			256GB	PRL 010x: 13DD2AAh PRL 030x: 35A1F35h	
29h	1	bPSAStateTimeout		14h	PSA state timeout: This parameter specifies the command maximum timeout for a change in bPSAState state. 00h means undefined. Otherwise, the formula to calculate the maximum timeout value is: Production state timeout = 100µs × 2^bPSAStateTimeout For example: 01h means 100µs × 2^1 = 200µs 02h means 100µs × 2^2 = 400µs 17h means 100µs × 2^23 = 838.86s
2Ah	1	iProductRevisionLevel		04h	Product revision level: Index to the string which contains the product revision level
2Bh:3Fh	20	Reserved		–	Reserved
40h	2	wHPBVersion		0200h	HPB Specification Version: Bits[15:8] = major version in BCD format Bits[7:4] = minor version in BCD format Bits[3:0] = version suffix in BCD format Example: 1.2.3 = 0123h

Table 15: Device Descriptor (Continued)

Offset	Size	Name	Default Value	Description
42h	1	bHPBControl	01h	HPB Control Mode: 00h: host control mode 01h: device control mode Others: reserved
43h:4Eh	11	Reserved	–	Reserved
4Fh	4	dExtendedUFS FeaturesSupport[2]	03FFh	Extended UFS Features Support: This field indicates which features are supported by the device. A feature is supported if the related bit is set to 1. Bit[0]: Field firmware update (FFU) Bit[1]: Production state awareness (PSA) [4] Bit[2]: Device life span Bit[3]: Refresh operation Bit[4]: TOO_HIGH_TEMPERATURE Bit[5]: TOO_LOW_TEMPERATURE Bit[6]: Extended Temperature Bit[7]: Host performance Booster (HPB) Bit[8]: Write Booster Bit[9]: Performance throttling Others: Reserved Bit 0 shall be set to 1
53h	1	bWriteBoosterBuffer NoUserSpaceReductionEn	00h	No User Space reduction mode 00h: User space shall be reduced if Write Booster Buffer is configured 01h: User space shall not be reduced if Write Booster Buffer is configured Others: Reserved
54h	1	bWriteBoosterBufferType	00h	Write Booster Buffer Type 00h: LU dedicated buffer type 01h: Single shared buffer type Others: Reserved
55h	4	dNumSharedWrite BoosterBufferAllocUnits	00h	The Write Booster Buffer size for the shared Write Booster Buffer configuration

Notes: 1. Some fields are user-configurable as they can be configured by the user writing the configuration descriptor.
2. The Device Life Span feature is supported as JEDEC interface only.
3. The reported values are referring to a fully provisioned device, with different values for different product revision level values.
4. For product revision level 010x, during Production State Awareness flow, programming operations are supported in 15-85°C temperature range. For product revision level 030x, during Production State Awareness flow, programming operations are supported in either 20-55°C or 15-85°C temperature range, based on programming size.

Table 16: Geometry Descriptor

Offset	Size	Name	Default Value	Description
00h	1	bLength	57h	Size of this descriptor
01h	1	bDescriptorIDN	07h	Geometry descriptor type identifier
02h	1	bMediaTechnology	00h	Reserved
03h	1	Reserved	00h	Reserved

Table 16: Geometry Descriptor (Continued)

Offset	Size	Name		Default Value	Description
04h	8	qTotalRawDevice Capacity	128GB	EE64000h	Total raw device capacity: Total memory quantity available to the user to configure the device logical units (RPMB excluded). It is expressed in unit of 512 bytes.
			256GB	1DCBC000h	
0Ch	1	bMaxNumberLU		01h	Maximum number of logical unit supported by the UFS device: 01h: 32 logical units
0Dh	4	dSegmentSize		2000h	Segment size: Value expressed in unit of 512 bytes
11h	1	bAllocationUnitSize		01h	Allocation unit size: Value expressed in number of segments. Each logical unit can be allocated as a multiple of allocation units.
12h	1	bMinAddrBlockSize		08h	Minimum addressable block size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB.
13h	1	bOptimalReadBlockSize		80h	Optimal read block size: Value expressed in unit of 512 bytes. This is optional parameter, 0 = not available.
14h	1	bOptimalWriteBlockSize		80h	Optimal write block size: Value expressed in unit of 512 bytes
15h	1	bMaxInBufferSize		40h	Maximum data-in buffer size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB.
16h	1	bMaxOutBufferSize		40h	Maximum data-out buffer size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB.
17h	1	bRPMB_ReadWriteSize		40h	Maximum number of RPMB frames (256-byte of data) allowed in security protocol in and security protocol out (for example, associated with a single command UPIU). If the data to be transferred is larger than bRPMB_ReadWriteSize x 256 bytes, the host will transfer it using multiple SECURITY PROTOCOL IN/OUT commands.
18h	1	bDynamicCapacity ResourcePolicy		01h	Dynamic capacity resource policy: This parameter specifies the device spare blocks resource management policy. 00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device. 01h: Spare blocks resource management policy is per memory type. The host may deallocate the required amount of logical blocks from any logical units with the same bMemoryType.

Table 16: Geometry Descriptor (Continued)

Offset	Size	Name	Default Value	Description
19h	1	bDataOrdering	00h	Support for out-of-order data transfer: 00h: Out-of-order data transfer is not supported by the device, in-order data transfer is required. 01h: Out-of-order data transfer is supported by the device. Others: Reserved
1Ah	1	bMaxContextIDNumber	20h	Maximum available number of contexts which are supported by the device: Minimum number of supported contexts shall be 5.
1Bh	1	bSysDataTagUnitSize	00h	bSysDataTagUnitSize provides system data tag unit size, which can be calculated as in the following (in bytes): Tag unit size = 2^(bSysDataTagUnitSize) × bMinAddrBlockSize × 512
1Ch	1	bSysDataTagResSize	06h	Maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism: Valid range from 0 to 6
1Dh	1	bSupportedSecRTypes	09h	Bit map which represents the supported secure removal types: Bit 0: Information removed by an erase of the physical memory Bit 1: Information removed by overwriting the addressed locations with a single character followed by an erase Bit 2: Information removed by overwriting the addressed locations with a character, its complement, then a random character. Bit 3: Information removed using a vendor define mechanism Others: Reserved A value of 1 means that the corresponding secure removal type is supported.
1Eh	2	wSupportedMemoryTypes	8009h	Bit map which represents the supported memory types: Bit 0: normal memory type Bit 1: System code memory type Bit 2: Non-persistent memory type Bit 3: Enhanced memory type 1 Bit 4: Enhanced memory type 2 Bit 5: Enhanced memory type 3 Bit 6: Enhanced memory type 4 Bit 7: Reserved … Bit 14: Reserved Bit 15: RPMB memory type A value 1 means that the corresponding memory type is supported. Bit 0 and Bit 15 shall be 1 for all UFS device.

Table 16: Geometry Descriptor (Continued)

Offset	Size	Name		Default Value	Description
20h	4	dSystemCodeMaxNAllocU		–	Not supported
24h	2	wSystemCodeCapAdjFac		–	
26h	4	dNonPersistMaxNAllocU		–	
2Ah	2	wNonPersistCapAdjFac		–	
2Ch	4	dEnhanced1Max NAllocU	128GB	7732h	Maximum number of allocation units for the enhanced memory type 1
			256GB	EE5Eh	
30h	2	wEnhanced1CapAdjFac		0300h	Capacity adjustment factor for the enhanced memory type 1
32h	4	dEnhanced2MaxNAllocU		–	Not supported
36h	2	wEnhanced2CapAdjFac		–	
38h	4	dEnhanced3MaxNAllocU		–	
3Ch	2	wEnhanced2CapAdjFac		–	
3Eh	4	dEnhanced4MaxNAllocU		–	
42h	2	wEnhanced4CapAdjFac		–	
44h	2	dOptimalLogicalBlockSize		–	
48h	1	bHPBRegionSize		13h	HPB Region size, which can be calculated as in the following (in bytes) HPB Region size = 512B x 2^bHPBRegionSize
49h	1	bHPBNumberLU		20h	Maximum number of HPB LU supported by the device 00h: HPB is not supported by the device 01h ~ 20h: Maximum number of HPB LU supported by the device Others : Reserved
4Ah	1	bHPBSubRegionSize		13h	HPB Sub-Region size, which can be calculated as in the following (in bytes) and shall be a multiple of Logical Block size HPB Sub-Region size = 512B x 2^bHPBSubRegion Size bHPBSubRegionSize shall not exceed bHPBRegionSize
4Bh	2	wDeviceMaxActive HPBRegions	128GB	1DDh	Maximum number of Active HPB Regions that is supported by the device The value shall not exceed maximum number of HPB Regions which is calculated by (qTotalRawDeviceCapacity - size of all Boot LUs)/HPBRegionSize
			256GB	3BAh	
4Fh	4	dWriteBoosterBuffer MaxNAllocUnits	128GB	1DCCh	Maximum total Write Booster Buffer size which is supported by the entire device. The summation of the Write Booster Buffer size for all LUs should be equal to or less than size value indicated by this descriptor
			256GB	3B97h	
53h	1	bDeviceMaxWriteBoosterLUs		01h	Number of maximum Write Booster Buffer supported by the device. In this version of the standard, the valid value of this field is 1. Other values are reserved

Table 16: Geometry Descriptor (Continued)

Offset	Size	Name	Default Value	Description
54h	1	bWriteBooster BufferCapAdjFac	03h	Capacity Adjustment Factor for the Write Booster Buffer memory type. This value is just to inform the LBA space reduction multiplication factor when Write Booster Buffer is configured in user space reduction mode. Therefore, the value of this descriptor is valid only if bWriteBoosterBufferNoUserSpaceReductionEn is 0. The LBA size will be decreased by bWriteBoosterBufferCapAdjFac *dLUNumWriteBoosterBufferAllocUnits (for example, 3 will be set for TLC NAND when SLC mode is used as Write Booster Buffer)
55h	1	bSupportedWriteBoosterBuffer UserSpaceReductionTypes	02h	The supportability of reduction mode and non-reduction mode 00h: Write Booster Buffer can be configured only in user space reduction type 01h: Write Booster Buffer can be configured only user space is not reduction type 02h: Device can be configured in either user space reduction type or user space non-reduction type Others: Reserved
56h	1	bSupportedWrite BoosterBufferTypes	02h	The supportability of Write Booster Buffer type 00h: LU based Write Booster Buffer configuration 01h: Single shared Write Booster Buffer configuration 02h: Supporting both LU based Write Booster Buffer and Single shared Write Booster Buffer configuration Others: Reserved

Table 17: Unit Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	2Dh	Size of this descriptor
01h	1	bDescriptorIDN	02h	Unit descriptor type identifier
02h	1	bUnitIndex	00h to 1Fh	Unit index
03h	1	bLUEnable	00h	Logical unit enable (user configurable): 00h: Logical unit disabled 01h: Logical unit enabled Others: Reserved
04h	1	bBootLunID	00h	Boot LUN ID (user configurable): 00h: Not bootable 01h: Boot LU A 02h: Boot LU B Others: Reserved

Table 17: Unit Descriptor (Continued)

Offset	Size	Name	Value	Description
05h	1	BLUWriteProtect	00h	Logical unit write protect (user configurable): 00h: LU not write protected 01h: LU write protected when fPowerOnWPEn = 1 02h: LU permanently write protected when fPermanentWPEn = 1 03h: Reserved (for UFS Security Extension specification) Others: Reserved
06h	1	bLUQueueDepth	00h	Logical unit queue depth: Queue depth available in this LU. Queue depth of 0 means best effort by device to service the command task.
07h	1	bPSASensitive	01h	00h: LU is not sensitive to soldering 01h: LU is sensitive to soldering Others: Reserved
08h	1	bMemoryType	00h	Memory type defines the logical unit memory type (user configurable): 00h: Normal memory 01h: System code memory type 02h: Non-persistent memory type 03h: Enhanced memory type 1 04h: Enhanced memory type 2 05h: Enhanced memory type 3 06h: Enhanced memory type 4 Others: Reserved
09h	1	bDataReliability	00h	Data reliability (user configurable): 00h: The logical unit is not protected. Logical unit's entire data might be lost as a result of a power failure during a WRITE operation. 01h: The logical unit is protected. Logical unit's data is protected against power failure. Others: Reserved
0Ah	1	bLogicalBlockSize	0Ch	Logical block size (user configurable): 0Ch (minimum value which corresponds to 4KB)–0Fh
0Bh	8	qLogicalBlockCount	00h	Logical block count (user configurable): Total number of addressable logical blocks in the LU in logical block size unit
13h	4	dEraseBlockSize	00h	Erase block size: In number of logical blocks
17h	1	bProvisioningType	00h	Provisioning type (user configurable): 00h: Thin provisioning is disabled (default). 02h: Thin provisioning is enabled and TPRZ = 0. 03h: Thin provisioning is enabled and TPRZ = 1. Others: Reserved
18h:1Fh	8	qPhyMemResourceCount	00h	Physical memory resource count: Total physical memory resource available in the logical unit

Table 17: Unit Descriptor (Continued)

Offset	Size	Name	Value	Description
20h	2	wContextCapabilities	00h	(User configurable) Bits[3:0]: MaxContextID is the maximum amount of contexts that the LU supports simultaneously. The sum of all MaXContextID must not exceed bMaxContexIDNumber. Bits[6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 Bits[15:7]: Reserved
22h	1	bLargeUnitGranularity_M1	00h	Granularity of the large unit, minus 1: Large unit granularity = 1MB (bLargeUnitGranularity_M1 + 1)
23h	2	wLUMaxActive HPBRegions	00h	Maximum Number of Active HPB Regions Maximum number of HPB Active Regions supported by the logical unit. Since wLUMaxActiveHPBRegions number includes the number of wNumHPBPinnedRegions, the value of wLUMaxActiveHPBRegions shall be greater or equal to the value of wNumHPBPinnedRegions. Otherwise, the query request shall fail and the Query Response field shall be set to “General failure”. During the configuration time of this descriptor, the sum of this maximum number of active HPB Regions of all LUs shall not exceed the wDeviceMaxActiveHPBRegions in HPB Geometry Descriptor. If exceeded, the query request shall fail and the Query Response field shall be set to “General failure”
25h	2	wHPBPinnedRegion StartIdx	00h	HPB Pinned Region Start Offset
27h	2	wNumHPBPinned Regions	00h	Number of HPB Pinned Regions Number of HPB pinned Regions assigned to the HPB logical unit. Value ‘0’ means that there is no pinned Region for this LU. wNumHPBPinnedRegions shall be no greater than wLUMaxActiveHPBRegions. A query request that attempts to set a value greater than wLUMaxActiveHPBRegions shall fail and return Query Response field set to “General failure”
29h	4	dLUNumWriteBooster BufferAllocUnits	00h	(User configurable) The Write Booster Buffer size for the Logical Unit

Notes: 1. Some fields are user configurable as they can be configured by the user writing the configuration descriptor.
2. Logical unit reconfiguration is allowed for engineering activities in laboratories and in limited preconditioning conditions. When reconfiguration is performed on a device with a cycled block (>10 cycles), the reconfiguration voids the warranty. Additional information will be provided in a separate document upon customer request.

Table 18: RPMB Unit Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	23h	Size of this descriptor
01h	1	bDescriptorIDN	02h	Unit descriptor type identifier
02h	1	bUnitIndex	C4h	Unit index

Table 18: RPMB Unit Descriptor (Continued)

Offset	Size	Name	Value	Description
03h	1	bLUEnable	01h	Logical unit enable
04h	1	bBootLunID	00h	Boot LUN ID
05h	1	bLUWriteProtect	00h	Logical unit write protect
06h	1	bLUQueueDepth	00h	Logical unit queue depth
07h	1	bPSASensitive	00h	LU sensitiveness to soldering
08h	1	bMemoryType	0Fh	Memory type 0Fh: RPMB memory type
09h	1	bRPMBRegionEnable	00h	(User configurable) RPMB region enable
0Ah	1	bLogicalBlockSize	08h	Logical block size
0Bh	8	qLogicalBlockCount	10000h	Logical block count
13h	1	bRPMBRegion0Size	80h	(User configurable) RPMB region 0 size
14h	1	bRPMBRegion1Size	00h	(User configurable) RPMB region 1 size
15h	1	bRPMBRegion2Size	00h	(User configurable) RPMB region 2 size
16h	1	bRPMBRegion3Size	00h	(User configurable) RPMB region 3 size
17h	1	bProvisioningType	00h	Provisioning type
18h:1Fh	8	qPhyMem ResourceCount	10000h	Physical memory resource count
20h:22h	3	Reserved	–	Reserved

Table 19: Power Parameters Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	62h	Size of this descriptor
01h	1	bDescriptorIDN	08h	Power parameters descriptor type identifier
02h	2	wActiveICCLevelsVCC[0]	8320h	Maximum V_{CC} current value for bActiveICCLevel = 0
04h	2	wActiveICCLevelsVCC[1]	8320h	Maximum V_{CC} current value for bActiveICCLevel = 1
...	...	...	...	...
20h	2	wActiveICCLevelsVCC[15]	8320h	Maximum V_{CC} current value for bActiveICCLevel = 15
22h	2	wActiveICCLevelsVCCQ[0]	83E8h	Maximum V_{CCQ} current value for bActiveICCLevel = 0
24h	2	wActiveICCLevelsVCCQ[1]	83E8h	Maximum V_{CCQ} current value for bActiveICCLevel = 1
...	...	...	...	...
40h	2	wActiveICCLevelsVCCQ[15]	83E8h	Maximum V_{CCQ} current value for bActiveICCLevel = 15
42h	2	wActiveICCLevelsVCCQ2[0]	00h	Maximum V_{CCQ2} current value for bActiveICCLevel = 0
44h	2	wActiveICCLevelsVCCQ2[1]	00h	Maximum V_{CCQ2} current value for bActiveICCLevel = 1
...	...	...	...	...
60h	2	wActiveICCLevelsVCCQ2[15]	00h	Maximum V_{CCQ2} current value for bActiveICCLevel = 15

Note: 1. For Product Revision Level 030x, values report peak current values for -AIT devices only. In case of -AAT devices with Product Revision Level 030x, wActiveICCLevelsVCCQ[n] values are not applicable: refer to peak current consumption in the Active Current Consumption table (level 030x).

Table 20: Interconnect Descriptor

Offset	Name	Value	Description
00h	bLength	06h	Size of this descriptor

Table 20: Interconnect Descriptor (Continued)

Offset	Name	Value	Description
01h	bDescriptorIDN	04h	Interconnect descriptor type identifier
02h	bcdUniproVersion	0180h	MIPI UniPro version number in BCD format (for example, version 1.80 = 0180h)
04h	bcdMphyVersion	0410h	MIPI M-PHY version number in BCD format (for example, version 4.10 = 0410h)

Table 21: Manufacturer Name String Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	12h	Size of this descriptor
01h	1	bDescriptorIDN	05h	String descriptor type identifier
02h	2	UC[0]	004Dh	Unicode string character
04h	2	UC[1]	0049h	Unicode string character
06h	2	UC[2]	0043h	Unicode string character
08h	2	UC[3]	0052h	Unicode string character
0Ah	2	UC[4]	004Fh	Unicode string character
0Ch	2	UC[5]	004Eh	Unicode string character
0Eh	2	UC[6]	0020h	Unicode string character
10h	2	UC[7]	0020h	Unicode string character

Table 22: Product Name String Descriptor

Offset	Size	Name		Value	Description
00h	1	bLength		22h	Size of this descriptor
01h	1	bDescriptorIDN		05h	String descriptor type identifier
02h	2	UC[0]		004Dh	Unicode string character
04h	2	UC[1]		0054h	Unicode string character
06h	2	UC[2]	128GB	0031h	Unicode string character
			256GB	0032h	
08h	2	UC[3]	128GB	0032h	Unicode string character
			256GB	0035h	
0Ah	2	UC[4]	128GB	0038h	Unicode string character
			256GB	0036h	
0Ch	2	UC[5]	128GB	0047h	Unicode string character
			256GB	0047h	
0Eh	2	UC[6]	128GB	0042h	Unicode string character
			256GB	0042h	
10h	2	UC[7]		0043h	Unicode string character
12h	2	UC[8]		0041h	Unicode string character
14h	2	UC[9]		0056h	Unicode string character
16h	2	UC[10]	128GB	0032h	Unicode string character
			256GB	0034h	

Table 22: Product Name String Descriptor (Continued)

Offset	Size	Name		Value	Description
18h	2	UC[11]		0055h	Unicode string character
1Ah	2	UC[12]	128GB	0033h	Unicode string character
			256GB	0033h	
1Ch	2	UC[13]	128GB	0031h	Unicode string character
			256GB	0031h	
1Eh	2	UC[14]	AIT	0041h	Unicode string character
			AAT	0041h	
20h	2	UC[15]	AIT	0049h	Unicode string character
			AAT	0041h	

Table 23: OEM ID String Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	0Eh	Size of this descriptor
01h	1	bDescriptorIDN	05h	String descriptor type identifier
02h	2	UC[0]	004Dh	Unicode string character
04h	2	UC[1]	0049h	Unicode string character
06h	2	UC[2]	0043h	Unicode string character
08h	2	UC[3]	0052h	Unicode string character
0Ah	2	UC[4]	004Fh	Unicode string character
0Ch	2	UC[5]	004Eh	Unicode string character

Table 24: Serial Number String Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	12h	Size of this descriptor
01h	1	bDescriptorIDN	05h	String descriptor type identifier
02h	2	UC[0]	–	Unicode string character
04h	2	UC[1]	–	Unicode string character
06h	2	UC[2]	–	Unicode string character
08h	2	UC[3]	–	Unicode string character
0Ah	2	UC[4]	–	Unicode string character
0Ch	2	UC[5]	–	Unicode string character
0Eh	2	UC[6]	–	Unicode string character
10h	2	UC[7]	–	Unicode string character

Note: 1. Serial number will contain Unicode string character by default.

Table 25: Product Revision Level String Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	0Ah	Size of this descriptor
01h	1	bDescriptorIDN	05h	String descriptor type identifier
02h	2	UC[0]	–	Unicode string character

Table 25: Product Revision Level String Descriptor (Continued)

Offset	Size	Name	Value	Description
04h	2	UC[1]	–	Unicode string character
06h	2	UC[2]	–	Unicode string character
08h	2	UC[3]	–	Unicode string character

Note: 1. Serial number will contain Unicode string character by default.

Table 26: Device Health Descriptor[1]

Offset	Size	Name	Value	Description
00h	1	bLength	2Dh	Size of this descriptor
01h	1	bDescriptorIDN	09h	Device health descriptor type identifier
02h	1	bPreEOLInfo	01h	Pre end-of-life information provides indication about device life time reflected by average reserved blocks: 01h: Normal
03h	1	bDeviceLifeTimeEstA	01h	This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method A. 01h: 0%–10% device life time used
04h	1	bDeviceLifeTimeEstB	01h	This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method B. 01h: 0%–10% device life time used
05h	32	VendorPropInfo	–	Reserved for vendor proprietary health report
25h	3	dRefreshTotalCount	00h	Total Refresh Count Indicates how many times the device complete refresh for the entire device; incremented by 1 when dRefreshProgress reach 100000
29h	4	dRefreshProgress	00h	Refresh Progress Indicates the refresh progress in %.

Note: 1. Product NAND endurance is limited as further specified under the applicable device qualification document and technical note health information sheets, which are incorporated herein by reference. The applicable qualification and reliability report is available on customer request at the qualification release milestone. The health information, as specified by JEDEC, must be used to monitor a device's memory usage and to retrieve the usage percentage. Refer to Technical Note Health Information for Micron Embedded UFS Devices, available on Micron.com.

UFS Flags, Attributes, and Commands

A flag is a single boolean value that represents 0 or 1 type of value. Flags are useful to enable or disable certain functions, modes, or states with the device.

Table 27: Flags

IDN	Name	Type	Default Value	Description
00h	Reserved	–	–	Reserved
01h	fDeviceInit	Read/ Set only	00h	Device initialization: 0b: Device initialization completed or not started yet 1b: Device initialization in progress
02h	fPermanentWPEn	Read/ Write once	00h	Permanent write protection enable: 00h: Permanent write protection disabled 01h: Permanent write protection enabled
03h	fPowerOnWPEn	Read/ Power on reset	00h	Power-on write protection enable: 00h: Power-on write protection disabled 01h: Power-on write protection enabled
04h	FBackgroundOpsEn	Read/Volatile	01h	Background operations enable: 00h: Device is not permitted to run background operations 01h: Device is permitted to run background operations
05h	fDeviceLifeSpanModeEn	Read/Volatile	00h	Device life span mode: 0b: Device life span mode is disabled 1b: Device life span mode is enabled
06h	fPurgeEnable	Write only/ Volatile	–	PURGE enable: 00h: PURGE operation is disabled 01h: PURGE operation is enabled
07h	fRefreshEnable	Write only/ Volatile	–	Refresh Enable: 0b: Refresh operation is disabled. 1b: Refresh operation is enabled
08h	fPhyResourceRemoval	Read/ Persistent	00h	Physical resource removal: The host sets this flag to 1 to indicate that the dynamic capacity operation commences upon device EndPointReset or hardware reset. The device resets this flag to 0 after completion of dynamic capacity operation. The host cannot reset this flag.
09h	fBusyRTC[3]	Read only	00h	Busy real-time clock: 00h: Device is not executing internal operation related to RTC 01h: Device is executing internal operation related to RTC
0Ah	Reserved	–	–	Reserved for unified memory extension standard
0Bh	fPermanentlyDisable FWUpdate	Read/ Write once	00h	Permanently disable firmware update: 00h: The UFS device firmware may be modified. 01h: The UFS device permanently disallows future firmware updates to the UFS device.

Table 27: Flags (Continued)

IDN	Name	Type	Default Value	Description
0Ch	Reserved	–	–	Reserved for unified memory extension standard
0Dh	Reserved	–	–	Reserved for unified memory extension standard
0Eh	fWriteBoosterEn	Read/Volatile	00h	Write Booster Enable: 0b: Write Booster is not enabled 1b: Write Booster is enabled
0Fh	fWriteBoosterBufferFlushEn	Read/Volatile	00h	Flush the data in Write Booster Buffer to the user area of storage 0b: Flush operation is not performed. 1b: Flush operation is performed
10h	fWriteBoosterBufferFlush DuringHibernate	Read/Volatile	00h	Flush Write Booster Buffer during hibernate state 0b: Device is not allowed to flush the Write Booster Buffer during link hibernate state 1b: Device is allowed to flush the Write Booster Buffer during link hibernate state
11h	fHPBReset	Read/Set only	00h	HPB Reset 0: HPB reset completed or not started yet 1: HPB reset in progress
12h	fHPBEn	Read/ Persistent	00h	HPB enable setting 0: HPB disabled 1: HPB enabled
13h	Reserved	–	–	–

All flags reported in the table are device level flags. They are addressed setting INDEX = 00h and SELECTOR = 00h.

An attribute is a parameter that represents a specific range of numeric values that can be written or read. Attribute size can be from 1-bit to 32-bit. Attributes of the same type can be organized in arrays, each element of them identified by an index.

Table 28: Attributes

IDN	Name	Type	Size (Byte)	Default Value	Description
00h	bBootLunEN	Read/ Persistent	1	00h	Boot LUN enable: 00h: Boot disabled 01h: Enabled boot from boot LU A 02h: Enabled boot from boot LU B All others: Reserved

Table 28: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
01h	bMAX_ DATA_SIZE_-FOR_ HPB_SINGLE_CMD	Read/ Read only	1	07h	Maximum HPB data size for using single HPB command recommended by the device. The sizeis calculated as (bMAX_ DATA_SIZE_FOR_HPB_SINGLE_CMD + 1) × 4KB. 00h: 4KB 01h: 8KB 02h: 12KB 03h: 16KB … FEh: 1020KB FFh: 1024KBFor example, if the value is 07h, only up to 32KB, data is expected to be issued with single HPB READ command, while bigger data is expected to be issued with HPB Read using HPB Read ID mode.
02h	bCurrentPowerMode	Read only	1	11h	Current power mode: 00h: Idle mode 10h: Pre-active mode 11h: Active mode 20h: Pre-sleep mode 22h: UFS-sleep mode 30h: Pre-power down mode 33h: UFS-power down mode Others: Reserved
03h	bActiveICCLevel	Read/ Volatile	1	00h	Active I_{CC} level: bActiveICCLevel defines the maximum current consumption allowed during active mode. 00h: Lowest active I_{CC} level 0Fh: Highest active I_{CC} level Others: Reserved
04h	bOutOfOrderDataEn	Read/ Write once	1	00h	Out-of-order data transfer enable: 00h: Out-of-order data transfer is disabled 01h: Out-of-order data transfer is enabled Others: Reserved
05h	bBackgroundOpStatus	Read only	1	00h	Background operations status device health status for background operation: 00h: Not required 01h: Required, not critical 02h: Required, performance impact 03h: Critical Others: Reserved
06h	bPurgeStatus	Read only	1	00h	PURGE operation status: 00h: Idle (PURGE operation disabled) 01h: PURGE operation in progress 02h: PURGE operation stopped prematurely 03h: PURGE operation completed successfully 04h: PURGE operation failed due to logical unit queue not empty 05h: PURGE operation general failure Others: Reserved
07h	bMaxDataInSize	Read/ Persistent	1	40h	Maximum data in size

Table 28: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
08h	bMaxDataOutSize	Read/ Persistent	1	40h	Maximum data out size
09h	dDynCapNeeded[3]	Read only	4	00h	Dynamic capacity needed
0Ah	bRefClkFreq	Read/ Persistent	1	01h	Reference clock frequency value: 00h: 19.2 MHz 01h: 26 MHz 02h: 38.4 MHz 03h: Obsolete Others: Reserved
0Bh	bConfigDescrLock	Read/ Write once	1	00h	Configuration descriptor lock: 00h: Configuration descriptor not locked 01h: Configuration descriptor locked Others: Reserved
0Ch	bMaxNumOfRTT	Read/ Persistent	1	02h	Maximum current number of outstanding RTTs in device that is allowed.
0Dh	wExceptionEventControl	Read/ Volatile	2	00h	Exception event control: Bit 0: DYNCAP_EVENT_EN Bit 1: SYSPOOL_EVENT_EN Bit 2: URGENT_BKOPS_EN Bit 3: TOO_HIGH_TEMP_EN Bit 4: TOO_LOW_TEMP_EN Bit 5: WRITEBOOSTER_EVENT_EN Bit 6: PERFORMANCE_THROTTLING_EN Bit 7–15: Reserved
0Eh	wExceptionEventStatus	Read only	2	00h	Bit 0: DYNCAP_NEEDED Bit 1: SYSPOOL_EXHAUSTED Bit 2: URGENT_BKOPS Bit 3: TOO_HIGH_TEMP Bit 4: TOO_LOW_TEMP Bit 5: WRITEBOOSTER_FLUSH_NEEDED Bit 6: PERFORMANCE_THROTTLING Bit 7–15: Reserved
0Fh	dSecondsPassed	Write only	4	00h	Bits[31:0]: Seconds passed from TIME BASELINE
10h	wContextConf	Read/ Volatile	2	00h	INDEX specifies the LU number. SELECTOR specifies the context ID within the LU. Valid values are 01h–Fh
11h	Obsolete	–	–	–	–
12h	Reserved	–	–	–	Reserved for Unified Memory Extension standard
13h	Reserved	–	–	–	–
14h	bDeviceFFUStatus	Read only	1	00h	Device FFU status: 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h–FEh: Reserved FFh: General error

Table 28: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
15h	bPSAState	Read/ Persistent	1	00h	00h: Off. PSA feature is off. 01h: Pre-soldering. PSA feature is on, device is in the pre-soldering state. 02h: Loading complete. PSA feature is on. The host will set to this value after the host finished writing data during pre-soldering state. 03h: Soldered. PSA feature is no longer available. Set by the device to indicate it is in post-soldering state. This attribute unchangeable after it is in soldered state.
16h	dPSADataSize	Read/ Persistent	4	00h	The amount of data that the host plans to load to all logical units with bPSASensitive set to 1.
17h	bRefClkGatingWaitTime	Read only	1	19h	Minimum time for which the reference clock is required by device during transition to LS-MODE or HIBERN8 state. The larger time requirement among the transition to LS-MODE and HIBERN8 states should be set for this attribute. 00h: Undefined 01h: 1 micro second … FFh: 255 micro seconds
18h	bDeviceCase RoughTemperature[4]	Read only	1	00h	Device's rough package case surface temperature. This value is valid when (TOO_HIGH_TEMPERATURE is supported and TOO_HIGH_TEMP_EN is enabled) or (TOO_LOW_TEMPERATURE is supported and TOO_LOW_TEMP_EN is enabled). 0 : Unknown Temperature 1~250 : (this value – 80) degrees in Celsius. (–79 °C~170 °C) Others: Reserved
19h	bDeviceTooHigh TempBoundary[4, 5]	Read only	1	-	High temperature boundary from which TOO_HIGH_TEMP in wExceptionEventStatus is turned on. 0: Unknown 100~250: (this value – 80) degrees in celcius. (20 °C~170 °C) Others: Reserved
1Ah	bDeviceTooLow TempBoundary[4]	Read only	1	-	Low temperature boundary from which TOO_LOW_TEMP in wExceptionEventStatus is turned on. 0: Unknown 1~80: (this value – 80) degrees in celcius. (–79 °C~0 °C) Others: Reserved
1Bh	bTrottling_Status[5]	Read only	1	00h	Each set bit represents an existing situation resulting in performance throttling. Bit 0: Temperature Others: Reserved

Table 28: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
1Ch	bWriteBooster BufferFlushStatus	Read only	1	00h	Flush operation status of Write Booster Buffer 00h: idle. Device is not flushing the Write Booster Buffer; either the Write Booster Buffer is empty or a flush has not been initiated 01h: Flush operation in progress. The Write Booster Buffer is not yet empty and a flush has been initiated 02h: Flush operation stopped prematurely. The Write Booster Buffer is not empty and the host stopped the in-progress flush 03h: Flush operation completed successfully 04h: Flush operation general failure Others: Reserved
1Dh	bAvailableWrite BoosterBufferSize	Read only	1	00h	Available Write Booster Buffer Size This available buffer size is decreased by Write Booster operation and increased by flush operation Value expressed in unit of 10% granularity 00h: 0% buffer remains 01h: 10% buffer remains 02h~09h: 20%~90% buffer remains 0Ah: 100% buffer remains Others: Reserved
1Eh	bWriteBooster BufferLifeTimeEst	Read only	1	00h	This field provides an indication of the Write Booster Buffer lifetime based on the amount of performed program/erase cycles. The detailed calculation method is vendor specific 00h: Information not available (Write Booster Buffer is disabled) 01h: 0%–10% Write Booster Buffer life time used 02h: 10%–20% Write Booster Buffer life time used 03h: 20%–30% Write Booster Buffer life time used 04h: 30%–40% Write Booster Buffer life time used 05h: 40%–50% Write Booster Buffer life time used 06h: 50%–60% Write Booster Buffer life time used 07h: 60%–70% Write Booster Buffer life time used 08h: 70%–80% Write Booster Buffer life time used 09h: 80%–90% Write Booster Buffer life time used 0Ah: 90%–100% Write Booster Buffer life time used 0Bh: Exceeded its maximum estimated Write Booster Buffer life time (write commands are processed as if Write Booster feature was disabled) Others: Reserved
1Fh	dCurrentWrite BoosterBufferSize	Read only	4	00h	The current Write Booster Buffer size Host can check the current Write Booster Buffer size by checking this attribute. Value expressed in unit of Allocation Units. If this value is 0, then the current Write Booster Buffer size is 0
20h:2Bh	Reserved	–	–	–	Reserved for Unified Memory Extension standard

Table 28: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
2Ch	bRefreshStatus	Read only	1	00h	Refresh Operation Status 00h: Idle (refresh operation disabled) 01h: Refresh operation in progress 02h: Refresh operation stopped prematurely 03h: Refresh operation completed successfully 04h: Refresh operation failed due to logical unit queue not empty 05h: Refresh operation general failure Others: Reserved
2Dh	bRefreshFreq	Read/ Persistent	1	00h	Refresh Frequency Host should make sure that dRefreshTotalCount will be incremented on this frequency 00h: Not defined 01h: 1 month 02h: 2 month … FFh: 255 month
2Eh	bRefreshUnit	Read/ Persistent	1	00h	Refresh Operation Unit This attribute may be set to adjust the minimum physical block numbers to be refreshed upon a single request 00h: Minimum refresh capability of Device 01h:100% (entire device) Others: Reserved
2Fh	bRefreshMethod	Read/ Persistent	1	00h	Refresh Method This parameter specifies the refresh operation method 00h: Not defined 01h: Manual-Force 02h: Manual-Selective Others: Reserved

Notes: 1. dDynCapNeeded and wContextConf are arrays of attributes.
2. Default value means attribute's value after device manufacturing.
3. The dynamic device capacity feature is supported only as a JEDEC interface.
4. bDeviceTooHighTempBoundary, bDeviceTooLowTempBoundary, bDeviceCaseRoughTemperature: additional information will be provided in a separate document upon customer request.
5. The UFS device supports algorithms to control temperature increase that reduce performance or limit the access to UFS at high temperature. The algorithms are based on internal junction temperature (T_j). T_j versus T_{case} relationship strictly depends on the platform. Refer to Micron representative for instructions on how to monitor the internal junction temperature (T_j).

Table 29: SCSI Commands

Command Name	Opcode	Command Name	Opcode
FORMAT UNIT	04h	SECURITY PROTOCOL IN	A2h
INQUIRY	12h	SECURITY PROTOCOL OUT	B5h
MODE SELECT (10)	55h	SEND DIAGNOSTIC	1Dh
MODE SENSE (10)	5Ah	START STOP UNIT	1Bh
PRE-FETCH (10)	34h	SYNCHRONIZE CACHE (10)	35h
PRE-FETCH (16)	90h	SYNCHRONIZE CACHE (16)	91h

Table 29: SCSI Commands (Continued)

Command Name	Opcode	Command Name	Opcode
READ (6)	08h	TEST UNIT READY	00h
READ (10)	28h	UNMAP	42h
READ (16)	88h	VERIFY (10)	2Fh
READ BUFFER	3Ch	WRITE (6)	0Ah
READ CAPACITY (10)	25h	WRITE (10)	2Ah
READ CAPACITY(16)	9Eh	WRITE (16)	8Ah
REPORT LUNS	A0h	WRITE BUFFER	3Bh
REQUEST SENSE	03h	–	–

UFS Supported Pages

Micron devices support the following UFS mode pages. For detailed information, refer to the JEDEC UFS specification.

Table 30: UFS Supported Pages

Page Name	Page Code	Subpage Code	Description
Control	0Ah	00h	Return control mode page
Read-write error recovery	01h	00h	Return read-write error recovery mode page
Caching	08h	00h	Return caching mode page
All pages	3Fh	00h	Return all mode pages (not including subpages)
All subpages	3Fh	FFh	Return all mode pages and subpages

Table 31: Control Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	0Ah	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	0Ah	Indicates the size in bytes of the following mode page parameters.
02h	0	RLEC	0h	Report log exception condition. Setting this bit to 0 specifies that the device server shall not report log exception conditions.
02h	1	GLTSD	0h	Global logging target save disable (GLTSD): Setting this bit to 0 specifies that the logical unit implicitly saves, at vendor specific intervals, each log parameter in which the TSD bit is set to 0.
02h	2	D_SENSE	0h	A descriptor format sense data (D_SENSE) bit set to 0 specifies that the device server shall return fixed format sense data when returning sense data in the same I_T_L_Q nexus transaction as the status.
02h	3	DPICZ	0h	A disable protection information check if protect field is 0 (DPICZ) bit set to 0 indicates that checking of protection information bytes is enabled.
02h	4	TMF_ONLY	0h	The allow task management functions only (TMF_ONLY) bit set to 0 specifies that the device server shall process commands with the auto contingent allegiance (ACA) task attribute received on the faulted I_T nexus when an ACA condition has been established.
02h	7:5	TST	0h	Indicates task set type (TST).
03h	0	Obsolete	0h	Not available

Table 31: Control Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
03h	2:1	QERR	0h	The queue error management (QERR) field specifies how the device server shall handle other commands when one command is terminated with check condition status. If an ACA condition is established, the affected commands in the task set shall resume after the ACA condition is cleared. Otherwise, all commands other than the command that received the check condition status shall be processed as if no error occurred.
03h	3	NUAR	0h	No unit attention on release (NUAR) bit set to 0 specifies that the device server shall establish a unit attention condition.
03h	7:4	QUEUE ALGORITHM MODIFIER	01h	A value of 1 in this field specifies that the device server may reorder the processing sequence of commands having the SIMPLE task attribute in any manner.
04h	2:0	Obsolete	0h	Not available
04h	3	SWP	0h	A software write protect (SWP) bit (user configurable)
04h	5:4	UA_INTLCK_CTRL	0h	The unit attention interlocks control (UA_INTLCK_CTRL) field set to 00b specifies that the logical unit shall clear any unit attention condition reported in the same I_T_L_Q nexus transaction as a check condition status and shall not establish a unit attention condition when a command is completed with busy, task set full, or reservation conflict status.
04h	6	RAC	0h	A report a check (RAC) bit set to 0 specifies that the device server may return busy status regardless of the length of time the reason for returning busy status may persist.
04h	7	VS	0h	Not available
05h	2:0	AUTOLOAD MODE	0h	This field specifies the action to be taken by a removable medium device server when a medium is inserted. Setting it to 0 means that medium shall be loaded for full access.
05h	3	Reserved	–	–
05h	4	RWWP	0h	A reject write without protection (RWWP) bit set to 0 specifies that WRITE commands without protection information shall be processed.
05h	5	ATMPE	0h	An application tag mode page enabled (ATMPE) bit set to 0 specifies that the application tag mode page is disabled and the contents of logical block application tags are not defined by this standard.
05h	6	TAS	0h	A task aborted status (TAS) bit set to 0 specifies that aborted commands shall be terminated by the device server without any response to the application client.

Table 31: Control Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
05h	7	ATO	0h	An application tag owner (ATO) bit set to 0 specifies that the device server may modify the contents of the LOGICAL BLOCK APPLICATION TAG field and, depending on the protection type, may modify the contents of the LOGICAL BLOCK REFERENCE TAG field.
06h	15:0	Obsolete	0h	Not available
08h	15:0	BUSY TIMEOUTPERIOD	01h	Busy timeout period: 0001h = 100ms
0Ah	15:0	EXTENDED SELF-TEST COMPLETION TIME	0h	This field contains advisory data that is the time in seconds that the device server requires to complete an extended self-test when the device server is not interrupted by subsequent commands and no errors occur during processing of the self-test.

Note: 1. Some fields are user-configurable.

Table 32: Read – Write Error Recovery Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	01h	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	0Ah	Indicates the size in bytes of the following mode page parameters.
02h	0	DCR	0h	A disable correction (DCR) bit set to 0 allows the use of additional information (for example, ECC bytes) for data error recovery. If the EER bit is set to 1, the DCR bit shall be set to 0.
02h	1	DTE	0h	A data terminate on error (DTE) bit set to 0 specifies that the device server shall not terminate the data-in or data-out buffer transfer of a command performing a READ or WRITE operation upon detection of a recovered error.
02h	2	PER	0h	A post error (PER) bit set to 0 specifies that if a recovered read error occurs during a command performing a READ or WRITE operation, then the device server shall perform error recovery procedures within the limits established by the error recovery parameters and only terminate the command with check condition status if the error becomes uncorrectable based on the established limits. If the DTE bit is set to 1, then the PER bit shall be set to 1.
02h	3	EER	0h	An enable early recovery (EER) bit set to 0 specifies that the device server shall use an error recovery procedure that minimizes the risk of error mis-detection or mis-correction.
02h	4	RC	0h	A read continuous (RC) bit set to 0 specifies that ERROR RECOVERY operations that cause delays during the data transfer are acceptable. Data shall not be fabricated.
02h	5	TB	0h	A transfer block (TB) bit set to 0 specifies that if an unrecovered read error occurs during a READ operation, then the device server shall not transfer any data for the logical block to the data-in buffer.
02h	6	ARRE	0h	An automatic read reassignment enabled (ARRE) bit set to 0 specifies that the device server shall not perform automatic reassignment of defective logical blocks during READ operations.
02h	7	AWRE	01h	An automatic write reassignment enabled (AWRE) bit set to 1 specifies that the device server shall enable automatic reassignment of defective logical blocks during WRITE operations.
03h	7:0	READ RETRY COUNT	01h	This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during READ operations.
04h	7:0	Obsolete	0h	Not available
05h	7:0	Obsolete	0h	Not available

Table 32: Read – Write Error Recovery Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
06h	7:0	Obsolete	0h	Not available
07h	1:0	Restricted for MMC-6	0h	Not available
07h	6:2	Reserved	–	–
07h	7	TPERE	0h	Not available
08h	7:0	WRITE RETRY COUNT	00h	This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during WRITE operations.
09h	7:0	Reserved	–	–
0Ah	15:0	RECOVERY TIME LIMIT	4B0h	This field (user configurable) specifies in milliseconds the maximum time duration that the device server shall use for data error recovery procedures. When both a retry count and a recovery time limit are specified, the field that specifies the recovery action of least duration shall have priority.

Table 33: Caching Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	08h	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	12h	Indicates the size in bytes of the following mode page parameters.
02h	0	RCD	0h	A read cache disable (RCD) bit (user configurable) set to 0 specifies that the device server may return data requested by a READ command by accessing either the cache or medium. A RCD bit set to 1 specifies that the device server shall transfer all of the data requested by a READ command from the medium (for example, data shall not be transferred from the cache).
02h	1	MF	0h	A multiplication factor (MF) bit set to 0 specifies that the device server shall interpret the MINIMUM PREFETCH field and the MAXIMUM PREFETCH field in terms of the number of logical blocks for each of the respective types of prefetch.
02h	2	WCE	01h	A write back cache enable (WCE) bit (user configurable) set to 0 specifies that the device server shall complete a WRITE command with good status only after writing all of the data to the medium without error. A WCE bit set to 1 specifies that the device server may complete a WRITE command with good status after receiving the data without error and prior to having written the data to the medium.

Table 33: Caching Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
02h	3	SIZE	0h	A size enable (SIZE) bit set to 0 specifies that the NUMBER OF CACHE SEGMENTS field is used to control caching segmentation. Simultaneous use of both the number of segments and the segment size is vendor specific.
02h	4	DISC	0h	A discontinuity (DISC) bit set to 0 specifies that prefetches be truncated or wrapped at time discontinuities.
02h	5	CAP	0h	A caching analysis permitted (CAP) bit set to 0 specifies that caching analysis is disabled (for example, to reduce overhead time or to prevent non-pertinent operations from impacting tuning values).
02h	6	ABPF	0h	An abort prefetch (ABPF) bit set to 0 when the DRA bit set to 0 specifies that the termination of any active prefetch is dependent upon caching mode page bytes 4 through 11 and is vendor specific.
02h	7	IC	0h	An initiator control (IC) enable bit set to 0 specifies that the device server uses its own adaptive caching algorithm.
03h	3:0	WRITE RETENTION PRIORITY	0h	This field set to 0h means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch).
03h	7:4	DEMAND READ RETENTION PRIORITY	0h	This field set to 0 means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch).
04h	15:0	DISABLE PREFETCH TRANSFER LENGTH	0h	This field specifies the selective disabling of anticipatory prefetch on long transfer lengths. If this field is set to 0, then all anticipatory prefetching is disabled for any request for data, including those with a transfer length of 0.
06h	15:0	MINIMUM PREFETCH	0h	This field specifies the number of logical blocks to prefetch regardless of the delays it might cause in processing subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks.
08h	15:0	MAXIMUM PREFETCH	0h	This field specifies the number of logical blocks to prefetch if the prefetch does not delay processing of subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks.
0Ah	15:0	MAXIMUM PREFETCH CEILING	0h	This field specifies an upper limit on the number of logical blocks computed as the maximum prefetch. If this number of logical blocks is greater than the value in the MAXIMUM PREFETCH field, then the number of logical blocks to prefetch shall be truncated to the value stored in this field.
0Ch	0	NV_DIS	0h	An NV_DIS bit set to 0 specifies that the device server may use a nonvolatile cache and indicates that a nonvolatile cache may be present and enabled.
0Ch	2:1	Reserved	–	–

Table 33: Caching Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
0Ch	4:3	Vendor specific	0h	Vendor specific
0Ch	5	DRA	0h	A disable read-ahead (DRA) bit set to 0 specifies that the device server may continue to read logical blocks into the prefetch buffer beyond the addressed logical block(s).
0Ch	6	LBCSS	0h	A logical block cache segment size (LBCSS) bit set to 0 specifies that the CACHE SEGMENT SIZE field units shall be interpreted as bytes. The LBCSS shall not impact the units of other fields.
0Ch	7	FSW	0h	A force sequential write (FSW) bit set to 0 specifies that the device server may reorder the sequence of writing logical blocks (for example, in order to achieve faster command completion).
0Dh	7:0	NUMBER OF CACHE SEGMENTS	0h	This field specifies the number of segments into which the device server shall divide the cache.
0Eh	15:0	CACHE SEGMENT SIZE	0h	This field specifies the segment size in bytes if the LBCSS bit is set to 0 or in logical blocks if the LBCSS bit is set to 1. This field is valid only when the SIZE bit is set to 1.
10h	7:0	Reserved	–	–
11h	15:0	Obsolete	0h	Not available

Note: 1. Some fields are user-configurable.

UFS Vital Product Data Parameters

The vital product data (VPD) pages are returned by an INQUIRY command with the EVPD bit set to 1, and contain vendor-specific product information about a logical unit and SCSI target device. A UFS device supports the following VPD pages.

Table 34: Supported VPD Pages

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	0h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	08h	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	Supported VPD Page List[0]	0h	The supported VPD page list contains a list of all VPD page codes implemented by the logical unit in ascending order beginning with page code 00h: SUPPORTED_VPD_PAGE
05h	7:0	Supported VPD Page List[1]	80h	UNIT_SERIAL_NUM
06h	7:0	Supported VPD Page List[2]	83h	DEVICE_ID
07h	7:0	Supported VPD Page List[3]	86h	EXTENDED INQUIRY VPD
08h	7:0	Supported VPD Page List[4]	87h	MODE_PAGE_POLICY
09h	7:0	Supported VPD Page List[5]	B0h	BLOCK_LIMITS
0Ah	7:0	Supported VPD Page List[6]	B1h	BLOCK_DEVICE_CHARACTERISTICS
0Bh	7:0	Supported VPD Page List[7]	B2h	LOGICAL_BLOCK_PROVISIONING

Table 35: Unit Serial Number VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICETYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	80h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.

Table 35: Unit Serial Number VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
02h	15:0	PAGE LENGTH	08h	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	PRODUCT SERIALNUMBER	–	This field contains right-aligned ASCII data that is vendor-assigned serial number.

Table 36: Device Identification VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	83h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	4:0	CODE SET	2h	This field contains a code set enumeration that indicates the format of the DESIGNATOR field.
04h	7:5	PROTOCOL IDENTIFIER	0h	This field may indicate the SCSI transport protocol to which the designation descriptor applies.
05h	3:0	DESIGNATOR TYPE	1h	This field indicates the format and assignment authority for the designator.
05h	5:4	ASSOCIATION	0h	This field indicates the entity with which the DESIGNATOR field is associated. If a logical unit returns a designation descriptor with this field set to 00b or 10b, it shall return the same descriptor when it is accessed through any other I_T nexus.
05h	6	Reserved	–	–
05h	7	PIV	0h	A protocol identifier valid (PIV) bit set to 0 indicates the PROTOCOL IDENTIFIER field contents are reserved.
06h	7:0	Reserved	–	–
07h	7:0	DESIGNATOR LENGTH	8h	This field indicates the length in bytes of the DESIGNATOR field.
08h	23:0	IEEE COMPANY ID	–	–
0Bh	39:0	VENDOR SPECIFIC EXTENSION IDENTIFIER	–	–

Table 37: Mode Page Policy VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	87h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
Mode page policy descriptor [0]				
04h	5:0	Policy page code	1h	Contains information describing the mode page policy for read-write error recovery mode page.
04h	7:6	Reserved1	0h	
05h	7:0	Policy subpage code	0h	
06h	1:0	ModePagePolicy	0h	
06h	6:2	Reserved 2	0h	
06h	7	MLUS	1h	
07h	7:0	Reserved 3	0h	
Mode page policy descriptor [1]				
08h	5:0	Policy page code	8h	Contains information describing the mode page policy for caching mode page.
08h	7:6	Reserved1	0h	
09h	7:0	Policy subpage code	0h	
0Ah	1:0	Mode page policy	0h	
0Ah	6:2	Reserved 2	0h	
0Ah	7	MLUS	00h	
0Bh	7:0	Reserved 3	0h	
Mode page policy descriptor [2]				
0Ch	5:0	Policy page code	Ah	Contains information describing the mode page policy for control mode page.
0Ch	7:6	Reserved 1	0h	
0Dh	7:0	Policy subpage code	0h	
0Eh	1:0	ModePagePolicy	0h	
0Eh	6:2	Reserved 2	0h	
0Eh	7	MLUS	0h	
0Fh	7:0	Reserved 3	0h	

Table 38: Block Limits VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	B0h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	3Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	Reserved	–	–
05h	7:0	MAXIMUM COMPARE AND WRITE LENGTH	0h	This field is set to 0, if the device server does not support this command.
06h	15:0	OPTIMAL TRANSFER LENGTH GRANULARITY	01h	This field indicates the optimal transfer length granularity in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command.
08h	31:0	MAXIMUM TRANSFER LENGTH	0h	This field indicates the maximum transfer length in blocks that the device server accepts for a single ORWRITE command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDWRITEREAD command, or XPWRITE command.
0Ch	31:0	OPTIMAL TRANSFER LENGTH	80h	This field indicates the optimal transfer length in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command.

Table 38: Block Limits VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
10h	31:0	MAXIMUM PREFETCH XDREAD XDWRITE TRANSFER LENGTH	100h	This field indicates: a) the maximum transfer length in blocks that the device server accepts for a single PREFETCH command b) if the XOR control mode page is implemented, then the maximum value supported by the MAXIMUM XOR WRITE SIZE field in the XOR control mode page. c) if the XOR control mode page is not implemented, then the maximum transfer length in blocks that the device server accepts for a single XDWRITE command or XDREAD command. The device server should set this field to less than or equal to the MAXIMUM TRANSFER LENGTH field.
14h	31:0	MAXIMUM UNMAP LBA COUNT	FFFFFFFFh	This field indicates the maximum number of LBAs that may be unmapped by an UNMAP command. If the number of LBAs that may be unmapped by an UNMAP command is constrained only by the amount of data that may be contained in the UNMAP parameter list, then the device server shall set this field to FFFF_FFFFh. If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.
18h	31:0	MAXIMUM UNMAP BLOCK DESCRIPTOR COUNT	10h	This field indicates the maximum number of unmap block descriptors that shall be contained in the parameter data transferred to the device server for an UNMAP command. If there is no limit on the number of unmap block descriptors contained in the parameter data, then the device server shall set this field to FFFF_FFFFh. If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.
1Ch	31:0	OPTIMAL UNMAP GRANULARITY	1h	This field indicates the optimal granularity in logical blocks for unmap requests. An unmap request with a number of logical blocks that is not a multiple of this value may result in UNMAP operations on fewer LBAs than requested. If this field is set to 0000_0000h, then the optimal unmap granularity is not specified.
20h	30:0	UNMAP GRANULARITY ALIGNMENT	0h	This field indicates the LBA of the first logical block to which the OPTIMAL UNMAP GRANULARITY field applies. The unmap granularity alignment is used to calculate an optimal unmap request starting LBA as follows: Optimal unmap request starting LBA = (n × OPTIMAL UNMAP GRANULARITY) + UNMAP GRANULARITY ALIGNMENT Where n is 0 or any positive integer value.

Table 38: Block Limits VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
20h	31	Reserved	–	–

Table 39: Block Device Characteristics

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	000h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	B1h	This fields identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	3Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	15:0	MEDIUM ROTATION RATE	0001h	0001h means device is a non-rotating medium (for example, solid state).
06h	7:0	Reserved	–	–
07h	3:0	NOMINAL FORM FACTOR	00h	This field indicates the nominal form factor of the device containing the logical unit.
07h	7:4	Reserved	–	–

Table 40: Logical Block Provisioning

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	000h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	B2h	This fields identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	04h	This field indicates the length in bytes of the VPD parameters that follow this field.

Table 40: Logical Block Provisioning (Continued)

Offset	Bit	Field	Default Value	Description
04h	7:0	THRESHOLD EXPONENT	16h	This field indicates the threshold set size in LBAs as a power of 2.
05h	0	DP	00h	A descriptor present (DP) bit set to 0 indicates that a PROVISIONING GROUP DESCRIPTOR is not present.
05h	1	ANC_SUP	00h	This bit set to 0 indicates that the device server does not support anchored LBAs.
05h	5:2	Reserved	–	–
05h	6	TBPWS	00h	This bit set to 0 indicates that the device server does not support the use of the WRITE SAME (16) command to unmap LBAs.
05h	7	TPU	01h	This bit set to 1 indicates that the device server supports the UNMAP command.
06h	7:0	Reserved	–	–
07h	7:0	Reserved	–	–

When the EVPD bit is set to 0 and page code = 0, the standard INQUIRY DATA is responded to INQUIRY command. The standard INQUIRY DATA format is shown in the following table:

Table 41: Standard Inquiry Data

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	6:0	Reserved	–	–
01h	7	RMB	0h	A removable medium (RMB) bit set to 0 indicates that the medium is not removable.
02h	7:0	VERSION	6h	This field indicates the implemented version of this standard. This field set to 06h means the conformance to SPC.
03h	3:0	RESPONSE DATA FORMAT	2h	This field value of two indicates that the data shall be in the format defined in SPC.
03h	7:4	NA1	0h	Not available in UFS standard
04h	7:0	ADDITIONAL LENGTH	1Fh	This field indicates the length in bytes of the remaining standard INQUIRY data.
05h	7:0	NA2	0h	Not available in UFS standard
06h	7:0	NA3	0h	Not available in UFS standard
07h	0	NA4	0h	Not available in UFS standard

Table 41: Standard Inquiry Data (Continued)

Offset	Bit	Field	Default Value	Description
07h	1	CMDQUE	1h	This bit is set to 1 indicating that the logical unit supports the command management model (SAM).
07h	7:2	NA5	0h	Not available in UFS standard
08h	15:0	VENDOR IDENTIFICATION	–	This field contains left-aligned ASCII data identifying the vendor of the product.
10h	15:0	PRODUCT IDENTIFICATION	–	This field contains left-aligned ASCII data defined by the vendor.
20h	15:0	PRODUCT REVISION LEVEL	–	This field contains left-aligned ASCII data defined by the vendor.

The extended INQUIRY DATA format is shown in the following table:

Table 42: Extended Inquiry Data

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device. 1Eh: Well-known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	86h	This field identifies the VPD page.
02h	15:0	PAGE LENGTH	3Ch	The PAGE LENGTH field specifies the length of the VPD page data.
04h	7:6	ACTIVATE MICROCODE	B0h	This field indicates how a device server activates microcode and establishes a unit attention condition when a WRITE BUFFER command with the download microcode mode set to 05h or 07h is processed.
04h	5:0	Reserved	–	–
05h	7:6	Reserved	–	–
05h	5:0	FEATURES SUPPORT	37h	These fields indicate if some specific functions are supported by the device.
06h	7:1	Reserved	–	–
06h	0	V_SUP	1h	This bit is set to 1 when the device server supports a volatile cache and the applicable command standard defines features using this cache.
07h	7:5	Reserved	–	–
07h	4	P_I_I_SUP	0h	This bit is set to 0, indicating that the logical unit does not support protection information intervals.

Table 42: Extended Inquiry Data (Continued)

Offset	Bit	Field	Default Value	Description
07h	3:0	Reserved	–	–
08h	7:5	Reserved	–	–
08h	4	R_SUP	0h	This bit is set to 0, indicating that the device server does not support referrals.
08h	3:0	Reserved	–	–
09h	7:4	Reserved	–	–
09h	3:0	MULTI I_T NEXUS MICROCODE DOWNLOAD	5h	This field indicates how the device server handles concurrent attempts to download microcode using the WRITE BUFFER command from multiple I_T nexuses.
10h	15:0	EXTENDED SELF_TEST COMPLETION MINUTES	0h	A value of 0h indicates that the EXTENDED SELF-TEST COMPLETION MINUTES field is not supported.
12h	7:0	Reserved	–	–

Electrical Specifications

According to JEDEC UFS v3.1 specification, power-up timing starts when the supply voltage crosses 300mV and ends when it reaches the minimum operating value. Micron device only supports V_{CC} and V_{CCQ}. V_{CCQ2} is not used.

Table 43: Power Supply Parameters

Parameter	Symbol	Min	Max	Unit
V_{CC} operating range	V_{CC}	2.4	2.7	V
		2.7	3.6	
V_{CCQ} operating range	V_{CCQ}	1.14	1.26	–
V_{CCQ2} operating range	V_{CCQ2}	–	–	–
Supply power-up timing for 3.3V	^{t}PRUH	–	35	ms
Supply power-up timing for 1.8V	^{t}PRUL	–	–	–
Supply power-up timing for 1.2V	^{t}PRUV	–	20	ms

Table 44: Reference Clock Parameters

Parameter	Symbol	Min	Max	Units
Frequency	^{f}ref	19.2 26 38.4		MHz
Frequency error	^{f}ERROR	–150	+150	ppm
Input HIGH voltage	V_{IH}	0.65 × V_{CCQ}	–	V
Input LOW voltage	V_{IL}	–	0.35 × V_{CCQ}	V
Input clock rise time	^{t}IRISE	–	2	ns
Input clock fall time	^{t}IFALL	–	2	ns
Duty cycle	^{t}DC	45	55	%
Phase noise	N	–	–66	dBc
Noise floor density	Ndensity	–	–140	dBc/Hz
Input impedance	RL_{RX}	100	–	kΩ
	CL_{RX}	–	5	pF

Note: 1. ^{t}RSTW MIN is 1.1µs.

Revision History

Rev. G – 10/2023

- Updated Performance/Current Consumption – Product Revision Level 030x: Removed the first paragraph
- Updated Device Health Descriptor table in UFS Descriptors: Added note 1
- Updated Attributes table in UFS Flags, Attributes, and Commands: Added note 5 to IDN 19h and 1Bh

Rev. F – 09/2023

- Removed references to 050x.
- Updated performance and consumption values in tables 5, 6, 7.
- Updated UFS attributes in table 28.

Rev. E – 05/2023

- Added Performance/Current Consumption - Product Revision Level 030x/050x.
- Revised title for Performance/Current Consumption - Product Revision Level 010x.
- Revised Device Descriptor Table to add PRL 010x and PRL 030x/050x.
- Revised Notes for Device Descriptor Table.
- Reformat tables for consistency and to improve presentation

Rev. D – 12/2022

- Preliminary to Production
- Reformat tables for consistency and to improve presentation

Rev. C – 12/2022

- Removed engineering sample (ES) designation from part numbers
- Added Performance throttling notification under Features
- Updated Features Note 3
- Updated Performance table values
- Updated UFS Performance and Current Consumption section
- Updated Active Current Consumption table Note 2
- Updated Architecture section
- Updated Geometry Descriptor table
- Added Note 2 to Unit Descriptor table
- Added Note 1 to Serial Number String Descriptor table
- Updated 0Dh and 0Eh descriptions in Attributes table
- Added Notes 3 and 4 with references to Attributes table
- Added Note 1 to Reference Clock Parameters table

Rev. B – 07/2022

- Updated status to Preliminary
- Updated UFS performance values in Table 2
- Updated Figure 2 values
- Updated default value for offset 1Ch in Table 13
- Updated information for offset 09h and 19h:22h in Table 15

- Updated values in Table 19
- Updated values for IDN 12h and 13h in Table 24
- Updated description for 0Ah in Table 25
- Updated default values and description for IDNs 19h, 1Ah, and 1Bh in Table 25
- Updated default value for offset 02h in Table 32

Rev. A – 05/2022

- Initial release

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