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Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Datasheet

iWave Global

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1. INTRODUCTION

1.1 Purpose

This document is the datasheet for the **Zynq Ultrascale+ MPSoC System on Module** based on the Xilinx Zynq Ultrascale+ MPSoC (ZU11/17/19EG). This board is fully supported iWave Global. This Guide provides detailed information on the overall design and usage of the Zynq Ultrascale+ MPSoC System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The **Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM** SOM is an extension of **Zynq Ultrascale+ MPSoC. Zynq Ultrascale+ MPSoC SOM** has a form factor of 110mm x 75mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors and Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Zynq Ultrascale+ MPSoC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NPTH	Non Plated Through hole
PCB	Printed Circuit Board

Acronyms	Abbreviations
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminology description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/Output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

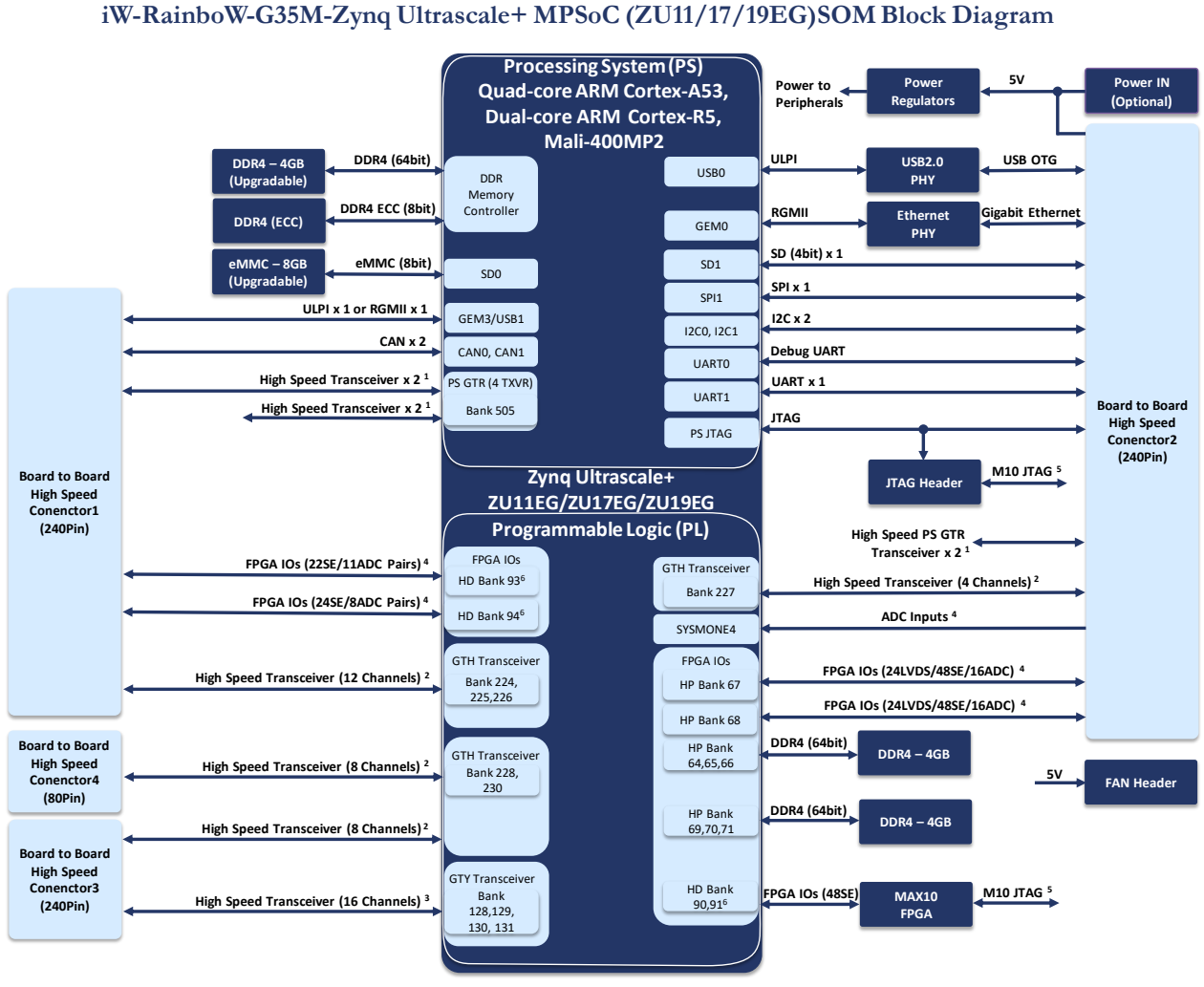
1.5 References

- Zynq Ultrascale+ MPSoC Technical Reference Manual
- Zynq Ultrascale+ MPSoC Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Zynq Ultrascale+ MPSoC (ZU11/17/19EG) Block Diagram



[1] PS GTR Transceiver supports data rates up to 6Gb/s and can be configured as PCIe/SATA/USB3.0/DisplayPort/Ethernet SGMII.
[2] PL GTH Transceiver supports data rates up to 16.3Gb/s.
[3] PL GTY Transceiver supports data rates up to 32.75Gb/s
[4] SYSMONE4 supports 10bit 200KSPS ADC and supports upto 17 Analog Inputs (One dedicated Analog input and 16 auxiliary analog input from any PL BANKs)
[5] The MAX10 JTAG Signals and the PS JTAG Signals are connected to JTAG Connector in JTAG Chain.
[6] In ZU11EG MPSoC device, the PL Bank90, 91, 93 & 94 is called as PL Bank88, 89, 90 & 91 respectively. Only the Bank Numbering is different and all other functionalities remain same.

Figure 1: Block Diagram

2.2 Zynq Ultrascale+ MPSoC SOM features.

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM supports the following features.

SoC

- Xilinx Zynq Ultrascale+ MPSoC.
  - Compatible Zynq Ultrascale+ MPSoC Family (FFVC1760) – ZU11EG, ZU17EG, ZU19EG Programming Logic with up to 1.1M Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and Mali™-400 MP2 Graphics Processor.

PMIC

- Dialog's DA9062 PMIC with RTC.

Memory

- 4GB DDR4 SDRAM (64bit) with ECC for PS (Expandable)
- 4GB DDR4 SDRAM1 (64bit) for PL (Expandable)
- 4GB DDR4 SDRAM2 (64bit) for PL (Expandable)
- 8GB eMMC Flash (Expandable)

Other On SOM Features

- Gigabit Ethernet PHY Transceiver
- USB2.0 Transceiver
- JTAG Header
- Fan Header

Board-to-Board Connector1 Interfaces (240pin)

From PS Block

- PS-GTR High Speed Transceivers (upto 6Gbps) x 2
- RGMII Interface or ULPI Interface x 1 Port
- CAN x 2 Ports

From PL Block

- PL-GTH High Speed Transceivers (upto 16.3Gbps) x 12
- PL IOs - HD Bank93[2,3]
  - Upto 11 DIFF IOs/22 Single ended (SE) IOs
    - Upto 3 HDGC Global Clock Input pins (LVDS/SE)
    - Upto 11 ADC Input pins (Differential/Single Ended)

- PL IOs - HD Bank94[2, 3]
  - Upto 12 DIFF IOs/24 Single Ended (SE) IOs
    - Upto 4 HDGC Global Clock Input pins (LVDS/SE)
    - Upto 8 ADC Input pins (Differential/Single Ended)

Board-to-Board Connector2 Interfaces (240pin)

From PS Block

- PS-GTR High Speed Transceivers (upto 6Gbps) x 2
- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port
- SPI x 1 Port
- Debug UART x 1 Port
- Data UART x 1 Port
- I2C x 2 Ports
- PS JTAG

From PL Block

- PL-GTH High Speed Transceivers (upto 16.3Gbps) x 4
- PL IOs - HP Bank67[2,]
  - Upto 24 LVDS IOs/48 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 16 ADC Input pins (Differential/Single Ended)
- PL IOs - HP Bank68[2,]
  - Upto 24 LVDS IOs/48 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 16 ADC Input pins (Differential/Single Ended)

Board-to-Board Connector3 Interfaces (240pin)

From PL Block

- PL-GTY High Speed Transceivers (upto 32.75Gbps) x 16
- PL-GTH High Speed Transceivers (upto 16.3Gbps) x 8

Board-to-Board Connector4 Interfaces (80pin)

From PL Block

- PL-GTH High Speed Transceivers (upto 16.3Gbps) x 8

General Specification

- Power Supply : 5V (from Board-to-Board Connector2)
- Form Factor: 110mm x 75mm

In Zynq Ultrascale+ MPSoC PS, GEM3 RGMII interface & USB1 ULPI interface signals are multiplexed in same pins and so either GEM3 or USB1 only can be supported.

[2] In Zynq Ultrascale+ MPSoC SOM, PL HP BANK67 & 68 and PL HD BANK93 & 94 supports variable IO voltage setting and configurable through software.

[3] In ZU11EG MPSoC device, the PL Bank90, 91, 93 & 94 is called as PL Bank88, 89, 90 & 91 respectively. Only the Bank Numbering is different and all other functionalities remain same.

Important Note: In ZU19/17/11EG MPSoC SOM, All the GTY, GTH, GTR transceivers and PL Bank pair's P & N (Intra pair) are length matched within 1ps with internal 19EG MPSoC package delay. Inter Pair length match is not done. To add delay tuning in carrier board wherever required.

2.3 Zynq Ultrascale+ MPSoC

Xilinx's SoC portfolio integrates the software programmability of a processor with the hardware programmability of an FPGA, providing unrivalled levels of system performance, flexibility, and scalability. Unlike traditional SoC processing solutions, the flexible programmable logic provides optimization and differentiation, allowing to add the peripherals and accelerators for a broad base of applications.

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM is based on Xilinx Zynq Ultrascale+ MPSoC (ZU11/17/19EG) with FFVC1760 package. Zynq Ultrascale+ MPSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. MPSoC's Processing system includes feature-rich Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz of Application processor, Dual-core ARM Cortex-R5 MPCore up to 600MHz and Mali™-400 MP2 of Graphics Processor. The Block Diagram of Zynq Ultrascale+ MPSoC from Xilinx website is shown below for reference.

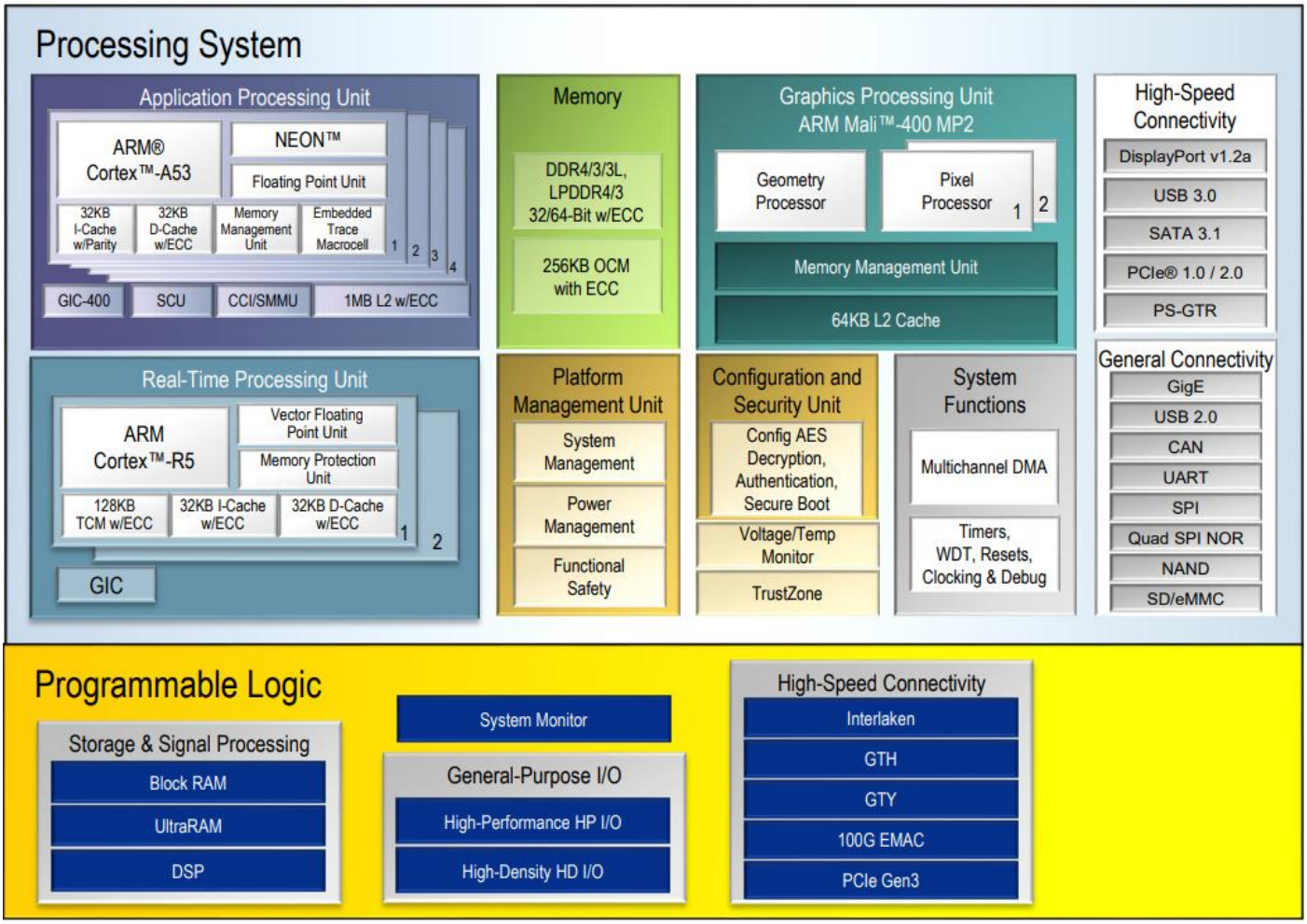


Figure 2: Zynq Ultrascale+ MPSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq Ultrascale+ MPSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq Ultrascale+ MPSoC SOM is compatible to ZU11EG, ZU17EG and ZU19EG MPSoC devices and feature comparison between these devices are shown below

	ZU11EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3;External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	Arm Mali™-400 MP2; 64KB L2 Cache		
System Logic Cells	6,53,100	9,26,194	11,43,450
CLB Flip-Flops	5,97,120	8,46,806	10,45,440
CLB LUTs	2,98,560	4,23,403	5,22,720
Distributed RAM (Mb)	9.1	8	9.8
Block RAM Blocks	600	796	984
Block RAM (Mb)	21.1	28	34.6
UltraRAM Blocks	80	102	128
UltraRAM (Mb)	22.5	28.7	36
DSP Slices	2,928	1,590	1,968
CMTs	8	11	11
Max. HP I/O	416	416	416
Max. HD I/O	96	96	96
System Monitor	2	2	2
GTH Transceiver 16.3Gb/s	32	32	32
GTY Transceiver 28Gb/s	16	16	16
Transceiver Fractional PLLs	24	36	36
PCIe Gen3 x16	4	4	5
150G Interlaken	1	2	4
100G Ethernet w/ RS-FEC	2	2	4

Figure 3: SoC Devices Comparison

The Zynq Ultrascale+ MPSoC's PS has 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for the PS peripheral interfaces. These 78 MIO pins are divided into three banks (PS BANK500, 501 & 502) and each bank includes 26 device pins. Since 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in MPSoC to route most of the IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Zynq Ultrascale+ MPSoC's PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, or • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

The Zynq Ultrascale+ MPSoC's PL Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-feature I/Os organized in banks of 24pins.

In Zynq Ultrascale+ MPSoC PL, each bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers.

Also, Zynq Ultrascale+ MPSoC supports three types of high-speed transceivers namely GTY, GTH and PS-GTR. These transceivers are arranged in groups of four known as a transceiver Quad. GTY & GTH transceivers are from PL and PS-GTR transceivers are from PS.

2.3.1 MPSoC Power

The Zynq Ultrascale+ MPSoC SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for MPSoC power management. In SOM, PS low-power domain, PS full-power domain & PL power domain supply voltage (VCC_PSINTLP, VCC_PSINTFP, VCCINT) is fixed to 0.85V or 0.9V based on the speed grade of the MPSoC. Also, all PS Bank (VCCO_PSIO) I/O voltage is fixed to 1.8V.

The I/O voltage of PL HP Banks (PL Bank 67 & 68) and PL HD Banks (PL Bank 93 & 94) which are connected to Board-to-Board Connectors are generated from PMIC LDO1 and LDO4 respectively. By default, HP Banks voltages are set to 1.0V & HD Banks voltages are set to 1.2V and configurable through software after bootup.

2.3.2 MPSoC Reset

The Zynq Ultrascale+ MPSoC SOM uses PMIC's Reset output (nRESET) for PS Power On Reset and connected to PS_POR_B pin of MPSoC. Also, it supports warm reset input from Board-to-Board Connector2 pin35 and connected to PS_SRST_B pin of MPSoC.

2.3.3 Reference Clocks

The Zynq Ultrascale+ MPSoC SOM supports on board clock oscillators for reference clock to different blocks of Zynq Ultrascale+ MPSoC. These reference clock details are mentioned in the below table.

Table 3: Zynq Ultrascale+ MPSoC SOM Reference Clock

Sl. No	On-SOM Oscillator Frequency	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description	Stability
1	33.3333 MHz	PS_REF_CLK	503	AC27	1.8V, LVCMOS	33.33MHz single ended reference clock for PS.	±50ppm
2	100MHz	IO_L5P_HDGC_AD7P_93	93	G7	1.8V[2], LVCMOS	100MHz single ended reference clock for PL. This is connected to PL Bank93 HDGC Global clock pin.	±25ppm
3	300MHz	IO_L13N_T2L_N1_GC_QBC_64	64	AT21	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM1. This is connected to PL Bank64 Global clock pins.	±100ppm
		IO_L13P_T2L_N0_GC_QBC_64		AT22			
4	300MHz	IO_L13N_T2L_N1_GC_QBC_69	69	D324	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM2. This is connected to PL Bank69 Global clock pins.	±100ppm
		IO_L13P_T2L_N0_GC_QBC_69		E32			

[1] *Important Note: I/O voltage of PL Bank93 is software configurable. Since this oscillator supports 1.8V to 3.3V VCC only, this reference clock can be used only if the I/O voltage of PL Bank93 is set between 1.8V to 3.3V.*

[2] *Mentioned voltage level is based on after uboot bootup I/O voltage set to PL Bank93.*

2.3.4 MPSoC Configuration & Status

The Zynq Ultrascale+ MPSoC uses multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the PS and can load and configure the PL or configuration of the PL can be deferred to a later stage.

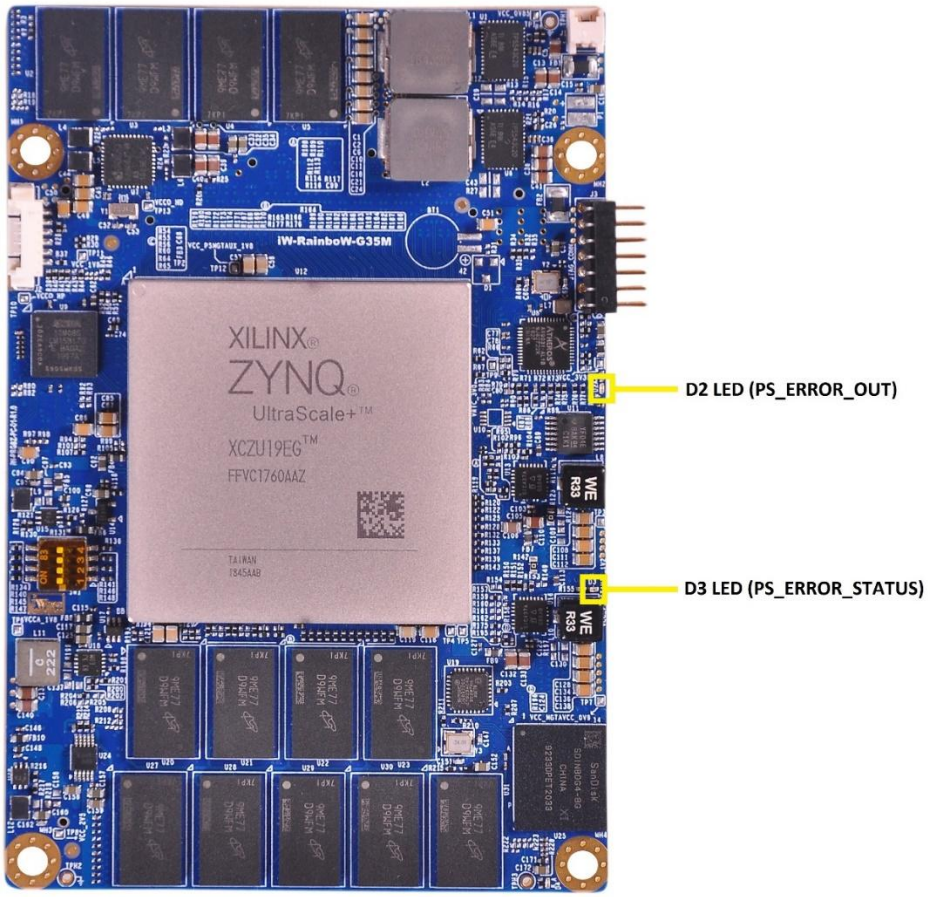


Figure 4: Error Status Indication LEDs

The Zynq Ultrascale+ MPSoC SOM supports two LEDs for the MPSoC error status indication namely PS_ERROR_OUT and PS_ERROR_STATUS. LED D2 is for PS_ERROR_OUT and it is asserted for accidental loss of power, a hardware error, or an exception in the PMU. LED D3 is for PS_ERROR_STATUS and it indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.

The Zynq Ultrascale+ MPSoC SOM supports three dedicated input and output configuration pins. By default, PUDC_B pin is connected to 1.8V(Weak pre configuration I/O pull-up resistors disabled), POR_OVERRIDE pin is connected to Ground (Standard PL power-on delay time) and PS-Done pin is connected to VCC_1V8 through 4.7K.

2.3.5 MPSoC Boot Mode Switch

The Zynq Ultrascale+ MPSoC always boots from PS first and configures the PL through software. MPSoC can support eMMC, SD1, USB0 & JTAG as boot device and configurable through mode pins. Upon device reset, MPSoC mode pins are read to determine the primary boot device

The Zynq Ultrascale+ MPSoC SOM supports Boot Mode switch (SW1) to select the required boot device. By default, eMMC is supported as boot device. Refer the below table to select the required boot device.

Table 4: Boot Mode Switch Truth Table

Zynq Ultrascale+ MPSoC Boot Mode	SW1 (4 Position Switch)				
	PS Mode 3	PS Mode 2	PS Mode 1	PS Mode 0	Switch Position Images
PS JTAG	OFF	OFF	OFF	OFF	
SD1	OFF	ON	OFF	ON	
eMMC (Default)	OFF	ON	ON	OFF	
USB0	OFF	ON	ON	ON	

2.3.6 MPSoC System Monitor/ADC

The Zynq Ultrascale+ MPSoC contain two System Monitor block (SYSMONE4), one in the PL (PL SYSMON) and another in the PS (PS SYSMON). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The PL SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature in the PL and several internal PL and PS power supply nodes. The PL SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any PL Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Zynq Ultrascale+ MPSoC SOM, 1.25V external voltage reference is supported.

The PS SYSMON uses 10-bit 1MSPS ADC to digitize the sensor inputs. It is located in the PS LPD and monitors two temperature points & several internal fixed voltage nodes. The PS has two temperature sensors, one is physically located in the PS SYSMON near the RPU. The second, remote sensor is located in the FPD near the APU. The ADC always uses an internally generated voltage reference.

2.4 PMIC with RTC

The Zynq Ultrascale+ MPSoC SOM supports Dialog semiconductor DA9062 PMIC. The I2C0 module of Zynq Ultrascale+ MPSoC PS is used for PMIC interface through MIO pins with I2C address 0x58.

PMIC's LDO1 is connected to I/O voltage of PL HP Banks (PL Bank 67 & 68) and by default set to 1.0V. Also, same PMIC LDO1 output is connected to I/O voltage of MAX 10 FPGA BANK8 which is interfaced to MPSoC PL HP Bank. The I/O voltage is configurable through software after bootup.

PMIC's LDO4 is connected to I/O voltage of PL HD Banks (PL Bank 90, 91, 93 & 94) and by default set to 1.2V. Also, same PMIC LDO4 output is connected to I/O voltage of MAX 10 FPGA Banks (BANK1A, 2, 3, 5 and 6) which are interface to MPSoC PL HD banks. The I/O voltage is configurable through software after bootup.

PMIC supports reset output and connected to Zynq Ultrascale+ MPSoC PS (PS_POR_B) for power on reset. Also, PMIC supports IRQ output for events indication and connected to MPSoC's PS GPIO (PS_MIO2_500).

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector2 pin68 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting

2.5 Memory

2.5.1 DDR4 SDRAM with ECC for PS

The Zynq Ultrascale+ MPSoC SOM supports 64bit, 4GB DDR4 RAM memory for MPSoC's PS. Four 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. Also, Zynq Ultrascale+ MPSoC SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 2400Mbps datarate. DDR4 memory is connected to the hard memory controller of the MPSoC PS. The RAM size can be expandable up to maximum of 8GB based on the availability of higher density 16bit DDR4 device.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.2 DDR4 SDRAM1 for PL

The Zynq Ultrascale+ MPSoC SOM supports 64bit, 4GB DDR4 RAM memory for MPSoC's PL. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for PL. These DDR4 devices operates at 2400Mbps datarate. In Zynq Ultrascale+ MPSoC SOM, Bank64, 65 & 66 is used for PL DDR4 interface. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Zynq Ultrascale+ MPSoC SOM supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank64 AT21 & AT22 dedicated clock input pins through AC Coupling capacitors.

Note: Zynq Ultrascale+ MPSoC SOM with -2 & -3 speed grade MPSoC can support upto 2666Mbps datarate for PL DDR4.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.3 DDR4 SDRAM2 for PL

The Zynq Ultrascale+ MPSoC SOM supports 64bit, 4GB DDR4 RAM memory for MPSoC's PL. Four 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 4GB for PL. These DDR4 devices operates at 2400Mbps datarate. In Zynq Ultrascale+ MPSoC SOM, Bank69, 70 & 71 is used for PL DDR4 interface. The RAM size can be expandable up to maximum of 16GB based on the availability of higher density 16bit DDR4 device.

The Zynq Ultrascale+ MPSoC SOM supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank69 D32 & E32 dedicated clock input pins through AC Coupling capacitors.

Note: Zynq Ultrascale+ MPSoC SOM with -2 & -3 speed grade MPSoC can support upto 2666Mbps datarate for PL DDR4.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.4 eMMC Flash

The Zynq Ultrascale+ MPSoC SOM supports 8GB eMMC Flash memory for Boot & Storage of Zynq Ultrascale+ MPSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the MPSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
M6	eMMC_CLK(PS_MIO22_500)	PS_MIO22_500	500	AH32	O, 1.8V LVCMOS	eMMC Clock
M5	eMMC_CMD(PS_MIO21_500)	PS_MIO21_500	500	AF35	IO, 1.8V LVCMOS	eMMC Command for device initialization and command transfer
A3	eMMC_DATA0(PS_MIO13_500)	PS_MIO13_500	500	AD34	IO, 1.8V LVCMOS	eMMC Bidirectional Data 0.
A4	eMMC_DATA1(PS_MIO14_500)	PS_MIO14_500	500	AJ32	IO, 1.8V LVCMOS	eMMC Bidirectional Data 1.
A5	eMMC_DATA2(PS_MIO15_500)	PS_MIO15_500	500	AD35	IO, 1.8V LVCMOS	eMMC Bidirectional Data 2.
B2	eMMC_DATA3(PS_MIO16_500)	PS_MIO16_500	500	AJ31	IO, 1.8V LVCMOS	eMMC Bidirectional Data 3.
B3	eMMC_DATA4(PS_MIO17_500)	PS_MIO17_500	500	AJ30	IO, 1.8V LVCMOS	eMMC Bidirectional Data 4.
B4	eMMC_DATA5(PS_MIO18_500)	PS_MIO18_500	500	AE34	IO, 1.8V LVCMOS	eMMC Bidirectional Data 5.
B5	eMMC_DATA6(PS_MIO19_500)	PS_MIO19_500	500	AE35	IO, 1.8V LVCMOS	eMMC Bidirectional Data 6.
B6	eMMC_DATA7(PS_MIO20_500)	PS_MIO20_500	500	AH34	IO, 1.8V LVCMOS	eMMC Bidirectional Data 7.
K5	eMMC_RST(PS_MIO23_500)	PS_MIO23_500	500	AG35	O, 1.8V LVCMOS	eMMC Reset

2.6 On SOM Features

2.6.1 JTAG Header

The Zynq Ultrascale+ MPSoC SOM supports 14Pin JTAG Header (J3) for JTAG interface. JTAG Interface Signals from MPSoC's PS BANK503 & MAX 10 FPGA is daisy chained and connected to this Header. The Zynq Ultrascale+ MPSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale MPSoC. These JTAG interface signals are at 1.8V Voltage level.

The JTAG Header (J3) is physically located on topside of the SOM as shown below. JTAG-HS2 Programming Cable can be directly connected to this JTAG Header. JTAG interface signals are also connected to Board-to-Board Connector2 to access from carrier board.

Number of Pins - 14

Connector Part - 877601416 from Molex

Mating Connector - 0791077006 from Molex

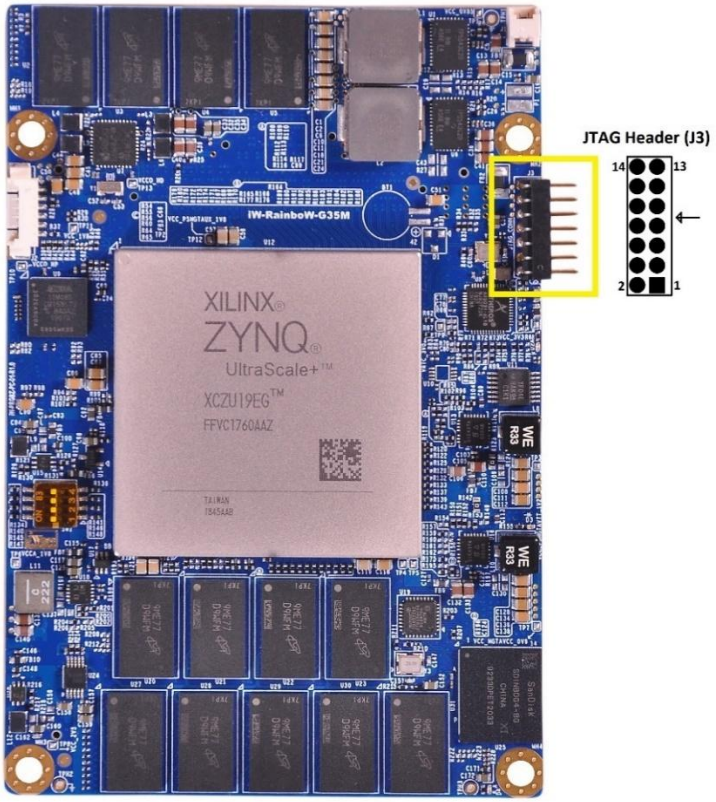


Figure 5: JTAG Header

Table 5: JTAG Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	-	-	NC.
2	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	GND	Power	Ground.
4	PS_JTAG_TMS	I, 1.8V LVCMOS/4.7K PU	JTAG Test Mode Select.
5	GND	Power	Ground.
6	PS_JTAG_TCK	I, 1.8V LVCMOS/4.7K PU	JTAG Test Clock.
7	GND	Power	Ground.
8	JTAG_TDO	O, 1.8V LVCMOS	JTAG Test Data Output.
9	GND	Power	Ground.
10	JTAG_TDI	I, 1.8V LVCMOS/4.7K PU	JTAG Test Data Input.
11	GND	Power	Ground.
12	-	-	NC.
13	GND	Power	Ground.
14	-	-	NC.

2.6.2 Fan Header

The Zynq Ultrascale+ MPSoC SOM supports a Fan Header (J1) to connect cooling Fan if required. The Fan Header (J1) is physically located on topside of the SOM as shown below.

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

Compatible Fan (Example) - AFB0505MB from Delta Electronics

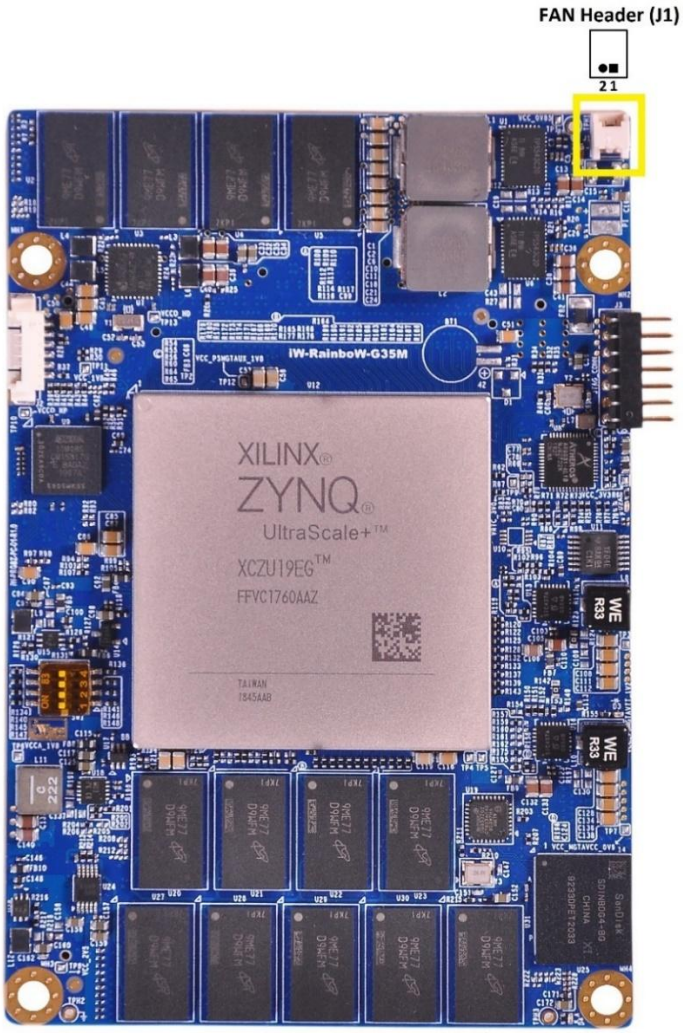


Figure 6: Fan Header

Table 6: Fan Header Pinout

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	VCC_5V	-	-	-	O, 5V Power	Supply Voltage.
2	GND	-	-	-	Power	Ground.

2.7 Board-to-Board Connector 1

The Zynq Ultrascale+ MPSoC SOM supports two 240 pin high speed ruggedized terminal strip connectors, One 240pin High-Speed High-Density connector and One 80pin High-Speed High-Density connector for interfaces expansion. All the effort is made in Zynq Ultrascale+ MPSoC SOM design to provide the maximum interfaces of Zynq Ultrascale+ MPSoC to the carrier board by adding these two Board to Board Connectors.

The Zynq Ultrascale+ MPSoC SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J7) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - QTH-120-01-L-D-A from Samtech
Mating Connector - QSH-120-01-L-D-A from Samtech
Staking Height - 5mm

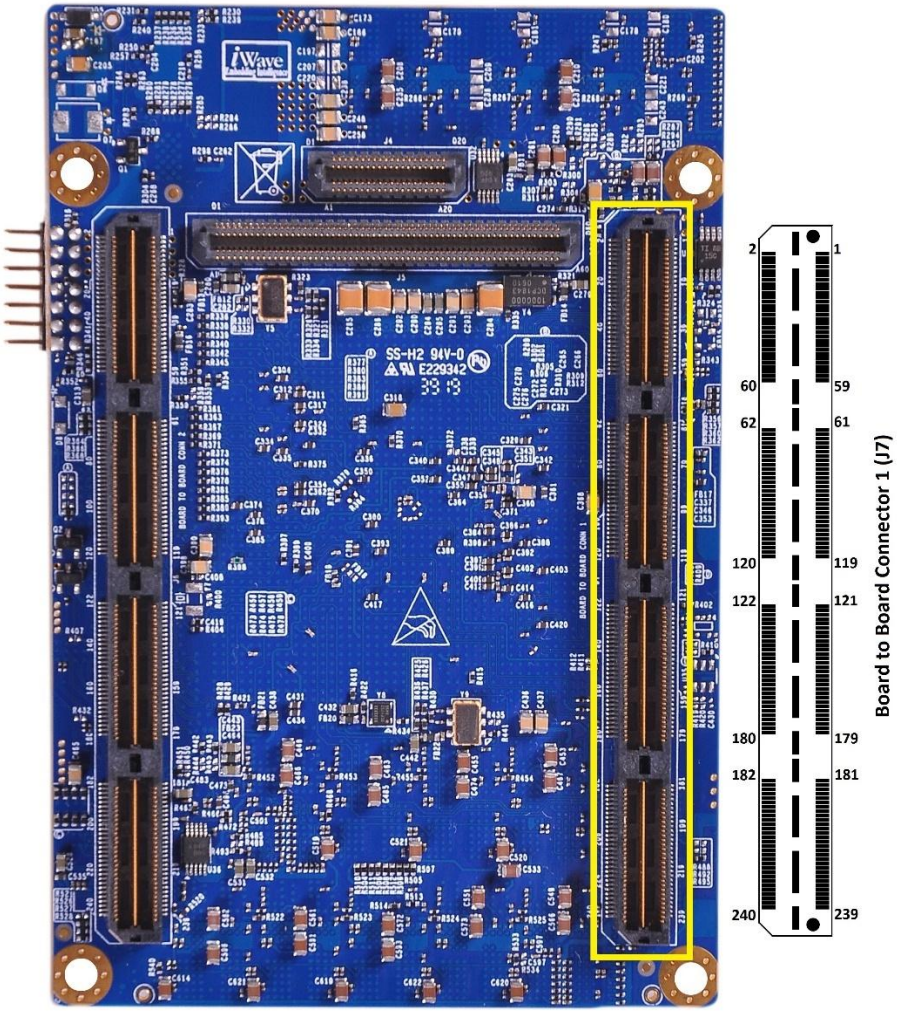


Figure 7: Board-to-Board Connector 1

Table 7: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
GTHTXP0_224	3	4	GTREFCLK0P_224
GTHTXN0_224	5	6	GTREFCLK0N_224
GND	7	8	GND
GTHTXP1_224	9	10	NC
GTHTXN1_224	11	12	PL_B8_LVDS93_L11P
GND	13	14	PL_A8_LVDS93_L11N
GTHRXN1_224	15	16	PL_J9_LVDS93_L3P
GTHRXP1_224	17	18	PL_H9_LVDS93_L3N
GND	19	20	GND
GTHRXN0_224	21	22	PL_C8_LVDS93_L8N_HDGC
GTHRXP0_224	23	24	PL_D8_LVDS93_L8P_HDGC
GND	25	26	GND
PL_J8_LVDS93_L2P	27	28	PL_E9_LVDS93_L4N
PL_H8_LVDS93_L2N	29	30	PL_F9_LVDS93_L4P
PL_B7_LVDS93_L10P	31	32	PL_D9_LVDS93_L12P
PL_A7_LVDS93_L10N	33	34	PL_C9_LVDS93_L12N
GND	35	36	GND
GTHTXP2_224	37	38	PL_E6_LVDS93_L9P
GTHTXN2_224	39	40	PL_D6_LVDS93_L9N
GND	41	42	PL_F6_LVDS93_L1N
GTHTXP3_224	43	44	PL_G6_LVDS93_L1P
GTHTXN3_224	45	46	PL_A5_LVDS94_L12P
GND	47	48	PL_A4_LVDS94_L12N
GTHRXN3_224	49	50	PL_B2_LVDS94_L9P
GTHRXP3_224	51	52	PL_B1_LVDS94_L9N
GND	53	54	GND
GTHRXN2_224	55	56	PL_D7_LVDS93_L7N_HDGC
GTHRXP2_224	57	58	PL_E7_LVDS93_L7P_HDGC
GND	59	60	GND
GND	61	62	GND
PS_MGTRTXP0_505	63	64	GTREFCLK1P_224
PS_MGTRTXN0_505	65	66	GTREFCLK1N_224
GND	67	68	GND
NC	69	70	PL_B6_LVDS94_L11P
NC	71	72	PL_B5_LVDS94_L11N
GND	73	74	PL_B3_LVDS94_L10P
PS_MGTREFCLK0N_505	75	76	PL_A3_LVDS94_L10N
PS_MGTREFCLK0P_505	77	78	NC
GND	79	80	GND
PS_MGTRRXN0_505	81	82	PL_F8_LVDS93_L6N_HDGC
PS_MGTRRXP0_505	83	84	PL_G8_LVDS93_L6P_HDGC
GND	85	86	GND
PL_F5_LVDS94_L1P	87	88	PL_E2_LVDS94_L3N
PL_F4_LVDS94_L1N	89	90	PL_E3_LVDS94_L3P

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
PL_E5_LVDS94_L2P	91	92	PL_E1_LVDS94_L4P
PL_E4_LVDS94_L2N	93	94	PL_D1_LVDS94_L4N
GND	95	96	GND
GTHTXP0_225	97	98	GTREFCLK0P_225
GTHTXN0_225	99	100	GTREFCLK0N_225
GND	101	102	GND
GTHTXP1_225	103	104	NC
GTHTXN1_225	105	106	NC
GND	107	108	NC
GTHRXN1_225	109	110	NC
GTHRXP1_225	111	112	NC
GND	113	114	GND
GTHRXN0_225	115	116	PL_D3_LVDS94_L5N_HDGC
GTHRXP0_225	117	118	PL_D4_LVDS94_L5P_HDGC
GND	119	120	GND
GND	121	122	GND
GTHTXP2_225	123	124	PL_D2_LVDS94_L6P_HDGC
GTHTXN2_225	125	126	PL_C1_LVDS94_L6N_HDGC
GND	127	128	NC
GTHTXP3_225	129	130	PL_C6_LVDS94_L7P_HDGC
GTHTXN3_225	131	132	PL_C5_LVDS94_L7N_HDGC
GND	133	134	NC
GTHRXN3_225	135	136	NC
GTHRXP3_225	137	138	NC
GND	139	140	GND
GTHRXN2_225	141	142	PL_C3_LVDS94_L8N_HDGC
GTHRXP2_225	143	144	PL_C4_LVDS94_L8P_HDGC
GND	145	146	GND
NC	147	148	NC
NC	149	150	NC
NC	151	152	NC
NC	153	154	NC
GND	155	156	GND
PS_MGTRTXP1_505	157	158	GTREFCLK1P_225
PS_MGTRTXN1_505	159	160	GTREFCLK1N_225
GND	161	162	GND
NC	163	164	NC
NC	165	166	NC
GND	167	168	NC
PS_MGTREFCLK1N_505	169	170	PL_PCIe_RSTn
PS_MGTREFCLK1P_505	171	172	NC
GND	173	174	GND
PS_MGTRRXN1_505	175	176	NC
PS_MGTRRXP1_505	177	178	SPI0_SS2(PS_MIO1_500)
GND	179	180	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	181	182	GND
GTHTXP0_226	183	184	GTREFCLK0P_226
GTHTXN0_226	185	186	GTREFCLK0N_226
GND	187	188	GND
GTHTXP1_226	189	190	GEM3_TX_CLK/USB1_CLK(PS_MIO64_502)
GTHTXN1_226	191	192	GEM3_TXD0/USB1_DIR(PS_MIO65_502)
GND	193	194	GEM3_TXD1/USB1_DATA2(PS_MIO66_502)
GTHRXN1_226	195	196	GEM3_TXD2/USB1_NXT(PS_MIO67_502)
GTHRXP1_226	197	198	GEM3_TXD3/USB1_DATA0(PS_MIO68_502)
GND	199	200	GND
GTHRXN0_226	201	202	NC
GTHRXP0_226	203	204	NC
GND	205	206	GND
CAN0_RX(PS_MIO38_501)	207	208	NC
CAN0_TX(PS_MIO39_501)	209	210	GEM3_TX_CTL/USB1_DATA1(PS_MIO69_502)
CAN1_RX(PS_MIO41_501)	211	212	GEM3_RX_CLK/USB1_STP(PS_MIO70_502)
CAN1_TX(PS_MIO40_501)	213	214	GEM3_RX_CTL/USB1_DATA7(PS_MIO75_502)
GND	215	216	GND
GTHTXP2_226	217	218	GTREFCLK1P_226
GTHTXN2_226	219	220	GTREFCLK1N_226
GND	221	222	GND
GTHTXP3_226	223	224	GEM3_RXD0/USB1_DATA3(PS_MIO71_502)
GTHTXN3_226	225	226	GEM3_RXD1/USB1_DATA4(PS_MIO72_502)
GND	227	228	GEM3_RXD2/USB1_DATA5(PS_MIO73_502)
GTHRXN3_226	229	230	GEM3_RXD3/USB1_DATA6(PS_MIO74_502)
GTHRXP3_226	231	232	SOMPWR_EN
GND	233	234	GND
GTHRXN2_226	235	236	NC
GTHRXP2_226	237	238	NC
GND	239	240	GND

2.7.1 PS Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Zynq Ultrascale+ MPSoC's PS is explained in the following section.

2.7.1.1 PS GTR Transceivers

The Zynq Ultrascale+ MPSoC supports four Multi-Gigabit PS-GTR transceivers with data rate from 1.25Gbps to 6.0Gbps. This PS-GTR transceiver lanes provide I/O path for MPSoC MAC controllers and their link partner outside. At any given time, these four lanes can be used for any of below mentioned peripheral standards.

- x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
- 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
- 1 or 2 USB3.0 channels at 5.0Gb/s
- 1-4 Ethernet SGMII channels at 1.25Gb/s

The available peripheral standard option for each PS-GTR transceiver lane in Zynq Ultrascale+ MPSoC is shown below. This is user programmable via the high-speed I/O multiplexer (HS-MIO) of MPSoC.

PS Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	-
USB1	-	-	-	USB1
SGMII0	SGMII0	-	-	-
SGMII1	-	SGMII1	-	-
SGMII2	-	-	SGMII2	-
SGMII3	-	-	-	SGMII3

The Zynq Ultrascale+ MPSoC SOM supports two PS GTR transceivers (Lane0 & Lane1) on Board-to-Board Connector1 and another two PS GTR transceivers (Lane2 & Lane3) on Board-to-Board Connector2. Each PS GTR transceiver lane supports one dedicated reference clock input pair with the ability to share reference clocks between lanes.

In Zynq Ultrascale+ MPSoC SOM, the end user is responsible for sourcing the reference clocks to the PS-GTR lanes through Board-to-Board Connectors. This gives full flexibility to end user to select the required peripheral standards on PS-GTR lanes.

For more details on PS-GTR transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
PS-GTR Lane0 Pins						
63	PS_MGTRTXP0_505	PS_MGTRTXP0_505	505	AH39	O, DIFF	PS-GTR Lane0 High speed differential transmitter positive.
65	PS_MGTRTXN0_505	PS_MGTRTXN0_505	505	AH40	O, DIFF	PS-GTR Lane0 High speed differential transmitter negative.
81	PS_MGTRRXN0_505	PS_MGTRRXN0_505	505	AG42	I, DIFF	PS-GTR Lane0 High speed differential receiver negative.
83	PS_MGTRRXP0_505	PS_MGTRRXP0_505	505	AG41	I, DIFF	PS-GTR Lane0 High speed differential receiver positive.
75	PS_MGTREFCLK0N_505	PS_MGTREFCLK0N_505	505	AG38	I, DIFF	PS-GTR Lane0 differential reference clock negative.
77	PS_MGTREFCLK0P_505	PS_MGTREFCLK0P_505	505	AG37	I, DIFF	PS-GTR Lane0 differential reference clock positive.
PS-GTR Lane1 Pins						
157	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	AF39	O, DIFF	PS-GTR Lane1 High speed differential transmitter positive.
159	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	AF40	O, DIFF	PS-GTR Lane1 High speed differential transmitter negative.
175	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	AE42	I, DIFF	PS-GTR Lane1 High speed differential receiver negative.
177	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	AE41	I, DIFF	PS-GTR Lane1 High speed differential receiver positive.
169	PS_MGTREFCLK1N_505	PS_MGTREFCLK1N_505	505	AE38	I, DIFF	PS-GTR Lane1 differential reference clock negative.
171	PS_MGTREFCLK1P_505	PS_MGTREFCLK1P_505	505	AE37	I, DIFF	PS-GTR Lane1 differential reference clock positive.

2.7.1.2 RGMII/ULPI Interface

The Zynq Ultrascale+ MPSoC SOM supports RGMII or ULPI interface on Board-to-Board Connector1. In Zynq Ultrascale+ MPSoC PS, GEM3 RGMII interface and USB1 ULPI interface are multiplexed on the same pins. So, either one interface only can be used at a time. In Zynq Ultrascale+ MPSoC SOM, these MIO pins are directly connected from MPSoC to Board-to-Board connector1. If RGMII/ULPI interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.11** for available alternate functions.

The Zynq Ultrascale+ MPSoC gigabit Ethernet controller (GEM) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through any PL Bank IOs through EMIO interface in SOM.

The Zynq Ultrascale+ MPSoC USB2.0 OTG controller is capable for USB2.0 implementations as a host, a device, or On-the-Go. This controller uses the ULPI protocol to connect external ULPI PHY. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

For more details on RGMII/ULPI Interface pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
190	GEM3_TX_CLK/USB1_CLK(PS_MIO64_502)	PS_MIO64_502	502	AD32	O, 1.8V LVCMOS	GEM3 RGMII Transmit Clock. Or USB1 ULPI Clock.
192	GEM3_TXD0/USB1_DIR(PS_MIO65_502)	PS_MIO65_502	502	AE29	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA0. Or USB1 ULPI Direction Control.
194	GEM3_TXD1/USB1_DATA2(PS_MIO66_502)	PS_MIO66_502	502	AD33	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA1. Or USB1 ULPI Bi-Directional Data2.
196	GEM3_TXD2/USB1_NXT(PS_MIO67_502)	PS_MIO67_502	502	AE30	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA2. Or USB1 ULPI NXT.
198	GEM3_TXD3/USB1_DATA0(PS_MIO68_502)	PS_MIO68_502	502	AE33	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA3. Or USB1 ULPI Bi-Directional Data0.
210	GEM3_TX_CTL/USB1_DATA1(PS_MIO69_502)	PS_MIO69_502	502	AE32	O, 1.8V LVCMOS	GEM3 RGMII Transmit Control. Or USB1 ULPI Bi-Directional Data1.
212	GEM3_RX_CLK/USB1_STP(PS_MIO70_502)	PS_MIO70_502	502	AF30	I, 1.8V LVCMOS	GEM3 RGMII Receive Clock. Or USB1 ULPI STP.
214	GEM3_RX_CTL/USB1_DATA7(PS_MIO75_502)	PS_MIO75_502	502	AF33	I, 1.8V LVCMOS	GEM3 RGMII Receive control. Or USB1 ULPI Bi-Directional Data7.
224	GEM3_RXD0/USB1_DATA3(PS_MIO71_502)	PS_MIO71_502	502	AF31	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA0. Or USB1 ULPI Bi-Directional Data3.
226	GEM3_RXD1/USB1_DATA4(PS_MIO72_502)	PS_MIO72_502	502	AF32	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA1. Or USB1 ULPI Bi-Directional Data4.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
228	GEM3_RXD2/USB1_DATA5(PS_MIO73_502)	PS_MIO73_502	502	AG30	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA2. Or USB1 ULPI Bi-Directional Data5.
230	GEM3_RXD3/USB1_DATA6(PS_MIO74_502)	PS_MIO74_502	502	AG33	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA3. Or USB1 ULPI Bi-Directional Data6.

2.7.1.3 CAN Interface

The Zynq Ultrascale+ MPSoC SOM supports two CAN interfaces on Board-to-Board Connector1. The CAN0 & CAN1 controller of MPSoC's PS is used for CAN interface through MIO pins. This CAN controller is compatible with the ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. And it supports bit rates up to 1Mb/s.

If CAN interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section**Error! Reference source not found.** for available alternate functions.

For more details on CAN Interface pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
207	CAN0_RX(PS_MIO38_501)	PS_MIO38_501	501	R27	I, 1.8V LVCMOS	CAN0 Receive data.
209	CAN0_TX(PS_MIO39_501)	PS_MIO39_501	501	P29	O,1.8V LVCMOS	CAN0 Transmit data.
211	CAN1_RX(PS_MIO41_501)	PS_MIO41_501	501	P30	I, 1.8V LVCMOS	CAN1 Receive data.
213	CAN1_TX(PS_MIO40_501)	PS_MIO40_501	501	P28	O,1.8V LVCMOS	CAN1 Transmit data.

2.7.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.7.2.1 GTH High Speed Transceivers

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) supports 32 GTH transceivers through Eight transceiver Quad (Bank 224, 225, 226, 227, 228, 229, 230 & 231) with line rate from 500Mbps to 16.375Gbps based on the speed grade of the MPSoC. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTH transceiver quad supports two dedicated reference clock input pairs.

Zynq Ultrascale+ MPSoC Speed Grade	GTH Transceiver line rate (min)	GTH Transceiver line rate (max)
-1 Speed Grade	0.5 Gbps	12.5 Gbps
-2 Speed Grade	0.5 Gbps	16.375 Gbps
-3 Speed Grade	0.5 Gbps	16.375 Gbps

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) is capable of supporting the requirements for the different speed and temperature grade as shown below.

Zynq Ultrascale+ MPSoC Speed Grade	VCCINT	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	Units
-3E Speed Grade	0.90	0.90	0.90	0.90	V
-2E Speed Grade	0.85	0.85	0.85	0.85	V
-2I Speed Grade	0.85	0.85	0.85	0.85	V
-2LE Speed Grade	0.85	0.85	0.85	0.85	V
-1E Speed Grade	0.85	0.85	0.85	0.85	V
-1I Speed Grade	0.85	0.85	0.85	0.85	V
-1Q Speed Grade	0.85	0.85	0.85	0.85	V
-1M Speed Grade	0.85	0.85	0.85	0.85	V
-1LI Speed Grade	0.85	0.85	0.85	0.85	V

Zynq Ultrascale+ MPSoC (ZU11/17/19EG) VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR, VCCINT, VCCINT, VCCINT_IO, Voltages are sourced from the same regulator. By default, Zynq Ultrascale+ MPSoC (ZU11/17/19EG) 0.85V is sourced.

The Zynq Ultrascale+ MPSoC SOM Supports 12 GTH transceivers along with the reference clock inputs (Bank 224, 225 & 226) on Board-to-Board Conenctor1, 4 GTH transceivers along with reference clock inputs (Bank 227) on Board-to-Board Connector2, 8 GTH transceivers along with reference clock inputs (Bank 229 & 231) on Board-to-Board Connector3 and 8 GTH transceivers along with reference clock inputs (Bank 228 & 230) on Board-to-Board Connector4.

In Zynq Ultrascale+ MPSoC SOM, On board reference clock to the GTH transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTH transceivers. This gives full flexibility to end user to select the required peripheral standards on GTH transceivers. Also, On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommended.

For more details on GTH transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank224 Transceiver Quad Pins						
3	GTHTXP0_224	MGTHTXP0_224	224	AY4	O, DIFF	GTH Bank224 channel0 High speed differential transmitter positive.
5	GTHTXN0_224	MGTHTXN0_224	224	AY3	O, DIFF	GTH Bank224 channel0 High speed differential transmitter negative.
21	GTHRXN0_224	MGTHRXN0_224	224	BA1	I, DIFF	GTH Bank224 channel0 High speed differential receiver negative.
23	GTHRXP0_224	MGTHRXP0_224	224	BA2	I, DIFF	GTH Bank224 channel0 High speed differential receiver positive.
9	GTHTXP1_224	MGTHTXP1_224	224	AW6	O, DIFF	GTH Bank224 channel1 High speed differential transmitter positive.
11	GTHTXN1_224	MGTHTXN1_224	224	AW5	O, DIFF	GTH Bank224 channel1 High speed differential transmitter negative.
15	GTHRXN1_224	MGTHRXN1_224	224	AW1	I, DIFF	GTH Bank224 channel1 High speed differential receiver negative.
17	GTHRXP1_224	MGTHRXP1_224	224	AW2	I, DIFF	GTH Bank224 channel1 High speed differential receiver positive.
37	GTHTXP2_224	MGTHTXP2_224	224	AU6	O, DIFF	GTH Bank224 channel2 High speed differential transmitter positive.
39	GTHTXN2_224	MGTHTXN2_224	224	AU5	O, DIFF	GTH Bank224 channel2 High speed differential transmitter negative.
55	GTHRXN2_224	MGTHRXN2_224	224	AV3	I, DIFF	GTH Bank224 channel2 High speed differential receiver negative.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
57	GTHRXP2_224	MGTHRXP2_224	224	AV4	I, DIFF	GTH Bank224 channel2 High speed differential receiver positive.
43	GTHTXP3_224	MGTHTXP3_224	224	AT8	O, DIFF	GTH Bank224 channel3 High speed differential transmitter positive.
45	GTHTXN3_224	MGTHTXN3_224	224	AT7	O, DIFF	GTH Bank224 channel3 High speed differential transmitter negative.
49	GTHRXN3_224	MGTHRXN3_224	224	AU1	I, DIFF	GTH Bank224 channel3 High speed differential receiver negative.
51	GTHRXP3_224	MGTHRXP3_224	224	AU2	I, DIFF	GTH Bank224 channel3 High speed differential receiver positive.
4	GTREFCLK0P_224	MGTREFCLK0P_224	224	AK12	I, DIFF	GTH Bank224 differential reference clock0 positive.
6	GTREFCLK0N_224	MGTREFCLK0N_224	224	AK11	I, DIFF	GTH Bank224 differential reference clock0 negative.
64	GTREFCLK1P_224	MGTREFCLK1P_224	224	AJ10	I, DIFF	GTH Bank224 differential reference clock1 positive.
66	GTREFCLK1N_224	MGTREFCLK1N_224	224	AJ9	I, DIFF	GTH Bank224 differential reference clock1 negative.
Bank225 Transceiver Quad Pins						
97	GTHTXP0_225	MGTHTXP0_225	225	AR6	O, DIFF	GTH Bank225 channel0 High speed differential transmitter positive.
99	GTHTXN0_225	MGTHTXN0_225	225	AR5	O, DIFF	GTH Bank225 channel0 High speed differential transmitter negative.
115	GTHRXN0_225	MGTHRXN0_225	225	AT3	I, DIFF	GTH Bank225 channel0 High speed differential receiver negative.
117	GTHRXP0_225	MGTHRXP0_225	225	AT4	I, DIFF	GTH Bank225 channel0 High speed differential receiver positive.
103	GTHTXP1_225	MGTHTXP1_225	225	AP8	O, DIFF	GTH Bank225 channel1 High speed differential transmitter positive.
105	GTHTXN1_225	MGTHTXN1_225	225	AP7	O, DIFF	GTH Bank225 channel1 High speed differential transmitter negative.
109	GTHRXN1_225	MGTHRXN1_225	225	AR1	I, DIFF	GTH Bank225 channel1 High speed differential receiver negative.
111	GTHRXP1_225	MGTHRXP1_225	225	AR2	I, DIFF	GTH Bank225 channel1 High speed differential receiver positive.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
123	GTHTXP2_225	MGTHTXP2_225	225	AN6	O, DIFF	GTH Bank225 channel2 High speed differential transmitter positive.
125	GTHTXN2_225	MGTHTXN2_225	225	AN5	O, DIFF	GTH Bank225 channel2 High speed differential transmitter negative.
141	GTHRXN2_225	MGTHRXN2_225	225	AP3	I, DIFF	GTH Bank225 channel2 High speed differential receiver negative.
143	GTHRXP2_225	MGTHRXP2_225	225	AP4	I, DIFF	GTH Bank225 channel2 High speed differential receiver positive.
129	GTHTXP3_225	MGTHTXP3_225	225	AM8	O, DIFF	GTH Bank225 channel3 High speed differential transmitter positive.
131	GTHTXN3_225	MGTHTXN3_225	225	AM7	O, DIFF	GTH Bank225 channel3 High speed differential transmitter negative.
135	GTHRXN3_225	MGTHRXN3_225	225	AN1	I, DIFF	GTH Bank225 channel3 High speed differential receiver negative.
137	GTHRXP3_225	MGTHRXP3_225	225	AN2	I, DIFF	GTH Bank225 channel3 High speed differential receiver positive.
98	GTREFCLK0P_225	MGTREFCLK0P_225	225	AH12	I, DIFF	GTH Bank225 differential reference clock0 positive.
100	GTREFCLK0N_225	MGTREFCLK0N_225	225	AH11	I, DIFF	GTH Bank225 differential reference clock0 negative.
158	GTREFCLK1P_225	MGTREFCLK1P_225	225	AG10	I, DIFF	GTH Bank225 differential reference clock1 positive.
160	GTREFCLK1N_225	MGTREFCLK1N_225	225	AG9	I, DIFF	GTH Bank225 differential reference clock1 negative.
Bank226 Transceiver Quad Pins						
183	GTHTXP0_226	MGTHTXP0_226	226	AL6	O, DIFF	GTH Bank226 channel0 High speed differential transmitter positive.
185	GTHTXN0_226	MGTHTXN0_226	226	AL5	O, DIFF	GTH Bank226 channel0 High speed differential transmitter negative.
201	GTHRXN0_226	MGTHRXN0_226	226	AM3	I, DIFF	GTH Bank226 channel0 High speed differential receiver negative.
203	GTHRXP0_226	MGTHRXP0_226	226	AM4	I, DIFF	GTH Bank226 channel0 High speed differential receiver positive.
189	GTHTXP1_226	MGTHTXP1_226	226	AK8	O, DIFF	GTH Bank226 channel1 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
191	GTHTXN1_226	MGTHTXN1_226	226	AK7	O, DIFF	GTH Bank226 channel1 High speed differential transmitter negative.
195	GTHRXN1_226	MGTHRXN1_226	226	AL1	I, DIFF	GTH Bank226 channel1 High speed differential receiver negative.
197	GTHRXP1_226	MGTHRXP1_226	226	AL2	I, DIFF	GTH Bank226 channel1 High speed differential receiver positive.
217	GTHTXP2_226	MGTHTXP2_226	226	AJ6	O, DIFF	GTH Bank226 channel2 High speed differential transmitter positive.
219	GTHTXN2_226	MGTHTXN2_226	226	AJ5	O, DIFF	GTH Bank226 channel2 High speed differential transmitter negative.
235	GTHRXN2_226	MGTHRXN2_226	226	AK3	I, DIFF	GTH Bank226 channel2 High speed differential receiver negative.
237	GTHRXP2_226	MGTHRXP2_226	226	AK4	I, DIFF	GTH Bank226 channel2 High speed differential receiver positive.
223	GTHTXP3_226	MGTHTXP3_226	226	AH8	O, DIFF	GTH Bank226 channel3 High speed differential transmitter positive.
225	GTHTXN3_226	MGTHTXN3_226	226	AH7	O, DIFF	GTH Bank226 channel3 High speed differential transmitter negative.
229	GTHRXN3_226	MGTHRXN3_226	226	AJ1	I, DIFF	GTH Bank226 channel3 High speed differential receiver negative.
231	GTHRXP3_226	MGTHRXP3_226	226	AJ2	I, DIFF	GTH Bank226 channel3 High speed differential receiver positive.
184	GTREFCLK0P_226	MGTREFCLK0P_226	226	AF12	I, DIFF	GTH Bank226 differential reference clock0 positive.
186	GTREFCLK0N_226	MGTREFCLK0N_226	226	AF11	I, DIFF	GTH Bank226 differential reference clock0 negative.
218	GTREFCLK1P_226	MGTREFCLK1P_226	226	AE10	I, DIFF	GTH Bank226 differential reference clock1 positive.
220	GTREFCLK1N_226	MGTREFCLK1N_226	226	AE9	I, DIFF	GTH Bank226 differential reference clock1 negative.

2.7.2.2 PL IOs – HD BANK93

The Zynq Ultrascale+ MPSoC SOM supports 11 DIFF IOs/22 Single Ended (SE) IOs on Board-to-Board Connector1 from MPSoC's PL High-Density (HD) Bank93. Upon these 11 DIFF IOs/22 SE IOs, upto 3 HDGC Global Clock Inputs and upto 11 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank93 (& Bank90, 91 & 94) is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank93. By default, IO voltage of PL Bank93 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank93 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank93 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins 22, 24, 56, 58, 82 and 84 are HDGC Global Clock Input capable pins of PL Bank93. Also, Board to Board Connector1 pins 12, 14, 16, 18, 22, 24, 27, 28, 29, 30, 31, 32, 33, 34, 38, 40, 42, 44, 56, 58, 82 and 84 are PLSYSMON auxiliary analog Input capable pins of PL Bank93.

Important Note: While changing the I/O voltage of PL Bank93, make sure to change the I/O standard of MPSoC Banks (Bank90, 91, 93 & 94), since all are sharing the same I/O power rail from PMIC LDO4.

Note: In ZU11EG MPSoC device, the PL Bank90, 91, 93 & 94 is called as PL Bank88, 89, 90 & 91 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank93 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
12	PL_B8_LVDS93_L11P	IO_L11P_AD1P_93	93	B8	IO, 1.8V	PL Bank93 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
14	PL_A8_LVDS93_L11N	IO_L11N_AD1N_93	93	A8	IO, 1.8V	PL Bank93 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
16	PL_J9_LVDS93_L3P	IO_L3P_AD9P_93	93	J9	IO, 1.8V	PL Bank93 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
18	PL_H9_LVDS93_L3N	IO_L3N_AD9N_93	93	H9	IO, 1.8V	PL Bank93 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
22	PL_C8_LVDS93_L8N_HDGC	IO_L8N_HDGC_AD4N_93	93	C8	IO, 1.8V	PL Bank93 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.
24	PL_D8_LVDS93_L8P_HDGC	IO_L8P_HDGC_AD4P_93	93	D8	IO, 1.8V	PL Bank93 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input4 positive or Single ended I/O.
27	PL_J8_LVDS93_L2P	IO_L2P_AD10P_93	93	J8	IO, 1.8V	PL Bank93 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
28	PL_E9_LVDS93_L4N	IO_L4N_AD8N_93	93	E9	IO, 1.8V	PL Bank93 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
29	PL_H8_LVDS93_L2N	IO_L2N_AD10N_93	93	H8	IO, 1.8V	PL Bank93 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
30	PL_F9_LVDS93_L4P	IO_L4P_AD8P_93	93	F9	IO, 1.8V	PL Bank93 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
31	PL_B7_LVDS93_L10P	IO_L10P_AD2P_93	93	B7	IO, 1.8V	PL Bank93 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
32	PL_D9_LVDS93_L12P	IO_L12P_AD0P_93	93	D9	IO, 1.8V	PL Bank93 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
33	PL_A7_LVDS93_L10N	IO_L10N_AD2N_93	93	A7	IO, 1.8V	PL Bank93 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
34	PL_C9_LVDS93_L12N	IO_L12N_AD0N_93	93	C9	IO, 1.8V	PL Bank93 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
38	PL_E6_LVDS93_L9P	IO_L9P_AD3P_93	93	E6	IO, 1.8V	PL Bank93 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
40	PL_D6_LVDS93_L9N	IO_L9N_AD3N_93	93	D6	IO, 1.8V	PL Bank93 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
42	PL_F6_LVDS93_L1N	IO_L1N_AD11N_93	93	F6	IO, 1.8V	PL Bank93 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
44	PL_G6_LVDS93_L1P	IO_L1P_AD11P_93	93	G6	IO, 1.8V	PL Bank93 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
56	PL_D7_LVDS93_L7N_HDGC	IO_L7N_HDGC_AD5N_93	93	D7	IO, 1.8V	PL Bank93 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input5 negative or Single ended I/O.
58	PL_E7_LVDS93_L7P_HDGC	IO_L7P_HDGC_AD5P_93	93	E7	IO, 1.8V	PL Bank93 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input5 positive or Single ended I/O.
82	PL_F8_LVDS93_L6N_HDGC	IO_L6N_HDGC_AD6N_93	93	F8	IO, 1.8V	PL Bank93 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input6 negative or Single ended I/O.
84	PL_G8_LVDS93_L6P_HDGC	IO_L6P_HDGC_AD6P_93	93	G8	IO, 1.8V	PL Bank93 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input6 positive or Single ended I/O.

**IO Type of IOs originating from ZU19/17/11 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU19/17/11 MPSoC datasheet.*

2.7.2.3 PL IOs – HD BANK94

The Zynq Ultrascale+ MPSoC SOM supports 12 DIFF IOs/24 Single Ended (SE) IOs on Board-to-Board Connector1 from MPSoC's PL High-Density (HD) Bank94. Upon these 12 DIFF IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank94 (& Bank90, 91 & 93) is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.14V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank94. By default, IO voltage of PL Bank94 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank94 signals are routed as DIFF IOs to Board-to-Board Connector1. Even though PL Bank94 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins 116, 118, 124, 126, 130, 132, 142 and 144 are HDGC Global Clock Input capable pins of PL Bank94. Also Board to Board Connector1 pins 46, 48, 50, 52, 70, 72, 74, 76, 87, 88, 89, 90, 91, 92, 93 and 94 are PLSYSMON auxiliary analog Input capable pins of PL Bank94.

Important Note: While changing the I/O voltage of PL Bank94, make sure to change the I/O standard of MPSoC Banks (Bank90, 91, 93 & 94), since all are sharing the same I/O power rail from PMIC LDO4.

Note: In ZU11EG MPSoC device, the PL Bank90, 91, 93 & 94 is called as PL Bank88, 89, 90 & 91 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank94 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
46	PL_A5_LVDS94_L12P	IO_L12P_AD8P_94	94	A5	IO, 1.8V	PL Bank94 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
48	PL_A4_LVDS94_L12N	IO_L12N_AD8N_94	94	A4	IO, 1.8V	PL Bank94 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
50	PL_B2_LVDS94_L9P	IO_L9P_AD11P_94	94	B2	IO, 1.8V	PL Bank94 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
52	PL_B1_LVDS94_L9N	IO_L9N_AD11N_94	94	B1	IO, 1.8V	PL Bank94 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
70	PL_B6_LVDS94_L11P	IO_L11P_AD9P_94	94	B6	IO, 1.8V	PL Bank94 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
72	PL_B5_LVDS94_L11N	IO_L11N_AD9N_94	94	B5	IO, 1.8V	PL Bank94 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
74	PL_B3_LVDS94_L10P	IO_L10P_AD10P_94	94	B3	IO, 1.8V	PL Bank94 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
76	PL_A3_LVDS94_L10N	IO_L10N_AD10N_94	94	A3	IO, 1.8V	PL Bank94 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
87	PL_F5_LVDS94_L1P	IO_L1P_AD15P_94	94	F5	IO, 1.8V	PL Bank94 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
88	PL_E2_LVDS94_L3N	IO_L3N_AD13N_94	94	E2	IO, 1.8V	PL Bank94 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
89	PL_F4_LVDS94_L1N	IO_L1N_AD15N_94	94	F4	IO, 1.8V	PL Bank94 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
90	PL_E3_LVDS94_L3P	IO_L3P_AD13P_94	94	E3	IO, 1.8V	PL Bank94 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
91	PL_E5_LVDS94_L2P	IO_L2P_AD14P_94	94	E5	IO, 1.8V	PL Bank94 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
92	PL_E1_LVDS94_L4P	IO_L4P_AD12P_94	94	E1	IO, 1.8V	PL Bank94 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
93	PL_E4_LVDS94_L2N	IO_L2N_AD14N_94	94	E4	IO, 1.8V	PL Bank94 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
94	PL_D1_LVDS94_L4N	IO_L4N_AD12N_94	94	D1	IO, 1.8V	PL Bank94 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
116	PL_D3_LVDS94_L5N_HDGC	IO_L5N_HDGC_94	94	D3	IO, 1.8V	PL Bank94 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
118	PL_D4_LVDS94_L5P_HDGC	IO_L5P_HDGC_94	94	D4	IO, 1.8V	PL Bank94 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
124	PL_D2_LVDS94_L6P_HDGC	IO_L6P_HDGC_94	94	D2	IO, 1.8V	PL Bank94 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
126	PL_C1_LVDS94_L6N_HDGC	IO_L6N_HDGC_94	94	C1	IO, 1.8V	PL Bank94 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
130	PL_C6_LVDS94_L7P_HDGC	IO_L7P_HDGC_94	94	C6	IO, 1.8V	PL Bank94 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
132	PL_C5_LVDS94_L7N_HDGC	IO_L7N_HDGC_94	94	C5	IO, 1.8V	PL Bank94 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
142	PL_C3_LVDS94_L8N_HDGC	IO_L8N_HDGC_94	94	C3	IO, 1.8V	PL Bank94 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
144	PL_C4_LVDS94_L8P_HDGC	IO_L8P_HDGC_94	94	C4	IO, 1.8V	PL Bank94 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.

**IO Type of IOs originating from ZU19/17/11 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU19/17/11 MPSoC datasheet.*

2.7.3 Power Control Input

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin in Board-to-Board Connector1. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
232	SOMPWR_EN	NA	NA	NA	I, 5V	Active High SOM power enable. *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	NA	NA	Power	Ground.

2.8 Board-to-Board Connector 2

The Zynq Ultrascale+ MPSoC SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtech

Mating Connector - QSH-120-01-L-D-A from Samtech

Staking Height - 5mm

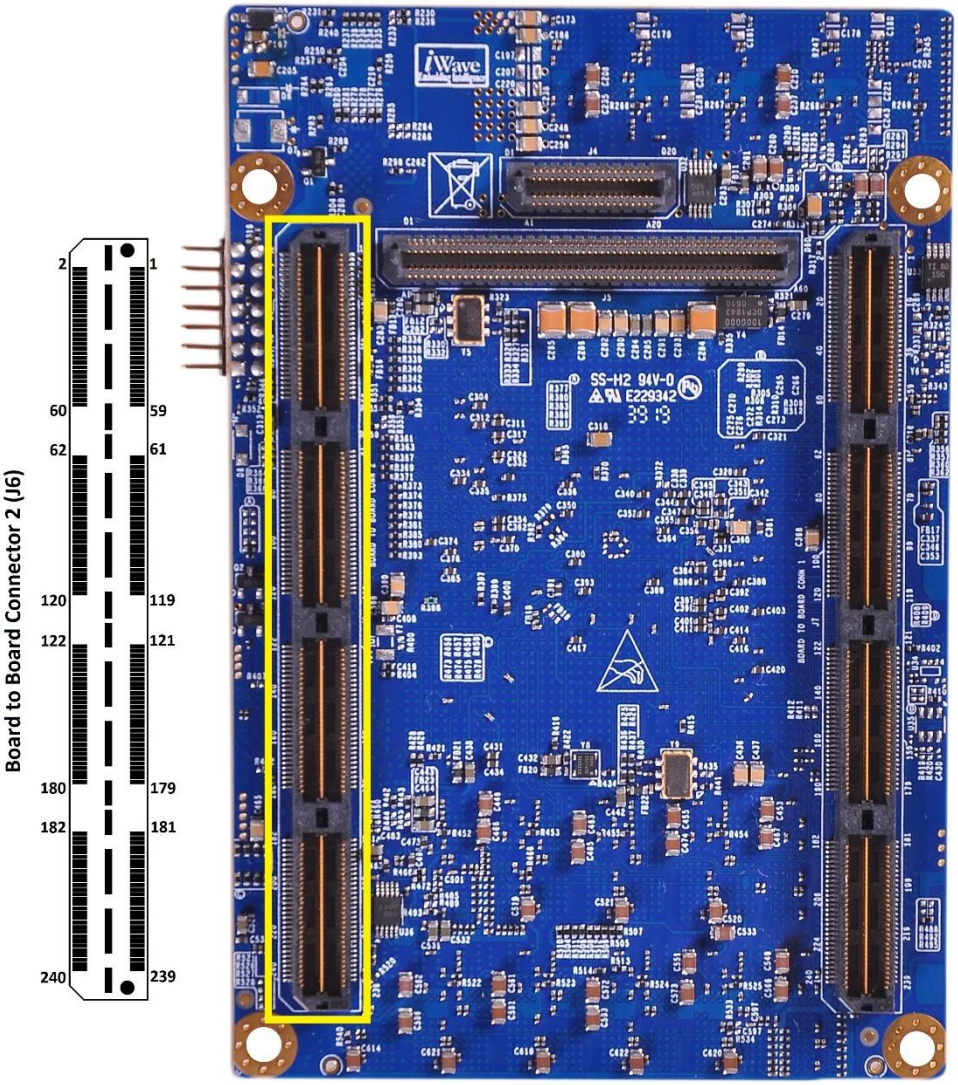


Figure 8: Board-to-Board Connector 2

Table 8: Board to Board Connector1 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
NC	25	26	USB_OTG_DM
JTAG_TDI	27	28	USB_OTG_DP
PS_JTAG_TMS	29	30	GND
PS_JTAG_TCK	31	32	USB_PWR_EN
JTAG_TDO	33	34	USB_OTG_ID
RESET_SW_IN	35	36	VBUS_USB
GND	37	38	I2C1_SDA(PS_MIO25_500)
GPHY_DTXRXM	39	40	SD1_WP(PS_MIO44_501)
GPHY_DTXRXP	41	42	SD1_CD(PS_MIO45_501)
GND	43	44	SD1_PWR(PS_MIO43_501)
GPHY_CTXRXM	45	46	I2C0_SDA(PS_MIO11_500)
GPHY_CTXRXP	47	48	I2C0_SCL(PS_MIO10_500)
GND	49	50	UART1_TX(PS_MIO08_500)
GPHY_BTXRXM	51	52	UART1_RX(PS_MIO09_500)
GPHY_BTXRXP	53	54	UART0_TX(PS_MIO07_500)
GND	55	56	UART0_RX(PS_MIO06_500)
GPHY_ATXRXM	57	58	GPHY_LINK_LED2
GPHY_ATXRXP	59	60	GPHY_ACTIVITY_LED1
SPI0_SCLK(PS_MIO0_500)	61	62	SD1_DATA3(PS_MIO49_501)
SPI0_SS0(PS_MIO3_500)	63	64	SD1_DATA2(PS_MIO48_501)
SPI0_MOSI(PS_MIO5_500)	65	66	SD1_DATA1(PS_MIO47_501)
SPI0_MISO(PS_MIO4_500)	67	68	VRTC_3V0
SD1_DATA0(PS_MIO46_501)	69	70	I2C1_SCL(PS_MIO24_500)
SD1_CMD(PS_MIO50_501)	71	72	SD1_CLK(PS_MIO51_501)
GND	73	74	GND
PL_B15_LVDS68_L18N	75	76	PL_A14_LVDS68_L17P
PL_C15_LVDS68_L18P	77	78	PL_A13_LVDS68_L17N
PL_A18_LVDS68_L24N	79	80	PL_B16_LVDS68_L20N
PL_B18_LVDS68_L24P	81	82	PL_C16_LVDS68_L20P
PL_K17_LVDS68_L6N	83	84	PL_A17_LVDS68_L22N_DBC
PL_L17_LVDS68_L6P	85	86	PL_B17_LVDS68_L22P_DBC
PL_E17_LVDS68_L21P	87	88	PL_M15_LVDS68_L4P_DBC

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
PL_D17_LVDS68_L21N	89	90	PL_L15_LVDS68_L4N_DBC
PL_J18_LVDS68_L9P	91	92	PL_B13_LVDS68_L16P_QBC
PL_H18_LVDS68_L9N	93	94	PL_A12_LVDS68_L16N_QBC
PL_K16_LVDS68_L5P	95	96	PL_C18_LVDS68_L23N
PL_K15_LVDS68_L5N	97	98	PL_D18_LVDS68_L23P
PL_J16_LVDS68_L8P	99	100	PL_G18_LVDS68_L10P_QBC
PL_H16_LVDS68_L8N	101	102	PL_F18_LVDS68_L10N_QBC
PL_E16_LVDS68_L19P_DBC	103	104	PL_P15_LVDS68_L1P_DBC
PL_D16_LVDS68_L19N_DBC	105	106	PL_N15_LVDS68_L1N_DBC
GND	107	108	GND
PL_G16_LVDS68_L12P_GC	109	110	PL_E15_LVDS68_L14P_GC
PL_F15_LVDS68_L12N_GC	111	112	PL_D14_LVDS68_L14N_GC
GND	113	114	GND
PL_F14_LVDS68_L13P_GC	115	116	PL_G17_LVDS68_L11P_GC
PL_E14_LVDS68_L13N_GC	117	118	PL_F17_LVDS68_L11N_GC
GND	119	120	GND
PL_M16_LVDS68_L3N	121	122	PL_AM10_LVDS67_L18P
PL_M17_LVDS68_L3P	123	124	PL_AN10_LVDS67_L18N
PL_G15_LVDS68_L7N_QBC	125	126	PL_AL15_LVDS67_L19P_DBC
PL_H15_LVDS68_L7P_QBC	127	128	PL_AM15_LVDS67_L19N_DBC
GND	129	130	GND
PL_AM11_LVDS67_L17P	131	132	PL_BB9_LVDS67_L2P
PL_AN11_LVDS67_L17N	133	134	PL_BB8_LVDS67_L2N
PL_AJ15_LVDS67_L20P	135	136	PL_AN14_LVDS67_L22P_DBC
PL_AK15_LVDS67_L20N	137	138	PL_AP14_LVDS67_L22N_DBC
PL_D13_LVDS68_L15P	139	140	PL_AJ14_LVDS67_L24P
PL_C13_LVDS68_L15N	141	142	PL_AK14_LVDS67_L24N
PL_N16_LVDS68_L2N	143	144	PL_AL14_LVDS67_L21P
PL_P16_LVDS68_L2P	145	146	PL_AM14_LVDS67_L21N
PL_AR15_LVDS67_L15P	147	148	PL_BB5_LVDS67_L6P
PL_AR14_LVDS67_L15N	149	150	PL_BB4_LVDS67_L6N
PL_AU11_LVDS67_L8P	151	152	PL_AM13_LVDS67_L23P
PL_AV11_LVDS67_L8N	153	154	PL_AN13_LVDS67_L23N
PL_AW11_LVDS67_L9P	155	156	PL_AW8_LVDS67_L3P
PL_AW10_LVDS67_L9N	157	158	PL_AY8_LVDS67_L3N
PL_AW9_LVDS67_L1P_DBC	159	160	PL_BB6_LVDS67_L5N
PL_AY9_LVDS67_L1N_DBC	161	162	PL_BA6_LVDS67_L5P
PL_BA8_LVDS67_L4P_DBC	163	164	PL_AV9_LVDS67_L10P_QBC
PL_BA7_LVDS67_L4N_DBC	165	166	PL_AV8_LVDS67_L10N_QBC
GND	167	168	GND
PL_AP10_LVDS67_L14P_GC	169	170	PL_AT11_LVDS67_L12P_GC
PL_AR10_LVDS67_L14N_GC	171	172	PL_AT10_LVDS67_L12N_GC
GND	173	174	GND
PL_AR13_LVDS67_L13P_GC	175	176	PL_AT13_LVDS67_L11P_GC
PL_AR12_LVDS67_L13N_GC	177	178	PL_AT12_LVDS67_L11N_GC
GND	179	180	GND

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
PL_AW12_LVDS67_L7N_QBC	181	182	PL_AN12_LVDS67_L16P_QBC
PL_AV12_LVDS67_L7P_QBC	183	184	PL_AP12_LVDS67_L16N_QBC
GND	185	186	GND
GTHRXP0_227	187	188	GTREFCLK0P_227
GTHRXN0_227	189	190	GTREFCLK0N_227
GND	191	192	GND
GTHTXP0_227	193	194	GTHRXP3_227
GTHTXN0_227	195	196	GTHRXN3_227
GND	197	198	GND
GTHRXP1_227	199	200	GTHTXP3_227
GTHRXN1_227	201	202	GTHTXN3_227
GND	203	204	GND
GTHTXP1_227	205	206	PS_MGTRRXP3_505
GTHTXN1_227	207	208	PS_MGTRRXN3_505
GND	209	210	GND
GTHRXP2_227	211	212	PS_MGTRTXP3_505
GTHRXN2_227	213	214	PS_MGTRTXN3_505
GND	215	216	GND
GTHTXP2_227	217	218	PS_MGTREFCLK3P_505
GTHTXN2_227	219	220	PS_MGTREFCLK3N_505
GND	221	222	GND
GTREFCLK1P_227	223	224	NC
GTREFCLK1N_227	225	226	NC
GND	227	228	GND
PS_MGTRRXP2_505	229	230	PS_MGTREFCLK2P_505
PS_MGTRRXN2_505	231	232	PS_MGTREFCLK2N_505
GND	233	234	GND
PS_MGTRTXP2_505	235	236	NC
PS_MGTRTXN2_505	237	238	NC
GND	239	240	GND

2.8.1 PS Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from Zynq Ultrascale+ MPSoC's PS is explained in the following section.

2.8.1.1 PS-GTR High Speed Transceivers

The Zynq Ultrascale+ MPSoC SOM supports two PS GTR transceivers (Lane2 & Lane3) on Board-to-Board Connector2. For more details on PS-GTR transceivers, refer section **Error! Reference source not found.**.

For more details on PS-GTR transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
PS-GTR Lane2 Pins						
235	PS_MGTRTXP2_505	PS_MGTRTXP2_505	505	AD39	O, DIFF	PS-GTR Lane2 High speed differential transmitter positive.
237	PS_MGTRTXN2_505	PS_MGTRTXN2_505	505	AD40	O, DIFF	PS-GTR Lane2 High speed differential transmitter negative.
229	PS_MGTRRXP2_505	PS_MGTRRXP2_505	505	AC41	I, DIFF	PS-GTR Lane2 High speed differential receiver positive.
231	PS_MGTRRXN2_505	PS_MGTRRXN2_505	505	AC42	I, DIFF	PS-GTR Lane2 High speed differential receiver negative.
230	PS_MGTREFCLK2P_505	PS_MGTREFCLK2P_505	505	AC37	I, DIFF	PS-GTR Lane2 differential reference clock positive.
232	PS_MGTREFCLK2N_505	PS_MGTREFCLK2N_505	505	AC38	I, DIFF	PS-GTR Lane2 differential reference clock negative.
PS-GTR Lane3 Pins						
212	PS_MGTRTXP3_505	PS_MGTRTXP3_505	505	AB39	O, DIFF	PS-GTR Lane3 High speed differential transmitter positive.
214	PS_MGTRTXN3_505	PS_MGTRTXN3_505	505	AB40	O, DIFF	PS-GTR Lane3 High speed differential transmitter negative.
206	PS_MGTRRXP3_505	PS_MGTRRXP3_505	505	AA41	I, DIFF	PS-GTR Lane3 High speed differential receiver positive.
208	PS_MGTRRXN3_505	PS_MGTRRXN3_505	505	AA42	I, DIFF	PS-GTR Lane3 High speed differential receiver negative.
218	PS_MGTREFCLK3P_505	PS_MGTREFCLK3P_505	505	AA37	I, DIFF	PS-GTR Lane3 differential reference clock positive.
220	PS_MGTREFCLK3N_505	PS_MGTREFCLK3N_505	505	AA38	I, DIFF	PS-GTR Lane3 differential reference clock negative.

Note: if PS-GTR lane3 is selected as USB 3.0 then USB1 2.0 only can be used.

2.8.1.2 Gigabit Ethernet Interface

The Zynq Ultrascale+ MPSoC SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2. The MAC is integrated in the Zynq Ultrascale+ MPSoC PS and connected to the external Gigabit Ethernet PHY "AR8031" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of MPSoC's PS through MIO pins and works at 1.8V IO voltage level.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	GEM0_MDC(PS_MIO76_502)	PS_MIO76_502	501	AH31	O, 1.8V LVCMOS	MDC Clock
2	GPIO_42(PS_MIO42_501)	PS_MIO42_501	501	T30	O, 1.8V LVCMOS	Active Low Reset
5	GPIO_12(PS_MIO12_500)	PS_MIO12_500	500	AJ34	I, 3.3V LVCMOs	PHY Interrupt
27	GEM0_RXD3(PS_MIO36_501)	PS_MIO36_501	501	T27	I, 1.8V LVCMOS	RGMII Receive Data 3
28	GEM0_RXD2(PS_MIO35_501)	PS_MIO35_501	501	N29	I, 1.8V LVCMOS	RGMII Receive Data 2
30	GEM0_RXD1(PS_MIO34_501)	PS_MIO34_501	501	P27	I, 1.8V LVCMOS	RGMII Receive Data 1
31	GEM0_RXD0(PS_MIO33_501)	PS_MIO33_501	501	N28	I, 1.8V LVCMOS	RGMII Receive Data 0
32	GEM0_RX_CTL(PS_MIO37_501)	PS_MIO37_501	501	N30	I, 1.8V LVCMOS	RGMII Receive Control.
33	GEM0_RX_CLK(PS_MIO32_501)	PS_MIO32_501	501	M30	I, 1.8V LVCMOS	RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz depending on speed.
34	GEM0_TX_CTL(PS_MIO31_501)	PS_MIO31_501	501	M28	O, 1.8V LVCMOS	RGMII Transmit Control.
35	GEM0_TX_CLK(PS_MIO26_501)	PS_MIO26_501	501	L27	O, 1.8V LVCMOS	RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz depending on speed.
36	GEM0_TXD0(PS_MIO27_501)	PS_MIO27_501	501	L29	O, 1.8V LVCMOS	RGMII Transmit Data0
37	GEM0_TXD1(PS_MIO28_501)	PS_MIO28_501	501	L28	O, 1.8V LVCMOS	RGMII Transmit Data1
38	GEM0_TXD2(PS_MIO29_501)	PS_MIO29_501	501	M27	O, 1.8V LVCMOS	RGMII Transmit Data2
39	GEM0_TXD3(PS_MIO30_501)	PS_MIO30_501	501	L30	O, 1.8V LVCMOS	RGMII Transmit Data3
48	GEM0_MDIO(PS_MIO77_502)	PS_MIO77_502	501	AG31	IO, 3.3V LVCMOS	MDIO Data In/Out

In Zynq Ultrascale+ MPSoC SOM, PS GPIO "PS_MIO42_501" is used for Ethernet PHY reset and also shared with USB ULPI PHY reset. Also, SOM supports Ethernet PHY interrupt through PS GPIO "PS_MIO12_500". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board.

In Zynq Ultrascale+ MPSoC SOM, GEM0 Ethernet PHY Address is fixed to 001 as per below table.

PHYADDRESS2	PHYADDRESS1	PHYADDRESS0	Ethernet PHY Address
GPHY_ACTIVITY_LED1	RXD1	RXD0	**1**
0(PD)	0(PD)	1(PU)	

Important Note: GPHY_ACTIVITY_LED1 signal is muxed with PHYADDRESS2 pin. The same GPHY_ACTIVITY_LED1 signal is connected to 60th pin of Board-to-Board connector2 to support Gigabit Ethernet Activity LED.

For more details on Gigabit Ethernet Interface pinouts on Board to Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
39	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
41	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
45	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
47	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
51	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
53	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
57	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
59	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
58	GPHY_LINK_LED2	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet 1000Mbps Link status LED (Active High).
60	GPHY_ACTIVITY_LED1	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet Activity LED (Active High).

2.8.1.3 USB 2.0 OTG Interface

The Zynq Ultrascale+ MPSoC SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB0 OTG controller of Zynq Ultrascale+ MPSoC PS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes. While using USB3.0 interface through PS-GTR, this USB2.0 OTG interface will co-work with USB3.0 interface.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	USB0_CLK(PS_MIO52_502)	PS_MIO52_502	502	W29	I, 1.8V LVCMOS	60MHz ULPI clock output.
2	USB0_NXT(PS_MIO55_502)	PS_MIO55_502	502	AB29	I, 1.8V LVCOMS	NXT Output.
3	USB0_DATA0(PS_MIO56_502)	PS_MIO56_502	502	AA30	IO ,1.8V LVCMOS	ULPI bi-directional DATA0
4	USB0_DATA1(PS_MIO57_502)	PS_MIO57_502	502	AB30	IO ,1.8V LVCMOS	ULPI bi-directional DATA1
5	USB0_DATA2(PS_MIO54_502)	PS_MIO54_502	502	Y29	IO ,1.8V LVCMOS	ULPI bi-directional DATA2
6	USB0_DATA3(PS_MIO59_502)	PS_MIO59_502	502	AC31	IO ,1.8V LVCMOS	ULPI bi-directional DATA3
7	USB0_DATA4(PS_MIO60_502)	PS_MIO60_502	502	AD29	IO ,1.8V LVCMOS	ULPI bi-directional DATA4
9	USB0_DATA5(PS_MIO61_502)	PS_MIO61_502	502	AC32	IO ,1.8V LVCMOS	ULPI bi-directional DATA5
10	USB0_DATA6(PS_MIO62_502)	PS_MIO62_502	502	AD31	IO ,1.8V LVCMOS	ULPI bi-directional DATA6
13	USB0_DATA7(PS_MIO63_502)	PS_MIO63_502	502	AD30	IO ,1.8V LVCMOS	ULPI bi-directional DATA7
27	GPIO_42(PS_MIO42_501)	PS_MIO42_501	502	T30	O, 1.8V LVCMOS	Reset
29	USB0_STP(PS_MIO58_502)	PS_MIO58_502	502	AC29	O, 1.8V LVCMOS	STP- Stop Signal
31	USB0_DIR(PS_MIO53_502)	PS_MIO53_502	502	Y30	I, 1.8V LVCOMS	Direction control of data bus.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Zynq Ultrascale+ MPSoC SOM supports “USB3320” ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Zynq Ultrascale+ MPSoC SOM, PS GPIO “PS_MIO42_501” is used for USB ULPI PHY reset and also shared with Gigabit Ethernet PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Zynq Ultrascale+ MPSoC SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
26	USB_OTG_DM	NA	NA	NA	IO, USB	USB OTG data negative.
28	USB_OTG_DP	NA	NA	NA	IO, USB	USB OTG data positive.
32	USB_PWR_EN	NA	NA	NA	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.
34	USB_OTG_ID	NA	NA	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
36	VBUS_USB	NA	NA	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.8.1.4 SD/SDIO Interface

The Zynq Ultrascale+ MPSoC SOM supports SD/SDIO interface on Board-to-Board Connector2. The SD1 controller of MPSoC's PS is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (19MHz), High Speed mode (50MHz), SDR12 (25MHz), SDR25 (25MHz), SDR50 (100MHz), SDR104 (200MHz) & DDR50 mode (50MHz). Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Zynq Ultrascale+ MPSoC SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through MIO pins.

For more details on SD/SDIO Interface pinouts on Board to Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
40	SD1_WP(PS_MIO 44_501)	PS_MIO44_ 501	501	R29	I, 1.8V LVCMOS/ 4.7K PU	SD1 Write Protect.
42	SD1_CD(PS_MIO4 5_501)	PS_MIO45_ 501	501	T29	I, 1.8V LVCMOS/ 4.7K PU	SD1 Card Detect.
44	SD1_PWR(PS_MI O43_501)	PS_MIO43_ 501	501	R30	O, 1.8V LVCMOS	SD1 Power Enable/Voltage select through PS GPIO.
62	SD1_DATA3(PS_M IO49_501)	PS_MIO49_ 501	501	U29	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA3.
64	SD1_DATA2(PS_M IO48_501)	PS_MIO48_ 501	501	V30	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA2.
66	SD1_DATA1(PS_M IO47_501)	PS_MIO47_ 501	501	T28	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA1.
69	SD1_DATA0(PS_M IO46_501)	PS_MIO46_ 501	501	U28	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA0.
71	SD1_CMD(PS_MI O50_501)	PS_MIO50_ 501	501	V29	IO, 1.8V LVCMOS/ 10K PU	SD1 Command.
72	SD1_CLK(PS_MIO 51_501)	PS_MIO51_ 501	501	W30	O, 1.8V LVCMOS/ 10K PU	SD1 Clock.

2.8.1.5 SPI Interface

The Zynq Ultrascale+ MPSoC SOM supports one SPI interface with one chip select on Board-to-Board Connector2 and second chip select on Board-to-Board conenctor1. The SPI0 controller of MPSoC's PS is used for SPI interface through MIO pins. It can function in master mode, slave mode or multi-master mode and supports full-duplex operation.

For more details on SPI Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
61	SPI0_SCLK(PS_MIO0_500)	PS_MIO0_500	500	AM33	O, 1.8V LVCMOS	SPI clock.
63	SPI0_SS0(PS_MIO3_500)	PS_MIO3_500	500	AM30	O, 1.8V LVCMOS	SPI chip select0.
65	SPI0_MOSI(PS_MIO5_500)	PS_MIO5_500	500	AL32	IO, 1.8V LVCMOS	SPI Master output Slave input.
67	SPI0_MISO(PS_MIO4_500)	PS_MIO4_500	500	AL33	IO, 1.8V LVCMOS	SPI Master input Slave output.
178	SPI0_SS2(PS_MIO1_500)	PS_MIO1_500	500	AM29	IO, 1.8V LVCMOS	SPI chip select2. Same pin can be configured as GPIO.

2.8.1.6 Debug UART Interface

The Zynq Ultrascale+ MPSoC SOM supports one Debug UART interface on Board-to-Board Connector2. The UART0 controller of MPSoC's PS is used for Debug UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
54	UART0_TX(PS_MIO07_500)	PS_MIO7_500	500	AL30	O, 1.8V LVCMOS	UART0 Transmit data line for Debug.
56	UART0_RX(PS_MIO06_500)	PS_MIO6_500	500	AL31	I, 1.8V LVCMOS	UART0 Receive data line for Debug.

2.8.1.7 Data UART Interface

The Zynq Ultrascale+ MPSoC SOM supports one DATA UART interface on Board-to-Board Connector2. The UART1 controller of MPSoC's PS is used for Data UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates. Each path includes a 64- Byte FIFIO.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
50	UART1_TX(PS_MIO08_500)	PS_MIO8_500	500	AK33	O, 1.8V LVCMOS	UART1 Transmit data line.
52	UART1_RX(PS_MIO09_500)	PS_MIO9_500	500	AK34	I, 1.8V LVCMOS	UART1 Receive data line.

2.8.1.8 I2C Interface

The Zynq Ultrascale+ MPSoC SOM supports one I2C interface on Board-to-Board Connector2. The I2C0 module of MPSoC's PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM PMIC with I2C address 0x58 in the Zynq Ultrascale+ MPSoC SOM. Also, one more I2C interface (I2C1) can be taken out on Board-to-Board Connector2 which is multiplexed with PS GPIOs.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
46	I2C0_SDA(PS_MIO11_500)	PS_MIO11_500	500	AK32	IO, 1.8V OD/ 4.7K PU	I2C0 data.
48	I2C0_SCL(PS_MIO10_500)	PS_MIO10_500	500	AK30	O, 1.8V OD/ 4.7K PU	I2C0 clock.
38	I2C1_SDA(PS_MIO25_500)	PS_MIO25_500	500	AG34	IO, 1.8V LVCMOS/ 4.7K PU	General Purpose Input/Output. Same pin can be used as I2C1 data.
70	I2C1_SCL(PS_MIO24_500)	PS_MIO24_500	500	AH33	O, 1.8V LVCOMS/ 4.7K PU	General Purpose Input/Output. Same pin can be used as I2C1 clock.

2.8.1.9 JTAG Interface

The Zynq Ultrascale+ MPSoC SOM supports JTAG interface on Board-to-Board Connector2. The Zynq Ultrascale+ MPSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale MPSoC. Also, the same JTAG pins are chained with MAX 10 FPGA JTAG interface pins in the SOM. These JTAG interface signals are also connected to on-board JTAG connector.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
27	JTAG_TDI	PS_JTAG_ TDI	503	AD25	I, 1.8V LVCMOS/4.7K	JTAG Test Data Input.
29	PS_JTAG_TMS	PS_JTAG_ TMS	503	AD26	I, 1.8V LVCMOS/4.7K	JTAG Test Mode Select.
31	PS_JTAG_TCK	PS_JTAG_ TCK	503	AC26	I, 1.8V LVCMOS/4.7K	JTAG Test Clock.
33	JTAG_TDO	PS_JTAG_ TDO	503	AD27	O, 1.8V LVCMOS	JTAG Test Data Output.

2.8.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.8.2.1 GTH High speed Transceivers

The Zynq Ultrascale+ MPSoC SOM Supports 4 GTH transceivers along with reference clock inputs (Bank227) on Board-to-Board Connector2. For more details on GTH transceivers, refer section **2.7.2.1**.

For more details on GTH transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank227 Transceiver Quad Pins						
187	GTHRXP0_227	MGTHRXP0_227	227	AH4	I, DIFF	GTH Bank227 channel0 High speed differential receiver positive.
189	GTHRXN0_227	MGTHRXN0_227	227	AH3	I, DIFF	GTH Bank227 channel0 High speed differential receiver negative.
193	GTHTXP0_227	MGTHTXP0_227	227	AG6	O, DIFF	GTH Bank227 channel0 High speed differential transmitter positive.
195	GTHTXN0_227	MGTHTXN0_227	227	AG5	O, DIFF	GTH Bank227 channel0 High speed differential transmitter negative.
199	GTHRXP1_227	MGTHRXP1_227	227	AG2	I, DIFF	GTH Bank227 channel1 High speed differential receiver positive.
201	GTHRXN1_227	MGTHRXN1_227	227	AG1	I, DIFF	GTH Bank227 channel1 High speed differential receiver negative.
205	GTHTXP1_227	MGTHTXP1_227	227	AF8	O, DIFF	GTH Bank227 channel1 High speed differential transmitter positive.
207	GTHTXN1_227	MGTHTXN1_227	227	AF7	O, DIFF	GTH Bank227 channel1 High speed differential transmitter negative.
211	GTHRXP2_227	MGTHRXP2_227	227	AF4	I, DIFF	GTH Bank227 channel2 High speed differential receiver positive.
213	GTHRXN2_227	MGTHRXN2_227	227	AF3	I, DIFF	GTH Bank227 channel2 High speed differential receiver negative.
217	GTHTXP2_227	MGTHTXP2_227	227	AE6	O, DIFF	GTH Bank227 channel2 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
219	GTHTXN2_227	MGTHTXN2_227	227	AE5	O, DIFF	GTH Bank227 channel2 High speed differential transmitter negative.
194	GTHRXP3_227	MGTHRXP3_227	227	AE2	I, DIFF	GTH Bank227 channel3 High speed differential receiver positive.
196	GTHRXN3_227	MGTHRXN3_227	227	AE1	I, DIFF	GTH Bank227 channel3 High speed differential receiver negative.
200	GTHTXP3_227	MGTHTXP3_227	227	AD8	O, DIFF	GTH Bank227 channel3 High speed differential transmitter positive.
202	GTHTXN3_227	MGTHTXN3_227	227	AD7	O, DIFF	GTH Bank227 channel3 High speed differential transmitter negative.
188	GTREFCLK0P_227	MGTREFCLK0P_227	227	AD12	I, DIFF	GTH Bank227 differential reference clock0 positive.
190	GTREFCLK0N_227	MGTREFCLK0N_227	227	AD11	I, DIFF	GTH Bank227 differential reference clock0 negative.
223	GTREFCLK1P_227	MGTREFCLK1P_227	227	AC10	I, DIFF	GTH Bank227 differential reference clock1 positive.
225	GTREFCLK1N_227	MGTREFCLK1N_227	227	AC9	I, DIFF	GTH Bank227 differential reference clock1 negative.

2.8.2.2 PL IOs – HP BANK67

The Zynq Ultrascale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector2 from MPSoC's PL High Performance (HP) Bank67. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank67 (& Bank68) is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank67. By default, IO voltage of PL Bank67 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank67 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though PL Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector2 pins 170, 172, 176, 178, 169, 171, 175, and 177 are GC Global Clock Input capable pins of PL Bank67. Also, Board to Board Connector2 pins 122, 124, 126, 128, 131, 133, 135, 136, 137, 138, 144, 146, 147, 148, 149, 150, 151, 153, 155, 156, 157, 158, 160, 162, 163, 164, 165, 166, 181, 182, 183 and 184 are PLSYSMON auxiliary analog Input capable pins of PL Bank67.

Important Note: While changing the I/O voltage of PL Bank67, make sure to change the I/O standard of MPSoC Banks (Bank67 & 68) and also MAX 10 FPGA Bank8, since all are sharing the same I/O power rail from PMIC LDO1.

For more details on PL HP Bank67 pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
144	PL_AL14_LVDS67_L21P	IO_L21P_T3L_N4_AD8P_67	67	AL14	IO, 1.8V	PL Bank67 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
146	PL_AM14_LVDS67_L21N	IO_L21N_T3L_N5_AD8N_67	67	AM14	IO, 1.8V	PL Bank67 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
148	PL_BB5_LVDS67_L6P	IO_L6P_T0U_N10_AD6P_67	67	BB5	IO, 1.8V	PL Bank67 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
150	PL_BB4_LVDS67_L6N	IO_L6N_T0U_N11_AD6N_67	67	BB4	IO, 1.8V	PL Bank67 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
152	PL_AM13_LVDS67_L23P	IO_L23P_T3U_N8_67	67	AM13	IO, 1.8V	PL Bank67 IO23 differential positive. Same pin can be configured as Single ended I/O.
154	PL_AN13_LVDS67_L23N	IO_L23N_T3U_N9_67	67	AN13	IO, 1.8V	PL Bank67 IO23 differential negative. Same pin can be configured as Single ended I/O.
156	PL_AW8_LVDS67_L3P	IO_L3P_T0L_N4_AD15P_67	67	AW8	IO, 1.8V	PL Bank67 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
158	PL_AY8_LVDS67_L3N	IO_L3N_T0L_N5_AD15N_67	67	AY8	IO, 1.8V	PL Bank67 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
160	PL_BB6_LVDS67_L5N	IO_L5N_T0U_N9_AD14N_67	67	BB6	IO, 1.8V	PL Bank67 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
162	PL_BA6_LVDS67_L5P	IO_L5P_T0U_N8_AD14P_67	67	BA6	IO, 1.8V	PL Bank67 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
164	PL_AV9_LVDS67_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_67	67	AV9	IO, 1.8V	PL Bank67 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
166	PL_AV8_LVDS67_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_67	67	AV8	IO, 1.8V	PL Bank67 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
170	PL_AT11_LVDS67_L12P_GC	IO_L12P_T1U_N10_GC_67	67	AT11	IO, 1.8V	PL Bank67 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
172	PL_AT10_LVDS67_L12N_GC	IO_L12N_T1U_N11_GC_67	67	AT10	IO, 1.8V	PL Bank67 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
176	PL_AT13_LVDS67_L11P_GC	IO_L11P_T1U_N8_GC_67	67	AT13	IO, 1.8V	PL Bank67 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
178	PL_AT12_LVDS67_L11N_GC	IO_L11N_T1U_N9_GC_67	67	AT12	IO, 1.8V	PL Bank67 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
182	PL_AN12_LVDS67_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_67	67	AN12	IO, 1.8V	PL Bank67 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
184	PL_AP12_LVDS67_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_67	67	AP12	IO, 1.8V	PL Bank67 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
131	PL_AM11_LVDS67_L17P	IO_L17P_T2U_N8_AD10P_67	67	AM11	IO, 1.8V	PL Bank67 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
133	PL_AN11_LVDS67_L17N	IO_L17N_T2U_N9_AD10N_67	67	AN11	IO, 1.8V	PL Bank67 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
135	PL_AJ15_LVDS67_L20P	IO_L20P_T3L_N2_AD1P_67	67	AJ15	IO, 1.8V	PL Bank67 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
137	PL_AK15_LVDS67_L20N	IO_L20N_T3L_N3_AD1N_67	67	AK15	IO, 1.8V	PL Bank67 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
147	PL_AR15_LVDS67_L15P	IO_L15P_T2L_N4_AD11P_67	67	AR15	IO, 1.8V	PL Bank67 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
149	PL_AR14_LVDS67_L15N	IO_L15N_T2L_N5_AD11N_67	67	AR14	IO, 1.8V	PL Bank67 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
151	PL_AU11_LVDS67_L8P	IO_L8P_T1L_N2_AD5P_67	67	AU11	IO, 1.8V	PL Bank67 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
153	PL_AV11_LVDS67_L8N	IO_L8N_T1L_N3_AD5N_67	67	AV11	IO, 1.8V	PL Bank67 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
155	PL_AW11_LVDS67_L9P	IO_L9P_T1L_N4_AD12P_67	67	AW11	IO, 1.8V	PL Bank67 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
157	PL_AW10_LVDS67_L9N	IO_L9N_T1L_N5_AD12N_67	67	AW10	IO, 1.8V	PL Bank67 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
159	PL_AW9_LVDS67_L1P_DBC	IO_L1P_T0L_N0_DBC_67	67	AW9	IO, 1.8V	PL Bank67 IO1 differential positive. Same pin can be configured as Single ended I/O.
161	PL_AY9_LVDS67_L1N_DBC	IO_L1N_T0L_N1_DBC_67	67	AY9	IO, 1.8V	PL Bank67 IO1 differential negative. Same pin can be configured as Single ended I/O.
163	PL_BA8_LVDS67_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_67	67	BA8	IO, 1.8V	PL Bank67 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
165	PL_BA7_LVDS67_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_67	67	BA7	IO, 1.8V	PL Bank67 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
169	PL_AP10_LVDS67_L14P_GC	IO_L14P_T2L_N2_GC_67	67	AP10	IO, 1.8V	PL Bank67 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
171	PL_AR10_LVDS67_L14N_GC	IO_L14N_T2L_N3_GC_67	67	AR10	IO, 1.8V	PL Bank67 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
175	PL_AR13_LVDS67_L13P_GC	IO_L13P_T2L_N0_GC_QBC_67	67	AR13	IO, 1.8V	PL Bank67 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
177	PL_AR12_LVDS67_L13N_GC	IO_L13N_T2L_N1_GC_QBC_67	67	AR12	IO, 1.8V	PL Bank67 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
181	PL_AW12_LVDS67_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_67	67	AW12	IO, 1.8V	PL Bank67 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
183	PL_AV12_LVDS67_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_67	67	AV12	IO, 1.8V	PL Bank67 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.

**IO Type of IOs originating from ZU19/17/11 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU19/17/11 MPSoC datasheet.*

2.8.2.3 PL IOs – HP BANK68

The Zynq Ultrascale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector2 from MPSoC's PL High Performance (HP) Bank68. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank68 (& Bank67) is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank68. By default, IO voltage of PL Bank68 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank68 signals are routed as LVDS IOs to Board-to-Board Connector2. Even though PL Bank68 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector2 pins 109, 110, 111, 112, 115, 116, 117 and 118 are GC Global Clock Input capable pins of PL Bank68. Also, Board to Board Connector2 pins 75, 76, 77, 78, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 97, 99, 100, 101, 102, 103, 105, 121, 123, 125, 127, 139 and 141 are PLSYSMON auxiliary analog Input capable pins of PL Bank68.

Important Note: While changing the I/O voltage of PL Bank68, make sure to change the I/O standard of MPSoC Banks (Bank67 & 68) and also MAX 10 FPGA Bank8, since all are sharing the same I/O power rail from PMIC LDO1.

For more details on PL HP Bank68 pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
76	PL_A14_LVDS68_L17P	IO_L17P_T2U_N8_AD10P_68	68	A14	IO, 1.8V	PL Bank68 IO17 differential positive Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
78	PL_A13_LVDS68_L17N	IO_L17N_T2U_N9_AD10N_68	68	A13	IO, 1.8V	PL Bank68 IO17 differential negative Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
80	PL_B16_LVDS68_L20N	IO_L20N_T3L_N3_AD1N_68	68	B16	IO, 1.8V	PL Bank68 IO20 differential negative Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
82	PL_C16_LVDS68_L20P	IO_L20P_T3L_N2_AD1P_68	68	C16	IO, 1.8V	PL Bank68 IO20 differential positive Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
84	PL_A17_LVDS68_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_68	68	A17	IO, 1.8V	PL Bank68 IO22 differential negative Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
86	PL_B17_LVDS68_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_68	68	B17	IO, 1.8V	PL Bank68 IO22 differential positive Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
88	PL_M15_LVDS68_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_68	68	M15	IO, 1.8V	PL Bank68 IO4 differential positive Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
90	PL_L15_LVDS68_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_68	68	L15	IO, 1.8V	PL Bank68 IO4 differential negative Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
92	PL_B13_LVDS68_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_68	68	B13	IO, 1.8V	PL Bank68 IO16 differential positive Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
94	PL_A12_LVDS68_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_68	68	A12	IO, 1.8V	PL Bank68 IO16 differential negative Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
96	PL_C18_LVDS68_L23N	IO_L23N_T3U_N9_68	68	C18	IO, 1.8V	PL Bank68 IO23 differential negative Same pin can be configured as Single ended I/O.
98	PL_D18_LVDS68_L23P	IO_L23P_T3U_N8_68	68	D18	IO, 1.8V	PL Bank68 IO23 differential positive Same pin can be configured as Single ended I/O.
100	PL_G18_LVDS68_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_68	68	G18	IO, 1.8V	PL Bank68 IO10 differential positive Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
102	PL_F18_LVDS68_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_68	68	F18	IO, 1.8V	PL Bank68 IO10 differential negative Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
104	PL_P15_LVDS68_L1P_DBC	IO_L1P_T0L_N0_DBC_68	68	P15	IO, 1.8V	PL Bank68 IO1 differential positive Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
106	PL_N15_LVDS68_L1N_DBC	IO_L1N_T0L_N1_DBC_68	68	N15	IO, 1.8V	PL Bank68 IO1 differential negative. Same pin can be configured as Single ended I/O.
110	PL_E15_LVDS68_L14P_GC	IO_L14P_T2L_N2_GC_68	68	E15	IO, 1.8V	PL Bank68 IO14 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
112	PL_D14_LVDS68_L14N_GC	IO_L14N_T2L_N3_GC_68	68	D14	IO, 1.8V	PL Bank68 IO14 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
116	PL_G17_LVDS68_L11P_GC	IO_L11P_T1U_N8_GC_68	68	G17	IO, 1.8V	PL Bank68 IO11 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
118	PL_F17_LVDS68_L11N_GC	IO_L11N_T1U_N9_GC_68	68	F17	IO, 1.8V	PL Bank68 IO11 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
75	PL_B15_LVDS68_L18N	IO_L18N_T2U_N11_AD2N_68	68	B15	IO, 1.8V	PL Bank68 IO18 differential negative Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
77	PL_C15_LVDS68_L18P	IO_L18P_T2U_N10_AD2P_68	68	C15	IO, 1.8V	PL Bank68 IO18 differential positive Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
79	PL_A18_LVDS68_L24N	IO_L24N_T3U_N11_68	68	A18	IO, 1.8V	PL Bank68 IO24 differential negative Same pin can be configured as Single ended I/O.
81	PL_B18_LVDS68_L24P	IO_L24P_T3U_N10_68	68	B18	IO, 1.8V	PL Bank68 IO24 differential positive Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
83	PL_K17_LVDS68_L6N	IO_L6N_T0U_N11_AD6N_68	68	K17	IO, 1.8V	PL Bank68 IO6 differential negative Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
85	PL_L17_LVDS68_L6P	IO_L6P_T0U_N10_AD6P_68	68	L17	IO, 1.8V	PL Bank68 IO6 differential positive Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
87	PL_E17_LVDS68_L21P	IO_L21P_T3L_N4_AD8P_68	68	E17	IO, 1.8V	PL Bank68 IO21 differential positive Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
89	PL_D17_LVDS68_L21N	IO_L21N_T3L_N5_AD8N_68	68	D17	IO, 1.8V	PL Bank68 IO21 differential negative Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
91	PL_J18_LVDS68_L9P	IO_L9P_T1L_N4_AD12P_68	68	J18	IO, 1.8V	PL Bank68 IO9 differential positive Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
93	PL_H18_LVDS68_L9N	IO_L9N_T1L_N5_AD12N_68	68	H18	IO, 1.8V	PL Bank68 IO9 differential negative Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
95	PL_K16_LVDS68_L5P	IO_L5P_T0U_N8_AD14P_68	68	K16	IO, 1.8V	PL Bank68 IO5 differential positive Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
97	PL_K15_LVDS68_L5N	IO_L5N_T0U_N9_AD14N_68	68	K15	IO, 1.8V	PL Bank68 IO5 differential negative Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
99	PL_J16_LVDS68_L8P	IO_L8P_T1L_N2_AD5P_68	68	J16	IO, 1.8V	PL Bank68 IO8 differential positive Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
101	PL_H16_LVDS68_L8N	IO_L8N_T1L_N3_AD5N_68	68	H16	IO, 1.8V	PL Bank68 IO8 differential negative Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
103	PL_E16_LVDS68_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_68	68	E16	IO, 1.8V	PL Bank68 IO19 differential positive Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
105	PL_D16_LVDS68_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_68	68	D16	IO, 1.8V	PL Bank68 IO19 differential negative Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
109	PL_G16_LVDS68_L12P_GC	IO_L12P_T1U_N10_GC_68	68	G16	IO, 1.8V	PL Bank68 IO12 differential positive Same pin can be configured as GC Global Clock Input differential positive or ended I/O.
111	PL_F15_LVDS68_L12N_GC	IO_L12N_T1U_N11_GC_68	68	F15	IO, 1.8V	PL Bank68 IO12 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
115	PL_F14_LVDS68_L13P_GC	IO_L13P_T2L_N0_GC_QBC_68	68	F14	IO, 1.8V	PL Bank68 IO13 differential positive Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
117	PL_E14_LVDS68_L13N_GC	IO_L13N_T2L_N1_GC_QBC_68	68	E14	IO, 1.8V	PL Bank68 IO13 differential negative Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
121	PL_M16_LVDS68_L3N	IO_L3N_T0L_N5_AD15N_68	68	M16	IO, 1.8V	PL Bank68 IO3 differential negative Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
123	PL_M17_LVDS68_L3P	IO_L3P_T0L_N4_AD15P_68	68	M17	IO, 1.8V	PL Bank68 IO3 differential positive Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
125	PL_G15_LVDS68_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_68	68	G15	IO, 1.8V	PL Bank68 IO7 differential negative Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
127	PL_H15_LVDS68_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_68	68	H15	IO, 1.8V	PL Bank68 IO7 differential positive Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
139	PL_D13_LVDS68_L15P	IO_L15P_T2L_N4_AD11P_68	68	D13	IO, 1.8V	PL Bank68 IO15 differential positive Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
141	PL_C13_LVDS68_L15N	IO_L15N_T2L_N5_AD11N_68	68	C13	IO, 1.8V	PL Bank68 IO15 differential negative Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
143	PL_N16_LVDS68_L2N	IO_L2N_T0L_N3_68	68	N16	IO, 1.8V	PL Bank68 IO2 differential negative Same pin can be configured as Single ended I/O.
145	PL_P16_LVDS68_L2P	IO_L2P_T0L_N2_68	68	P16	IO, 1.8V	PL Bank68 IO2 differential positive Same pin can be configured as Single ended I/O.

**IO Type of IOs originating from ZU19/17/11 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU19/17/11 MPSoC datasheet.*

2.8.3 Power & Reset Input

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin232) in Board-to-Board Connector1. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Zynq Ultrascale+ MPSoC SOM supports VCC_RTC coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage. Also, it supports warm reset input from Board-to-Board Connector2 and connected to PS_SRST_B pin of MPSoC.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	NA	NA	I, 5V Power	Supply Voltage.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	NA	NA	Power	Ground.
68	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.
35	RESET_SW_IN	PS_SRST_B	NA	AB27	I, 1.8V LVCMOS/ 4.7K PU	Active low reset input.

2.9 Board-to-Board Connector3

The Zynq Ultrascale+ MPSoC SOM Board to Board connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A from Samtech

Staking Height - 5mm

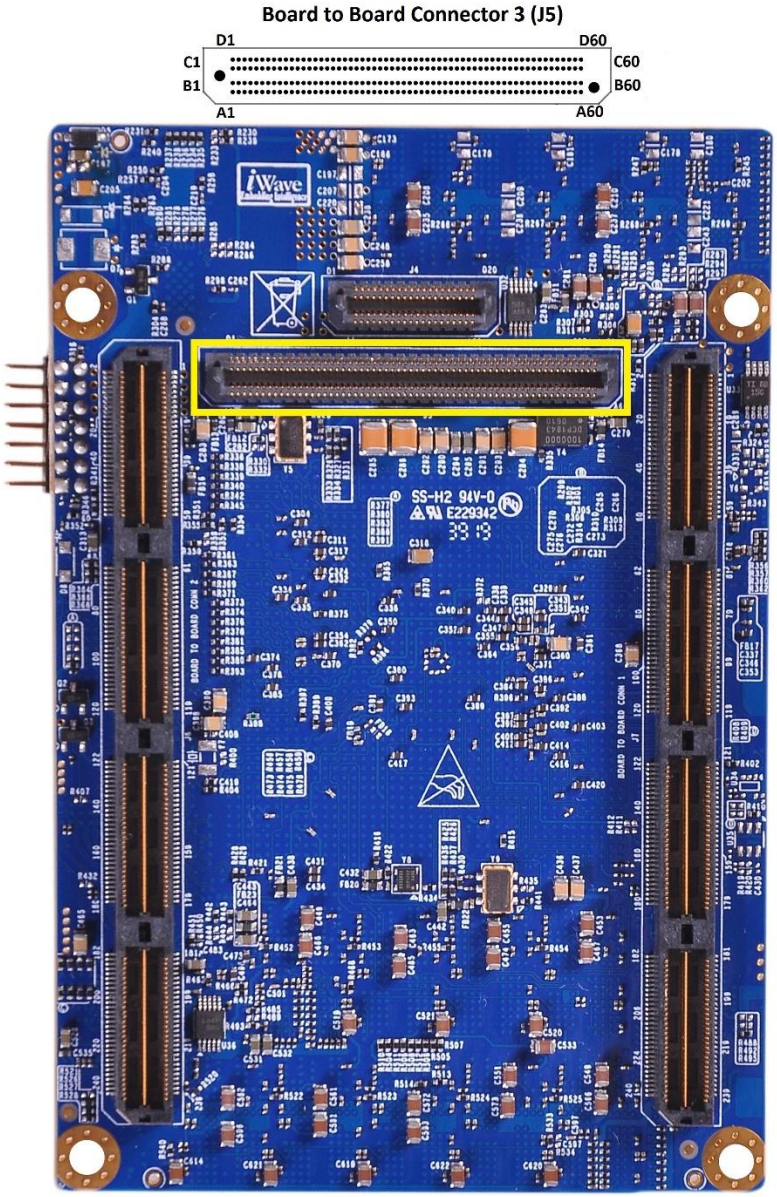


Figure 9: Board to Board Connector 3

Table 9: Board to Board Connector3 Pinout

B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name
A1	GTREFCLK1N_231	**B1**	GND	**C1**	NC	**D1**	GND
A2	GTREFCLK1P_231	**B2**	GTYRXN2_131	**C2**	GND	**D2**	GTREFCLK0P_128
A3	GND	**B3**	GTYRXP2_131	**C3**	GND	**D3**	GTREFCLK0N_128
A4	GTYRXN0_131	**B4**	GND	**C4**	GTYRXP2_130	**D4**	GND
A5	GTYRXP0_131	**B5**	GND	**C5**	GTYRXN2_130	**D5**	GND
A6	GND	**B6**	GTYRXN3_131	**C6**	GND	**D6**	GTYRXP3_128
A7	GND	**B7**	GTYRXP3_131	**C7**	GND	**D7**	GTYRXN3_128
A8	GTYRXN1_131	**B8**	GND	**C8**	GTYRXN0_130	**D8**	GND
A9	GTYRXP1_131	**B9**	GND	**C9**	GTYRXP0_130	**D9**	GND
A10	GND	**B10**	GTYTXN1_131	**C10**	GND	**D10**	GTYRXP2_128
A11	GND	**B11**	GTYTXP1_131	**C11**	GND	**D11**	GTYRXN2_128
A12	GTYTXN3_131	**B12**	GND	**C12**	GTYTXN1_130	**D12**	GND
A13	GTYTXP3_131	**B13**	GND	**C13**	GTYTXP1_130	**D13**	GND
A14	GND	**B14**	GTYTXN0_131	**C14**	GND	**D14**	GTYRXP1_128
A15	GND	**B15**	GTYTXP0_131	**C15**	GND	**D15**	GTYRXN1_128
A16	GTYTXN2_131	**B16**	GND	**C16**	GTREFCLK1N_130	**D16**	GND
A17	GTYTXP2_131	**B17**	GND	**C17**	GTREFCLK1P_130	**D17**	GND
A18	GND	**B18**	GTREFCLK0N_131	**C18**	GND	**D18**	GTYRXP0_128
A19	GND	**B19**	GTREFCLK0P_131	**C19**	GND	**D19**	GTYRXN0_128
A20	GTREFCLK1N_131	**B20**	GND	**C20**	GTREFCLK0P_130	**D20**	GND
A21	GTREFCLK1P_131	**B21**	GND	**C21**	GTREFCLK0N_130	**D21**	GND
A22	GND	**B22**	GTYRXN3_129	**C22**	GND	**D22**	GTYTXN3_128
A23	GND	**B23**	GTYRXP3_129	**C23**	GND	**D23**	GTYTXP3_128
A24	GTYRXN2_129	**B24**	GND	**C24**	GTYRXN3_130	**D24**	GND
A25	GTYRXP2_129	**B25**	GND	**C25**	GTYRXP3_130	**D25**	GND
A26	GND	**B26**	GTYTXP3_129	**C26**	GND	**D26**	GTYTXN2_128
A27	GND	**B27**	GTYTXN3_129	**C27**	GND	**D27**	GTYTXP2_128
A28	GTYTXP2_129	**B28**	GND	**C28**	GTYRXN1_130	**D28**	GND
A29	GTYTXN2_129	**B29**	GND	**C29**	GTYRXP1_130	**D29**	GND
A30	GND	**B30**	GTYTXP1_129	**C30**	GND	**D30**	GTYTXN1_128
A31	GND	**B31**	GTYTXN1_129	**C31**	GND	**D31**	GTYTXP1_128
A32	GTYTXP0_129	**B32**	GND	**C32**	GTYTXN3_130	**D32**	GND
A33	GTYTXN0_129	**B33**	GND	**C33**	GTYTXP3_130	**D33**	GND
A34	GND	**B34**	GTREFCLK1P_129	**C34**	GND	**D34**	GTYTXN0_128
A35	GND	**B35**	GTREFCLK1N_129	**C35**	GND	**D35**	GTYTXP0_128
A36	GTYRXP1_129	**B36**	GND	**C36**	GTYTXN2_130	**D36**	GND
A37	GTYRXN1_129	**B37**	GND	**C37**	GTYTXP2_130	**D37**	GND
A38	GND	**B38**	GTREFCLK0P_129	**C38**	GND	**D38**	GTREFCLK1N_128
A39	GND	**B39**	GTREFCLK0N_129	**C39**	GND	**D39**	GTREFCLK1P_128
A40	GTYRXP0_129	**B40**	GND	**C40**	GTYTXN0_130	**D40**	GND
A41	GTYRXN0_129	**B41**	GND	**C41**	GTYTXP0_130	**D41**	GND
A42	GND	**B42**	GTREFCLK0P_229	**C42**	GND	**D42**	GTHRXN1_231
A43	GND	**B43**	GTREFCLK0N_229	**C43**	GND	**D43**	GTHRXP1_231

B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name	B2B-3 Pin No.	Signal Name
A44	GTHTXP0_229	**B44**	GND	**C44**	GTHRXN2_231	**D44**	GND
A45	GTHTXN0_229	**B45**	GND	**C45**	GTHRXP2_231	**D45**	GND
A46	GND	**B46**	GTHTXP1_229	**C46**	GND	**D46**	GTHRXN3_231
A47	GND	**B47**	GTHTXN1_229	**C47**	GND	**D47**	GTHRXP3_231
A48	GTHTXP3_229	**B48**	GND	**C48**	GTREFCLK0P_231	**D48**	GND
A49	GTHTXN3_229	**B49**	GND	**C49**	GTREFCLK0N_231	**D49**	GND
A50	GND	**B50**	GTHRXP0_229	**C50**	GND	**D50**	GTHRXN0_231
A51	GND	**B51**	GTHRXN0_229	**C51**	GND	**D51**	GTHRXP0_231
A52	GTHTXP2_229	**B52**	GND	**C52**	GTHTXP0_231	**D52**	GND
A53	GTHTXN2_229	**B53**	GND	**C53**	GTHTXN0_231	**D53**	GND
A54	GND	**B54**	GTHRXP2_229	**C54**	GND	**D54**	GTHTXP2_231
A55	GND	**B55**	GTHRXN2_229	**C55**	GND	**D55**	GTHTXN2_231
A56	GTHRXP1_229	**B56**	GND	**C56**	GTHTXN1_231	**D56**	GND
A57	GTHRXN1_229	**B57**	GND	**C57**	GTHTXP1_231	**D57**	GND
A58	GND	**B58**	GTHRXP3_229	**C58**	GND	**D58**	GTHTXP3_231
A59	GTREFCLK1N_229	**B59**	GTHRXN3_229	**C59**	GND	**D59**	GTHTXN3_231
A60	GTREFCLK1P_229	**B60**	GND	**C60**	NC	**D60**	GND

2.9.1 PL Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.9.1.1 GTY High Speed Transceivers

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) supports 16 GTY transceivers through four transceiver Quad (Bank 128, 129, 130, & 131) with line rate from 500Mbps to 32.75Gbps based on the speed grade of the MPSoC. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

Zynq Ultrascale+ MPSoC Speed Grade	GTH Transceiver line rate (min)	GTH Transceiver line rate (max)
-1 Speed Grade	0.5 Gbps	25.785 Gbps
-2 Speed Grade	0.5 Gbps	28.21 Gbps
-3 Speed Grade	0.5 Gbps	32.75 Gbps

Note: For Backplane application, the transceiver maximum line rate may come down.

The Zynq Ultrascale+ MPSoC SOM Supports 16 GTY transceivers along with the reference clock inputs (Bank 128, 129, 130, & 131) on Board-to-Board Conenctor3.

In Zynq Ultrascale+ MPSoC SOM, On board reference clock to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers. Also, On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board as recommend.

For more details on GTY transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank128 Transceiver Quad Pins						
D35	GTYTXP0_128	MGTYTXP0_128	128	Y34	O, DIFF	GTY Bank128 channel0 High speed differential transmitter positive.
D34	GTYTXN0_128	MGTYTXN0_128	128	Y35	O, DIFF	GTY Bank128 channel0 High speed differential transmitter negative.
D18	GTYRXP0_128	MGTYRXP0_128	128	W41	I, DIFF	GTY Bank128 channel0 High speed differential receiver positive.
D19	GTYRXN0_128	MGTYRXN0_128	128	W42	I, DIFF	GTY Bank128 channel0 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D31	GTYTXP1_128	MGTYTXP1_128	128	W36	O, DIFF	GTY Bank128 channel1 High speed differential transmitter positive.
D30	GTYTXN1_128	MGTYTXN1_128	128	W37	O, DIFF	GTY Bank128 channel1 High speed differential transmitter negative.
D14	GTYRXP1_128	MGTYRXP1_128	128	V39	I, DIFF	GTY Bank128 channel1 High speed differential receiver positive.
D15	GTYRXN1_128	MGTYRXN1_128	128	V40	I, DIFF	GTY Bank128 channel1 High speed differential receiver negative.
D27	GTYTXP2_128	MGTYTXP2_128	128	V34	O, DIFF	GTY Bank128 channel2 High speed differential transmitter positive.
D26	GTYTXN2_128	MGTYTXN2_128	128	V35	O, DIFF	GTY Bank128 channel2 High speed differential transmitter negative.
D10	GTYRXP2_128	MGTYRXP2_128	128	U41	I, DIFF	GTY Bank128 channel2 High speed differential receiver positive.
D11	GTYRXN2_128	MGTYRXN2_128	128	U42	I, DIFF	GTY Bank128 channel2 High speed differential receiver negative.
D23	GTYTXP3_128	MGTYTXP3_128	128	U36	O, DIFF	GTY Bank128 channel3 High speed differential transmitter positive.
D22	GTYTXN3_128	MGTYTXN3_128	128	U37	O, DIFF	GTY Bank128 channel3 High speed differential transmitter negative.
D6	GTYRXP3_128	MGTYRXP3_128	128	T39	I, DIFF	GTY Bank128 channel3 High speed differential receiver positive.
D7	GTYRXN3_128	MGTYRXN3_128	128	T40	I, DIFF	GTY Bank128 channel3 High speed differential receiver negative.
D2	GTREFCLK0P_128	MGTREFCLK0P_128	128	AB34	I, DIFF	GTY Bank128 channel0 High speed differential reference clock0 positive.
D3	GTREFCLK0N_128	MGTREFCLK0N_128	128	AB35	I, DIFF	GTY Bank128 channel0 High speed differential reference clock0 negative.
D39	GTREFCLK1P_128	MGTREFCLK1P_128	128	AA32	I, DIFF	GTY Bank128 channel1 High speed differential reference clock1 positive.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D38	GTREFCLK1N_128	MGTREFCLK1N_128	128	AA33	I, DIFF	GTY Bank128 channel1 High speed differential reference clock1 negative.
Bank129 Transceiver Quad Pins						
A32	GTYTXP0_129	MGTYTXP0_129	129	T34	O, DIFF	GTY Bank129 channel0 High speed differential transmitter positive.
A33	GTYTXN0_129	MGTYTXN0_129	129	T35	O, DIFF	GTY Bank129 channel0 High speed differential transmitter negative.
A40	GTYRXP0_129	MGTYRXP0_129	129	R41	I, DIFF	GTY Bank129 channel0 High speed differential receiver positive.
A41	GTYRXN0_129	MGTYRXN0_129	129	R42	I, DIFF	GTY Bank129 channel0 High speed differential receiver negative.
B30	GTYTXP1_129	MGTYTXP1_129	129	R36	O, DIFF	GTY Bank129 channel1 High speed differential transmitter positive.
B31	GTYTXN1_129	MGTYTXN1_129	129	R37	O, DIFF	GTY Bank129 channel1 High speed differential transmitter negative.
A36	GTYRXP1_129	MGTYRXP1_129	129	P39	I, DIFF	GTY Bank129 channel1 High speed differential receiver positive.
A37	GTYRXN1_129	MGTYRXN1_129	129	P40	I, DIFF	GTY Bank129 channel1 High speed differential receiver negative.
A28	GTYTXP2_129	MGTYTXP2_129	129	P34	O, DIFF	GTY Bank129 channel2 High speed differential transmitter positive.
A29	GTYTXN2_129	MGTYTXN2_129	129	P35	O, DIFF	GTY Bank129 channel2 High speed differential transmitter negative.
A25	GTYRXP2_129	MGTYRXP2_129	129	N41	I, DIFF	GTY Bank129 channel2 High speed differential receiver positive.
A24	GTYRXN2_129	MGTYRXN2_129	129	N42	I, DIFF	GTY Bank129 channel2 High speed differential receiver negative.
B26	GTYTXP3_129	MGTYTXP3_129	129	N36	O, DIFF	GTY Bank129 channel3 High speed differential transmitter positive.
B27	GTYTXN3_129	MGTYTXN3_129	129	N37	O, DIFF	GTY Bank129 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B23	GTYRXP3_129	MGTYRXP3_129	129	M39	I, DIFF	GTY Bank129 channel3 High speed differential receiver positive.
B22	GTYRXN3_129	MGTYRXN3_129	129	M40	I, DIFF	GTY Bank129 channel3 High speed differential receiver negative.
B38	GTREFCLK0P_129	MGTREFCLK0P_129	129	W32	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 positive.
B39	GTREFCLK0N_129	MGTREFCLK0N_129	129	W33	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 negative.
B34	GTREFCLK1P_129	MGTREFCLK1P_129	129	U32	I, DIFF	GTY Bank129 channel1 High speed differential reference clock1 positive.
B35	GTREFCLK1N_129	MGTREFCLK1N_129	129	U33	I, DIFF	GTY Bank129 channel1 High speed differential reference clock1 negative.
Bank130 Transceiver Quad Pins						
C41	GTYTXP0_130	MGTYTXP0_130	130	M34	O, DIFF	GTY Bank130 channel0 High speed differential transmitter positive.
C40	GTYTXN0_130	MGTYTXN0_130	130	M35	O, DIFF	GTY Bank130 channel0 High speed differential transmitter negative.
C9	GTYRXP0_130	MGTYRXP0_130	130	L41	I, DIFF	GTY Bank130 channel0 High speed differential receiver positive.
C8	GTYRXN0_130	MGTYRXN0_130	130	L42	I, DIFF	GTY Bank130 channel0 High speed differential receiver negative.
C13	GTYTXP1_130	MGTYTXP1_130	130	L36	O, DIFF	GTY Bank130 channel1 High speed differential transmitter positive.
C12	GTYTXN1_130	MGTYTXN1_13	130	L37	O, DIFF	GTY Bank130 channel1 High speed differential transmitter negative.
C29	GTYRXP1_130	MGTYRXP1_130	130	K39	I, DIFF	GTY Bank130 channel1 High speed differential receiver positive.
C28	GTYRXN1_130	MGTYRXN1_130	130	K40	I, DIFF	GTY Bank130 channel1 High speed differential receiver negative.
C37	GTYTXP2_130	MGTYTXP2_130	130	K34	O, DIFF	GTY Bank130 channel2 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
C36	GTYTXN2_130	MGTYTXN2_130	130	K35	O, DIFF	GTY Bank130 channel2 High speed differential transmitter negative.
C4	GTYRXP2_130	MGTYRXP2_130	130	J41	I, DIFF	GTY Bank130 channel2 High speed differential receiver positive.
C5	GTYRXN2_130	MGTYRXN2_130	130	J42	I, DIFF	GTY Bank130 channel2 High speed differential receiver negative.
C33	GTYTXP3_130	MGTYTXP3_130	130	J36	O, DIFF	GTY Bank130 channel3 High speed differential transmitter positive.
C32	GTYTXN3_130	MGTYTXN3_130	130	J37	O, DIFF	GTY Bank130 channel3 High speed differential transmitter negative.
C25	GTYRXP3_130	MGTYRXP3_130	130	H39	I, DIFF	GTY Bank130 channel3 High speed differential receiver positive.
C24	GTYRXN3_130	MGTYRXN3_130	130	H40	I, DIFF	GTY Bank130 channel3 High speed differential receiver negative.
C20	GTREFCLK0P_130	MGTREFCLK0P_130	130	R32	I, DIFF	GTY Bank130 channel0 High speed differential reference clock0 positive.
C21	GTREFCLK0N_130	MGTREFCLK0N_130	130	R33	I, DIFF	GTY Bank130 channel0 High speed differential reference clock0 negative.
C17	GTREFCLK1P_130	MGTREFCLK1P_130	130	N32	I, DIFF	GTY Bank130 channel1 High speed differential reference clock1 positive.
C16	GTREFCLK1N_130	MGTREFCLK1N_130	130	N33	I, DIFF	GTY Bank130 channel1 High speed differential reference clock1 negative.
Bank131 Transceiver Quad Pins						
B15	GTYTXP0_131	MGTYTXP0_131	131	H34	O, DIFF	GTY Bank131 channel0 High speed differential transmitter positive.
B14	GTYTXN0_131	MGTYTXN0_131	131	H35	O, DIFF	GTY Bank131 channel0 High speed differential transmitter negative.
A5	GTYRXP0_131	MGTYRXP0_131	131	G41	I, DIFF	GTY Bank131 channel0 High speed differential receiver positive.
A4	GTYRXN0_131	MGTYRXN0_131	131	G42	I, DIFF	GTY Bank131 channel0 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B11	GTYTXP1_131	MGTYTXP1_131	131	G36	O, DIFF	GTY Bank131 channel1 High speed differential transmitter positive.
B10	GTYTXN1_131	MGTYTXN1_131	131	G37	O, DIFF	GTY Bank131 channel1 High speed differential transmitter negative.
A9	GTYRXP1_131	MGTYRXP1_131	131	F39	I, DIFF	GTY Bank131 channel1 High speed differential receiver positive.
A8	GTYRXN1_131	MGTYRXN1_131	131	F40	I, DIFF	GTY Bank131 channel1 High speed differential receiver negative.
A17	GTYTXP2_131	MGTYTXP2_131	131	F34	O, DIFF	GTY Bank131 channel2 High speed differential transmitter positive.
A16	GTYTXN2_131	MGTYTXN2_131	131	F35	O, DIFF	GTY Bank131 channel2 High speed differential transmitter negative.
B3	GTYRXP2_131	MGTYRXP2_131	131	E41	I, DIFF	GTY Bank131 channel2 High speed differential receiver positive.
B2	GTYRXN2_131	MGTYRXN2_131	131	E42	I, DIFF	GTY Bank131 channel2 High speed differential receiver negative.
A13	GTYTXP3_131	MGTYTXP3_131	131	E36	O, DIFF	GTY Bank131 channel3 High speed differential transmitter positive.
A12	GTYTXN3_131	MGTYTXN3_131	131	E37	O, DIFF	GTY Bank131 channel3 High speed differential transmitter negative.
B7	GTYRXP3_131	MGTYRXP3_131	131	D39	I, DIFF	GTY Bank131 channel3 High speed differential receiver positive.
B6	GTYRXN3_131	MGTYRXN3_131	131	D40	I, DIFF	GTY Bank131 channel3 High speed differential receiver negative.
B19	GTREFCLK0P_131	MGTREFCLK0P_131	131	L32	I, DIFF	GTY Bank131 channel0 High speed differential reference clock0 positive.
B18	GTREFCLK0N_131	MGTREFCLK0N_131	131	L33	I, DIFF	GTY Bank131 channel0 High speed differential reference clock0 negative.
A21	GTREFCLK1P_131	MGTREFCLK1P_131	131	J32	I, DIFF	GTY Bank131 channel1 High speed differential reference clock1 positive.
A20	GTREFCLK1N_131	MGTREFCLK1N_131	131	J33	I, DIFF	GTY Bank131 channel1 High speed differential reference clock1 negative.

2.9.1.2 GTH High Speed Transceivers

The Zynq Ultrascale+ MPSoC SOM Supports 8 GTH transceivers along with reference clock inputs (Bank229 & 231) on Board-to-Board Connector3. For more details on GTH transceivers, refer section **2.7.2.1**.

For more details on GTH transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank229 Transceiver Quad Pins						
A44	GTHTXP0_229	MGTHTXP0_229	229	W6	O, DIFF	GTH Bank229 channel0 High speed differential transmitter positive.
A45	GTHTXN0_229	MGTHTXN0_229	229	W5	O, DIFF	GTH Bank229 channel0 High speed differential transmitter negative.
B50	GTHRXP0_229	MGTHRXP0_229	229	Y4	I, DIFF	GTH Bank229 channel0 High speed differential receiver positive.
B51	GTHRXN0_229	MGTHRXN0_229	229	Y3	I, DIFF	GTH Bank229 channel0 High speed differential receiver negative.
B46	GTHTXP1_229	MGTHTXP1_229	229	V8	O, DIFF	GTH Bank229 channel1 High speed differential transmitter positive.
B47	GTHTXN1_229	MGTHTXN1_229	229	V7	O, DIFF	GTH Bank229 channel1 High speed differential transmitter negative.
A56	GTHRXP1_229	MGTHRXP1_229	229	W2	I, DIFF	GTH Bank229 channel1 High speed differential receiver positive.
A57	GTHRXN1_229	MGTHRXN1_229	229	W1	I, DIFF	GTH Bank229 channel1 High speed differential receiver negative.
A52	GTHTXP2_229	MGTHTXP2_229	229	U6	O, DIFF	GTH Bank229 channel2 High speed differential transmitter positive.
A53	GTHTXN2_229	MGTHTXN2_229	229	U5	O, DIFF	GTH Bank229 channel2 High speed differential transmitter negative.
B54	GTHRXP2_229	MGTHRXP2_229	229	V4	I, DIFF	GTH Bank229 channel2 High speed differential receiver positive.
B55	GTHRXN2_229	MGTHRXN2_229	229	V3	I, DIFF	GTH Bank229 channel2 High speed differential receiver negative.
A48	GTHTXP3_229	MGTHTXP3_229	229	T8	O, DIFF	GTH Bank229 channel3 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A49	GTHTXN3_229	MGTHTXN3_229	229	T7	O, DIFF	GTH Bank229 channel3 High speed differential transmitter negative.
B58	GTHRXP3_229	MGTHRXP3_229	229	U2	I, DIFF	GTH Bank229 channel3 High speed differential receiver positive.
B59	GTHRXN3_229	MGTHRXN3_229	229	U1	I, DIFF	GTH Bank229 channel3 High speed differential receiver negative.
B42	GTREFCLK0P_229	MGTREFCLK0P_229	229	Y12	I, DIFF	GTH Bank229 channel0 High speed differential reference clock0 positive.
B43	GTREFCLK0N_229	MGTREFCLK0N_229	229	Y11	I, DIFF	GTH Bank229 channel0 High speed differential reference clock0 negative.
A59	GTREFCLK1N_229	MGTREFCLK1N_229	229	W9	I, DIFF	GTH Bank229 channel1 High speed differential reference clock1 negative.
A60	GTREFCLK1P_229	MGTREFCLK1P_229	229	W10	I, DIFF	GTH Bank229 channel1 High speed differential reference clock1 positive.
Bank231 Transceiver Quad Pins						
C52	GTHTXP0_231	MGTHTXP0_231	231	L6	O, DIFF	GTH Bank231 channel0 High speed differential transmitter positive.
C53	GTHTXN0_231	MGTHTXN0_231	231	L5	O, DIFF	GTH Bank231 channel0 High speed differential transmitter negative.
D51	GTHRXP0_231	MGTHRXP0_231	231	M4	I, DIFF	GTH Bank231 channel0 High speed differential receiver positive.
D50	GTHRXN0_231	MGTHRXN0_231	231	M3	I, DIFF	GTH Bank231 channel0 High speed differential receiver negative.
C57	GTHTXP1_231	MGTHTXP1_231	231	K4	O, DIFF	GTH Bank231 channel1 High speed differential transmitter positive.
C56	GTHTXN1_231	MGTHTXN1_231	231	K3	O, DIFF	GTH Bank231 channel1 High speed differential transmitter negative.
D43	GTHRXP1_231	MGTHRXP1_231	231	L2	I, DIFF	GTH Bank231 channel1 High speed differential receiver positive.
D42	GTHRXN1_231	MGTHRXN1_231	231	L1	I, DIFF	GTH Bank231 channel1 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D54	GTHTXP2_231	MGTHTXP2_231	231	J6	O, DIFF	GTH Bank231 channel2 High speed differential transmitter positive.
D55	GTHTXN2_231	MGTHTXN2_231	231	J5	O, DIFF	GTH Bank231 channel2 High speed differential transmitter negative.
C45	GTHRXP2_231	MGTHRXP2_231	231	J2	I, DIFF	GTH Bank231 channel2 High speed differential receiver positive.
C44	GTHRXN2_231	MGTHRXN2_231	231	J1	I, DIFF	GTH Bank231 channel2 High speed differential receiver negative.
D58	GTHTXP3_231	MGTHTXP3_231	231	H4	O, DIFF	GTH Bank231 channel3 High speed differential transmitter positive.
D59	GTHTXN3_231	MGTHTXN3_231	231	H3	O, DIFF	GTH Bank231 channel3 High speed differential transmitter negative.
D47	GTHRXP3_231	MGTHRXP3_231	231	G2	I, DIFF	GTH Bank231 channel3 High speed differential receiver positive.
D46	GTHRXN3_231	MGTHRXN3_231	231	G1	I, DIFF	GTH Bank231 channel3 High speed differential receiver negative.
C48	GTREFCLK0P_231	MGTREFCLK0P_231	231	T12	I, DIFF	GTH Bank231 channel0 High speed differential reference clock0 positive.
C49	GTREFCLK0N_231	MGTREFCLK0N_231	231	T11	I, DIFF	GTH Bank231 channel0 High speed differential reference clock0 negative.
A2	GTREFCLK1P_231	MGTREFCLK1P_231	231	R10	I, DIFF	GTH Bank231 channel1 High speed differential reference clock1 positive.
A1	GTREFCLK1N_231	MGTREFCLK1N_231	231	R9	I, DIFF	GTH Bank231 channel1 High speed differential reference clock1 negative.

2.9.2 Power

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector 3 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A3, A6, A7, A10, A11, A14, A15, A18, A19, A22, A23, A26, A27, A30, A31, A34, A35, A38, A39, A42, A43, A46, A47, A50, A51, A54, A55, A58, B1, B4, B5, B8, B9, B12, B13, B16, B17, B20, B21, B24, B25, B28, B29, B32, B33, B36, B37, B40, B41, B44, B45, B48, B49, B52, B53, B56, B57, B60, C2, C3, C6, C7, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54, C55, C58, C59, D1, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, D24, D25, D28, D29, D32, D33, D36, D37, D40, D41, D44, D45, D48, D49, D52, D53, D56, D57, D60,	GND	NA	NA	NA	Power	Ground.

2.10 Board-to-Board Connector4

The Zynq Ultrascale+ MPSoC SOM Board to Board connector4 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector4 are explained in the following sections. The Board-to-Board Connector4 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 80

Connector Part Number - ADM6-20-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-20-03.5-L-4-2-A from Samtech

Staking Height - 5mm

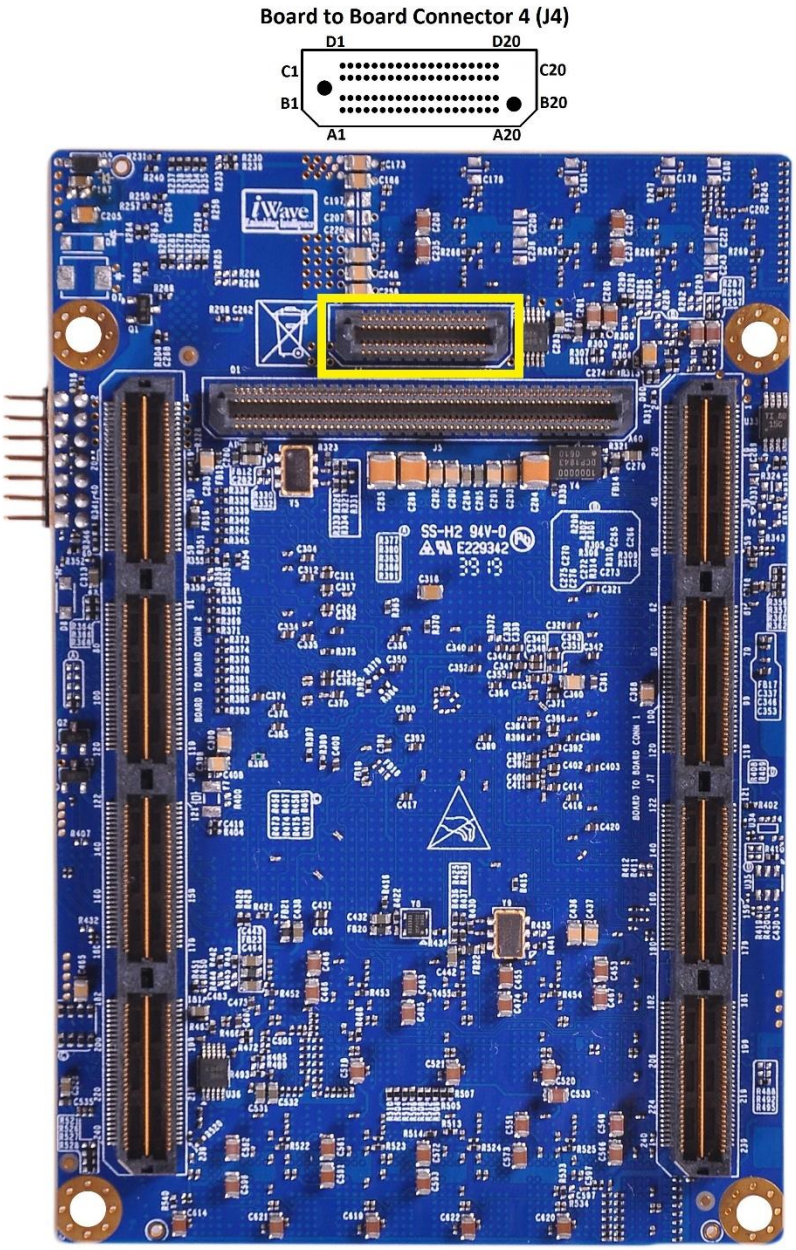


Figure 10: Board to Board Connector4

Table 10: Board to Board Connector4 Pinout

B2B-4 Pin No.	Signal Name	B2B-4 Pin No.	Signal Name	B2B-4 Pin No.	Signal Name	B2B-4 Pin No.	Signal Name
A1	GND	**B1**	GTREFCLK1N_230	**C1**	GND	**D1**	NC
A2	GTHRXN1_230	**B2**	GTREFCLK1P_230	**C2**	GTHTXP0_228	**D2**	GND
A3	GTHRXP1_230	**B3**	GND	**C3**	GTHTXN0_228	**D3**	GND
A4	GND	**B4**	GTHRXN3_230	**C4**	GND	**D4**	GTHTXP1_228
A5	GND	**B5**	GTHRXP3_230	**C5**	GND	**D5**	GTHTXN1_228
A6	GTREFCLK0P_230	**B6**	GND	**C6**	GTHTXP3_228	**D6**	GND
A7	GTREFCLK0N_230	**B7**	GND	**C7**	GTHTXN3_228	**D7**	GND
A8	GND	**B8**	GTHRXN2_230	**C8**	GND	**D8**	GTREFCLK0N_228
A9	GND	**B9**	GTHRXP2_230	**C9**	GND	**D9**	GTREFCLK0P_228
A10	GTHTXP0_230	**B10**	GND	**C10**	GTHTXN2_228	**D10**	GND
A11	GTHTXN0_230	**B11**	GND	**C11**	GTHTXP2_228	**D11**	GND
A12	GND	**B12**	GTHTXP3_230	**C12**	GND	**D12**	GTHRXN1_228
A13	GND	**B13**	GTHTXN3_230	**C13**	GND	**D13**	GTHRXP1_228
A14	GTHTXP1_230	**B14**	GND	**C14**	GTHRXP2_228	**D14**	GND
A15	GTHTXN1_230	**B15**	GND	**C15**	GTHRXN2_228	**D15**	GND
A16	GND	**B16**	GTHRXN0_230	**C16**	GND	**D16**	GTHRXP3_228
A17	GND	**B17**	GTHRXP0_230	**C17**	GND	**D17**	GTHRXN3_228
A18	GTHTXP2_230	**B18**	GND	**C18**	GTHRXN0_228	**D18**	GND
A19	GTHTXN2_230	**B19**	GND	**C19**	GTHRXP0_228	**D19**	GTREFCLK1N_228
A20	GND	**B20**	NC	**C20**	GND	**D20**	GTREFCLK1P_228

2.10.1 PL Interfaces

The interfaces which are supported in Board-to-Board Connector4 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.10.1.1 GTYHigh Speed Transceiver

The Zynq Ultrascale+ MPSoC SOM Supports 8 GTH transceivers along with reference clock inputs (Bank228 & 230) on Board-to-Board Connector4. For more details on GTH transceivers, refer section **2.7.2.1**.

For more details on GTH transceiver pinouts on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector4 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank228 Transceiver Quad Pins						
C2	GTHTXP0_228	MGTHTXP0_228	228	AC6	O, DIFF	GTH Bank228 channel0 High speed differential transmitter positive.
C3	GTHTXN0_228	MGTHTXN0_228	228	AC5	O, DIFF	GTH Bank228 channel0 High speed differential transmitter negative.
C19	GTHRXP0_228	MGTHRXP0_228	228	AD4	I, DIFF	GTH Bank228 channel0 High speed differential receiver positive.
C18	GTHRXN0_228	MGTHRXN0_228	228	AD3	I, DIFF	GTH Bank228 channel0 High speed differential receiver negative.
D4	GTHTXP1_228	MGTHTXP1_228	228	AB8	O, DIFF	GTH Bank228 channel1 High speed differential transmitter positive.
D5	GTHTXN1_228	MGTHTXN1_228	228	AB7	O, DIFF	GTH Bank228 channel1 High speed differential transmitter negative.
D13	GTHRXP1_228	MGTHRXP1_228	228	AC2	I, DIFF	GTH Bank228 channel1 High speed differential receiver positive.
D12	GTHRXN1_228	MGTHRXN1_228	228	AC1	I, DIFF	GTH Bank228 channel1 High speed differential receiver negative.
C11	GTHTXP2_228	MGTHTXP2_228	228	AA6	O, DIFF	GTH Bank228 channel2 High speed differential transmitter positive.
C10	GTHTXN2_228	MGTHTXN2_228	228	AA5	O, DIFF	GTH Bank228 channel2 High speed differential transmitter negative.
C14	GTHRXP2_228	MGTHRXP2_228	228	AB4	I, DIFF	GTH Bank228 channel2 High speed differential receiver positive.
C15	GTHRXN2_228	MGTHRXN2_228	228	AB3	I, DIFF	GTH Bank228 channel2 High speed differential receiver negative.

B2B-4 Pin No	B2B Connector4 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
C6	GTHTXP3_228	MGTHTXP3_228	228	Y8	O, DIFF	GTH Bank228 channel3 High speed differential transmitter positive.
C7	GTHTXN3_228	MGTHTXN3_228	228	Y7	O, DIFF	GTH Bank228 channel3 High speed differential transmitter negative.
D16	GTHRXP3_228	MGTHRXP3_228	228	AA2	I, DIFF	GTH Bank228 channel3 High speed differential receiver positive.
D17	GTHRXN3_228	MGTHRXN3_228	228	AA1	I, DIFF	GTH Bank228 channel3 High speed differential receiver negative.
D9	GTREFCLK0P_228	MGTREFCLK0P_228	228	AB12	I, DIFF	GTH Bank228 channel0 High speed differential reference clock0 positive.
D8	GTREFCLK0N_228	MGTREFCLK0N_228	228	AB11	I, DIFF	GTH Bank228 channel0 High speed differential reference clock0 negative.
D20	GTREFCLK1P_228	MGTREFCLK1P_228	228	AA10	I, DIFF	GTH Bank228 channel1 High speed differential reference clock1 positive.
D19	GTREFCLK1N_228	MGTREFCLK1N_228	228	AA9	I, DIFF	GTH Bank228 channel1 High speed differential reference clock1 negative.
Bank230 Transceiver Quad Pins						
A10	GTHTXP0_230	MGTHTXP0_230	230	R6	O, DIFF	GTH Bank230 channel0 High speed differential transmitter positive.
A11	GTHTXN0_230	MGTHTXN0_230	230	R5	O, DIFF	GTH Bank230 channel0 High speed differential transmitter negative.
B17	GTHRXP0_230	MGTHRXP0_230	230	T4	I, DIFF	GTH Bank230 channel0 High speed differential receiver positive.
B16	GTHRXN0_230	MGTHRXN0_230	230	T3	I, DIFF	GTH Bank230 channel0 High speed differential receiver negative.
A14	GTHTXP1_230	MGTHTXP1_230	230	P8	O, DIFF	GTH Bank230 channel1 High speed differential transmitter positive.
A15	GTHTXN1_230	MGTHTXN1_230	230	P7	O, DIFF	GTH Bank230 channel1 High speed differential transmitter negative.
A3	GTHRXP1_230	MGTHRXP1_230	230	R2	I, DIFF	GTH Bank230 channel1 High speed differential receiver positive.

B2B-4 Pin No	B2B Connector4 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A2	GTHRXN1_230	MGTHRXN1_230	230	R1	I, DIFF	GTH Bank230 channel1 High speed differential receiver negative.
A18	GTHTXP2_230	MGTHTXP2_230	230	N6	O, DIFF	GTH Bank230 channel2 High speed differential transmitter positive.
A19	GTHTXN2_230	MGTHTXN2_230	230	N5	O, DIFF	GTH Bank230 channel2 High speed differential transmitter negative.
B9	GTHRXP2_230	MGTHRXP2_230	230	P4	I, DIFF	GTH Bank230 channel2 High speed differential receiver positive.
B8	GTHRXN2_230	MGTHRXN2_230	230	P3	I, DIFF	GTH Bank230 channel2 High speed differential receiver negative.
B12	GTHTXP3_230	MGTHTXP3_230	230	M8	O, DIFF	GTH Bank230 channel3 High speed differential transmitter positive.
B13	GTHTXN3_230	MGTHTXN3_230	230	M7	O, DIFF	GTH Bank230 channel3 High speed differential transmitter negative.
B5	GTHRXP3_230	MGTHRXP3_230	230	N2	I, DIFF	GTH Bank230 channel3 High speed differential receiver positive.
B4	GTHRXN3_230	MGTHRXN3_230	230	N1	I, DIFF	GTH Bank230 channel3 High speed differential receiver negative.
A6	GTREFCLK0P_230	MGTREFCLK0P_230	230	V12	I, DIFF	GTH Bank230 channel0 High speed differential reference clock0 positive.
A7	GTREFCLK0N_230	MGTREFCLK0N_230	230	V11	I, DIFF	GTH Bank230 channel0 High speed differential reference clock0 negative.
B2	GTREFCLK1P_230	MGTREFCLK1P_230	230	U10	I, DIFF	GTH Bank230 channel1 High speed differential reference clock1 positive.
B1	GTREFCLK1N_230	MGTREFCLK1N_230	230	U9	I, DIFF	GTH Bank230 channel1 High speed differential reference clock1 negative.

2.10.2 Power

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector4, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector4, refer the below table.

B2B-4 Pin No	B2B Connector 4 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A1, A4, A5, A8, A9, A12, A13, A16, A17, A20, B3, B6, B7, B10, B11, B14, B15, B18, B19, C1, C4, C5, C8, C9, C12, C13, C16, C17, C20, D2, D3, D6, D7, D10, D11, D14, D15, D18	GND	NA	NA	NA	Power	Ground.

2.11 Zynq Ultrascale+ MPSoC PS Pin Multiplexing on Board-to-Board Connectors

The Zynq Ultrascale+ MPSoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of MPSoC PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq Ultrascale+ MPSoC (ZU11/17/19EG) with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 11: PS IOMUX on Zynq Ultrascale+ MPSoC SOM

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SOM Features from MPSoC PS																
eMMC FLASH	NA	PS_MIO13_500	GPIO13	NFC_CE	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
	NA	PS_MIO14_500	GPIO14	NFC_CLE	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	-
	NA	PS_MIO15_500	GPIO15	NFC_ALE	eMMC_DATA2	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO16_500	GPIO16	NFC_DATA0	eMMC _DATA3	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO17_500	GPIO17	NFC_DATA1	eMMC _DATA4	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	-
	NA	PS_MIO18_500	GPIO18	NFC_DATA2	eMMC _DATA5	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	-
	NA	PS_MIO19_500	GPIO19	NFC_DATA3	eMMC _DATA6	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	-
	NA	PS_MIO20_500	GPIO20	NFC_DATA4	eMMC _DATA7	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO21_500	GPIO21	NFC_DATA5	eMMC _CMD	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
	NA	PS_MIO22_500	GPIO22	NFC_WE_B	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
	NA	PS_MIO23_500	GPIO23	NFC_DATA6	eMMC_Reset	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
GEM0	NA	PS_MIO26_501	GPIO26	GEM0_TX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	NA	PS_MIO27_501	GPIO27	GEM0_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
	NA	PS_MIO28_501	GPIO28	GEM0_TXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	NA	PS_MIO29_501	GPIO29	GEM0_TXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
	NA	PS_MIO30_501	GPIO30	GEM0_TXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
	NA	PS_MIO31_501	GPIO31	GEM0_TX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO32_501	GPIO32	GEM0_RX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO33_501	GPIO33	GEM0_RXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO34_501	GPIO34	GEM0_RXD1	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO35_501	GPIO35	GEM0_RXD2	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO36_501	GPIO36	GEM0_RXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO37_501	GPIO37	GEM0_RX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO76_502	GPIO76	GEM0_MDC	-	SD1_CLK	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	-	-
	NA	PS_MIO77_502	GPIO77	GEM0_MDIO	-	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	-	-
	NA	PS_MIO12_500	GPIO12	-	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO42_501	GPIO42	GEM1_TXD3	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
USB2.0	NA	PS_MIO52_502	GPIO52	GEM2_TX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	USB0_CLK
	NA	PS_MIO53_502	GPIO53	GEM2_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	USB0_DIR
	NA	PS_MIO54_502	GPIO54	GEM2_TXD1	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	USB0_DATA2
	NA	PS_MIO55_502	GPIO55	GEM2_TXD2	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	USB0_NXT
	NA	PS_MIO56_502	GPIO56	GEM2_TXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-		UART1_TX	USB0_DATA0
	NA	PS_MIO57_502	GPIO57	GEM2_TX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-		UART1_RX	USB0_DATA1
	NA	PS_MIO58_502	GPIO58	GEM2_RX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	-	SPI1_SCLK	UART0_RX	-	USB0_STP
	NA	PS_MIO59_502	GPIO59	GEM2_RXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	-	SPI1_SS2	UART0_TX	-	USB0_DATA3
	NA	PS_MIO60_502	GPIO60	GEM2_RXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	-	SPI1_SS1	-	UART1_TX	USB0_DATA4
	NA	PS_MIO61_502	GPIO61	GEM2_RXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	-	SPI1_SS0	-	UART1_RX	USB0_DATA5
	NA	PS_MIO62_502	GPIO62	GEM2_RXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB0_DATA6
	NA	PS_MIO63_502	GPIO63	GEM2_RX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB0_DATA7

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SOM Features from MPSoC PS																
Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
Board to Board Connector1 Interfaces from MPSoC PS																
GEM3/USB1	190	PS_MIO64_502	GPIO64	GEM3_TX_CLK	eMMC _CLK	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_SCLK	-	-	UART1_TX	USB1_CLK
	192	PS_MIO65_502	GPIO65	GEM3_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_SS2	-	-	UART1_RX	USB1_DIR
	194	PS_MIO66_502	GPIO66	GEM3_TXD1	eMMC _CMD	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_SS1	-	UART0_RX	-	USB1_DATA2
	196	PS_MIO67_502	GPIO67	GEM3_TXD2	eMMC_DATA0	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_SS0	-	UART0_TX	-	USB1_NXT
	198	PS_MIO68_502	GPIO68	GEM3_TXD3	eMMC _DATA1	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	USB1_DATA0
	210	PS_MIO69_502	GPIO69	GEM3_TX_CTL	eMMC_DATA2	SD1_WP	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	USB1_DATA1
	212	PS_MIO70_502	GPIO70	GEM3_RX_CLK	eMMC _DATA3	SD1_PWR	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	USB1_STP
	224	PS_MIO71_502	GPIO71	GEM3_RXD0	eMMC _DATA4	SD1_DATA0	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	USB1_DATA3
	226	PS_MIO72_502	GPIO72	GEM3_RXD1	eMMC _DATA5	SD1_DATA1	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	USB1_DATA4
	228	PS_MIO73_502	GPIO73	GEM3_RXD2	eMMC _DATA6	SD1_DATA2	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	USB1_DATA5
	230	PS_MIO74_502	GPIO74	GEM3_RXD3	eMMC _DATA7	SD1_DATA3	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB1_DATA6
	214	PS_MIO75_502	GPIO75	GEM3_RX_CTL	eMMC_Reset	SD1_CMD	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB1_DATA7
CAN0	207	PS_MIO38_501	GPIO38	GEM1_TX_CLK	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	209	PS_MIO39_501	GPIO39	GEM1_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
CAN1	213	PS_MIO40_501	GPIO40	GEM1_TXD1	eMMC _CMD	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	211	PS_MIO41_501	GPIO41	GEM1_TXD2	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
GPIO	178	PS_MIO1_500	GPIO1	QSPI_MISO	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
Board to Board Connector2 Interfaces from MPSoC PS																
SD1(4-Bit)	40	PS_MIO44_501	GPIO44	GEM1_RX_CLK	eMMC _DATA3	SD1_WP	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	42	PS_MIO45_501	GPIO45	GEM1_RXD0	eMMC _DATA4	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	44	PS_MIO43_501	GPIO43	GEM1_TX_CTL	eMMC_DATA2	SD1_PWR	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	69	PS_MIO46_501	GPIO46	GEM1_RXD1	eMMC _DATA5	SD1_DATA0	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	66	PS_MIO47_501	GPIO47	GEM1_RXD2	eMMC _DATA6	SD1_DATA1	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	64	PS_MIO48_501	GPIO48	GEM1_RXD3	eMMC _DATA7	SD1_DATA2	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	62	PS_MIO49_501	GPIO49	GEM1_RX_CTL	eMMC_Reset	SD1_DATA3	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	71	PS_MIO50_501	GPIO50	GEM1_MDC	-	SD1_CMD	CAN0_RX	-	I2C0_SCL	-	-	-	-	UART0_RX	-	-
	72	PS_MIO51_501	GPIO51	GEM1_MDIO	-	SD1_CLK	CAN0_TX	-	I2C0_SDA	-	-	-	-	UART0_TX	-	-
SPI	61	PS_MIO0_500	GPIO0	QSPI_SCLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	63	PS_MIO3_500	GPIO3	QSPI_SS0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UAR`T0_TX	-	-
	67	PS_MIO4_500	GPIO4	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	65	PS_MIO5_500	GPIO5	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MOSI	-	-	UART1_RX	-
Debug UART (UART0)	54	PS_MIO07_500					CAN0_TX		I2C0_SDA				SPI1_SS2		UART0_TX	
	56	PS_MIO06_500					CAN0_RX		I2C0_SCL				SPI1_SCLK		UART0_RX	
UART1	50	PS_MIO08_500	GPIO8	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	52	PS_MIO09_500	GPIO9	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
I2C0	46	PS_MIO11_500	GPIO11	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
	48	PS_MIO10_500	GPIO10	NFC_RB_N	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
GPIOs/I2C1	38	PS_MIO25_500	GPIO25	NFC_RE_N	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	UART1_RX	-
	70	PS_MIO24_500	GPIO24	NFC_DATA7	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	UART1_TX	-
JTAG	27	PS_JTAG_TDI	-	PS_JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-
	29	PS_JTAG_TMS	-	PS_JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-
	31	PS_JTAG_TCK	-	PS_JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-
	33	PS_JTAG_TDO	-	PS_JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Specification

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM.

Table 12: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V [2]	0V	3V	3.15V	±20mV

[1] Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.

[2] Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board-to-Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

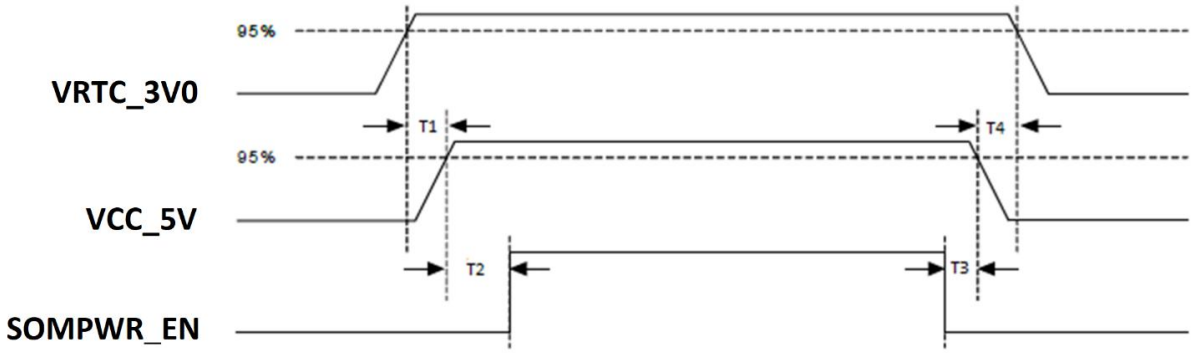


Figure 11: Power Input Sequencing

Table 13: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_5V input power to other all the powers are getting stable around 25ms in SOM, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

Table 14: Power Consumption

Task/Status	Power Rail	Current Drawn/Power Consumption
Only Booting Test (from Power-on to till Kernel)	VCC_5V	2.75A/13.75W
Ping Ethernet (Gem0) Ping Ethernet (Gem3) GPU DP eMMC Read/Write or SATA Read/Write or PCIex4 Storage device Read/Write or USB type-C Read/Write		2.9A/14.5W
SDI In/Out Test		2.8A/14W
FMC+ & FMC Loopback test		2.85A/14.25W
FMC+/FMC/FireFly/SFP/QSFP+ Transceiver Loopback test through iBERT.		7.5A/37.5W

Note: This measurement is done in ZU19EG -1 speed grade SOM with iWave's FPGA Design & PetaLinux BSP release

For more accurate power estimation, iWave recommends to use Xilinx Power Estimator (XPE) tool and calculate the MPSoC power. Also add extra 4A for other On-SOM peripherals power.

For reference, we have calculated the Zynq Ultrascale+ MPSoC (ZU11/17/19EG) Theoretical Power Estimation by using Xilinx Power Estimator (XPE) tool with various FPGA utilisation and ambient temperature as shown below.

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 5V			
	25 C Ambient		60 C Ambient	
	TYP	Max	TYP	Max
25	11.477A/57.385W	13.773A/68.865W	13.082A/65.41W	15.699A/78.495W
50	13.804A/69.02W	16.565A/82.825W	16.192A/80.96W	19.430A/97.15W
80	16.975A/84.875W	20.370A/101.85W	21.118/105.59W	25.342A/126.71W
100	18.534A/92.67W	22.228A/111.14W	21.604A/108.82W	25.918A/129.59W

Note: This calculation is based on 19EG device with maximum Process @ -3 Speed Grade

3.2 Environmental Characteristics

3.2.1 Temperature Specifiaction

The below table provides the Environment specification of Versal Premium SOM.

Table 15: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	100°C
Operating temperature range - Extended[1]	0°C	100°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 ROHS2 Compliance

iWave's Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

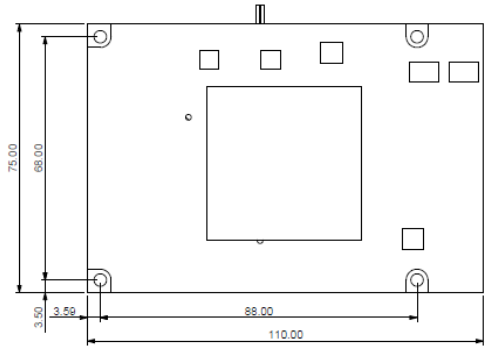


Fig 1.1

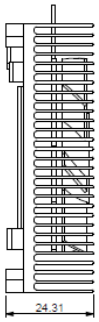


Fig 1.2

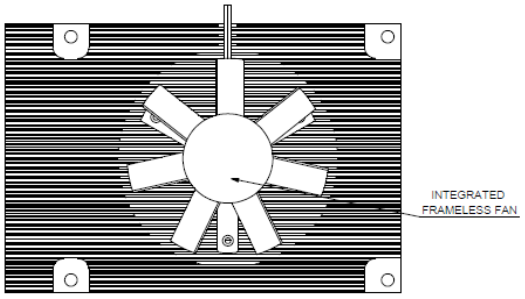


Fig 1.3

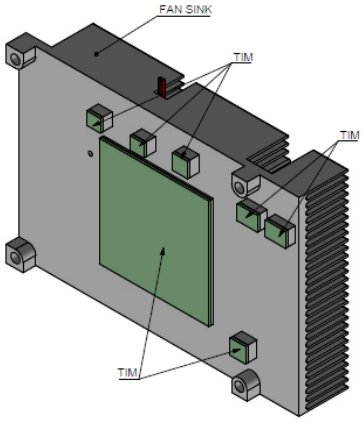


Fig 1.4

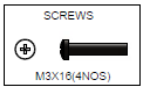


Fig 1.5

TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	T056010BHZC0U3aR
DIMENSIONS	60X60X10.5mm
AIR FLOW	18.14CFM 0.51m3/min
STATIC PRESSURE	3.00mmH2O
RATED VOLTAGE	5V
LIFE EXPECTANCY	50,000hours at 40°C (WITH 15~65% RH)
ROHS	YES

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	12.5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 12: Heat Sink

3.3 Mechanical Characteristics

3.3.1 Zynq Ultrascale+ MPSoC SOM Mechanical Dimension

Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM PCB size is 110mm x 75mm x 2.116mm and weight is 95g. SOM mechanical dimension is shown below.

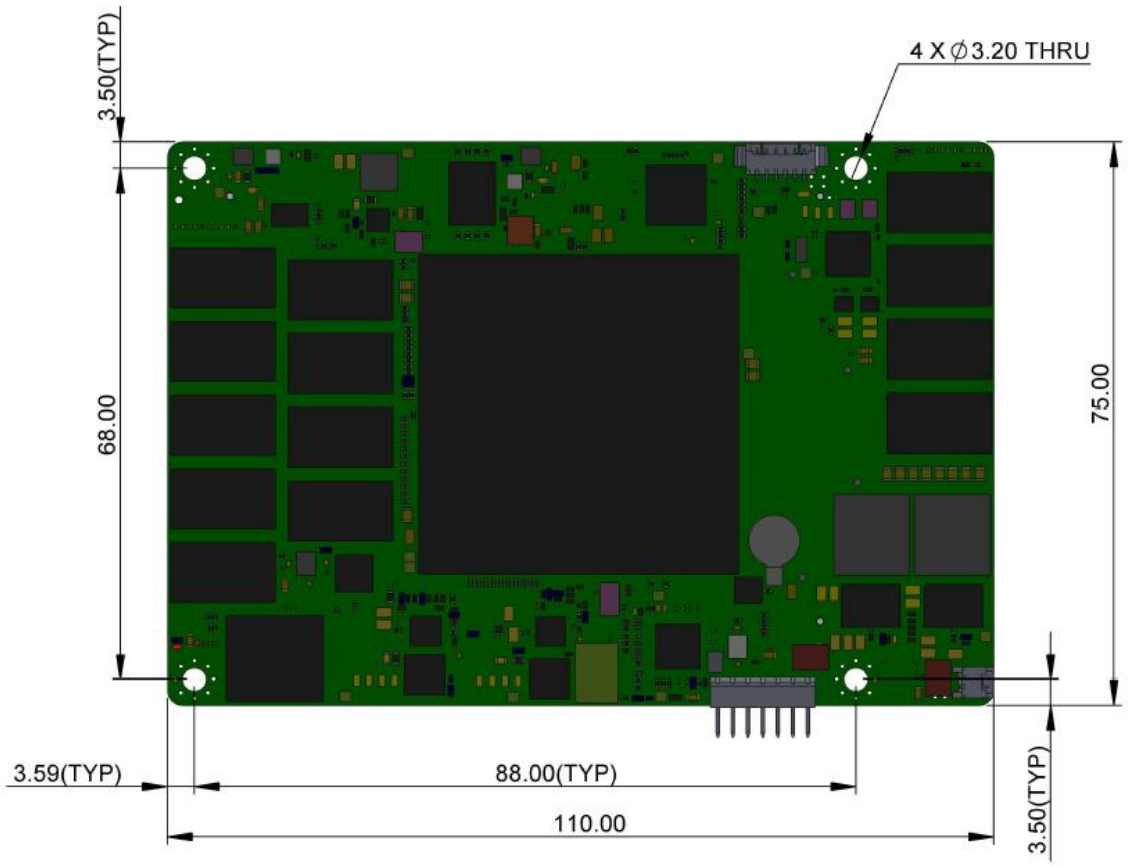


Figure 13:Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Top View

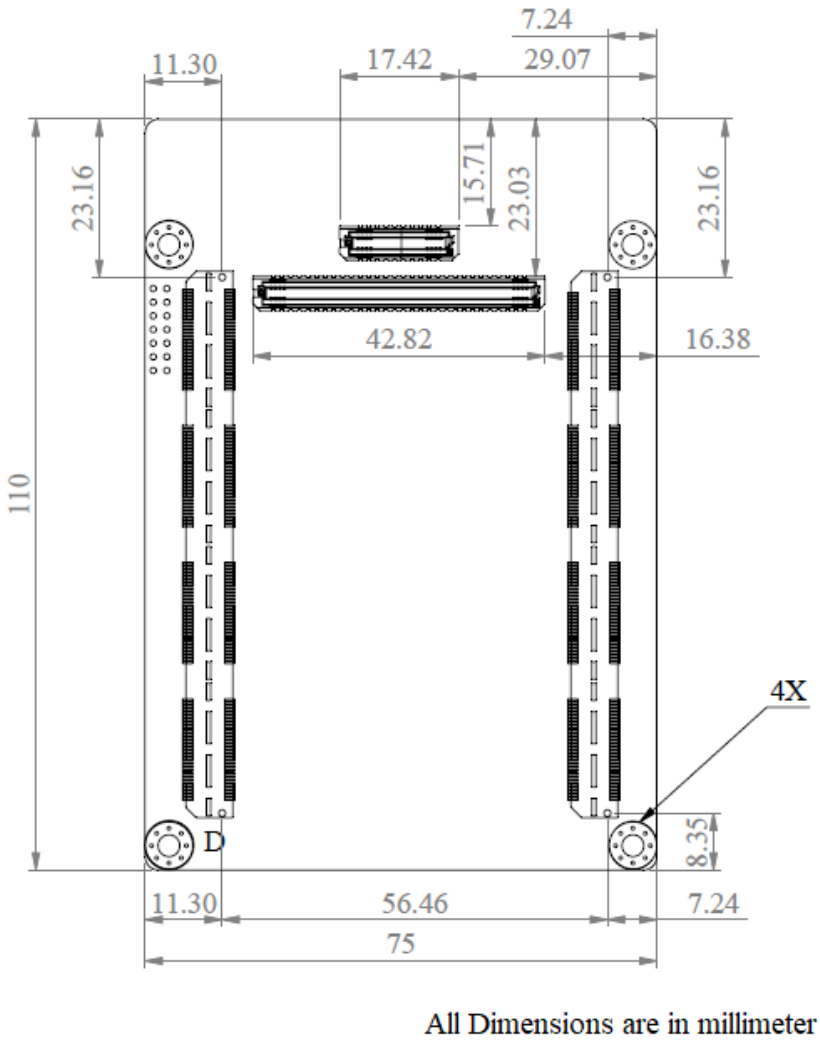


Figure 14: Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Bottom View

Zynq Ultrascale+ MPSoC (ZU11/17/19EG) PCB thickness is 2.116mm±0.1mm, top side maximum height component is JTAG Header J3 (4.30mm) followed by power inductors L1&L2 (4.00mm) and bottom side maximum height component is Board to Board connector 1 & 2 (4.27mm) followed by Board to Board connector 3(4.02mm). Please refer the below figure which gives height details of the Zynq Ultrascale+ MPSoC SOM.

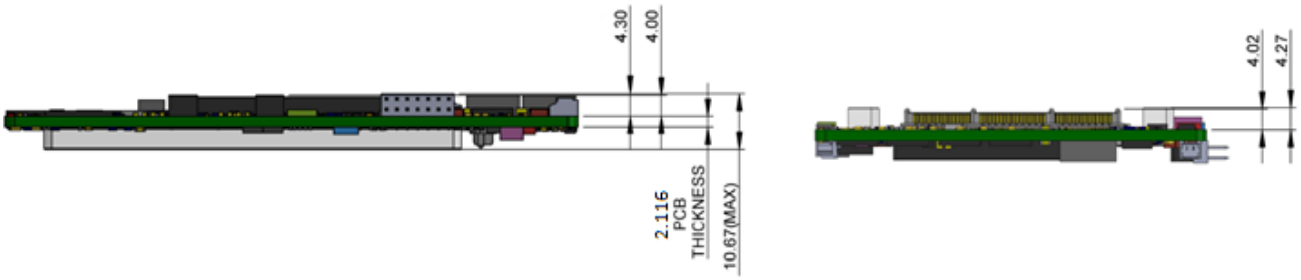


Figure 15: Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 16: Orderable Product Part Numbers

Product Part Number	Description	Temperature
ZU11 MPSoC based SOM		
iW-G35M-11EG-4E004G-E008G-BIA	ZU11EG (-1) MPSoC (XCZU11EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC, – Boot Code Loaded	Industrial
iW-G35M-11EG-4E004G-E008G-LIA	ZU11EG (-1) MPSoC (XCZU11EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC – Linux Loaded	Industrial
ZU17 MPSoC based SOM		
iW-G35M-17EG-4E004G-E008G-BIA	ZU17EG (-1) MPSoC (XCZU17EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC, - Boot Code Loaded	Industrial
iW-G35M-17EG-4E004G-E008G-LIA	ZU17EG (-1) MPSoC (XCZU17EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC – Linux Loaded	Industrial
ZU19 MPSoC based SOM		
iW-G35M-19EG-4E004G-E008G-BIA	ZU19EG (-1) MPSoC (XCZU19EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC– Boot Code Loaded	Industrial
iW-G35M-19EG-4E004G-E008G-LIA	ZU19EG (-1) MPSoC (XCZU19EG-1FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC- Linux Loaded	Industrial
iW-G35M-19EG-4E004G-E008G-BIE	ZU19EG (-2) MPSoC (XCZU19EG-2FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC- Boot Code Loaded	Industrial
iW-G35M-19EG-4E004G-E008G-LIE	ZU19EG (-2) MPSoC (XCZU19EG-2FFVC1760I), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC- Linux Loaded	Industrial
iW-G35M-19EG-4E004G-E008G-BEF	ZU19EG (-3) MPSoC (XCZU19EG-3FFVC1760E), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC- Boot Code Loaded	Extended
iW-G35M-19EG-4E004G-E008G-LEF	ZU19EG (-3) MPSoC (XCZU19EG-3FFVC1760E), 4GB PS DDR4 with ECC, Dual 4GB PL DDR4 and 8GB EMMC- Boot Code Loaded	Extended

5. APPENDIX

5.1 Zynq Ultrascale+ MPSoC SOM Development Platform

iWave Global supports iW-RainboW-G35D – Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Development Platform which is targeted for quick validation of Zynq Ultrascale+ MPSoC (ZU11/17/19EG) based SOM. iWave's Zynq Ultrascale+ MPSoC Development Board incorporates Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM and High-performance Carrier board with complete BSP support.

For more details on Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Development Platform, visit the below web link.

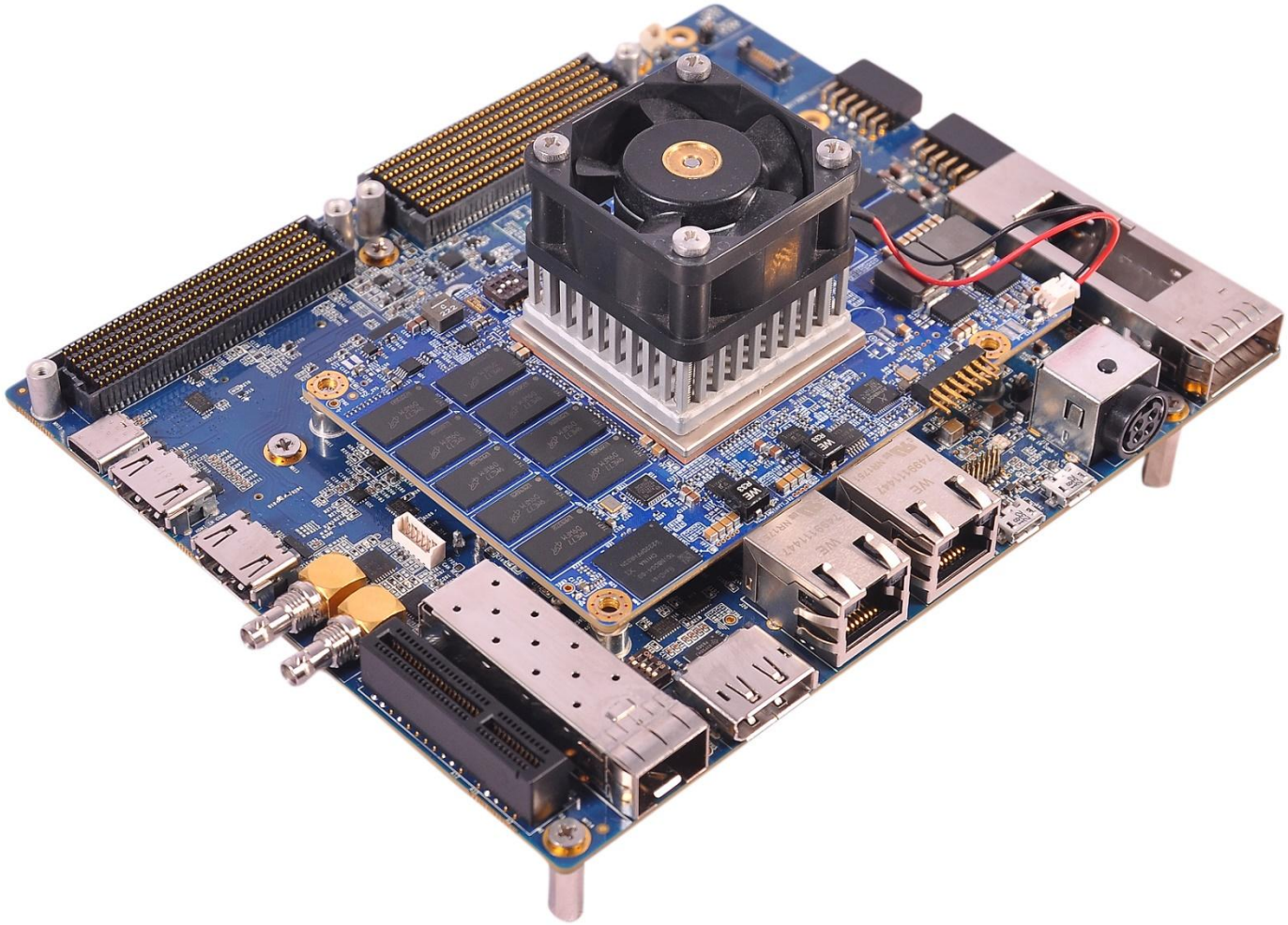


Figure 16: Zynq Ultrascale+ MPSoC (ZU11/17/19EG) SOM Development Platform

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Beyond our robust product ecosystem, we provide comprehensive ODM support with specialized custom design and manufacturing capabilities, enabling customers to accelerate and optimize their product development roadmaps. With a strategic focus on industrial, automotive, medical, and avionics markets, we deliver innovative technology solutions to global clients.

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