

Datasheet

Nitrogen8ULP SOM

Version 2.2

Revision History

Version	Date	Notes	Contributors	Approver
0.1	1 Nov 2023	Preliminary Release	Gary Bisson	Dan Kephart
1.0	27 Feb 2024	Update DC Power Consumption Table Updated Pin Muxing (Table 7) to match REV11B Added Default Muxing to J1: Pin 90/99, J2: Pin 36/45 Corrected GPIO Muxing on J2: Pin 99 Corrected Pin Muxing on J3: Pin 34, 36, and 48 Added comments to J3: Pin 5 and 54	Jody Van	Gary Bisson
2.0	25 Sep 2024	Ezurio rebranding. Added N8ULP_CAR to Ordering Information .	Sue White Dave Drogowski	Jonathan Kaye
2.1	20 Oct 2024	Update Table 2: Boot mode combinations Update I/O levels for USB0/1_VBUS_DETECT Update Table 5: Typical current consumption	Jody Van	Dave Drogowski
2.2	23 Oct 2024	Update Kit Information	Jody Van	Dave Drogowski

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1 Scope

This document describes key hardware aspects of Ezurio's Nitrogen8ULP SOM system-on-module which is based on the i.MX 8ULP processor family. Data in this document is drawn from several sources and includes information found in the documentation for NXP's i.MX 8ULP.



Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 Introduction

The i.MX 8ULP family of processors features NXP's advanced implementation of the dual Arm® Cortex®-A35 cores alongside an Arm Cortex-M33. This combined architecture enables the device to run a rich operating system (such as Linux) on the Cortex-A35 core and an RTOS (such as FreeRTOS) on the Cortex-M33 core. It also includes a Fusion DSP for low-power audio and a HiFi4 DSP for advanced audio and machine learning applications. The i.MX 8ULP processor provides a 32-bit LPDDR4 (X) memory interface and several other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays. Additionally, there are 2 co-processors connected to the Cortex-M33 core: PowerQuad and Casper, accelerating DSP and cryptography functions, respectively.

The Nitrogen8ULP module offers the latest high-speed interfaces for connectivity and fast data transfer with 2x USB 2.0, 2x SD/SDIO 3.0, 1x 100M Ethernet with EEE, AVB, IEEE 1588, in addition to 1x CAN interface. The memory interfaces supported are 16-bit LPDDR4X and eMMC 5.1.

The module also includes a 2-lane MIPI-CSI camera interface as well as a 4-lane MIPI-DSI output for multimedia applications.

The i.MX 8ULP family implements security via NXP's EdgeLock® secure enclave, a preconfigured, self-managed and autonomous security subsystem. EdgeLock eases the complexity of implementing robust, device-wide security intelligence for IoT applications through autonomous management of critical security functions, such as root of trust, run-time attestation, trust provisioning, secure boot, key management and cryptographic services while also simplifying the path to industry-standard security certifications.

The Nitrogen8ULP SOM has several product SKUs providing different eMMC and LPDDR4 memory configurations, see Ordering Information section.

3 Nitrogen8ULP SOM Features Summary

Key features of Nitrogen8ULP SOM are described in [Table 1](#).

Table 1: Key Features of Nitrogen8ULP SOM

Feature	Description
CPU	Dual Cortex®-A35 processors operation up to 1 GHz 32 KB L1 Instruction & Data Cache 512 KB L2 cache with SCU Cortex®-M33 core platform operating up to 216 MHz 32 KB Instruction & Data Cache 128 KB tightly coupled memory (TCM)
Memory interface	- On module: 32-bit LPDDR4 (size, please refer to Ordering Information) - On module: 8-bit eMMC 5.1 with HS400 speed (size, please refer Ordering Information)
Graphics Engine	Vivante GC Nano Ultra 3.1 3D GPU - Open GL ES 3.1 - Vulkan 1.1 - Open CL 2.x - Open VG1.1 Vivante GC520L for 2D acceleration - Render target compatibility between 3D and 2D GPU (super tile status buffer)
Display Controller	The LCDIF / DCNANO can drive: MIPI DSI: up to 1024x480p60
Image Sensor Interface (ISI)	- Standard pixel formats commonly used in many camera input protocols - Programmable resolutions up to 2K - Image processing for one source of up to 2K horizontal resolution - Image down scaling via decimation and bi-phase filtering - Color space conversion - Interlaced to progressive conversions

Feature	Description
Camera Interface	One 2-lane MIPI CSI-2 camera input: - Compliant with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.1 - Support up to 2 Rx data lanes (plus 1 clock lane)
Audio	Two SAI interface (I2S)
Connectivity	- One USB 2.0 OTG/Type-C interface - One USB 2.0 Host interface - One Ultra Secure Digital Host Controller (uSDHC) interface - One 100M Ethernet controller - One Controller Area Network (FlexCAN) modules - Four Universal Asynchronous Receiver/Transmitter (UART) modules - Four I2C modules - Two SPI modules
Debug Interface	- Trusted Resource Domain Controller (TRDC) - Arm® TrustZone® (TZ) architecture - On-chip RAM (OCRAM) secure region protection using OCRAM controller - EdgeLock® secure enclave - Advanced High Assurance Boot (AHAB)
RF output	RF output with MHF4 connector provides flexible external antenna selection for optimized performance for both Wi-Fi and BT

4 Block Diagram

The figure below shows the block diagram of the Nitrogen8ULP SOM which contains the NXP i.MX 8ULP processor, PMIC (PCA9460A).

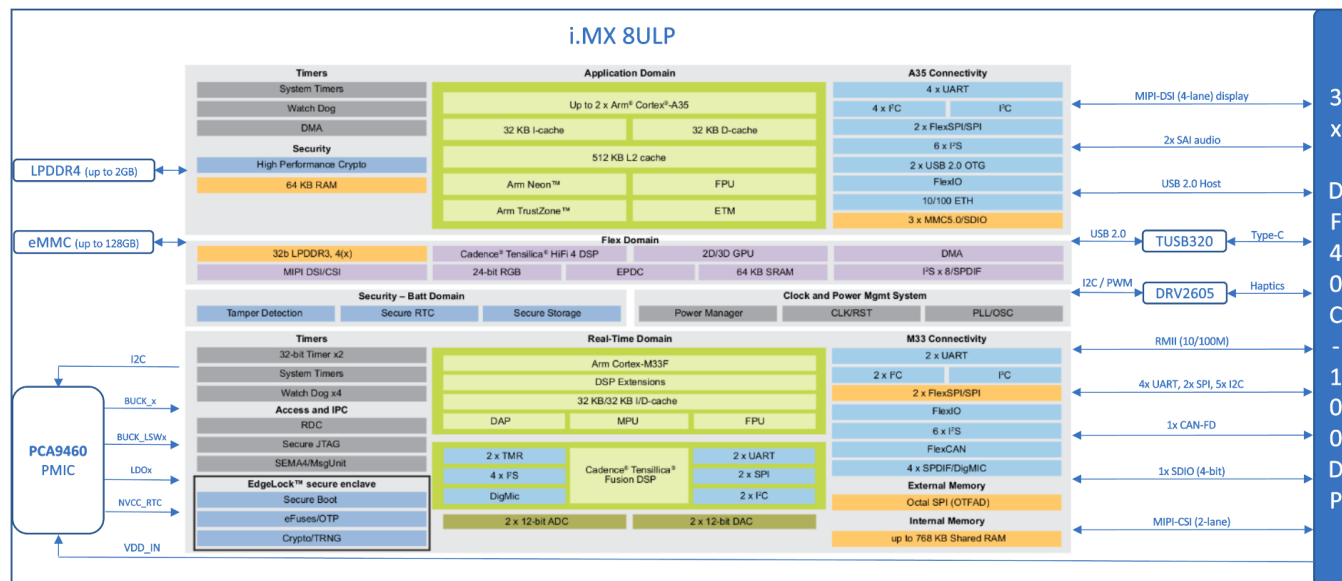


Figure 1:

Nitrogen8ULP SOM block diagram

5 DC Power Tree

The Nitrogen8ULP SOM requires a primary 5V power supply (VSYS) input. This supply is the main power domain to the on-module NXP PCA9460A power management IC (PMIC), which generates all required supply voltages for the module components.

5.1 Power Modes Diagram

NXP PCA9460A has six power states: OFF, SNVS, RUN, PWRDN, PWRUP and FAULT_SD. Below figure shows the state transition diagram showing the conditions to enter and exit each state.

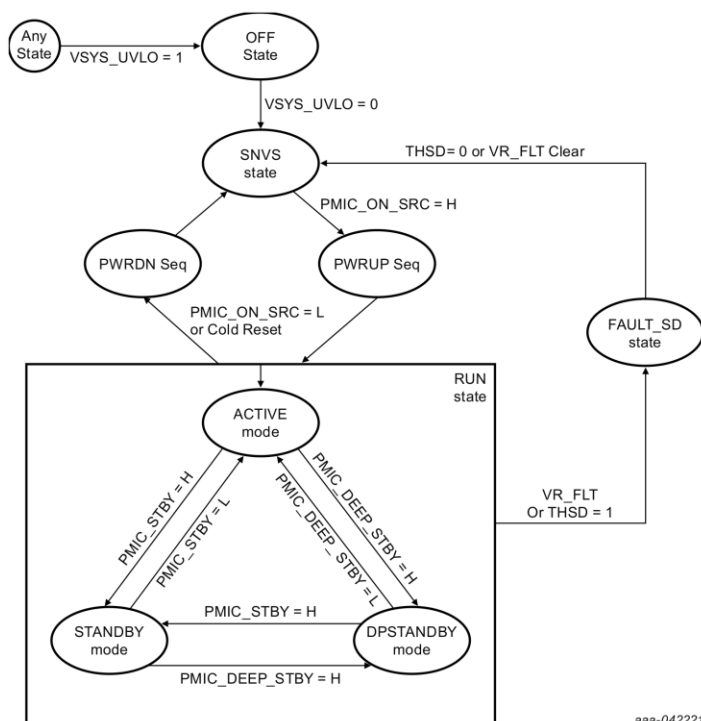


Figure 2: State transition diagram for PMIC

- OFF mode:**
 PCA9460 enters OFF state from any state when VSYS falls below VSYS_UVLO threshold. All regulators including LDO_SNVS are off, and all registers get reset in the state.
- SNVS Mode:**
 PCA9460 enters SNVS (SECURE Non-Volatile Storage MODE) when VSYS exceeds VSYS_UVLO rising threshold. LDO_SNVS is turned on within tSNVS. After turning LDO_SNVS on, it monitors power on source signals to move to PWRUP state.
- PWRUP Mode:**
 After RTC_RESET_B is released in SNVS mode, the PMIC starts power up with a pre-defined sequence with PMIC_ON_REQ asserted high. During PWRUP mode, PMIC_STBY_REQ signal is masked until POR_B is released. The PWRUP mode ends up releasing POR_B and the PMIC is transitioned to RUN mode.
- PWRDN Mode:**
 When PMIC_ON_SRC is asserted low in RUN state, PCA9460 enters PWRDN state, where it starts with pulling down POR_B, and then turning off each power rail in toFF_STEP and is transitioned to SNVS state.
- RUN Mode:**
 PCA9460 enters RUN state after PWRUP state. If PMIC_ON_SRC is asserted low, PCA9460 is transitioned to PWRDN state. When Cold reset event is triggered in RUN state, it is transitioned to PWRDN state. Regulator fault or Thermal shutdown happens in this state, it is transitioned to FAULT_SD state.

 There are three kinds of modes in RUN state, ACTIVE, STANDBY and DPSTANDBY modes, depending on PMIC_STBY_REQ pin and STANDBY_CFG bit in SYS_CFG1 register.

State	Mode	VSYS	PMIC_ON_SRC	STANDBY_CFG bit	PMIC_STBY_REQ
OFF	—	$VSYS < V_{SYS_UVLO}$	X	X	X
SNVS	—	$VSYS > V_{SYS_UVLO}$	Low	X	X
RUN	ACTIVE	$VSYS > V_{SYS_UVLO}$	High	X	Low
RUN	STANDBY	$VSYS > V_{SYS_UVLO}$	High	0b	High
RUN	DPSTANDBY	$VSYS > V_{SYS_UVLO}$	High	1b	High

- **FAULT_SD Mode:**

PCA9460A has two Fault shutdown sources.

- **Thermal shutdown:** Transition to SNVS mode or READY mode after FAULT_SD mode.
When junction temperature reaches 150°C, it enters FAULT_SD state after 20μs, where all regulators are turned off immediately after pulling down POR_B. It stays at FAULT_SD until junction temperature falls below 150°C. When the temperature drops below 150°C, then it transitions to SNVS state.
- **Voltage regulator fault in RUN MODE:** Transition to FAULT_SD state in 100ms after Fault is detected and then transition to SNVS state in 100ms

6 Boot Mode

The Nitrogen8ULP SOM module contains a switch (*SW1*) connected to BOOT_MODE0 thus allowing to switch from internal fuses boot (eMMC by default) to USB serial downloader.

The other boot mode signal (BOOT_MODE1) is not exposed to the carrier but a BOM change can select a custom boot mode (see resistors R20 to R122).

This allows more combinations as shown in [Table 2](#).

Table 2: Boot mode combinations

BOOT_MODE [1:0]	BOOT MODE
x0	Boot from Internal Fuses
x1	USB Serial Downloader

7 Electrical Characteristic and Power Consumption

7.1 Absolute Maximum Ratings

Table 3 summarizes the absolute maximum ratings and Table 4 lists the recommended operating conditions for the Nitrogen8ULP SOM product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 3: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS_5V	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNV5_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
T _{STORAGE}	Storage Temperature Range	-40	+125	°C
ESD	Electrostatic discharge tolerance	- 2000	+2000	V

7.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS_5V	Input voltage for the SOM	3.3	5.0	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNV5_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.

Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please [contact Ezurio](#) if you need information and guidance for thermal management.

7.3 DC Current Consumption

Several power saving modes are available and are listed in Table 5.

Note: These figures are estimates and subject to change.

Table 5: Typical current consumption

Mode	Description	Current (Avg)
Power Saving mode	CPU is on, Stay on Wi-Fi connection only.	104mA
RAM Suspend mode	CPU is on, memory and wireless connection are off.	20mA
Deep Sleep mode	CPU is in deep sleep mode, memory and wireless connection are off	2mA
Stress Test	Wi-Fi + Ethernet 1 & 2 + CPU	170mA

Stress Test	Wi-Fi + Ethernet 1 & 2 + iPerf.	156mA
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8 Module Pin Out and Pinmux Table

Table 6 lists the pin multiplexing (PIN-MUX) of the Nitrogen8ULP SOM.

PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

NXP process has configurable internal Pull-up (PU) and pull-down (PD) resistor whose values are listed below. During a reset condition, the PU and PD state are pre-defined and cannot be changed.

Table 6: Resistor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Pull-up (PU) resistor	VDD=1.65 to 1.95V	12	22	49	k Ω
Pull-down (PD) resistor	Temp=0 to 95°C	13	23	48	k Ω
Pull-up (PU) resistor	VDD=3.0 to 3.6V	18	37	72	k Ω
Pull-down (PD) resistor	Temp=0 to 95°C	24	43	87	k Ω

Pin configuration for the i.MX is achieved using a suite of evaluation and configuration tools that assists users from initial evaluation to production software development. Users can download the tool from the NXP website: https://www.nxp.com/design/designs/config-tools-for-i-mx-applications-processors:CONFIG-TOOLS-IMX?tab=Design_Tools_Tab

Table 7: Pinout table for Nitrogen8ULP SOM board to board connector #1 (J1)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
1	GND	GND	
2	GND	GND	
3	NC	NA	
4	GPIO: PTA21 FLEXIO: FXIO0_D13 SPI: LPSPI0_SOUT UART: LPUART1_RTS_b I2C: LPI2C1_SDA TPM: TPM1_CH1 I2S: I2S1_RXD3 MQS: MQS0_RIGHT JTAG: JTAG0_TDO	1.8V	
5	NC	NA	
6	GPIO: PTA22 FLEXIO: FXIO0_D14 SPI: LPSPI0_SCK UART: LPUART1_TX I3C: I3C0_SCL MQS: MQS0_LEFT JTAG: JTAG0_TDI	1.8V	
7	GND	GND	
8	GND	GND	
9	NC	NA	
10	GPIO: PTA23 FLEXIO: FXIO0_D15 SPI: LPSPI0_PCS0 UART: LPUART1_RX I3C: I3C0_SDA MQS: MQS0_RIGHT JTAG: JTAG0_TCLK	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
11	NC	NA	
12	ADC: ADC1_CH5B GPIO: PTA24 I3C: I3C0_PUR SYSTEM: EXT_AUD_MCLK0 WDOG: WDOG2_RST TIMER: LPTMR1_ALT1 WUU: WUU0_P16	1.8V	
13	GND	GND	
14	GND	GND	
15	NC	NA	
16	NC	NA	
17	NC	NA	
18	NC	NA	
19	GND	GND	
20	GND	GND	
21	NC	NA	
22	CSI_CLK_N	1.8V	
23	NC	NA	
24	CSI_CLK_P	1.8V	
25	GND	GND	
26	GND	GND	
27	NC	NA	
28	CSI_DATA0_P	1.8V	
29	NC	NA	
30	CSI_DATA0_N	1.8V	
31	GND	GND	
32	GND	GND	
33	NC	NA	
34	CSI_DATA1_P	1.8V	
35	NC	NA	
36	CSI_DATA1_N	1.8V	
37	GND	GND	
38	GND	GND	
39	NC	NA	
40	NC	NA	
41	NC	NA	
42	NC	NA	
43	GND	GND	
44	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
45	NC	NA	
46	NC	NA	
47	NC	NA	
48	NC	NA	
49	GND	GND	
50	GND	GND	
51	GPIO: PTF8 FLEXIO: FXIO1_D8 SPI: LPSPI4_SIN UART: LPUART4_CTS_b I2C: LPI2C4_SCL TPM: TPM7_CH3 MQS: MQS1_RIGHT SDHC: SDHC1_D6 ENET: ENET0_MDIO TRACE: TRACE0_D14 EPDC: EPDC0_D15 DCNano: DPI0_D15 SYSTEM: BT1_CFG0 DEBUG: DEBUG_MUX1_29	1.8V	
52	POR_B	1.8V	POR_B of PCA9460A (U6) RESET0_B of i.MX 8ULP (U1)
53	GPIO: PTF9 FLEXIO: FXIO1_D9 SPI: LPSPI4_SOUT UART: LPUART4_RTS_b I2C: LPI2C4_SDA TPM: TPM7_CH4 SYSTEM: EXT_AUD_MCLK2 SDHC: SDHC1_D7 ENET: ENET0_MDC TRACE: TRACE0_D13 EPDC: EPDC0_D14 DCNano: DPI0_D14 SYSTEM: BT1_CFG1 DEBUG: DEBUG_MUX1_30	1.8V	
54	NC	NA	
55	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
56	CMP: CMP1_IN1 GPIO: PTB13 FLEXIO: FXIO0_D29 SPI: LPSPI3_PCS0 UART: LPUART3_RTS_b I3C: I3C1_SCL TPM: TPM3_CH5 I2S: I2S3_RX_BCLK MICFIL: MICFIL0_DATA45 WDOG: WDOG2_RST TIMER: LPTMR1_ALT3 WUU: WUU0_P25	1.8V	
57	NC	NA	
58	CMP: CMP0_IN0 GPIO: PTB14 FLEXIO: FXIO0_D30 UART: LPUART3_TX I3C: I3C1_SDA I2S: I2S3_RX_FS MICFIL: MICFIL0_CLK01 TIMER: LPTMR1_ALT2 WUU: WUU0_P26	1.8V	
59	NC	NA	
60	NC	NA	
61	GND	GND	
62	GPIO: PTE3 FLEXIO: FXIO1_D20 SPDIF: SPDIF_PLOCK UART: LPUART4_RX TPM: TPM8_CH2 I2S: I2S6_MCLK SDHC: SDHC2_CMD SPI: FLEXSPI2_B_DATA5 ENET: ENET0_TXCLK DCNano: DBI0_RWX DCNano: DPI0_D22 WUU: WUU1_P2 DEBUG: DEBUG_MUX1_14	1.8V	
63	GPIO: PTE2 FLEXIO: FXIO1_D21 SPDIF: SPDIF_IN3 UART: LPUART4_TX I2C: LPI2C4_HREQ TPM: TPM8_CH1 SYSTEM: EXT_AUD_MCLK3 SDHC: SDHC2_CLK SPI: FLEXSPI2_B_DATA6 ENET: ENET0_TXER DCNano: DBI0_DCX DCNano: DPI0_D21 DEBUG: DEBUG_MUX1_13	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
64	GPIO: PTC6 SPI: LPSPi2_PCS3 SPI: FLEXSPi1_B_SCLK SPI: FLEXSPi1_A_SCLK I2S: I2S0_TXD1 SPI: FLEXSPi0_A_SCLK	1.8V	
65	ADC: ADC1_CH3B GPIO: PTA15 FLEXIO: FXIO0_D7 SPI: LPSPi1_PCS0 UART: LPUART0_RX I3C: I3C0_SDA TPM: TPM0_CH0 I2S: I2S1_TX_FS SYSTEM: CLKOUT0 CMP: CMP1_OUT WUU: WUU0_P12	1.8V	
66	GPIO: PTF12 FLEXIO: FXIO1_D12 SPI: LPSPi5_PCS1 UART: LPUART5_CTS_b I2C: LPI2C5_SCL TPM: TPM4_CH0 I2S: I2S4_RXD0 SDHC: SDHC2_WP ENET: ENET0_1588_TMR1 TRACE: TRACE0_D10 EPDC: EPDC0_D11 DCNano: DPI0_D11 SYSTEM: BT1_CFG4 DEBUG: DEBUG_MUX1_33	1.8V	
67	GPIO: PTF14 FLEXIO: FXIO1_D14 SPI: LPSPi5_PCS3 UART: LPUART5_TX I2C: LPI2C5_HREQ TPM: TPM4_CH2 I2S: I2S4_MCLK SDHC: SDHC2_VS ENET: ENET0_1588_TMR3 TRACE: TRACE0_D8 EPDC: EPDC0_D9 DCNano: DPI0_D9 SYSTEM: BT1_CFG6	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
68	GPIO: PTE13 FLEXIO: FXIO1_D10 SPI: LPSPi4_SOUT UART: LPUART7_RTS_b I2C: LPI2C7_SDA TPM: TPM4_CH5 I2S: I2S6_TXD1 SDHC: SDHC1_WP ENET: ENET0_1588_CLKIN DCNano: DBI0_D8 EPDC: EPDC0_PWRCTRL2	1.8V	
69	GPIO: PTF13 FLEXIO: FXIO1_D13 SPI: LPSPi5_PCS2 UART: LPUART5_RTS_b I2C: LPI2C5_SDA TPM: TPM4_CH1 I2S: I2S4_RXD1 SDHC: SDHC2_CD ENET: ENET0_1588_TMR2 TRACE: TRACE0_D9 EPDC: EPDC0_D10 DCNano: DPI0_D10 SYSTEM: BT1_CFG5	1.8V	
70	GPIO: PTE12 FLEXIO: FXIO1_D11 SPI: LPSPi4_SIN UART: LPUART7_CTS_b I2C: LPI2C7_SCL TPM: TPM4_CH4 I2S: I2S6_TXD0 SDHC: SDHC2_RESET_b SPI: FLEXSPi2_B_SS1_b ENET: ENET0_1588_TMR0 DCNano: DBI0_D7 EPDC: EPDC0_PWRCTRL1 WUU: WUU1_P5	1.8V	
71	ADC: ADC0_CH1B GPIO: PTB3 FLEXIO: FXIO0_D19 SPI: LPSPi2_SIN UART: LPUART2_RX I2C: LPI2C2_HREQ I3C: I3C1_PUR I2S: I2S2_RXD0 MICFIL: MICFI0_DATA23 TIMER: LPTMR0_ALT2 WUU: WUU0_P20	1.8V	
72	GPIO: PTC7 SPI: FLEXSPi1_B_DATA3 I2S: I2S0_TXD0 SPI: FLEXSPi0_A_DATA3	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
73	ADC: ADC0_CH3A GPIO: PTB6 FLEXIO: FXIO0_D22 SPI: LPSPi2_PCS0 UART: LPUART2_TX I3C: I3C1_SCL I2S: I2S2_TXD0 MICFIL: MICFIL0_CLK01 WUU: WUU0_P23	1.8V	
74	GND	GND	
75	ADC: ADC0_CH2A GPIO: PTB4 FLEXIO: FXIO0_D20 SPI: LPSPi2_SOUT UART: LPUART2_CTS_b I2C: LPI2C2_SCL I2S: I2S2_TX_BCLK MICFIL: MICFIL0_CLK01 WDOG: WDOG0_RST TIMER: LPTMR0_ALT3 WUU: WUU0_P21	1.8V	
76	CMP: CMP1_IN2 GPIO: PTA0 SPI: LPSPi0_PCS1 UART: LPUART0_CTS_b I2C: LPI2C0_SCL TPM: TPM0_CLKIN I2S: I2S0_RX_BCLK SYSTEM: BT0_CFG0 TIMER: LPTMR0_ALT1 WUU: WUU0_P0	1.8V	
77	ADC: ADC0_CH2B GPIO: PTB5 FLEXIO: FXIO0_D21 SPI: LPSPi2_SCK UART: LPUART2_RTS_b I2C: LPI2C2_SDA I2S: I2S2_TX_FS MICFIL: MICFIL0_DATA45 WDOG: WDOG1_RST WUU: WUU0_P22	1.8V	
78	CMP: CMP1_IN5 GPIO: PTA3 UART: LPUART0_RX I2C: LPI2C1_HREQ TPM: TPM0_CH2 I2S: I2S0_RXD1 POWERSYS: PMIC0_MODE2 SYSTEM: BT0_CFG3 CMP: CMP0_OUT WUU: WUU0_P1	1.8V	
79	PMIC_SYS_nRST	1.8V	From PCA9460A (U6)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
80	CMP: CMP1_IN4 GPIO: PTA2 SPI: LPSPI0_PCS3 UART: LPUART0_TX I2C: LPI2C0_HREQ TPM: TPM0_CH1 I2S: I2S0_RXD0 WDOG: WDOG0_RST SYSTEM: BT0_CFG2 TIMER: LPTMR0_ALT2 VBAT: RTC_CLKOUT	1.8V	
81	GPIO: PTD20 FLEXIO: FXIO1_D27 SPI: LPSPI4_SIN SPDIF: SPDIF_OUT1 TPM: TPM8_CLKIN I2S: I2S7_RXD1 SDHC: SDHC1_D1 SPI: FLEXSPI2_A_DATA6 TRACE: TRACE0_D1 EPDC: EPDC0_D15 DCNano: DPI0_D15	1.8V	
82	GPIO: PTC8 SPI: FLEXSPI1_B_DATA2 I2S: I2S0_TX_BCLK SPI: FLEXSPI0_A_DATA2	1.8V	
83	GPIO: PTC4 SPI: LPSPI2_PCS1 SPI: FLEXSPI1_B_DATA4 I2S: I2S0_RXD0 SPI: FLEXSPI0_A_DATA4	1.8V	
84	GPIO: PTE11 FLEXIO: FXIO1_D12 SPDIF: SPDIF_OUT2 UART: LPUART6_RX I3C: I3C2_SDA TPM: TPM4_CH3 I2S: I2S6_TX_FS SPI: FLEXSPI2_B_SCLK_b SPI: FLEXSPI2_B_SS0_b ENET: ENET0_1588_TMR1 DCNano: DBI0_D6 EPDC: EPDC0_PWRCTRL0	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
85	ADC: ADC0_CH1A GPIO: PTB2 FLEXIO: FXIO0_D18 SPI: LPSPi2_PCS3 UART: LPUART2_TX I2C: LPI2C2_HREQ TPM: TPM2_CH1 I2S: I2S2_RX_FS MICFIL: MICFIL0_CLK01 TIMER: LPTMR0_ALT1 WUU: WUU0_P19	1.8V	
86	GPIO: PTD16 FLEXIO: FXIO1_D31 SPI: LPSPi4_PCS1 SPDIF: SPDIF_PLOCK SDHC: SDHC1_CD SDHC: SDHC2_CLK I2S: I2S7_TX_FS SDHC: SDHC1_D5 SPI: FLEXSPi2_A_DATA1 TRACE: TRACE0_D5 EPDC: EPDC0_D11 DCNano: DPI0_D11	1.8V	
87	ADC: ADC0_CH3B GPIO: PTB7 FLEXIO: FXIO0_D23 SPI: LPSPi3_PCS1 UART: LPUART2_RX I3C: I3C1_SDA TPM: TPM3_CLKIN I2S: I2S2_MCLK SYSTEM: EXT_AUD_MCLK1 MICFIL: MICFIL0_DATA67 POWERSYS: PMIC0_MODE2	1.8V	
88	CMP: CMP0_IN2 GPIO: PTA4 SPI: LPSPi0_SIN UART: LPUART1_CTS_b I2C: LPI2C1_SCL TPM: TPM0_CH3 I2S: I2S0_MCLK SYSTEM: EXT_AUD_MCLK0 CAN: CAN0_TX POWERSYS: PMIC0_MODE1 SYSTEM: BT0_CFG4 TIMER: LPTMR0_ALT3 WUU: WUU0_P2	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
89	GPIO: PTF22 FLEXIO: FXIO1_D22 SPDIF: SPDIF_IN1 UART: LPUART7_TX I2C: LPI2C7_HREQ TPM: TPM6_CH0 I2S: I2S5_RXD1 SDHC: SDHC2_D5 ENET: ENET0_COL TRACE: TRACE0_D0 EPDC: EPDC0_D1 DCNano: DPI0_D1 SYSTEM: BT1_CFG14	1.8V	
90	CMP: CMP0_IN3 GPIO: PTA5 SPI: LPSPi0_SOUT UART: LPUART1_RTS_b I2C: LPI2C1_SDA TPM: TPM0_CH4 I2S: I2S0_TX_BCLK CAN: CAN0_RX SYSTEM: BT0_CFG5 TIMER: LPTMR1_ALT1 VBAT: RTC_CLKOUT_b	1.8V	
91	GPIO: PTF23 FLEXIO: FXIO1_D23 SPDIF: SPDIF_OUT1 UART: LPUART7_RX I3C: I3C2_PUR TPM: TPM6_CH1 I2S: I2S5_RXD2 SDHC: SDHC2_D6 ENET: ENET0_TXER TRACE: TRACE0_CLKOUT EPDC: EPDC0_D0 DCNano: DPI0_D0 SYSTEM: BT1_CFG15	1.8V	
92	NC	NA	
93	GPIO: PTD18 FLEXIO: FXIO1_D29 SPI: LPSPi4_PCS3 SPDIF: SPDIF_OUTCLK SYSTEM: EXT_AUD_MCLK3 TPM: TPM8_CH0 I2S: I2S7_MCLK SDHC: SDHC1_D3 SPI: FLEXSPi2_A_DQS TRACE: TRACE0_D3 EPDC: EPDC0_D13 DCNano: DPI0_D13	1.8V	
94	BUCK_1V8	1.8V	
95	BUCK_1V8	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
96	BUCK_1V8	1.8V	
97	TP10	1.8V	
98	TP11	1.8V	
99	GPIO: PTF10 FLEXIO: FXIO1_D10 SPI: LPSPI4_SCK UART: LPUART4_TX I2C: LPI2C4_HREQ TPM: TPM7_CH5 I2S: I2S4_RX_BCLK SDHC: SDHC1_DQS ENET: ENET0_1588_CLKIN TRACE: TRACE0_D12 EPDC: EPDC0_D13 DCNano: DPI0_D13 SYSTEM: BT1_CFG2 DEBUG_MUX: DEBUG_MUX1_31	1.8V	
100	3P0V	3.0V	

Table 8: Pinout table for Nitrogen8ULP SOM board to board connector #2 (J2)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
1	VSYS	5V	
2	GND	GND	
3	VSYS	5V	
4	GND	GND	
5	VSYS	5V	
6	VSYS	5V	
7	VSYS	5V	
8	VSYS	5V	
9	VSYS	5V	
10	VSYS	5V	
11	VSYS	5V	
12	VSYS	5V	
13	VSYS	5V	
14	VSYS	5V	
15	VSYS	5V	
16	NC	NA	
17	VSYS	5V	
18	NC	NA	
19	VSYS	5V	
20	NC	NA	
21	VSYS	5V	
22	NC	NA	
23	VSYS	5V	
24	NC	NA	
25	USB0_VBUS_DETECT	5.6V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
26	GPIO: PTF16 FLEXIO: FXIO1_D16 SPI: LPSPI5_SIN UART: LPUART6_CTS_B I2C: LPI2C6_SCL TPM: TPM4_CH4 I2S: I2S4_TX_FS SDHC: SDHC2_D0 ENET: ENET0_RXD3 TRACE: TRACE0_D6 EPDC: EPDC0_D7 DPIO: DPIO_D7 DBG: LP_HV_DBG_MUX_32	1.8V	Haptics IC (address 0x5a) is connected to I2C6 on the module.
27	NC	NA	
28	GPIO: PTF27 FLEXIO: FXIO1_D27 SPDIF: SPDIF_OUT2 TPM: TPM7_CH0 I2S: I2S5_TX_FS SDHC: SDHC2_WP EPDC: EPDC0_SDCE0 DPIO: DPIO_DE WUU: WUU1_P15	1.8V	
29	NC	NA	
30	ONOFF	1.8V	
31	NC	NA	
32	GPIO: PTC10 SPI: FLEXSPI1_B_DATA0 I2S: I2S0_MCLK SPI: FLEXSPI0_A_DATA0 SYSTEM: EXT_AUD_MCLK1	1.8V	
33	NC	NA	
34	GPIO: PTC11 SPI: FLEXSPI1_B_SS0_b SPI: FLEXSPI1_B_SS1_b TPM: TPM3_CLKIN I2S: I2S1_RXD3 SPI: FLEXSPI0_A_SS0_b SPI: FLEXSPI0_A_SS1_b SYSTEM: CLKOUT0	1.8V	
35	USB_C_CC2	3.3V	From TUSB32 (U28)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
36	GPIO: PTC14 SPI: LPSPI3_SOUT SPI: FLEXSPI1_A_DATA6 TPM: TPM3_CH2 I2S: I2S1_TXD2 SPI: FLEXSPI0_B_DATA6 TRACE: TRACE0_D1	1.8V	
37	USB_C_CC1	3.3V	From TUSB32 (U28)
38	NC	NA	
39	GPIO: PTD14 SPDIF: SPDIF_SRCLK USB: USB0_OC SDHC: SDHC2_D1 I2S: I2S7_RXD0 SDHC: SDHC1_D7 SPI: FLEXSPI2_A_DATA3 TRACE: TRACE0_D7 EPDC: EPDC0_D9 DCNano: DPI0_D9	1.8V	
40	GPIO: PTC15 SPI: LPSPI3_SCK SPI: FLEXSPI1_A_DATA5 TPM: TPM3_CH3 I2S: I2S1_RX_BCLK SPI: FLEXSPI0_B_DATA5 TRACE: TRACE0_D2	1.8V	
41	ADC: ADC1_CH0A GPIO: PTA8 FLEXIO: FXIO0_D0 SPI: LPSPI1_PCS1 UART: LPUART1_CTS_b I2C: LPI2C0_SCL TPM: TPM1_CH0 I2S: I2S0_TXD1 POWERSYS: PMIC0_MODE0 SYSTEM: BT0_CFG8 TIMER: LPTMR1_ALT3 WUU: WUU0_P5	1.8V	
42	GPIO: PTC12 SPI: FLEXSPI1_A_DQS TPM: TPM3_CH0 I2S: I2S1_RXD2 SPI: FLEXSPI0_B_DQS TRACE: TRACE0_CLKOUT	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
43	GPIO: PTD22 FLEXIO: FXIO1_D25 SPI: LPSPI4_SCK SPDIF: SPDIF_OUT2 USB: USB1_OC TPM: TPM8_CH3 I2S: I2S7_TXD2 SDHC: SDHC1_CLK SPI: FLEXSPI2_A_DATA4 TRACE: TRACE0_CLKOUT DCNano: DPI0_D17	1.8V	
44	GPIO: PTD12 USB: USB0_ID SDHC: SDHC2_D3 I2S: I2S7_RX_BCLK SDHC: SDHC1_DQS SPI: FLEXSPI2_A_SS0_b SPI: FLEXSPI2_B_SS1_b EPDC: EPDC0_D7 DCNano: DPI0_D7	1.8V	
45	GPIO: PTD15 SPDIF: SPDIF_IN3 SDHC: SDHC1_VS SDHC: SDHC2_D0 I2S: I2S7_TX_BCLK SDHC: SDHC1_D6 SPI: FLEXSPI2_A_DATA2 TRACE: TRACE0_D6 EPDC: EPDC0_D10 DCNano: DPI0_D10	1.8V	
46	NC	NA	
47	HAPT_OUT_N	3.3V	From DRV2605 (U8)
48	GPIO: PTD23 FLEXIO: FXIO1_D24 SPI: LPSPI4_PCS0 USB: USB1_ID TPM: TPM8_CH4 I2S: I2S7_TXD3 SDHC: SDHC1_CMD SPI: FLEXSPI2_A_SS0_b SPI: FLEXSPI2_A_SCLK_b DCNano: DPI0_D18	1.8V	
49	HAPT_OUT_P	3.3V	From DRV2605 (U8)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
50	GPIO: PTD19 FLEXIO: FXIO1_D28 SPDIF: SPDIF_IN1 TPM: TPM8_CH1 I2S: I2S6_RXD3 SDHC: SDHC1_D2 SPI: FLEXSPI2_A_DATA7 TRACE: TRACE0_D2 EPDC: EPDC0_D14 DCNano: DPI0_D14	1.8V	
51	GPIO: PTD13 SPDIF: SPDIF_IN4 USB: USB0_PWR SDHC: SDHC2_D2 I2S: I2S7_RX_FS SDHC: SDHC1_RESET_b SPI: FLEXSPI2_A_SCLK SYSTEM: CLKOUT2 EPDC: EPDC0_D8 DCNano: DPI0_D8 SYSTEM: CLKOUT1	1.8V	
52	GPIOC: PTC19 SPI: LPSPI3_PCS3 SPI: FLEXSPI1_A_DATA3 I2S: I2S1_TXD1 SPI: FLEXSPI0_B_DATA3 TRACE: TRACE0_D4	1.8V	
53	CMP: CMP0_IN4 GPIO: PTA6 SPI: LPSPI0_SCK UART: LPUART1_TX I3C: I3C0_SCL TPM: TPM0_CH5 I2S: I2S0_TX_FS SYSTEM: BT0_CFG6 VBAT: RTC_CLKOUT WUU: WUU0_P3	1.8V	
54	GPIO: PTC20 SPI: FLEXSPI1_A_DATA2 I2S: I2S1_TXD0 SPI: FLEXSPI0_B_DATA2 TRACE: TRACE0_D5	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
55	GPIO: PTE1 FLEXIO: FXIO1_D22 SPDIF: SPDIF_SRCLK UART: LPUART4_RTS_b I2C: LPI2C4_SDA TPM: TPM8_CH0 I2S: I2S7_RXD3 SDHC: SDHC2_D0 SPI: FLEXSPI2_B_DATA7 ENET: ENET0_COL DCNano: DBI0_CSX DCNano: DPI0_D20 WUU: WUU1_P1 DEBUG: DEBUG_MUX1_12	1.8V	
56	ADC: ADC1_CH4B GPIO: PTA17 FLEXIO: FXIO0_D9 SPI: LPSPI1_SOUT UART: LPUART0_RTS_b I2C: LPI2C0_SDA TPM: TPM0_CH2 I2S: I2S1_TXD1 CAN: CAN0_RX WDOG: WDOG1_RST SYSTEM: BT0_CFG15 VBAT: RTC_CLKOUT WUU: WUU0_P14	1.8V	
57	CMP: CMP0_IN5 GPIO: PTA7 SPI: LPSPI0_PCS0 UART: LPUART1_RX I3C: I3C0_SDA TPM: TPM1_CLKIN I2S: I2S0_TXD0 WDOG: WDOG1_RST SYSTEM: BT0_CFG7 TIMER: LPTMR1_ALT2 WUU: WUU0_P4	1.8V	
58	GPIO: PTC18 SPI: LPSPI3_PCS2 SPI: FLEXSPI1_A_SCLK I2S: I2S1_RXD1 SPI: FLEXSPI0_B_SCLK	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
59	GPIO: PTD21 FLEXIO: FXIO1_D26 SPI: LPSPI4_SOUT SPDIF: SPDIF_IN2 USB: USB1_PWR TPM: TPM8_CH2 I2S: I2S7_TXD1 SDHC: SDHC1_D0 SPI: FLEXSPI2_A_DATA5 TRACE: TRACE0_D0 DCNano: DPI0_D16 WDOG: WDOG5_RST	1.8V	
60	GND	GND	
61	GPIO: PTA19 FLEXIO: FXIO0_D11 SPI: LPSPI1_PCS0 UART: LPUART0_RX I2C: LPI2C1_HREQ TPM: TPM1_CLKIN I2S: I2S1_TXD3 MQS: MQS0_LEFT JTAG: JTAG0_TRST_b TIMER: LPTMR0_ALT2	1.8V	
62	NC	NA	
63	NC	NA	
64	NC	NA	
65	CMP: CMP1_IN3 GPIO: PTA1 SPI: LPSPI0_PCS2 UART: LPUART0_RTS_b I2C: LPI2C0_SDA TPM: TPM0_CH0 I2S: I2S0_RX_FS SYSTEM: BT0_CFG1 EWM: EWM0_OUT_b VBAT: RTC_CLKOUT_b	1.8V	
66	GND	GND	
67	GND	GND	
68	GPIO: PTC16 SPI: LPSPI3_PCS0 SPI: FLEXSPI1_A_DATA4 TPM: TPM3_CH4 I2S: I2S1_RX_FS SPI: FLEXSPI0_B_DATA4 TRACE: TRACE0_D3	1.8V	
69	NC	NA	
70	NC	NA	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
71	CMP : CMP1_IN0 GPIO : PTB12 FLEXIO : FXIO0_D28 SPI : LPSPI3_SCK UART : LPUART3_CTS_b I2C : LPI2C3_SCL TPM : TPM3_CH4 I2S : I2S3_RXD0 MICFIL : MICFIL0_CLK01 WUU : WUU0_P24	1.8V	
72	GPIO : PTC17 SPI : LPSPI3_PCS1 SPI : FLEXSPI1_A_SS0_b SPI : FLEXSPI1_A_SCLK_b TPM : TPM3_CH5 I2S : I2S1_RXD0 SPI : FLEXSPI0_B_SS0_b SPI : FLEXSPI0_B_SCLK_b	1.8V	
73	GND	GND	
74	GPIO : PTE15 FLEXIO : FXIO1_D8 SPI : LPSPI4_PCS0 UART : LPUART7_RX I3C : I3C2_PUR TPM : TPM5_CH0 I2S : I2S6_TXD3 MQS : MQS1_LEFT ENET : ENET0_MDC DCNano : DBI0_D10 EPDC : EPDC0_PWRCOM WUU : WUU1_P6	1.8V	
75	NC	NA	
76	GPIO : PTE16 FLEXIO : FXIO1_D7 SPI : LPSPI5_PCS1 UART : LPUART4_CTS_b I2C : LPI2C4_SCL TPM : TPM5_CH1 MQS : MQS1_LEFT MQS : MQS1_RIGHT USB : USB0_ID ENET : ENET0_TXEN DCNano : DBI0_D11 EPDC : EPDC0_PWRIRQ WDOG : WDOG3_RST	1.8V	
77	NC	NA	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
78	GPIO: PTE17 FLEXIO: FXIO1_D6 SPI: LPSPI5_PCS2 UART: LPUART4_RTS_b I2C: LPI2C4_SDA MQS: MQS1_RIGHT SDHC: SDHC1_VS USB: USB0_PWR ENET: ENET0_RXER DCNano: DBI0_D12 EPDC: EPDC0_PWRSTAT	1.8V	
79	GND	GND	
80	GPIO: PTE18 FLEXIO: FXIO1_D5 SPI: LPSPI5_PCS3 UART: LPUART4_TX I2C: LPI2C4_HREQ I2S: I2S7_TX_BCLK USB: USB0_OC ENET: ENET0_CRS_DV DCNano: DBI0_D13 EPDC: EPDC0_PWRWAKE	1.8V	
81	NC	NA	
82	GPIO: PTE19 FLEXIO: FXIO1_D4 UART: LPUART4_RX I2C: LPI2C5_HREQ I3C: I3C2_PUR I2S: I2S7_TX_FS USB: USB1_PWR ENET: ENET0_REFCLK DCNano: DBI0_D14 EPDC: EPDC0_GDCLK WUU: WUU1_P7	1.8V	
83	NC	NA	
84	GPIO: PTE22 FLEXIO: FXIO1_D1 SPI: LPSPI5_SCK UART: LPUART5_TX I3C: I3C2_SCL TPM: TPM6_CH0 I2S: I2S7_TXD2 SYSTEM: EXT_AUD_MCLK3 ENET: ENET0_TXD1 EPDC: EPDC0_SDOED SYSTEM: CLKOUT2	1.8V	
85	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
86	GPIO: PTE23 FLEXIO: FXIO1_D0 SPI: LPSPI5_PCS0 UART: LPUART5_RX I3C: I3C2_SDA TPM: TPM6_CH1 I2S: I2S7_TXD3 SYSTEM: EXT_AUD_MCLK2 ENET: ENET0_TXD0 EPDC: EPDC0_SDOEZ SYSTEM: CLKOUT1	1.8V	
87	ADC: ADC1_CH1A GPIO: PTA10 FLEXIO: FXIO0_D2 SPI: LPSPI1_PCS3 UART: LPUART1_TX I2C: LPI2C0_HREQ I3C: I3C0_PUR I2S: I2S1_RX_FS SYSTEM: BT0_CFG10 EWM: EWM0_IN WUU: WUU0_P7	1.8V	
88	GPIO: PTE20 FLEXIO: FXIO1_D3 SPI: LPSPI5_SIN UART: LPUART5_CTS_b I2C: LPI2C5_SCL I2S: I2S7_TXD0 USB: USB1_OC ENET: ENET0_RXD1 DCNano: DBI0_D15 EPDC: EPDC0_GDOE	1.8V	
89	ADC: ADC1_CH1B GPIO: PTA11 FLEXIO: FXIO0_D3 UART: LPUART1_RX I2C: LPI2C1_HREQ I3C: I3C0_PUR I2S: I2S1_RXD0 WDOG: WDOG0_RST SYSTEM: BT0_CFG11 TIMER: LPTMR0_ALT1 WUU: WUU0_P8	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
90	GPIO: PTE21 FLEXIO: FXIO1_D2 SPI: LPSPI5_SOUT UART: LPUART5_RTS_b I2C: LPI2C5_SDA TPM: TPM6_CLKIN I2S: I2S7_TXD1 USB: USB1_ID ENET: ENET0_RXD0 EPDC: EPDC0_GDRL WDOG: WDOG4_RST	1.8V	
91	GPIOA: PTA20 FLEXIO: FXIO0_D12 SPI: LPSPI0_SIN UART: LPUART1_CTS_b I2C: LPI2C1_SCL TPM: TPM1_CH0 I2S: I2S1_RXD2 JTAG: JTAG0_TMS/SWD0_DIO TIMER: LPTMR0_ALT3	1.8V	
92	GPIO: PTE10 FLEXIO: FXIO1_D13 SPI: LPSPI4_PCS3 UART: LPUART6_TX I3C: I3C2_SCL TPM: TPM4_CH2 I2S: I2S6_TX_BCLK SDHC: SDHC2_DQS SPI: FLEXSPI2_B_DATA0 ENET: ENET0_1588_TMR2 DCNano: DBI0_D5 EPDC: EPDC0_VCOM0 DEBUG: DEBUG_MUX1_21	NA	
93	ADC: ADC1_CH2A GPIO: PTA12 FLEXIO: FXIO0_D4 SPI: LPSPI1_SIN UART: LPUART0_CTS_b I2C: LPI2C1_SCL I2S: I2S1_RXD1 CAN: CAN0_TX POWERSYS: PMIC0_SDA SYSTEM: BT0_CFG12 EWM: EWM0_IN WUU: WUU0_P9	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
94	GPIO: PTF11 FLEXIO: FXIO1_D11 SPI: LPSPI4_PCS0 UART: LPUART4_RX TPM: TPM4_CLKIN I2S: I2S4_RX_FS SDHC: SDHC1_RESET_b ENET: ENET0_1588_TMR0 TRACE: TRACE0_D11 EPDC: EPDC0_D12 DCNano: DPI0_D12 SYSTEM: BT1_CFG3 DEBUG: DEBUG_MUX1_32	1.8V	
95	ADC: ADC1_CH2B GPIO: PTA13 FLEXIO: FXIO0_D5 SPI: LPSPI1_SOUT UART: LPUART0_RTS_b I2C: LPI2C1_SDA I2S: I2S1_MCLK SYSTEM: EXT_AUD_MCLK0 CAN: CAN0_RX POWERSYS: PMIC0_SCL SYSTEM: BT0_CFG13 CMP: CMP0_OUT WUU: WUU0_P10	1.8V	
96	ADC: ADC1_CH4A GPIO: PTA16 FLEXIO: FXIO0_D8 SPI: LPSPI1_SIN UART: LPUART0_CTS_b I2C: LPI2C0_SCL TPM: TPM0_CH1 I2S: I2S1_TXD0 CAN: CAN0_TX SYSTEM: BT0_CFG14 VBAT: RTC_CLKOUT_b WUU: WUU0_P13	1.8V	
97	ADC: ADC1_CH5A GPIO: PTA18 FLEXIO: FXIO0_D10 SPI: LPSPI1_SCK UART: LPUART0_TX I2C: LPI2C0_HREQ TPM: TPM0_CH3 I2S: I2S1_TXD2 SYSTEM: NMI1_b WUU: WUU0_P15	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
98	GPIO: PTC13 SPI: LPSPI3_SIN SPI: FLEXSPI1_A_DATA7 TPM: TPM3_CH1 I2S: I2S1_TXD3 SPI: FLEXSPI0_B_DATA7 TRACE: TRACE0_D0	1.8V	
99	GPIO: PTA9 FLEXIO: FXIO0_D11 SPI: LPSPI1_PCS0 UART: LPUART0_RX I2C: LPI2C1_HREQ TPM: TPM1_CLKIN I2S: I2S1_TXD3 MQS: MQS0_LEFT JTAG: JTAG0_TRST_b TIMER: LPTMR0_ALT2	1.8V	
100	NC	NA	

Table 9: Pinout table for Nitrogen8ULP SOM board to board connector #3 (J3)

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
1	NC	NA	
2	NC	NA	
3	GPIO: PTE9 FLEXIO: FXIO1_D14 SPI: LPSPI4_PCS2 UART: LPUART6_RTS_b I2C: LPI2C6_SDA TPM: TPM4_CH1 I2S: I2S6_RXD3 SDHC: SDHC2_D7 SPI: FLEXSPI2_B_DATA1 ENET: ENET0_1588_TMR3 DCNano: DBI0_D4 EPDC: EPDC0_VCOM1 DEBUG: DEBUG_MUX1_20	1.8V	
4	NC	NA	
5	GPIO: PTE8 FLEXIO: FXIO1_D15 SPI: LPSPI4_PCS1 UART: LPUART6_CTS_b I2C: LPI2C6_SCL TPM: TPM4_CH0 I2S: I2S6_RXD2 SDHC: SDHC2_D6 SPI: FLEXSPI2_B_DATA2 ENET: ENET0_RXD2 DCNano: DBI0_D3 EPDC: EPDC0_BDR0 DEBUG: DEBUG_MUX1_19	1.8V	
6	NC	NA	
7	GPIO: PTE7 FLEXIO: FXIO1_D16 SPDIF: SPDIF_IN2 UART: LPUART5_RX I2C: LPI2C6_HREQ TPM: TPM4_CLKIN I2S: I2S6_RXD1 SDHC: SDHC2_D5 SPI: FLEXSPI2_B_DATA3 ENET: ENET0_RXD3 DCNano: DBI0_D2 EPDC: EPDC0_BDR1 WUU: WUU1_P4 DEBUG: DEBUG_MUX1_18	1.8V	
8	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
9	GPIO: PTE6 FLEXIO: FXIO1_D17 SPDIF: SPDIF_OUT1 UART: LPUART5_TX I2C: LPI2C5_HREQ TPM: TPM8_CH5 I2S: I2S6_RXD0 SDHC: SDHC2_D4 SPI: FLEXSPI2_B_SCLK ENET: ENET0_RXCLK DCNano: DBI0_D1 WDOG: WDOG5_RST DEBUG: DEBUG_MUX1_17	1.8V	
10	DSI_DATA3_N	1.8V	
11	ADC: ADC0_CH0B GPIO: PTB1 FLEXIO: FXIO0_D17 SPI: LPSPI2_PCS2 UART: LPUART2_RTS_b I2C: LPI2C2_SDA TPM: TPM2_CH0 I2S: I2S2_RX_BCLK MICFIL: MICFIL0_DATA01 WDOG: WDOG2_RST WUU: WUU0_P18	1.8V	
12	DSI_DATA3_P	1.8V	
13	ADC: ADC0_CH0A GPIO: PTB0 FLEXIO: FXIO0_D16 SPI: LPSPI2_PCS1 UART: LPUART2_CTS_b I2C: LPI2C2_SCL TPM: TPM2_CLKIN I2S: I2S2_RXD1 MQS: MQS0_LEFT MICFIL: MICFIL0_CLK01 WUU: WUU0_P17	1.8V	
14	GND	GND	
15	GPIO: PTE4 FLEXIO: FXIO1_D19 SPDIF: SPDIF_OUTCLK UART: LPUART5_CTS_b I2C: LPI2C5_SCL TPM: TPM8_CH3 I2S: I2S6_RX_BCLK SDHC: SDHC2_D3 SPI: FLEXSPI2_B_DATA4 ENET: ENET0_TXD3 DCNano: DBI0_E DCNano: DPI0_D23 WUU: WUU1_P3 DEBUG: DEBUG_MUX1_15	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
16	DSI_DATA2_N	1.8V	
17	GPIO: PTF4 FLEXIO: FXIO1_D4 SPI: LPSPI4_PCS1 UART: LPUART7_CTS_b I2C: LPI2C7_SCL TPM: TPM7_CLKIN I2S: I2S7_RXD2 SDHC: SDHC1_D3 ENET: ENET0_TXEN USB: USB0_OC EPDC: EPDC0_SDCE7 DCNano: DPI0_D19 WUU: WUU1_P10 DEBUG: DEBUG_MUX1_25	1.8V	
18	DSI_DATA2_P	1.8V	
19	GPIO: PTE5 FLEXIO: FXIO1_D18 SPDIF: SPDIF_IN1 UART: LPUART5_RTS_b I2C: LPI2C5_SDA TPM: TPM8_CH4 I2S: I2S6_RX_FS SDHC: SDHC2_D2 SPI: FLEXSPI2_B_SS0_b ENET: ENET0_TXD2 DCNano: DBI0_D0 DEBUG: DEBUG_MUX1_16	1.8V	
20	GND	GND	
21	GPIO: PTE0 FLEXIO: FXIO1_D23 SPDIF: SPDIF_IN4 UART: LPUART4_CTS_b I2C: LPI2C4_SCL TPM: TPM8_CLKIN I2S: I2S7_RXD2 SDHC: SDHC2_D1 SPI: FLEXSPI2_B_DQS ENET: ENET0_CRS DCNano: DBI0_WRX DCNano: DPI0_D19 WUU: WUU1_P0 DEBUG: DEBUG_MUX1_11	1.8V	
22	DSI_CLK_P	1.8V	
23	GND	GND	
24	DSI_CLK_N	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
25	GPIO: PTF5 FLEXIO: FXIO1_D5 SPI: LPSPI4_PCS2 UART: LPUART7_RTS_b I2C: LPI2C7_SDA TPM: TPM7_CH0 I2S: I2S7_RXD3 SDHC: SDHC1_D2 ENET: ENET0_RXER USB: USB1_PWR EPDC: EPDC0_SDCE6 DCNano: DPI0_D18 DEBUG: DEBUG_MUX1_26	1.8V	
26	GND	GND	
27	USB1_VBUS_DETECT	5.6V	
28	DSI_DATA1_N	1.8V	
29	GND	GND	
30	DSI_DATA1_P	1.8V	
31	GPIO: PTF3 FLEXIO: FXIO1_D3 UART: LPUART6_RX I2C: LPI2C7_HREQ I2S: I2S7_RXD1 SDHC: SDHC1_CMD ENET: ENET0_TXD0 USB: USB0_PWR EPDC: EPDC0_SDCE8 DCNano: DPI0_D20 WUU: WUU1_P9 DEBUG: DEBUG_MUX1_24	1.8V	
32	GND	GND	
33	GPIO: PTF2 FLEXIO: FXIO1_D2 UART: LPUART6_TX I2C: LPI2C6_HREQ I2S: I2S7_RXD0 SDHC: SDHC1_CLK ENET: ENET0_TXD1 USB: USB0_ID EPDC: EPDC0_SDCE9 DCNano: DPI0_D21 DEBUG: DEBUG_MUX1_23	1.8V	
34	DSI_DATA0_P	1.8V	
35	GND	GND	
36	DSI_DATA0_N	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
37	GPIO: PTF1 FLEXIO: FXIO1_D1 UART: LPUART6_RTS_b I2C: LPI2C6_SDA I2S: I2S7_RX_FS SDHC: SDHC1_D0 ENET: ENET0_RXD0 EPDC: EPDC0_SDSHR DCNano: DPI0_D22 WDOG: WDOG3_RST DEBUG: DEBUG_MUX1_22	1.8V	
38	GND	GND	
39	GPIO: PTF0 FLEXIO: FXIO1_D0 UART: LPUART6_CTS_b I2C: LPI2C6_SCL I2S: I2S7_RX_BCLK SDHC: SDHC1_D1 ENET: ENET0_RXD1 USB: USB1_ID EPDC: EPDC0_SDOE DCNano: DPI0_D23 WUU: WUU1_P8	1.8V	
40	ADC: ADC0_CH4B GPIO: PTB9 FLEXIO: FXIO0_D25 SPI: LPSPI3_PCS3 UART: LPUART3_RTS_b I2C: LPI2C3_SDA TPM: TPM3_CH1 I2S: I2S3_TX_BCLK MICFIL: MICFIL0_DATA01 POWERSYS: PMIC0_MODE0	1.8V	
41	GND	GND	
42	ADC: ADC0_CH4A GPIO: PTB8 FLEXIO: FXIO0_D24 SPI: LPSPI3_PCS2 UART: LPUART3_CTS_b I2C: LPI2C3_SCL TPM: TPM3_CH0 I2S: I2S2_TXD1 MQS: MQS0_RIGHT MICFIL: MICFIL0_CLK01 POWERSYS: PMIC0_MODE1	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
43	GPIO: PTF7 FLEXIO: FXIO1_D7 UART: LPUART7_RX I3C: I3C2_SDA TPM: TPM7_CH2 MQS: MQS1_LEFT SDHC: SDHC1_D5 ENET: ENET0_REFCLK TRACE: TRACE0_D15 EPDC: EPDC0_SDCE4 DCNano: DPI0_D16 WUU: WUU1_P11 DEBUG: DEBUG_MUX1_28	1.8V	
44	GPIO: PTC9 SPI: FLEXSPI1_B_DATA1 I2S: I2S0_TX_FS SPI: FLEXSPI0_A_DATA1	1.8V	
45	GPIO: PTF6 FLEXIO: FXIO1_D6 SPI: LPSPI4_PCS3 UART: LPUART7_TX I3C: I3C2_SCL TPM: TPM7_CH1 I2S: I2S7_MCLK SDHC: SDHC1_D4 ENET: ENET0_CRS_DV USB: USB1_OC EPDC: EPDC0_SDCE5 DCNano: DPI0_D17 WDOG: WDOG4_RST DEBUG: DEBUG_MUX1_27	1.8V	
46	NC	NA	
47	GND	GND	
48	V_COIN	3.3V	
49	NC	NA	
50	BUCK_1V8	1.8V	
51	NC	NA	
52	BOOT_MODE0	1.8V	
53	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
54	GPIO: PTF17 FLEXIO: FXIO1_D17 SPI: LPSPI5_SOUT UART: LPUART6_RTS_b I2C: LPI2C6_SDA TPM: TPM4_CH5 I2S: I2S4_TXD0 SDHC: SDHC2_CLK ENET: ENET0_RXCLK TRACE: TRACE0_D5 EPDC: EPDC0_D6 DCNano: DPI0_D6 SYSTEM: BT1_CFG9	1.8V	Haptics IC (address 0x5a) is connected to I2C6 on the module.
55	NC	NA	
56	NC	NA	
57	NC	NA	
58	NC	NA	
59	GND	GND	
60	GPIO: PTF20 FLEXIO: FXIO1_D20 UART: LPUART7_CTS_b I2C: LPI2C7_SCL TPM: TPM5_CH1 I2S: I2S5_RX_FS SDHC: SDHC2_D2 ENET: ENET0_TXCLK TRACE: TRACE0_D2 EPDC: EPDC0_D3 DCNano: DPI0_D3 SYSTEM: BT1_CFG12	1.8V	
61	GPIO: PTC5 SPI: LPSPI2_PCS2 SPI: FLEXSPI1_B_SS0_b SPI: FLEXSPI1_B_SCLK_b SPI: FLEXSPI1_A_SS0_b I2S: I2S0_RXD1 SPI: FLEXSPI0_A_SS0_b SPI: FLEXSPI0_A_SCLK_b	1.8V	
62	GPIO: PTF26 FLEXIO: FXIO1_D26 SPDIF: SPDIF_IN3 TPM: TPM7_CLKIN I2S: I2S5_TX_BCLK SDHC: SDHC2_RESET_b EPDC: EPDC0_SDLE DCNano: DPI0_HSYNC WUU: WUU1_P14	1.8V	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
63	GPIO: PTC2 SPI: LPSPI2_SCK SPI: FLEXSPI1_B_DATA6 TPM: TPM2_CH1 I2S: I2S0_RX_BCLK SPI: FLEXSPI0_A_DATA6	1.8V	
64	GPIO: PTF18 FLEXIO: FXIO1_D18 SPI: LPSPI5_SCK UART: LPUART6_TX I2C: LPI2C6_HREQ TPM: TPM5_CLKIN I2S: I2S4_TXD1 SDHC: SDHC2_CMD ENET: ENET0_TXD2 TRACE: TRACE0_D4 EPDC: EPDC0_D5 DCNano: DPI0_D5 SYSTEM: BT1_CFG10	1.8V	
65	GPIO: PTC0 SPI: LPSPI2_SIN SPI: FLEXSPI1_B_DQS TPM: TPM2_CLKIN I2S: I2S3_RXD1 SPI: FLEXSPI0_A_DQS MQS: MQS0_LEFT	1.8V	
66	GPIO: PTF19 FLEXIO: FXIO1_D19 SPI: LPSPI5_PCS0 UART: LPUART6_RX TPM: TPM5_CH0 I2S: I2S5_RX_BCLK SDHC: SDHC2_D3 ENET: ENET0_TXD3 TRACE: TRACE0_D3 EPDC: EPDC0_D4 DCNano: DPI0_D4 SYSTEM: BT1_CFG11	1.8V	
67	GPIO: PTC1 SPI: LPSPI2_SOUT SPI: FLEXSPI1_B_DATA7 TPM: TPM2_CH0 I2S: I2S3_TXD1 SPI: FLEXSPI0_A_DATA7 MQS: MQS0_RIGHT	1.8V	

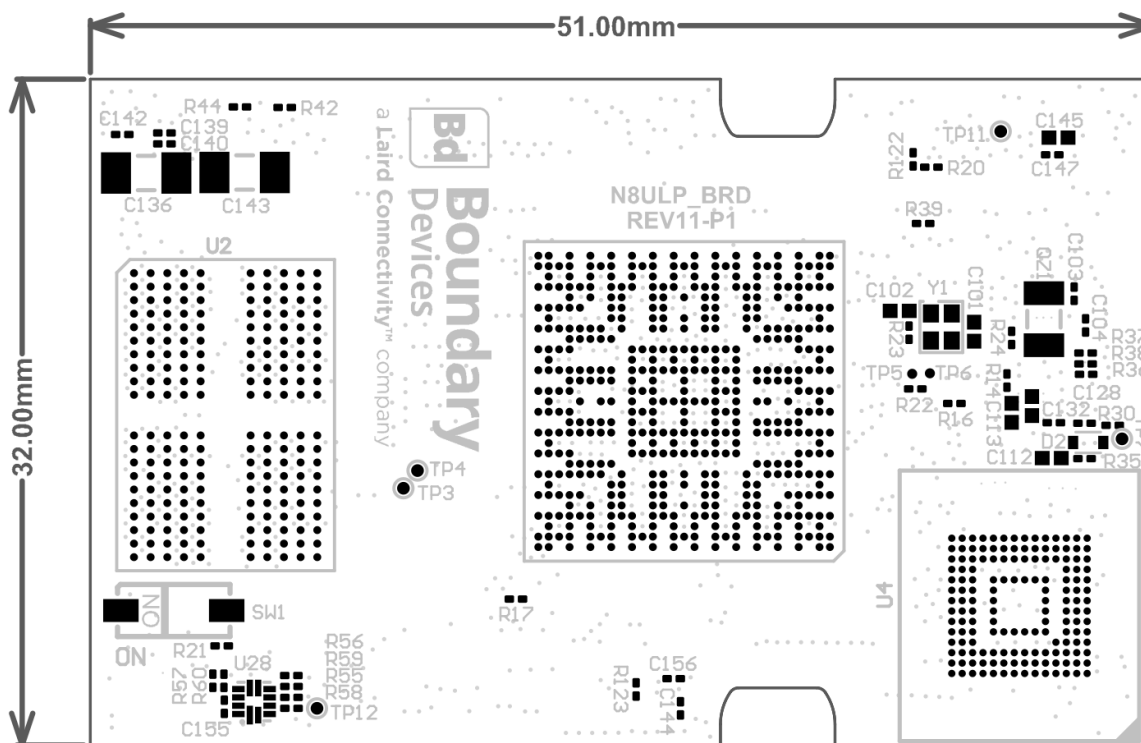
Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
68	GPIO: PTF21 FLEXIO: FXIO1_D21 SPDIF: SPDIF_OUTCLK UART: LPUART7_RTS_b I2C: LPI2C7_SDA TPM: TPM6_CLKIN I2S: I2S5_RXD0 SDHC: SDHC2_D4 ENET: ENET0_CRS TRACE: TRACE0_D1 EPDC: EPDC0_D2 DCNano: DPI0_D2 SYSTEM: BT1_CFG13	1.8V	
69	GPIO: PTC3 SPI: LPSPI2_PCS0 SPI: FLEXSPI1_B_DATA5 I2S: I2S0_RX_FS SPI: FLEXSPI0_A_DATA5	1.8V	
70	GPIO: PTF24 FLEXIO: FXIO1_D24 SPDIF: SPDIF_IN2 I3C: I3C2_SCL I2S: I2S5_RXD3 SDHC: SDHC2_D7 DCNano: DBI0_WRX EPDC: EPDC0_SDCLK DCNano: DPI0_PCLK WUU: WUU1_P12	1.8V	
71	GND	GND	
72	GPIO: PTF25 FLEXIO: FXIO1_D25 SPDIF: SPDIF_OUT2 I3C: I3C2_SDA TPM: TPM7_CH5 I2S: I2S5_MCLK SDHC: SDHC2_DQS SYSTEM: EXT_AUD_MCLK2 EPDC: EPDC0_GDSP DCNano: DPI0_VSYNC WUU: WUU1_P13	1.8V	
73	NC	NA	
74	NC	NA	
75	NC	NA	
76	GPIO: PTF28 FLEXIO: FXIO1_D28 SPDIF: SPDIF_IN4 TPM: TPM7_CH1 I2S: I2S5_TXD0 SDHC: SDHC2_CD EPDC: EPDC0_SDCLK_b	1.8V	
77	GND	GND	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
78	GPIO: PTC21 SPI: FLEXSPI1_A_DATA1 I2S: I2S1_TX_BCLK SPI: FLEXSPI0_B_DATA1 TRACE: TRACE0_D6	1.8V	
79	USB1_DN	3.3V	
80	GPIO: PTC22 SPI: FLEXSPI1_A_DATA0 I2S: I2S1_TX_FS SPI: FLEXSPI0_B_DATA0 TRACE: TRACE0_D7	1.8V	
81	USB1_DP	3.3V	
82	GPIO: PTC23 SPI: FLEXSPI1_A_SS0_b SPI: FLEXSPI1_A_SS1_b I2S: I2S1_MCLK SPI: FLEXSPI0_B_SS0_b SPI: FLEXSPI0_B_SS1_b	1.8V	
83	GND	GND	
84	GND	GND	
85	DAC0_OUT	1.8V	
86	USB0_DP	3.3V	
87	DAC1_OUT	1.8V	
88	USB0_DN	3.3V	
89	GND	GND	
90	GND	GND	
91	NC	NA	
92	NC	NA	
93	RESET1_B	1.8V	
94	NC	NA	
95	GND	GND	
96	GND	GND	
97	GPIO: PTD17 FLEXIO: FXIO1_D30 SPI: LPSPI4_PCS2 SYSTEM: EXT_AUD_MCLK3 SDHC: SDHC1_WP SDHC: SDHC2_CMD I2S: I2S7_TXD0 SDHC: SDHC1_D4 SPI: FLEXSPI2_A_DATA0 TRACE: TRACE0_D4 EPDC: EPDC0_D12 DCNano: DPI0_D12	1.8V	
98	NC	NA	

Pin #	PIN definition / Multiplexing options (red = default muxing)	I/O Level	Comments
99	GPIO: PTE14 FLEXIO: FXIO1_D9 SPI: LPSPI4_SCK UART: LPUART7_TX I2C: LPI2C7_HREQ TPM: TPM5_CLKIN I2S: I2S6_TXD2 SDHC: SDHC1_CD ENET: ENET0_MDIO DCNano: DBI0_D9 EPDC: EPDC0_PWRCTRL3	1.8V	
100	NC	NA	

9 Mechanical and PCB Footprint Specification

Module dimensions of the Nitrogen8ULP SOM are 51x32 mm. Detail drawings are shown below.



10 Storage Instructions

Required Storage Conditions:

- **Prior to Opening the Dry Packing**

The following are required storage conditions prior to opening the dry packing:

- Normal temperature: 5~40°C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

11 Ordering Information

Order Model	Description
N8ULP_SOM_2r16e	SOM: i.MX 8ULP Dual / 2GB / 16GB eMMC
N8ULP_SOM_2r16e_i	SOM: i.MX 8ULP Dual / 2GB / 16GB eMMC / Industrial Temp
N8ULP_CAR	Nitrogen8ULP Carrier Kit – Includes Carrier board, Power Supply, DB9 Serial Cable
N8ULP_CAR_BRD	Carrier board for the N8ULP_SOM

12 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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