FMC/FMC+ Loopback Test Module Datasheet

iWave Global

Document Revision History

Document Number		iG-PRGXD-UM-01-R1.0-REL0.2-Datasheet
Release	**Date**	**Description**
0.1	23th May 2025	Initial Version
0.2	28th May 2025	* Added Section 5. Appendix. * Added Section 5.1 Circuit Reference.

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware Datasheet for the FMC/FMC+ Loopback Test Module and provides detailed information on the overall design & usage of the FMC/FMC+ Loopback Test Module from a Hardware System perspective.

1.2 Overview

The FMC/FMC+ Loopback Test Module can be used for quick validation for TX to RX loopbacks on the multi-gigabit data pairs DP0 to DP9 up to 25Gbps for FMC and Multi-gigabit data pairs DP0 to DP23 up to 28Gbps for FMC+ respectively. Also, Loopback of LA Bank [33:0], HA Bank [23:0] and HB Bank [21:0].

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
C2M	Connector to Module
CH	Channel
DP	Differential Pair
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
Gbps	Gigabits per second
GPIO	General Purpose Input Output
HA	High Pin Count A
HB	High Pin Count B
HPC	High Pin Count
HSPC	High Serial Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LA	Low-Pin Count
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
M2C	Module to Connector
Mbps	Megabits per second
MHz	Mega Hertz
NC	No Connect
PCB	Printed Circuit Board
RX	Receiver
TX	Transmitter
TXVR	Transceiver

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
Analog	Analog Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
I	Input Signal
IO	Bidirectional Input/output Signal
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
NA	Not Applicable
NC	Not Connected
O	Output Signal
OC	Open Collector Signal
OD	Open Drain Signal
PD	Pull Down
Power	Power Pin
PU	Pull Up

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Vita 57.1 FMC Specification
- Vita57.4 FMC+ Specification

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the FMC/FMC+ Loopback Test Module features with high level block diagram and detailed information about each block.

2.1 FMC/FMC+ Loopback Test Module Block Diagram

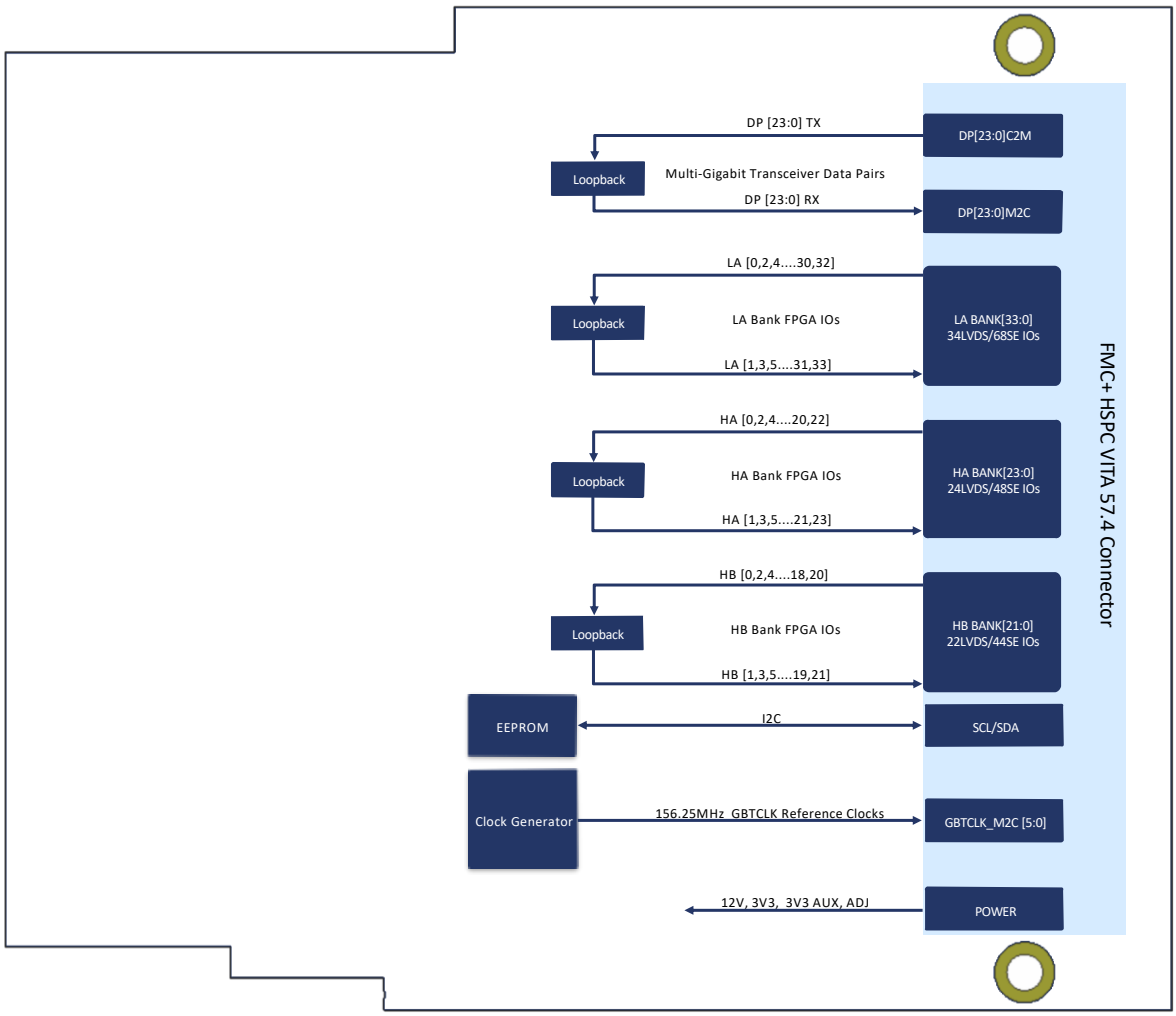


Figure 1: FMC/FMC+ Loopback Test Module Block Diagram

Note: FMC Loopback test module supports DP0 to DP9 Multi-Gigabit Transceiver Data pairs

2.2 FMC/FMC+ Loopback Test Module Features

The FMC/FMC+ Loopback Test Module supports the following features through ANSI/VITA 57.4 FMC+ HSPC or ANSI/VITA 57.1 FMC HPC Connector.

- VITA 57.4 FMC+ HSPC/VITA 57.1 FMC HPC Connector
- TX to RX loopbacks on the multi-gigabit data pairs DP0 to DP23 up to 28Gbps for FMC+
- Loopback of LA Bank [33:0], HA Bank [23:0] and HB Bank [21:0]
- On-board 10-Bit Clock Synthesizer
- EEPROM

Additional Features

- LED Indicators for Powers.

General Specification

- 12V, 3.3V, VADJ from FMC/FMC+ Connector
- Form Factor: 78.5mm X 69mm

2.2.1 VITA 57.4 FMC+ HSPC Connector

The FMC/FMC+ Loopback Test Module supports one 560-pin standard FMC+ VITA 57.4 HSPC connector, with 24 multi-gigabit transceiver data pairs loopback and 80 differential or 160 Single-Ended Signals (LA Bank [33:0], HA Bank [23:0] and HB Bank [21:0]) loopback, making it capable of handling high-speed serialized signals and suitable for on-module interfaces.

Note: The FMC Loopback Test Module supports only 10 multi-gigabit transceivers.

This 560 Pin VITA 57.4 FMC+ HSPC Connector (J1) is physically located at the bottom of the module as shown below.

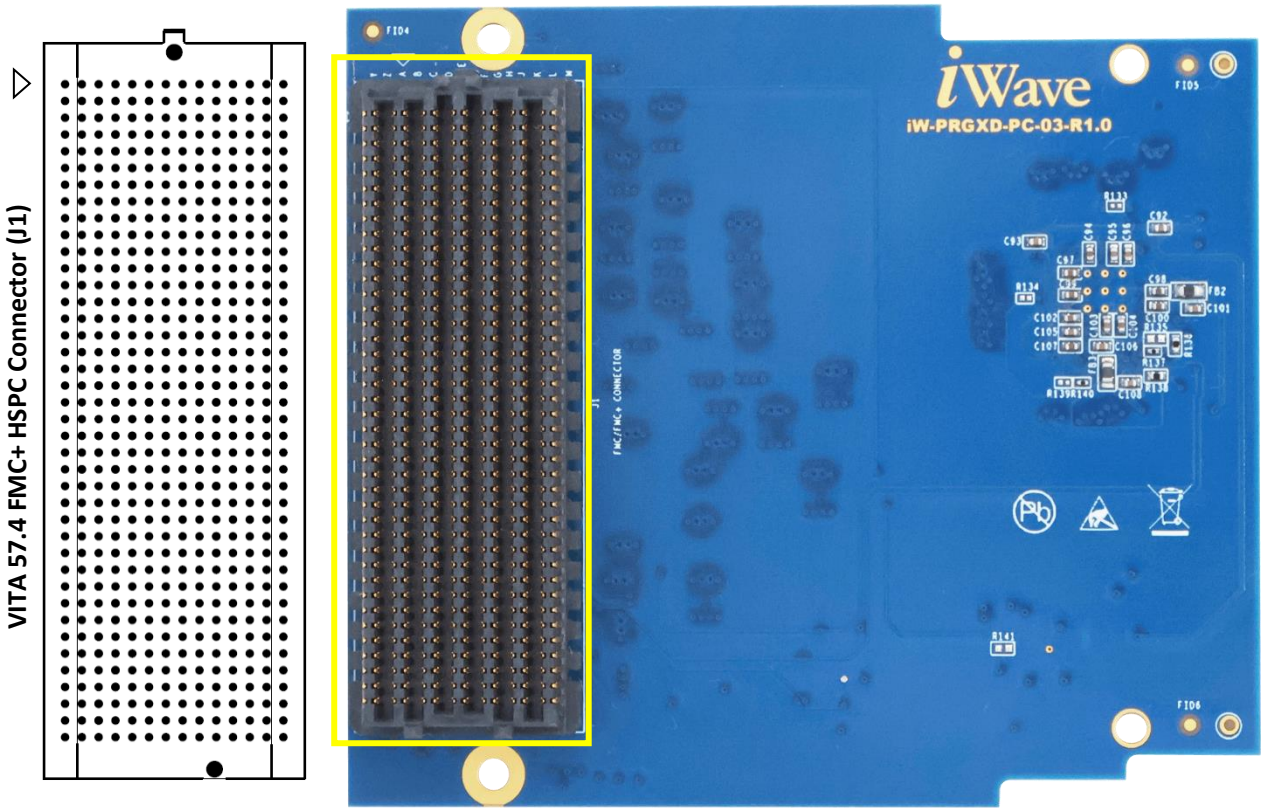


Figure 2: VITA 57.4 FMC+ HSPC Connector

VITA 57.4 FMC+ HSPC connector (J1) pin mapping is shown below.

	Y	Z	A	B	C	D	E	F	G	H	J	K	L	M
1	GND1	HSPC_PRSNT_M2C_L	GND	CLK_DIR	GND	PG_C2M	GND	NC	GND	NC	GND	NC	RES1	GND1
2	DP23_C2M_P	GND1	DP1_M2C_P	GND	DP0_C2M_P	GND	HA01_P_CC	GND	CLK1_M2C_P	PRSNT_M2C_L	CLK3_BIDIR_P	GND	GND1	DP23_M2C_P
3	DP23_C2M_N	GND2	DP1_M2C_N	GND	DP0_C2M_N	GND	HA01_N_CC	GND	CLK1_M2C_N	GND	CLK3_BIDIR_N	GND	GND2	DP23_M2C_N
4	GND2	DP22_C2M_P	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND	HA00_P_CC	GND	CLK0_M2C_P	GND	CLK2_BIDIR_P	GBTCLK4_M2C_P	GND2
5	GND3	DP22_C2M_N	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND	HA00_N_CC	GND	CLK0_M2C_N	GND	CLK2_BIDIR_N	GBTCLK4_M2C_N	GND3
6	DP21_C2M_P	GND3	DP2_M2C_P	GND	DP0_M2C_P	GND	HA05_P	GND	LA00_P_CC	GND	HA03_P	GND	GND3	DP22_M2C_P
7	DP21_C2M_N	GND4	DP2_M2C_N	GND	DP0_M2C_N	GND	HA05_N	HA04_P	LA00_N_CC	LA02_P	HA03_N	HA02_P	GND4	DP22_M2C_N
8	GND4	DP20_C2M_P	GND	DP8_M2C_P	GND	LA01_P_CC	GND	HA04_N	GND	LA02_N	GND	HA02_N	GBTCLK3_M2C_P	GND4
9	GND5	DP20_C2M_N	GND	DP8_M2C_N	GND	LA01_N_CC	HA09_P	GND	LA03_P	GND	HA07_P	GND	GBTCLK3_M2C_N	GND5
10	DP10_M2C_P	GND5	DP3_M2C_P	GND	LA06_P	GND	HA09_N	HA08_P	LA03_N	LA04_P	HA07_N	HA06_P	GND5	DP21_M2C_P
11	DP10_M2C_N	GND6	DP3_M2C_N	GND	LA06_N	LA05_P	GND	HA08_N	GND	LA04_N	GND	HA06_N	GND6	DP21_M2C_N
12	GND6	DP11_M2C_P	GND	DP7_M2C_P	GND	LA05_N	HA13_P	GND	LA08_P	GND	HA11_P	GND	GBTCLK2_M2C_P	GND6
13	GND7	DP11_M2C_N	GND	DP7_M2C_N	GND	GND	HA13_N	HA12_P	LA08_N	LA07_P	HA11_N	HA10_P	GBTCLK2_M2C_N	GND7
14	DP12_M2C_P	GND7	DP4_M2C_P	GND	LA10_P	LA09_P	GND	HA12_N	GND	LA07_N	GND	HA10_N	GND7	DP20_M2C_P
15	DP12_M2C_N	GND8	DP4_M2C_N	GND	LA10_N	LA09_N	HA16_P	GND	LA12_P	GND	HA14_P	GND	GND8	DP20_M2C_N
16	GND8	DP13_M2C_P	GND	DP6_M2C_P	GND	GND	HA16_N	HA15_P	LA12_N	LA11_P	HA14_N	HA17_P_CC	SYNC_C2M_P	GND8
17	GND9	DP13_M2C_N	GND	DP6_M2C_N	GND	LA13_P	GND	HA15_N	GND	LA11_N	GND	HA17_N_CC	SYNC_C2M_N	GND9
18	DP14_M2C_P	GND9	DP5_M2C_P	GND	LA14_P	LA13_N	HA20_P	GND	LA16_P	GND	HA18_P	GND	GND9	DP14_C2M_P
19	DP14_M2C_N	GND10	DP5_M2C_N	GND	LA14_N	GND	HA20_N	HA19_P	LA16_N	LA15_P	HA18_N	HA21_P	GND10	DP14_C2M_N
20	GND10	GBTCLK5_M2C_P	GND	GBTCLK1_M2C_P	GND	LA17_P_CC	GND	HA19_N	GND	LA15_N	GND	HA21_N	REFCLK_C2M_P	GND10
21	GND11	GBTCLK5_M2C_N	GND	GBTCLK1_M2C_N	GND	LA17_N_CC	HB03_P	GND	LA20_P	GND	HA22_P	GND	REFCLK_C2M_N	GND11
22	DP15_M2C_P	GND11	DP1_C2M_P	GND	LA18_P_CC	GND	HB03_N	HB02_P	LA20_N	LA19_P	HA22_N	HA23_P	GND11	DP15_C2M_P
23	DP15_M2C_N	GND12	DP1_C2M_N	GND	LA18_N_CC	LA23_P	GND	HB02_N	GND	LA19_N	GND	HA23_N	GND12	DP15_C2M_N
24	GND12	DP10_C2M_P	GND	DP9_C2M_P	GND	LA23_N	HB05_P	GND	LA22_P	GND	HB01_P	GND	REFCLK_M2C_P	GND12
25	GND13	DP10_C2M_N	GND	DP9_C2M_N	GND	GND	HB05_N	HB04_P	LA22_N	LA21_P	HB01_N	HB00_P_CC	REFCLK_M2C_N	GND13
26	DP11_C2M_P	GND13	DP2_C2M_P	GND	LA27_P	LA26_P	GND	HB04_N	GND	LA21_N	GND	HB00_N_CC	GND13	DP16_C2M_P
27	DP11_C2M_N	GND14	DP2_C2M_N	GND	LA27_N	LA26_N	HB09_P	GND	LA25_P	GND	HB07_P	GND	GND14	DP16_C2M_N
28	GND14	DP12_C2M_P	GND	DP8_C2M_P	GND	GND	HB09_N	HB08_P	LA25_N	LA24_P	HB07_N	HB06_P_CC	SYNC_M2C_P	GND14
29	GND15	DP12_C2M_N	GND	DP8_C2M_N	GND	NC	GND	HB08_N	GND	LA24_N	GND	HB06_N_CC	SYNC_M2C_N	GND15
30	DP13_C2M_P	GND15	DP3_C2M_P	GND	SCL	TDI	HB13_P	GND	LA29_P	GND	HB11_P	GND	GND15	DP17_C2M_P
31	DP13_C2M_N	GND16	DP3_C2M_N	GND	SDA	TDO	HB13_N	HB12_P	LA29_N	LA28_P	HB11_N	HB10_P	GND16	DP17_C2M_N
32	GND16	DP16_M2C_P	GND	DP7_C2M_P	GND	3P3VAUX	GND	HB12_N	GND	LA28_N	GND	HB10_N	RES2	GND16
33	GND17	DP16_M2C_N	GND	DP7_C2M_N	GND	NC	HB19_P	GND	LA31_P	GND	HB15_P	GND	RES3	GND17
34	DP17_M2C_P	GND17	DP4_C2M_P	GND	GA0	NC	HB19_N	HB16_P	LA31_N	LA30_P	HB15_N	HB14_P	GND17	DP18_C2M_P
35	DP17_M2C_N	GND18	DP4_C2M_N	GND	12P0V	GA1	GND	HB16_N	GND	LA30_N	GND	HB14_N	GND18	DP18_C2M_N
36	GND18	DP18_M2C_P	GND	DP6_C2M_P	GND	3P3V	HB21_P	GND	LA33_P	GND	HB18_P	GND	12P0V	GND18
37	GND19	DP18_M2C_N	GND	DP6_C2M_N	12P0V	GND	HB21_N	HB20_P	LA33_N	LA32_P	HB18_N	HB17_P_CC	12P0V	GND19
38	DP19_M2C_P	GND19	DP5_C2M_P	GND	GND	3P3V	GND	HB20_N	GND	LA32_N	GND	HB17_N_CC	GND19	DP19_C2M_P
39	DP19_M2C_N	GND20	DP5_C2M_N	GND	3P3V	GND	VADJ	GND	VADJ	GND	NC	GND	GND20	DP19_C2M_N
40	GND20	3P3V	GND	NC	GND	3P3V	GND	VADJ	GND	VADJ	GND	NC	12P0V	GND20

Note: Pin mapping column Y, Z , L , and M will not be available in FMC Loopback Test Module

Figure 3: VITA 57.4 FMC+ HSPC Connector Pin Out

Table 3: VITA 57.4 FMC+ HSPC Connector Pin Assignment

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	DP1_M2C_P	O, DIFF	Gigabit Transceiver 1 Positive Module to Connector.
A3	DP1_M2C_N	DP1_M2C_N	O, DIFF	Gigabit Transceiver 1 Negative Module to Connector.
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	DP2_M2C_P	O, DIFF	Gigabit Transceiver 2 Positive Module to Connector.
A7	DP2_M2C_N	DP2_M2C_N	O, DIFF	Gigabit Transceiver 2 Negative Module to Connector.
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	DP3_M2C_P	O, DIFF	Gigabit Transceiver 3 Positive Module to Connector.
A11	DP3_M2C_N	DP3_M2C_N	O, DIFF	Gigabit Transceiver 3 Negative Module to Connector.
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	DP4_M2C_P	O, DIFF	Gigabit Transceiver 4 Positive Module to Connector.
A15	DP4_M2C_N	DP4_M2C_N	O, DIFF	Gigabit Transceiver 4 Negative Module to Connector.
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	DP5_M2C_P	O, DIFF	Gigabit Transceiver 5 Positive Module to Connector.
A19	DP5_M2C_N	DP5_M2C_N	O, DIFF	Gigabit Transceiver 5 Negative Module to Connector.
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	DP1_C2M_P	I, DIFF	Gigabit Transceiver 1 Positive Connector to Module.
A23	DP1_C2M_N	DP1_C2M_N	I, DIFF	Gigabit Transceiver 1 Negative Connector to Module.
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	DP2_C2M_P	I, DIFF	Gigabit Transceiver 2 Positive Connector to Module.
A27	DP2_C2M_N	DP2_C2M_N	I, DIFF	Gigabit Transceiver 2 Negative Connector to Module.
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	DP3_C2M_P	I, DIFF	Gigabit Transceiver 3 Positive Connector to Module.
A31	DP3_C2M_N	DP3_C2M_N	I, DIFF	Gigabit Transceiver 3 Negative Connector to Module.
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
A34	DP4_C2M_P	DP4_C2M_P	I, DIFF	Gigabit Transceiver 4 Positive Connector to Module.
A35	DP4_C2M_N	DP4_C2M_N	I, DIFF	Gigabit Transceiver 4 Negative Connector to Module.
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	DP5_C2M_P	I, DIFF	Gigabit Transceiver 5 Positive Connector to Module.
A39	DP5_C2M_N	DP5_C2M_N	I, DIFF	Gigabit Transceiver 5 Negative Connector to Module.
A40	GND	GND	Power	Ground.
B1	CLK_DIR	CLK_DIR	IO, 3.3V CMOS 10K PD	Clock Direction.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	DP9_M2C_P	O, DIFF	Gigabit Transceiver 9 Positive Connector to Module.
B5	DP9_M2C_N	DP9_M2C_N	O, DIFF	Gigabit Transceiver 9 Negative Connector to Module.
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	DP8_M2C_P	O, DIFF	Gigabit Transceiver 8 Positive Module to Connector.
B9	DP8_M2C_N	DP8_M2C_N	O, DIFF	Gigabit Transceiver 8 Negative Module to Connector.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	DP7_M2C_P	O, DIFF	Gigabit Transceiver 7 Positive Module to Connector.
B13	DP7_M2C_N	DP7_M2C_N	O, DIFF	Gigabit Transceiver 7 Negative Module to Connector.
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	DP6_M2C_P	O, DIFF	Gigabit Transceiver 6 Positive Module to Connector.
B17	DP6_M2C_N	DP6_M2C_N	O, DIFF	Gigabit Transceiver 6 Negative Module to Connector.
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	GBTCLK1_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 1 Positive.
B21	GBTCLK1_M2C_N	GBTCLK1_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 1 Negative.
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	DP9_C2M_P	I, DIFF	Gigabit Transceiver 9 Positive Connector to Module.
B25	DP9_C2M_N	DP9_C2M_N	I, DIFF	Gigabit Transceiver 9 Negative Connector to Module.
B26	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	DP8_C2M_P	I, DIFF	Gigabit Transceiver 8 Positive Connector to Module.
B29	DP8_C2M_N	DP8_C2M_N	I, DIFF	Gigabit Transceiver 8 Negative Connector to Module.
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	DP7_C2M_P	I, DIFF	Gigabit Transceiver 7 Positive Connector to Module.
B33	DP7_C2M_N	DP7_C2M_N	I, DIFF	Gigabit Transceiver 7 Negative Connector to Module.
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	DP6_C2M_P	I, DIFF	Gigabit Transceiver 6 Positive Connector to Module.
B37	DP6_C2M_N	DP6_C2M_N	I, DIFF	Gigabit Transceiver 6 Negative Connector to Module.
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	RES0	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	DP0_C2M_P	I, DIFF	Gigabit Transceiver 0 Positive Connector to Module.
C3	DP0_C2M_N	DP0_C2M_N	I, DIFF	Gigabit Transceiver 0 Negative Connector to Module.
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DP0_M2C_P	DP0_M2C_P	O, DIFF	Gigabit Transceiver 0 Positive Module to Connector.
C7	DP0_M2C_N	DP0_M2C_N	O, DIFF	Gigabit Transceiver 0 Negative Module to Connector.
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	LA06_P	IO, LVCMOS	LA Bank IO6 Positive.
C11	LA06_N	LA06_N	IO, LVCMOS	LA Bank IO6 Negative.
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	LA10_P	IO, LVCMOS	LA Bank IO10 Positive.
C15	LA10_N	LA10_N	IO, LVCMOS	LA Bank IO10 Negative.
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	LA14_P	IO, LVCMOS	LA Bank IO14 Positive.
C19	LA14_N	LA14_N	IO, LVCMOS	LA Bank IO14 Negative.
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	LA18_P_CC	IO, LVCMOS	LA Bank IO18 Positive.
C23	LA18_N_CC	LA18_N_CC	IO, LVCMOS	LA Bank IO18 Negative.
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	LA27_P	IO, LVCMOS	LA Bank IO27 Positive.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
C27	LA27_N	LA27_N	IO, LVCMOS	LA Bank IO27 Negative.
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	FMC+_SCL	I, 3.3V CMOS	I2C Serial Clock. Connected to EEPROM
C31	SDA	FMC+_SDA	IO, 3.3V CMOS	I2C Serial Data. Connected to EEPROM
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0_FMC+	I, 3.3V CMOS	Geographical address 0. EEPROM slave address can be configured using this pin.
C35	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.
D1	PG_C2M	FMC+_PG_C2M	I, 3.3V CMOS	Power good from carrier to module.
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	GBTCLK0_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 0 Positive.
D5	GBTCLK0_M2C_N	GBTCLK0_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 0 Negative.
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	LA01_P_CC	IO, LVCMOS	LA Bank IO01 Positive.
D9	LA01_N_CC	LA01_N_CC	IO, LVCMOS	LA Bank IO01 Negative.
D10	GND	GND	Power	Ground.
D11	LA05_P	LA05_P	IO, LVCMOS	LA Bank IO05 Positive.
D12	LA05_N	LA05_N	IO, LVCMOS	LA Bank IO05 Negative.
D13	GND	GND	Power	Ground.
D14	LA09_P	LA09_P	IO, LVCMOS	LA Bank IO09 Positive.
D15	LA09_N	LA09_N	IO, LVCMOS	LA Bank IO09 Negative.
D16	GND	GND	Power	Ground.
D17	LA13_P	LA13_P	IO, LVCMOS	LA Bank IO13 Positive.
D18	LA13_N	LA13_N	IO, LVCMOS	LA Bank IO13 Negative.
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	LA17_P_CC	IO, LVCMOS	LA Bank IO17 Positive.
D21	LA17_N_CC	LA17_N_CC	IO, LVCMOS	LA Bank IO17 Negative.
D22	GND	GND	Power	Ground.
D23	LA23_P	LA23_P	IO, LVCMOS	LA Bank IO23 Positive.
D24	LA23_N	LA23_N	IO, LVCMOS	LA Bank IO23 Negative.
D25	GND	GND	Power	Ground.
D26	LA26_P	LA26_P	IO, LVCMOS	LA Bank IO26 Positive.
D27	LA26_N	LA26_N	IO, LVCMOS	LA Bank IO26 Negative.
D28	GND	GND	Power	Ground.
D29	TCK	TCK	NA	NC.
D30	TDI	TDI	I, LVCMOS	Connected to TDO.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
D31	TDO	TDO	O, LVCMOS	Connected to TDI.
D32	3P3VAUX	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D33	TMS	TMS	NA	NC.
D34	TRST_L	TRST_L	NA	NC.
D35	GA1	GA1_FMC+	I, 3.3V CMOS	Geographical address1. EEPROM slave address can be configured using this pin.
D36	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	HA01_P_CC	IO, LVCMOS	HA Bank IO01 Positive.
E3	HA01_N_CC	HA01_N_CC	IO, LVCMOS	HA Bank IO01 Negative.
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.
E6	HA05_P	HA05_P	IO, LVCMOS	HA Bank IO05 Positive.
E7	HA05_N	HA05_N	IO, LVCMOS	HA Bank IO05 Negative.
E8	GND	GND	Power	Ground.
E9	HA09_P	HA09_P	IO, LVCMOS	HA Bank IO09 Positive.
E10	HA09_N	HA09_N	IO, LVCMOS	HA Bank IO09 Negative.
E11	GND	GND	Power	Ground.
E12	HA13_P	HA13_P	IO, LVCMOS	HA Bank IO13 Positive.
E13	HA13_N	HA13_N	IO, LVCMOS	HA Bank IO13 Negative.
E14	GND	GND	Power	Ground.
E15	HA16_P	HA16_P	IO, LVCMOS	HA Bank IO16 Positive.
E16	HA16_N	HA16_N	IO, LVCMOS	HA Bank IO16 Negative.
E17	GND	GND	Power	Ground.
E18	HA20_P	HA20_P	IO, LVCMOS	HA Bank IO20 Positive.
E19	HA20_N	HA20_N	IO, LVCMOS	HA Bank IO20 Negative.
E20	GND	GND	Power	Ground.
E21	HB03_P	HB03_P	IO, LVCMOS	HB Bank IO03 Positive.
E22	HB03_N	HB03_N	IO, LVCMOS	HB Bank IO03 Negative.
E23	GND	GND	Power	Ground.
E24	HB05_P	HB05_P	IO, LVCMOS	HB Bank IO05 Positive.
E25	HB05_N	HB05_N	IO, LVCMOS	HB Bank IO05 Negative.
E26	GND	GND	Power	Ground.
E27	HB09_P	HB09_P	IO, LVCMOS	HB Bank IO09 Positive.
E28	HB09_N	HB09_N	IO, LVCMOS	HB Bank IO09 Negative.
E29	GND	GND	Power	Ground.
E30	HB13_P	HB13_P	IO, LVCMOS	HB Bank IO05 Positive.
E31	HB13_N	HB13_N	IO, LVCMOS	HB Bank IO05 Negative.
E32	GND	GND	Power	Ground.
E33	HB19_P	HB19_P	IO, LVCMOS	HB Bank IO19 Positive.
E34	HB19_N	HB19_N	IO, LVCMOS	HB Bank IO19 Negative.
E35	GND	GND	Power	Ground.
E36	HB21_P	HB21_P	IO, LVCMOS	HB Bank IO21 Positive.
E37	HB21_N	HB21_N	IO, LVCMOS	HB Bank IO21 Negative.
E38	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
E39	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Supply Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	NA	NA	NC.
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	HA00_P_CC	IO, LVCMOS	HA Bank IO00 Positive.
F5	HA00_N_CC	HA00_N_CC	IO, LVCMOS	HA Bank IO00 Negative.
F6	GND	GND	Power	Ground.
F7	HA04_P	HA04_P	IO, LVCMOS	HA Bank IO04 Positive.
F8	HA04_N	HA04_N	IO, LVCMOS	HA Bank IO04 Negative.
F9	GND	GND	Power	Ground.
F10	HA08_P	HA08_P	IO, LVCMOS	HA Bank IO08 Positive.
F11	HA08_N	HA08_N	IO, LVCMOS	HA Bank IO08 Negative.
F12	GND	GND	Power	Ground.
F13	HA12_P	HA12_P	IO, LVCMOS	HA Bank IO12 Positive.
F14	HA12_N	HA12_N	IO, LVCMOS	HA Bank IO12 Negative.
F15	GND	GND	Power	Ground.
F16	HA15_P	HA15_P	IO, LVCMOS	HA Bank IO15 Positive.
F17	HA15_N	HA15_N	IO, LVCMOS	HA Bank IO15 Negative.
F18	GND	GND	Power	Ground.
F19	HA19_P	HA19_P	IO, LVCMOS	HA Bank IO19 Positive.
F20	HA19_N	HA19_N	IO, LVCMOS	HA Bank IO19 Negative.
F21	GND	GND	Power	Ground.
F22	HB02_P	HB02_P	IO, LVCMOS	HB Bank IO02 Positive.
F23	HB02_N	HB02_N	IO, LVCMOS	HB Bank IO02 Negative.
F24	GND	GND	Power	Ground.
F25	HB04_P	HB04_P	IO, LVCMOS	HB Bank IO04 Positive.
F26	HB04_N	HB04_N	IO, LVCMOS	HB Bank IO04 Negative.
F27	GND	GND	Power	Ground.
F28	HB08_P	HB08_P	IO, LVCMOS	HB Bank IO08 Positive.
F29	HB08_N	HB08_N	IO, LVCMOS	HB Bank IO08 Negative.
F30	GND	GND	Power	Ground.
F31	HB12_P	HB12_P	IO, LVCMOS	HB Bank IO12 Positive.
F32	HB12_N	HB12_N	IO, LVCMOS	HB Bank IO12 Negative.
F33	GND	GND	Power	Ground.
F34	HB16_P	HB16_P	IO, LVCMOS	HB Bank IO16 Positive.
F35	HB16_N	HB16_N	IO, LVCMOS	HB Bank IO16 Negative.
F36	GND	GND	Power	Ground.
F37	HB20_P	HB20_P	IO, LVCMOS	HB Bank IO20 Positive.
F38	HB20_N	HB20_N	IO, LVCMOS	HB Bank IO20 Negative.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Supply Voltage.
G1	GND	GND	Power	Ground.
G2	CLK1_M2C_P	CLK1_M2C_P	O, LVDS	Optional Clock from 10-Bit clock synthesizer OUT 8.
G3	CLK1_M2C_N	CLK1_M2C_N	O, LVDS	Optional Clock from 10-Bit clock synthesizer OUT 8b.
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	LA00_P_CC	IO, LVCMOS	LA Bank IO00 Positive.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
G7	LA00_N_CC	LA00_N_CC	IO, LVCMOS	LA Bank IO00 Negative.
G8	GND	GND	Power	Ground.
G9	LA03_P	LA03_P	IO, LVCMOS	LA Bank IO03 Positive.
G10	LA03_N	LA03_N	IO, LVCMOS	LA Bank IO03 Negative.
G11	GND	GND	Power	Ground.
G12	LA08_P	LA08_P	IO, LVCMOS	LA Bank IO08 Positive.
G13	LA08_N	LA08_N	IO, LVCMOS	LA Bank IO08 Negative.
G14	GND	GND	Power	Ground.
G15	LA12_P	LA12_P	IO, LVCMOS	LA Bank IO12 Positive.
G16	LA12_N	LA12_N	IO, LVCMOS	LA Bank IO12 Negative.
G17	GND	GND	Power	Ground.
G18	LA16_P	LA16_P	IO, LVCMOS	LA Bank IO16 Positive.
G19	LA16_N	LA16_N	IO, LVCMOS	LA Bank IO16 Negative.
G20	GND	GND	Power	Ground.
G21	LA20_P	LA20_P	IO, LVCMOS	LA Bank IO20 Positive.
G22	LA20_N	LA20_N	IO, LVCMOS	LA Bank IO20 Negative.
G23	GND	GND	Power	Ground.
G24	LA22_P	LA22_P	IO, LVCMOS	LA Bank IO22 Positive.
G25	LA22_N	LA22_N	IO, LVCMOS	LA Bank IO22 Negative.
G26	GND	GND	Power	Ground.
G27	LA25_P	LA25_P	IO, LVCMOS	LA Bank IO25 Positive.
G28	LA25_N	LA25_N	IO, LVCMOS	LA Bank IO25 Negative.
G29	GND	GND	Power	Ground.
G30	LA29_P	LA29_P	IO, LVCMOS	LA Bank IO29 Positive.
G31	LA29_N	LA29_N	IO, LVCMOS	LA Bank IO29 Negative.
G32	GND	GND	Power	Ground.
G33	LA31_P	LA31_P	IO, LVCMOS	LA Bank IO31 Positive.
G34	LA31_N	LA31_N	IO, LVCMOS	LA Bank IO31 Negative.
G35	GND	GND	Power	Ground.
G36	LA33_P	LA33_P	IO, LVCMOS	LA Bank IO33 Positive.
G37	LA33_N	LA33_N	IO, LVCMOS	LA Bank IO33 Negative.
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Supply Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC
H2	PRSNT_M2C_L	PRSNT_M2C_L	O, 0E PD	Module Present Signal.
H3	GND	GND	Power	Ground.
H4	CLK0_M2C_P	CLK0_M2C_P	O, LVDS	Optional Clock from 10-Bit clock synthesizer OUT 7.
H5	CLK0_M2C_N	CLK0_M2C_N	O, LVDS	Optional Clock from 10-Bit clock synthesizer OUT 7b.
H6	GND	GND	Power	Ground.
H7	LA02_P	LA02_P	IO, LVCMOS	LA Bank IO02 Positive.
H8	LA02_N	LA02_N	IO, LVCMOS	LA Bank IO02 Negative.
H9	GND	GND	Power	Ground.
H10	LA04_P	LA04_P	IO, LVCMOS	LA Bank IO04 Positive.
H11	LA04_N	LA04_N	IO, LVCMOS	LA Bank IO04 Negative.
H12	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
H13	LA07_P	LA07_P	IO, LVCMOS	LA Bank IO07 Positive.
H14	LA07_N	LA07_N	IO, LVCMOS	LA Bank IO07 Negative.
H15	GND	GND	Power	Ground.
H16	LA11_P	LA11_P	IO, LVCMOS	LA Bank IO11 Positive.
H17	LA11_N	LA11_N	IO, LVCMOS	LA Bank IO11 Negative.
H18	GND	GND	Power	Ground.
H19	LA15_P	LA15_P	IO, LVCMOS	LA Bank IO15 Positive.
H20	LA15_N	LA15_N	IO, LVCMOS	LA Bank IO15 Negative.
H21	GND	GND	Power	Ground.
H22	LA19_P	LA19_P	IO, LVCMOS	LA Bank IO19 Positive.
H23	LA19_N	LA19_N	IO, LVCMOS	LA Bank IO19 Negative.
H24	GND	GND	Power	Ground.
H25	LA21_P	LA21_P	IO, LVCMOS	LA Bank IO21 Positive.
H26	LA21_N	LA21_N	IO, LVCMOS	LA Bank IO21 Negative.
H27	GND	GND	Power	Ground.
H28	LA24_P	LA24_P	IO, LVCMOS	LA Bank IO24 Positive.
H29	LA24_N	LA24_N	IO, LVCMOS	LA Bank IO24 Negative.
H30	GND	GND	Power	Ground.
H31	LA28_P	LA28_P	IO, LVCMOS	LA Bank IO28 Positive.
H32	LA28_N	LA28_N	IO, LVCMOS	LA Bank IO28 Negative.
H33	GND	GND	Power	Ground.
H34	LA30_P	LA30_P	IO, LVCMOS	LA Bank IO30 Positive.
H35	LA30_N	LA30_N	IO, LVCMOS	LA Bank IO30 Negative.
H36	GND	GND	Power	Ground.
H37	LA32_P	LA32_P	IO, LVCMOS	LA Bank IO32 Positive.
H38	LA32_N	LA32_N	IO, LVCMOS	LA Bank IO32 Negative.
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_FMC+_ADJ	I, VADJ Power	Supply Voltage.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	CLK3_BIDIR_P	IO, LVDS	Optional Clock Output from 10-bit clock synthesizer OUT9.
J3	CLK3_BIDIR_N	CLK3_BIDIR_N	IO, LVDS	Optional Clock Output from 10-bit clock synthesizer OUT9b.
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	HA03_P	IO, LVCMOS	HA Bank IO03 Positive.
J7	HA03_N	HA03_N	IO, LVCMOS	HA Bank IO03 Negative.
J8	GND	GND	Power	Ground.
J9	HA07_P	HA07_P	IO, LVCMOS	HA Bank IO07 Positive.
J10	HA07_N	HA07_N	IO, LVCMOS	HA Bank IO07 Negative.
J11	GND	GND	Power	Ground.
J12	HA11_P	HA11_P	IO, LVCMOS	HA Bank IO11 Positive.
J13	HA11_N	HA11_N	IO, LVCMOS	HA Bank IO11 Negative.
J14	GND	GND	Power	Ground.
J15	HA14_P	HA14_P	IO, LVCMOS	HA Bank IO14 Positive.
J16	HA14_N	HA14_N	IO, LVCMOS	HA Bank IO14 Negative.
J17	GND	GND	Power	Ground.
J18	HA18_P	HA18_P	IO, LVCMOS	HA Bank IO18 Positive.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
J19	HA18_N	HA18_N	IO, LVCMOS	HA Bank IO18 Negative.
J20	GND	GND	Power	Ground.
J21	HA22_P	HA22_P	IO, LVCMOS	HA Bank IO22 Positive.
J22	HA22_N	HA22_N	IO, LVCMOS	HA Bank IO22 Negative.
J23	GND	GND	Power	Ground.
J24	HB01_P	HB01_P	IO, LVCMOS	HB Bank IO01 Positive.
J25	HB01_N	HB01_N	IO, LVCMOS	HB Bank IO01 Negative.
J26	GND	GND	Power	Ground.
J27	HB07_P	HB07_P	IO, LVCMOS	HB Bank IO07 Positive.
J28	HB07_N	HB07_N	IO, LVCMOS	HB Bank IO07 Negative.
J29	GND	GND	Power	Ground.
J30	HB11_P	HB11_P	IO, LVCMOS	HB Bank IO11 Positive.
J31	HB11_N	HB11_N	IO, LVCMOS	HB Bank IO11 Negative.
J32	GND	GND	Power	Ground.
J33	HB15_P	HB15_P	IO, LVCMOS	HB Bank IO15 Positive.
J34	HB15_N	HB15_N	IO, LVCMOS	HB Bank IO15 Negative.
J35	GND	GND	Power	Ground.
J36	HB18_P	HB18_P	IO, LVCMOS	HB Bank IO18 Positive.
J37	HB18_N	HB18_N	IO, LVCMOS	HB Bank IO18 Negative.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	CLK2_BIDIR_P	IO, LVDS	Optional Clock Output from 10-bit clock synthesizer OUT9.
K5	CLK2_BIDIR_N	CLK2_BIDIR_N	IO, LVDS	Optional Clock Output from 10-bit clock synthesizer OUT9b.
K6	GND	GND	Power	Ground.
K7	HA02_P	HA02_P	IO, LVCMOS	HA Bank IO02 Positive.
K8	HA02_N	HA02_N	IO, LVCMOS	HA Bank IO02 Negative.
K9	GND	GND	Power	Ground.
K10	HA06_P	HA06_P	IO, LVCMOS	HA Bank IO06 Positive.
K11	HA06_N	HA06_N	IO, LVCMOS	HA Bank IO06 Negative.
K12	GND	GND	Power	Ground.
K13	HA10_P	HA10_P	IO, LVCMOS	HA Bank IO10 Positive.
K14	HA10_N	HA10_N	IO, LVCMOS	HA Bank IO10 Negative.
K15	GND	GND	IO, LVCMOS	Ground.
K16	HA17_P_CC	HA17_P_CC	IO, LVCMOS	HA Bank IO17 Positive.
K17	HA17_N_CC	HA17_N_CC	IO, LVCMOS	HA Bank IO17 Negative.
K18	GND	GND	Power	Ground.
K19	HA21_P	HA21_P	IO, LVCMOS	HA Bank IO21 Positive.
K20	HA21_N	HA21_N	IO, LVCMOS	HA Bank IO21 Negative.
K21	GND	GND	Power	Ground.
K22	HA23_P	HA23_P	IO, LVCMOS	HA Bank IO23 Positive.
K23	HA23_N	HA23_N	IO, LVCMOS	HA Bank IO23 Negative.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	HB00_P_CC	IO, LVCMOS	HB Bank IO00 Positive.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
K26	HB00_N_CC	HB00_N_CC	IO, LVCMOS	HB Bank IO00 Negative.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	HB06_P_CC	IO, LVCMOS	HB Bank IO06 Positive.
K29	HB06_N_CC	HB06_N_CC	IO, LVCMOS	HB Bank IO06 Negative.
K30	GND	GND	Power	Ground.
K31	HB10_P	HB10_P	IO, LVCMOS	HB Bank IO10 Positive.
K32	HB10_N	HB10_N	IO, LVCMOS	HB Bank IO10 Negative.
K33	GND	GND	Power	Ground.
K34	HB14_P	HB14_P	IO, LVCMOS	HB Bank IO14 Positive.
K35	HB14_N	HB14_N	IO, LVCMOS	HB Bank IO14 Negative.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	HB17_P_CC	IO, LVCMOS	HB Bank IO17 Positive.
K38	HB17_N_CC	HB17_N_CC	IO, LVCMOS	HB Bank IO17 Negative.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.
L1	RES1	NA	NA	NC.
L2	GND	GND	Power	Ground.
L3	GND	GND	Power	Ground.
L4	GBTCLK4_M2C_P	GBTCLK4_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 4 Positive.
L5	GBTCLK4_M2C_N	GBTCLK4_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 4 Negative.
L6	GND	GND	Power	Ground.
L7	GND	GND	Power	Ground.
L8	GBTCLK3_M2C_P	GBTCLK3_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 3 Positive.
L9	GBTCLK3_M2C_N	GBTCLK3_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 3 Negative.
L10	GND	GND	Power	Ground.
L11	GND	GND	Power	Ground.
L12	GBTCLK2_M2C_P	GBTCLK2_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 2 Positive.
L13	GBTCLK2_M2C_N	GBTCLK2_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 2 Negative.
L14	GND	GND	Power	Ground.
L15	GND	GND	Power	Ground.
L16	SYNC_C2M_P	SYNC_C2M_P	NA	NC.
L17	SYNC_C2M_N	SYNC_C2M_N	NA	NC.
L18	GND	GND10	Power	Ground.
L19	GND	GND11	Power	Ground.
L20	REFCLK_C2M_P	REFCLK_C2M_P	I, LVDS	NC. Note: Optionally connected to 10-bit clock synthesizer Input.
L21	REFCLK_C2M_N	REFCLK_C2M_N	I, LVDS	NC. Note: Optionally connected to 10-bit clock synthesizer Input.
L22	GND	GND	Power	Ground.
L23	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
L24	REFCLK_M2C_P	REFCLK_M2C_P	O, LVDS	NC. Optionally connected from 10-bit clock synthesizer OUT6.
L25	REFCLK_M2C_N	REFCLK_M2C_N	O, LVDS	NC. Optionally connected from 10-bit clock synthesizer OUT6b.
L26	GND	GND	Power	Ground.
L27	GND	GND	Power	Ground.
L28	SYNC_M2C_P	SYNC_M2C_P	NA	NC.
L29	SYNC_M2C_N	SYNC_M2C_N	NA	NC.
L30	GND	GND	Power	Ground.
L31	GND	GND	Power	Ground.
L32	RES2	NA	NA	NC.
L33	RES3	NA	NA	NC.
L34	GND	GND	Power	Ground.
L35	GND	GND	Power	Ground.
L36	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
L37	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
L38	GND	GND	Power	Ground.
L39	GND	GND	Power	Ground.
L40	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
M1	GND	GND	Power	Ground.
M2	DP23_M2C_P	DP23_M2C_P	O, DIFF	Gigabit Transceiver 23 Positive Module to Connector.
M3	DP23_M2C_N	DP23_M2C_N	O, DIFF	Gigabit Transceiver 23 Negative Module to Connector.
M4	GND	GND	Power	Ground.
M5	GND	GND	Power	Ground.
M6	DP22_M2C_P	DP22_M2C_P	O, DIFF	Gigabit Transceiver 22 Positive Module to Connector.
M7	DP22_M2C_N	DP22_M2C_N	O, DIFF	Gigabit Transceiver 22 Negative Module to Connector.
M8	GND	GND	Power	Ground.
M9	GND	GND	Power	Ground.
M10	DP21_M2C_P	DP21_M2C_P	O, DIFF	Gigabit Transceiver 21 Positive Module to Connector.
M11	DP21_M2C_N	DP21_M2C_N	O, DIFF	Gigabit Transceiver 21 Negative Module to Connector.
M12	GND	GND	Power	Ground.
M13	GND	GND	Power	Ground.
M14	DP20_M2C_P	DP20_M2C_P	O, DIFF	Gigabit Transceiver 20 Positive Module to Connector.
M15	DP20_M2C_N	DP20_M2C_N	O, DIFF	Gigabit Transceiver 20 Negative Module to Connector.
M16	GND	GND	Power	Ground.
M17	GND	GND	Power	Ground.
M18	DP14_C2M_P	DP14_C2M_P	I, DIFF	Gigabit Transceiver 14 Positive Connector to Module.
M19	DP14_C2M_N	DP14_C2M_N	I, DIFF	Gigabit Transceiver 14 Negative Connector to Module.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
M20	GND	GND	Power	Ground.
M21	GND	GND	Power	Ground.
M22	DP15_C2M_P	DP15_C2M_P	I, DIFF	Gigabit Transceiver 15 Positive Connector to Module.
M23	DP15_C2M_N	DP15_C2M_N	I, DIFF	Gigabit Transceiver 15 Negative Connector to Module.
M24	GND	GND	Power	Ground.
M25	GND	GND	Power	Ground.
M26	DP16_C2M_P	DP16_C2M_P	I, DIFF	Gigabit Transceiver 16 Positive Connector to Module.
M27	DP16_C2M_N	DP16_C2M_N	I, DIFF	Gigabit Transceiver 16 Negative Connector to Module.
M28	GND	GND	Power	Ground.
M29	GND	GND	Power	Ground.
M30	DP17_C2M_P	DP17_C2M_P	I, DIFF	Gigabit Transceiver 17 Positive Connector to Module.
M31	DP17_C2M_N	DP17_C2M_N	I, DIFF	Gigabit Transceiver 17 Negative Connector to Module.
M32	GND	GND	Power	Ground.
M33	GND	GND	Power	Ground.
M34	DP18_C2M_P	DP18_C2M_P	I, DIFF	Gigabit Transceiver 18 Positive Connector to Module.
M35	DP18_C2M_N	DP18_C2M_N	I, DIFF	Gigabit Transceiver 18 Negative Connector to Module.
M36	GND	GND	Power	Ground.
M37	GND	GND	Power	Ground.
M38	DP19_C2M_P	DP19_C2M_P	I, DIFF	Gigabit Transceiver 19 Positive Connector to Module.
M39	DP19_C2M_N	DP19_C2M_N	I, DIFF	Gigabit Transceiver 19 Negative Connector to Module.
M40	GND	GND	Power	Ground.
Y1	GND	GND	Power	Ground.
Y2	DP23_C2M_P	DP23_C2M_P	I, DIFF	Gigabit Transceiver 23 Positive Connector to Module.
Y3	DP23_C2M_N	DP23_C2M_N	I, DIFF	Gigabit Transceiver 23 Negative Connector to Module.
Y4	GND	GND	Power	Ground.
Y5	GND	GND	Power	Ground.
Y6	DP21_C2M_P	DP21_C2M_P	I, DIFF	Gigabit Transceiver 21 Positive Connector to Module.
Y7	DP21_C2M_N	DP21_C2M_N	I, DIFF	Gigabit Transceiver 21 Negative Connector to Module.
Y8	GND	GND	Power	Ground.
Y9	GND	GND	Power	Ground.
Y10	DP10_M2C_P	DP10_M2C_P	O, DIFF	Gigabit Transceiver 20 Positive Module to Connector.
Y11	DP10_M2C_N	DP10_M2C_N	O, DIFF	Gigabit Transceiver 20 Negative Module to Connector.
Y12	GND	GND	Power	Ground.
Y13	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
Y14	DP12_M2C_P	DP12_M2C_P	O, DIFF	Gigabit Transceiver 12 Positive Module to Connector.
Y15	DP12_M2C_N	DP12_M2C_N	O, DIFF	Gigabit Transceiver 12 Negative Module to Connector.
Y16	GND	GND	Power	Ground.
Y17	GND	GND	Power	Ground.
Y18	DP14_M2C_P	DP14_M2C_P	O, DIFF	Gigabit Transceiver 14 Positive Module to Connector.
Y19	DP14_M2C_N	DP14_M2C_N	O, DIFF	Gigabit Transceiver 14 Negative Module to Connector.
Y20	GND	GND	Power	Ground.
Y21	GND	GND	Power	Ground.
Y22	DP15_M2C_P	DP15_M2C_P	O, DIFF	Gigabit Transceiver 15 Positive Module to Connector.
Y23	DP15_M2C_N	DP15_M2C_N	O, DIFF	Gigabit Transceiver 15 Negative Module to Connector.
Y24	GND	GND	Power	Ground.
Y25	GND	GND	Power	Ground.
Y26	DP11_C2M_P	DP11_C2M_P	I, DIFF	Gigabit Transceiver 11 Positive Connector to Module.
Y27	DP11_C2M_N	DP11_C2M_N	I, DIFF	Gigabit Transceiver 11 Negative Connector to Module.
Y28	GND	GND	Power	Ground.
Y29	GND	GND	Power	Ground.
Y30	DP13_C2M_P	DP13_C2M_P	I, DIFF	Gigabit Transceiver 13 Positive Connector to Module.
Y31	DP13_C2M_N	DP13_C2M_N	I, DIFF	Gigabit Transceiver 13 Negative Connector to Module.
Y32	GND	GND	Power	Ground.
Y33	GND	GND	Power	Ground.
Y34	DP17_M2C_P	DP17_M2C_P	O, DIFF	Gigabit Transceiver 17 Positive Module to Connector.
Y35	DP17_M2C_N	DP17_M2C_N	O, DIFF	Gigabit Transceiver 17 Negative Module to Connector.
Y36	GND	GND	Power	Ground.
Y37	GND	GND	Power	Ground.
Y38	DP19_M2C_P	DP19_M2C_P	O, DIFF	Gigabit Transceiver 19 Positive Module to Connector.
Y39	DP19_M2C_N	DP19_M2C_N	O, DIFF	Gigabit Transceiver 19 Negative Module to Connector.
Y40	GND	GND	Power	Ground.
Z1	HSPC_PRSNT_M2C_L	HSPC_PRSNT_M2C_L	O, 0E PD	Module Present Signal.
Z2	GND	GND	Power	Ground.
Z3	GND	GND	Power	Ground.
Z4	DP22_C2M_P	DP22_C2M_P	I, DIFF	Gigabit Transceiver 22 Positive Connector to Module.
Z5	DP22_C2M_N	DP22_C2M_N	I, DIFF	Gigabit Transceiver 22 Negative Connector to Module.
Z6	GND	GND	Power	Ground.
Z7	GND	GND	Power	Ground.
Z8	DP20_C2M_P	DP20_C2M_P	I, DIFF	Gigabit Transceiver 20 Positive

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/Termination	Description
				Connector to Module.
Z9	DP20_C2M_N	DP20_C2M_N	I, DIFF	Gigabit Transceiver 20 Negative Connector to Module.
Z10	GND	GND	Power	Ground.
Z11	GND	GND	Power	Ground.
Z12	DP11_M2C_P	DP11_M2C_P	O, DIFF	Gigabit Transceiver 11 Positive Module to Connector.
Z13	DP11_M2C_N	DP11_M2C_N	O, DIFF	Gigabit Transceiver 11 Negative Module to Connector.
Z14	GND	GND	Power	Ground.
Z15	GND	GND	Power	Ground.
Z16	DP13_M2C_P	DP13_M2C_P	O, DIFF	Gigabit Transceiver 13 Positive Module to Connector.
Z17	DP13_M2C_N	DP13_M2C_N	O, DIFF	Gigabit Transceiver 13 Negative Module to Connector.
Z18	GND	GND	Power	Ground.
Z19	GND	GND	Power	Ground.
Z20	GBTCLK5_M2C_P	GBTCLK5_M2C_P	O, LVDS	Gigabit Transceiver Reference Clock 5 Positive.
Z21	GBTCLK5_M2C_N	GBTCLK5_M2C_N	O, LVDS	Gigabit Transceiver Reference Clock 5 Negative.
Z22	GND	GND	Power	Ground.
Z23	GND	GND	Power	Ground.
Z24	DP10_C2M_P	DP10_C2M_P	I, DIFF	Gigabit Transceiver 10 Positive Connector to Module.
Z25	DP10_C2M_N	DP10_C2M_N	I, DIFF	Gigabit Transceiver 10 Negative Connector to Module.
Z26	GND	GND	Power	Ground.
Z27	GND	GND	Power	Ground.
Z28	DP12_C2M_P	DP12_C2M_P	I, DIFF	Gigabit Transceiver 12 Positive Connector to Module.
Z29	DP12_C2M_N	DP12_C2M_N	I, DIFF	Gigabit Transceiver 12 Negative Connector to Module.
Z30	GND	GND	Power	Ground.
Z31	GND	GND	Power	Ground.
Z32	DP16_M2C_P	DP16_M2C_P	O, DIFF	Gigabit Transceiver 16 Positive Module to Connector.
Z33	DP16_M2C_N	DP16_M2C_N	O, DIFF	Gigabit Transceiver 16 Negative Module to Connector.
Z34	GND	GND	Power	Ground.
Z35	GND	GND	Power	Ground.
Z36	DP18_M2C_P	DP18_M2C_P	O, DIFF	Gigabit Transceiver 18 Positive Module to Connector.
Z37	DP18_M2C_N	DP18_M2C_N	O, DIFF	Gigabit Transceiver 18 Negative Module to Connector.
Z38	GND	GND	Power	Ground.
Z39	GND	GND	Power	Ground.
Z40	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.

Note: Pin No. Y1 to Y40, Z1 to Z40, L1 to L40 and M1 to M40 will not be available in FMC Loopback Test Module.

2.2.2 FMC/FMC+ Loopback Test Module's Loopback Configuration

2.2.2.1 DP (Differential Pair) Pins

FMC/FMC+ Loopback Test module will support all gigabit transceiver channel, DP [23:0]. All the DPx_M2C pins are connected to DPx_C2M pins through 0.01uF capacitor, where x represents the channel number from 0 to 23. Refer the block diagram Figure 1 for information on loopback connection.

2.2.2.2 LA (Low Pin Count) Pins

FMC/FMC+ Loopback Test module will support 34 LVDS/68 single ended signal from LA bank. The module supports the loopback in the following manner in the board, LA[2^x] to LA[2^{x+1}] where x is IO pair number from 0 to 33.

2.2.2.3 HA (High Pin Count A) Pins

FMC/FMC+ Loopback Test module will support 24 LVDS/48 single ended signal from HA bank. The module supports the loopback in the following manner in the board, HA[2^x] to HA[$^{2x+1}$] where x is IO pair number from 0 to 23.

2.2.2.4 HB (High Pin Count B) Pins

FMC/FMC+ Loopback Test module will support 22 LVDS/44 single ended signal from HB bank. The module supports the loopback in the following manner in the board, HB[^{2x}] to HB[$^{2x+1}$] where x is IO pair number from 0 to

2.2.3 10-Bit Clock Synthesizer

This FMC/FMC+ Loopback test module supports SI5341B-D-GM 10-bit clock synthesizer for Gigabit transceivers reference clocks. By default, 156.25MHz clock frequency is pre-programmed in the IC NVM storage.

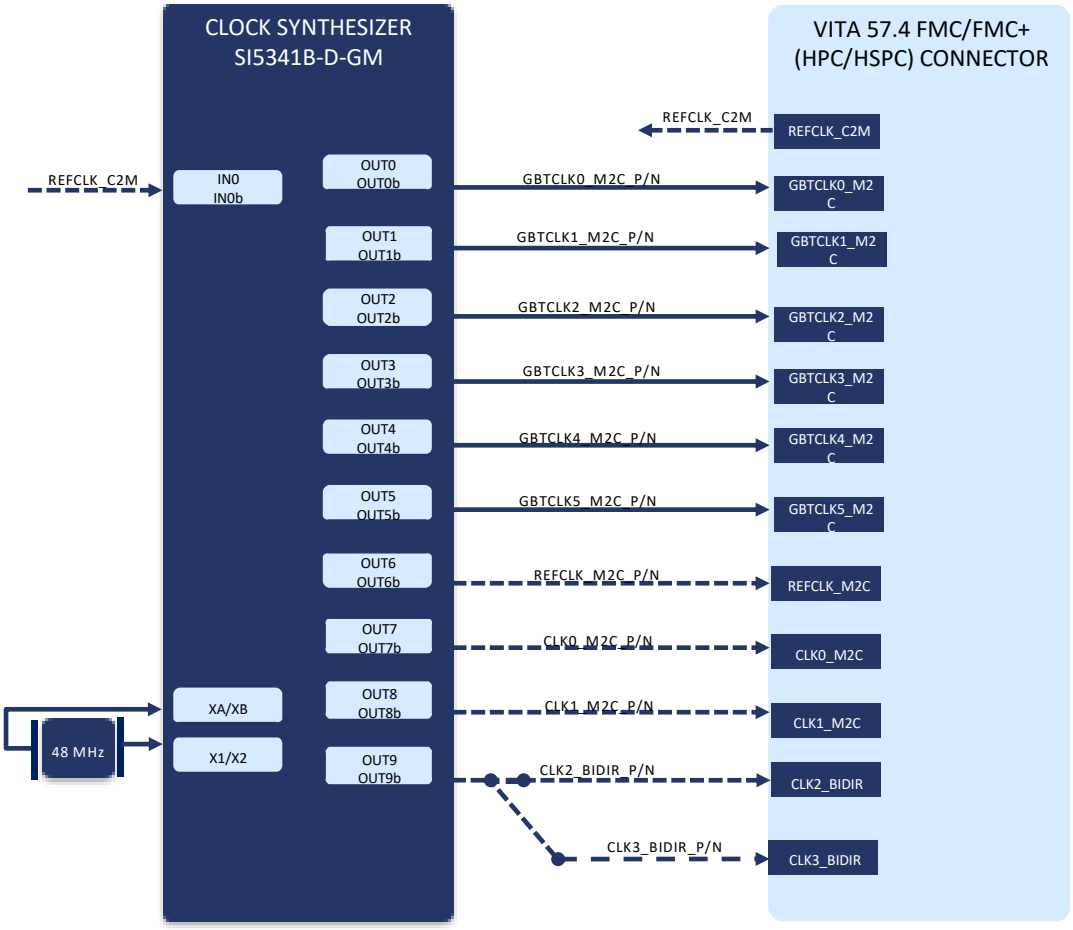


Figure 4: FMC/FMC+ Loopback Test Module Clock Tree

2.2.4 EEPROM

The FMC/FMC+ Loopback Test Module supports EEPROM “M24C32-FMC6TG” to store FMC FRU details. This EEPROM is interfaced to SCL & SDA pins of the FMC/FMC+ connector. Also, its I2C address setting pins E1 & E0 is connected to FMC/FMC+ connector pins GA0 & GA1 respectively in FMC/FMC+ Loopback Test Module.

Table 4: EEPROM Address Configuration

Address Bit	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	1	**0**	**1**	**0**	**E2**	**E1**	**E0**	**R/W**
Bit Logic Level	1	0	1	0	0	GA0	GA1	R/W

Bit Logic Level -1 : High
Bit Logic Level -0 : Low

3. TECHNICAL SPECIFICATION

This section provides detailed information about the FMC/FMC+ Loopback Test Module technical specification with Electrical and Environmental characteristics.

3.1 Power Input Requirement

The FMC/FMC+ Loopback Test Module is designed to work with power from FMC/FMC+ Connector. The below table provides the Power Input Requirement of FMC/FMC+ Loopback Test Module.

Table 5: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)
1	VCC_FMC+_ADJ	0	VADJ	3.3
2	VCC_3V3_FMC+	3.15	3.3	3.45
3	VCC_3V3_AUX	3.15	3.3	3.45
4	VCC_12V_FMC+	11.75	12	12.25

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of FMC/FMC+ Loopback Test Module.

Table 6: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.2.2 RoHS Compliance

The FMC/FMC+ Loopback Test Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

The FMC/FMC+ Loopback Test Module is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 FMC/FMC+ Loopback Test Module Mechanical Dimensions

The FMC/FMC+ Loopback Test Module PCB form factor is 78.5mm X 69mm and Board mechanical dimension is shown below.

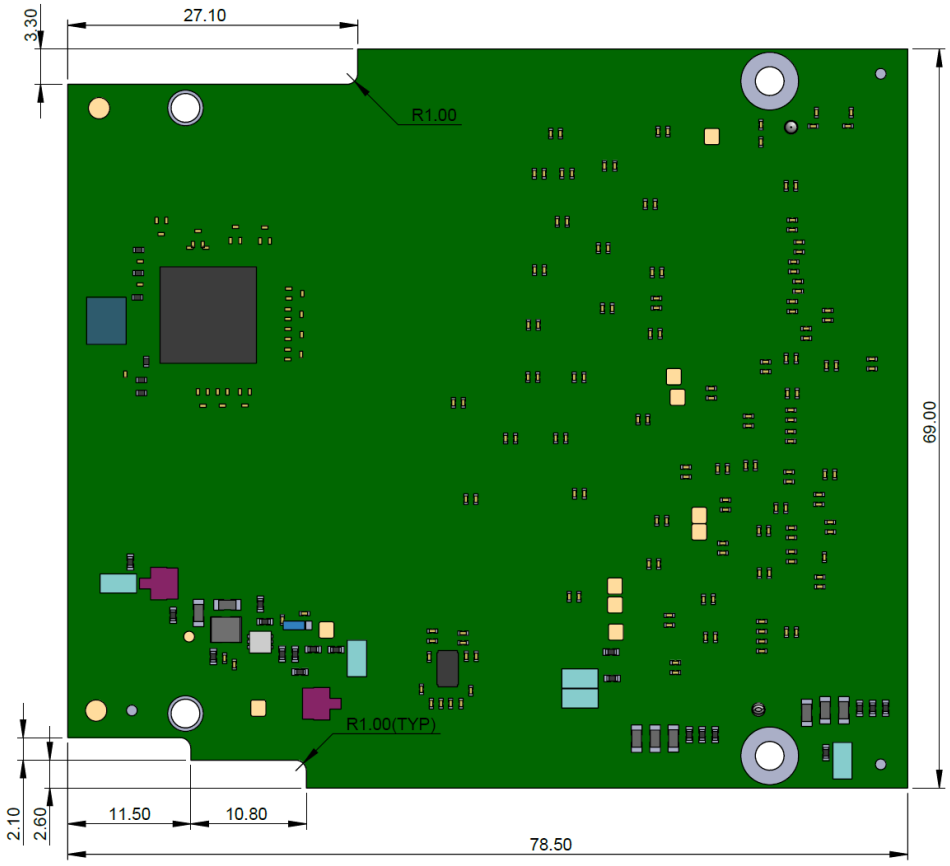


Figure 5: FMC/FMC+ Loopback Test Module Mechanical dimension – Top View

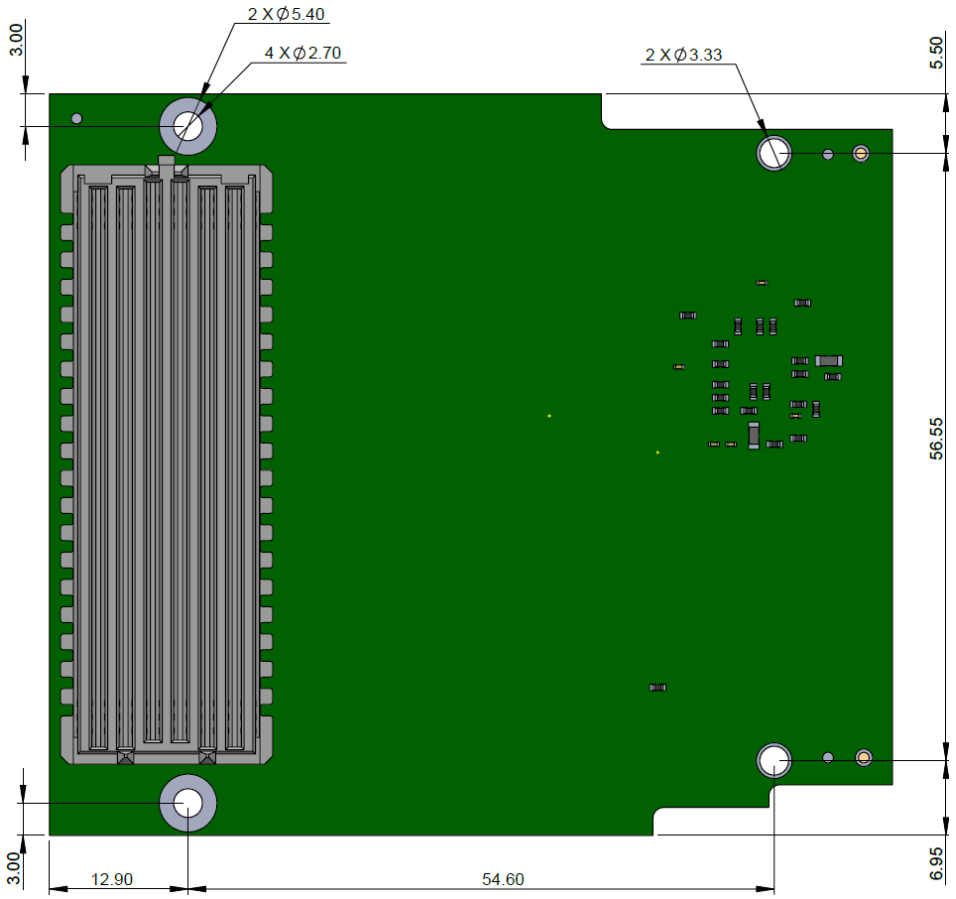


Figure 6: FMC/FMC+ Loopback Test Module Mechanical dimension – Bottom View

The FMC/FMC+ Loopback Test Module PCB thickness is 1.6mm±0.1mm, top side maximum height component is MOSFET (1.20mm) and bottom side maximum height component is FMC+ HSPC Connector (7.11mm). Please refer the below figure for height details of the FMC/FMC+ Loopback Test Module.

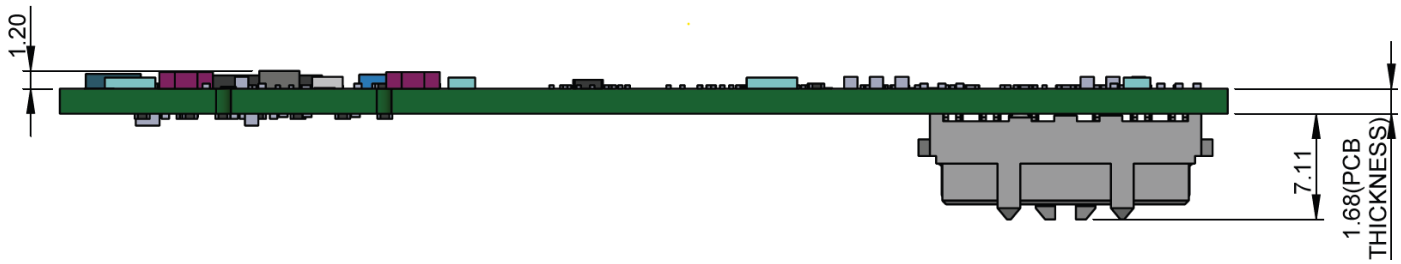


Figure 7: FMC/FMC+ Loopback Test Module Mechanical dimension – Side View

4. ORDERING INFORMATION

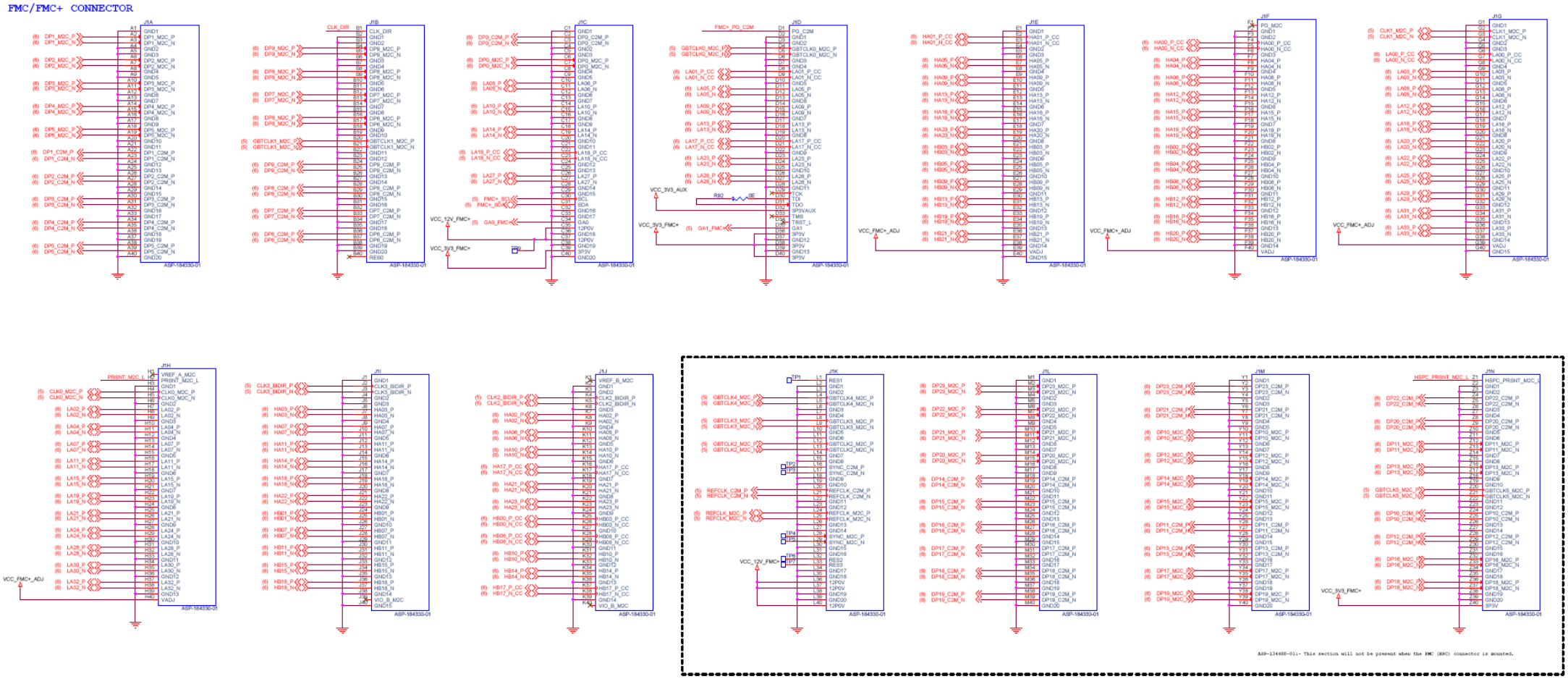
The below table provides the standard orderable part numbers for FMC/FMC+ Loopback Test Module.

Table 7: Orderable Product Part Numbers

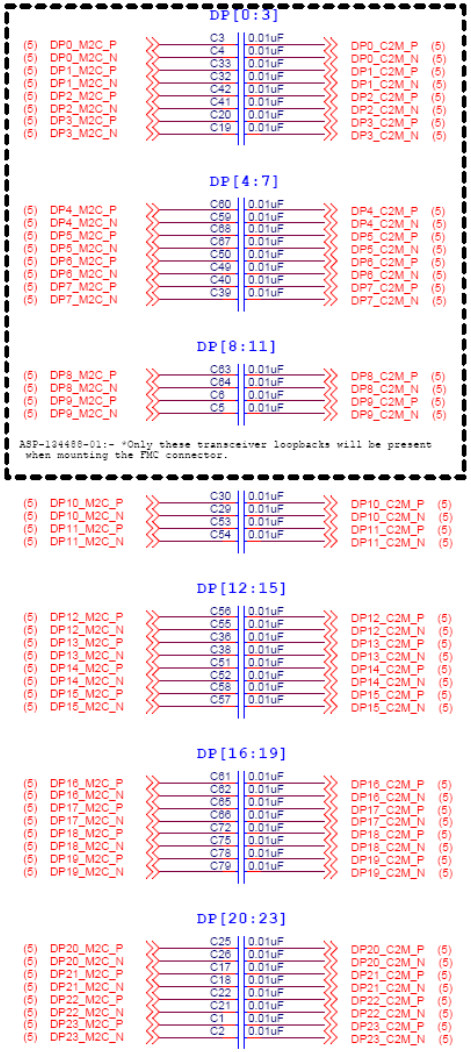
Product Part Number	Description	Temperature
iG-FMC-LBFMCP-I1	VITA 57.4 FMC+ Loopback Test Module.	Industrial
iG-FMC-LBFMC-I1	VITA 57.1 FMC Loopback Test Module.	Industrial

5. APPENDIX

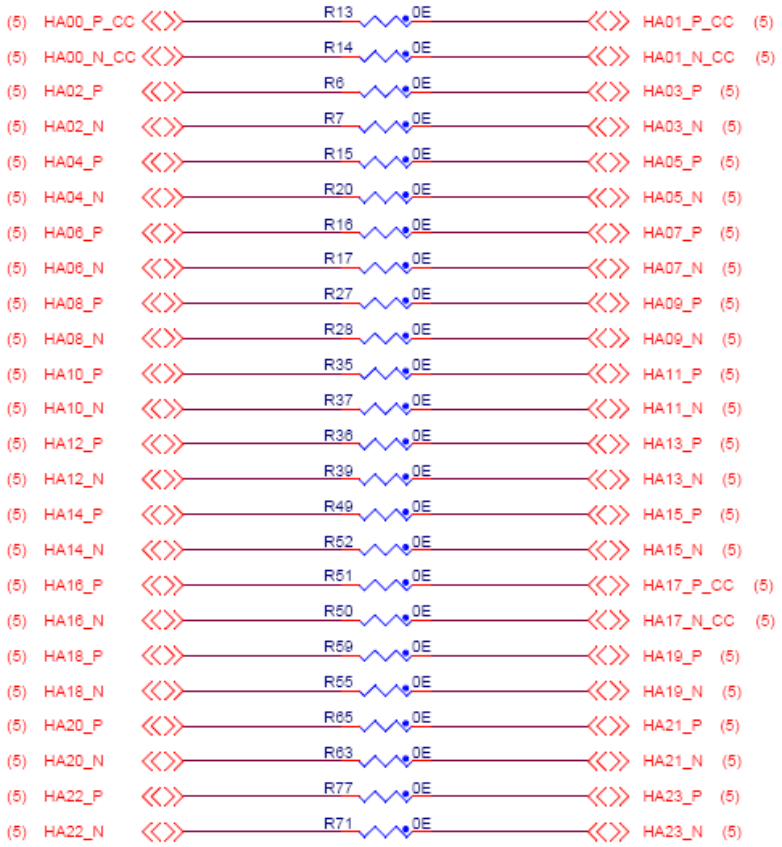
5.1 Circuit Reference



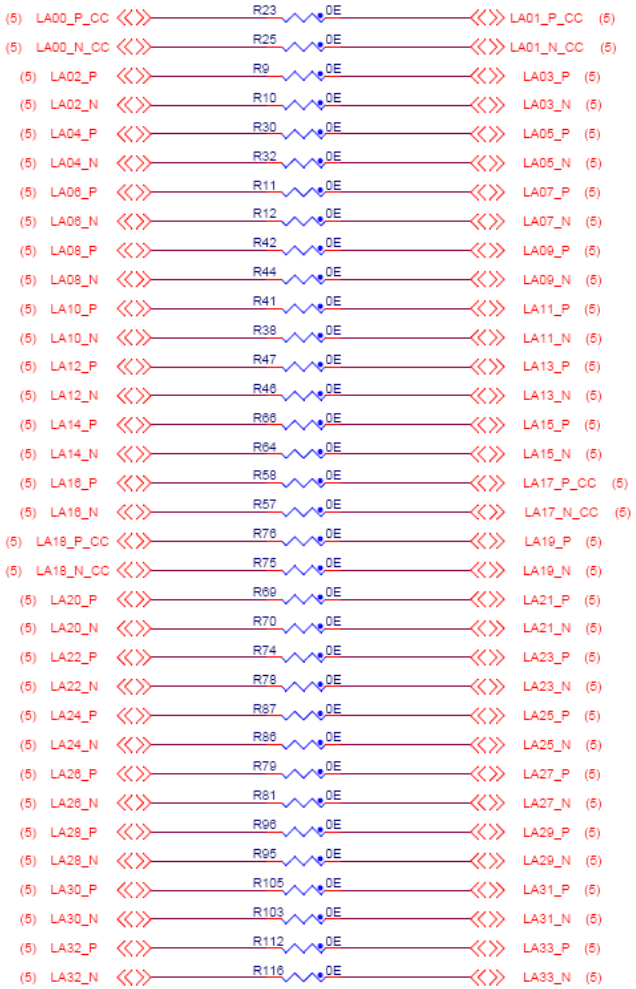
HIGH SPEED TRANSCEIVERS LOOPBACK



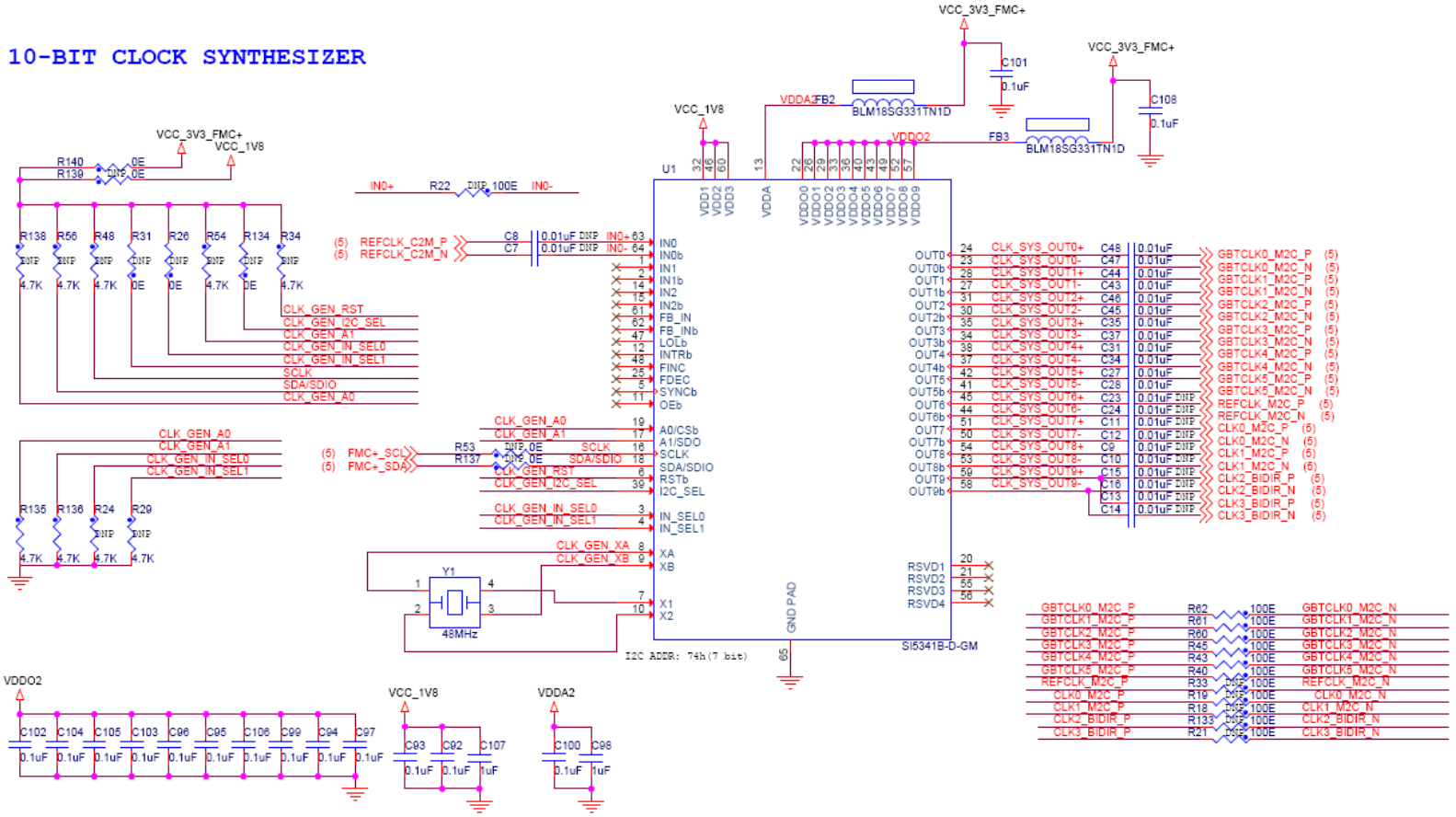
FPGA I/OS LOOPBACK (HA BANK)



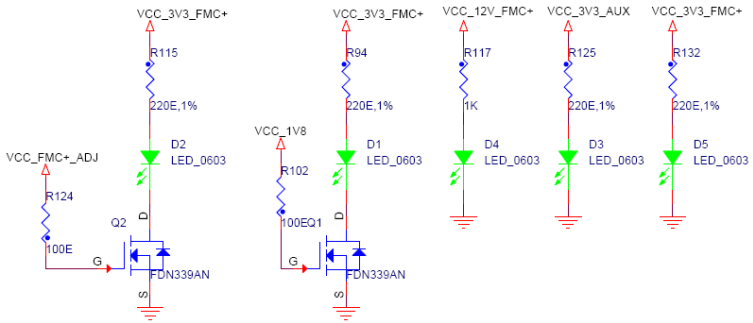
FPGA I/OS LOOPBACK (LA BANK)



10-BIT CLOCK SYNTHESIZER



POWER LEDs



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