



Versal Prime Series Data Sheet: DC and AC Switching Characteristics

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Product Specification

Summary

The AMD Versal™ Prime devices are available in -3 (highest performance), -2, -1 speed grades. The -3 devices can operate at a V_{CCINT} voltage of 0.88V (H). The -2 devices can operate at a V_{CCINT} voltage of 0.88V (H), 0.80V (M), or depending upon the speed grade, 0.70V (L) or 0.725V (L). The -1 devices can operate at a V_{CCINT} voltage of 0.80V (M) or 0.70V (L). Primary supply operating voltages typically scale with V_{CCINT} , except for supported overdrive of the V_{CC_PMC} , V_{CC_PSFP} , V_{CC_PSLP} , and V_{CC_CPM5} at 0.88V (H) when V_{CCINT} and other primary supplies operate at 0.80V (M) or 0.70V (L). Similar to speed grades, a higher operating voltage typically has higher performance specifications. All devices are screened for standard (S) or low (L) maximum static power. See *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) for available device ordering options.

DC and AC characteristics are specified in extended (E), industrial (I), and military (M) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade and operating voltage (that is, the timing characteristics of a -1 speed grade extended (E) temperature range device operating at a V_{CCINT} voltage of 0.80V (M) are the same as for a -1 speed grade industrial (I) temperature range device operating at a V_{CCINT} voltage of 0.80V (M)). However, only selected speed grades, operating voltages, maximum static power screens, and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Versal adaptive SoCs, is available on the AMD website at <https://www.amd.com/versal>.

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DC Characteristics

Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings—Power, Voltages, and Current

Symbol	Description ¹	Min	Max	Units
V _{CCAUX}	Programmable logic auxiliary power supply	–0.500	1.650	V
V _{CCAUX_PMC}	Platform management controller (PMC) auxiliary power supply voltage	–0.500	1.650	V
V _{CCAUX_SMON} ²	PMC system monitor power supply relative to GND_SMON	–0.500	1.650	V
V _{CC_BATT}	Battery power supply	–0.500	1.650	V
V _{CC_FUSE}	eFUSE programming power supply	–0.500	2.000	V
V _{CCINT}	Programmable logic primary power supply	–0.500	0.970	V
V _{CCINT_GT}	GTM primary power supply	–0.500	0.970	V
V _{CC_CPM5}	CPM5 primary power supply	–0.500	0.970	V
V _{CC_IO} ³	XPIO power supply or X5IO power supply	–0.500	0.970	V
V _{CCO} ⁴	X5IO bank 7## output driver power supply Where the bank number is the three-digit bank number beginning with 7	–0.500	1.32	V
	XPIO bank 7## and bank 8## output driver power supply Where the bank number is the three-digit bank number beginning with 7 or 8	–0.500	1.650	V
	HDIO bank 4## output driver power supply Where the bank number is the three-digit bank number beginning with 4	–0.500	3.63	V
	PSIO bank 5## power supplies Where the bank number is the three-digit bank number beginning with 5	–0.500	3.63	V
V _{CC_PMC}	PMC primary power supply	–0.500	0.970	V
V _{CC_PSPF}	PS full-power domain power supply	–0.500	0.970	V
V _{CC_PSLP}	PS low-power domain power supply	–0.500	0.970	V
V _{CC_RAM}	PL RAM and clocking network power supply	–0.500	0.970	V
V _{CC_SOC} ³	Network on Chip (NoC) and integrated DDR memory controller power supply	–0.500	0.970	V
V _{IN} ^{4, 5}	I/O input voltage for PSIO, HDIO, and XPIO banks	–0.550	V _{CCO} + 0.550	V
	I/O input voltage for X5IO	–0.200	V _{CCO} + 0.450	V
V _{REF}	PMC system monitor reference input (V _{REFP} /V _{REFN}) relative to GND_SMON	–0.500	1.120	V
GTYP and GTYP (or GTM) Transceivers				
V _{GTYP_AVCC} V _{GTYP_AVCC} V _{GTM_AVCC}	GTYP and GTYP (or GTM) transceiver primary analog power supply ⁶	–0.500	0.97	V
V _{GTYP_AVCCAUX} V _{GTYP_AVCCAUX} V _{GTM_AVCCAUX}	GTYP and GTYP (or GTM) transceiver auxiliary analog (PLL) power supply ⁶	–0.500	1.650	V
V _{GTYP_AVTT} V _{GTYP_AVTT} V _{GTM_AVTT}	GTYP and GTYP (or GTM) transceiver termination power supply ⁶	–0.500	1.320	V
V _{GTYP_AVTTTRCAL} V _{GTYP_AVTTTRCAL} V _{GTM_AVTTTRCAL}	GTYP and GTYP (or GTM) transceiver analog resistor calibration power supply ⁶	–0.500	1.320	V

Table 1: Absolute Maximum Ratings—Power, Voltages, and Current (cont'd)

Symbol	Description ¹		Min	Max	Units
V _{GTY_REFCLK_DC} V _{GTYP_REFCLK_DC} V _{GTM_REFCLK_DC}	Transceiver reference clock absolute input DC voltage		–0.500	1.000	V
V _{GTY_REFCLK_AC} V _{GTYP_REFCLK_AC} V _{GTM_REFCLK_AC}	Transceiver reference clock absolute input AC voltage ⁷		–0.500	1.350	V
V _{IN_DC}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute DC voltage	Unpowered	–0.800	0.800	V
		Powered	–0.300	1.000	V
V _{IN_AC+DC}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute AC plus DC voltage	Unpowered	–0.800	0.800	V
		Powered	–0.500	1.250	V
I _{DCIN_FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating ⁸		–	10	mA
I _{DCIN_GTY_AVTT} I _{DCIN_GTYP_AVTT}	DC input current for GTY and GTYP receiver input pins DC coupled RX termination = V _{GTY_AVTT} or V _{GTYP_AVTT}		–	16	mA
I _{DCIN_GTM_AVTT}	DC input current for GTM receiver input pins DC coupled RX termination = V _{GTM_AVTT}		–	16	mA
I _{DCIN_GTY_GND} I _{DCIN_GTYP_GND}	DC input current for GTY and GTYP receiver input pins DC coupled RX termination = GND ¹⁰		–	16	mA
I _{DCIN_GTM_GND}	DC input current for GTM receiver input pins DC coupled RX termination = GND		–	16	mA
I _{DCIN_PROG}	DC input current for receiver input pins DC coupled RX termination = programmable ⁹		–	0	mA
I _{DCOUT_FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating		–	6	mA
I _{DCOUT_GTY_AVTT} I _{DCOUT_GTYP_AVTT}	DC output current for transmitter pins DC coupled RX termination = V _{GTY_AVTT} or V _{GTYP_AVTT}		–	6	mA
Other Ratings					
I _{DC}	Available output current at the pad		–20	20	mA
I _{RMS}	Available RMS output current at the pad		–20	20	mA

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- V_{CCAUX_SMON} must be connected to V_{CCAUX_PMC}. See *Versal Adaptive SoC System Monitor Architecture Manual (AM006)* for V_{CCAUX_SMON} information and filter considerations.
- V_{CC_IO} must be connected to V_{CC_SOC}.
- When operating outside of the recommended operating conditions, refer to the specifications in the [V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot](#) section.
- The lower absolute voltage specification always applies.
- For more information on supported GTY and GTYP (or GTM) transceiver terminations see the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual (AM002)* or *Versal Adaptive SoC GTM Transceivers Architecture Manual (AM017)*.
- The GTY_REFCLK AC or GTYP_REFCLK AC signal operates in the reference clock frequency range. See the [GTY and GTYP Transceiver Reference Clock Switching Characteristics](#).
- AC coupled operation is not supported for RX termination = floating.
- DC coupled operation is not supported for RX termination = programmable.
- For DC coupled links with RX termination set to ground, the transmitter or the board should insure that the RX input common mode voltage is set between 0.2V and 0.8V.

Table 2: Absolute Maximum Ratings—Temperature

Symbol	Description ¹	Min	Max	Units
T _{STG}	Storage temperature (ambient, unpowered)	–55	150	°C
T _{SOL} ²	Maximum dry rework soldering temperature	–	260	°C
T _j	Maximum junction temperature	–	125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- For soldering guidelines and thermal considerations, see the *Versal Adaptive SoC Packaging and Pinouts Architecture Manual* (AM013).

Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Symbol	Description ^{1, 2, 3}	Min	Typ	Max	Units
V _{CCAUX}	Auxiliary power supply	1.455	1.500	1.545	V
V _{CCAUX_PMC}	PMC auxiliary power supply voltage	1.455	1.500	1.545	V
V _{CCAUX_SMON} ⁴	PMC system monitor power supply relative to GND_SMON	1.455	1.500	1.545	V
V _{CC_BATT} ⁵	Battery power supply to the battery-backed RAM and battery-backed real-time clock (RTC)	1.200	–	1.500	V
V _{CC_FUSE} ⁶	eFUSE programming power supply	1.745	1.800	1.854	V
V _{CCINT}	PL primary power supply, low (L) voltage	0.676	0.700	0.724	V
	PL primary power supply, low (L) voltage for -2LLI devices ⁷	0.701	0.725	0.749	V
	PL primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	PL primary power supply, high (H) voltage	0.854	0.880	0.906	V
V _{CCINT_GT}	GTM primary power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	GTM primary power supply, high (H) voltage	0.854	0.880	0.906	V
V _{CC_CPM5}	CPM5 primary power supply, low (L) voltage	0.676	0.700	0.724	V
	CPM5 primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	CPM5 primary power supply, high (H) voltage	0.854	0.880	0.906	V
	CPM5 primary power supply, overdrive voltage for higher CPM5 performance at specific speed grades. See Available Speed Grades and Operating Voltages .	0.854	0.880	0.906	V
V _{CC_IO} ⁸	XPIO or X5IO power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	XPIO or X5IO power supply, high (H) voltage	0.854	0.880	0.906	V
V _{CCO} ⁹	X5IO bank 7## output driver power supply Includes V _{CCO} of 1.0V, 1.1V, 1.2V at ±3% for all IOSTANDARDS that operate at a data rate that is 4.5 Gb/s or higher. For all IOSTANDARDS operating at a data rate below 4.5 Gb/s, the tolerance is ±5%.	0.95	1.0 to 1.2	1.26	V
	XPIO bank 7## and bank 8## output driver power supply Includes V _{CCO} of 1.0V, 1.1V, 1.2V, 1.35V, 1.5V at ±5%	0.950	–	1.575	V
	HDIO bank 4## output driver power supply Includes V _{CCO} of 1.8V, 2.5V at ±5%, and 3.3V at +3/–5%	1.710	–	3.400	V
	PSIO bank 5## power supplies Includes V _{CCO} of 1.8V, 2.5V at ±5%, and 3.3V at +3/–5%	1.710	–	3.400	V

Table 3: Recommended Operating Conditions (cont'd)

Symbol	Description ^{1, 2, 3}	Min	Typ	Max	Units
V _{CC_PMC} ¹⁰	PMC primary power supply, low (L) voltage	0.676	0.700	0.724	V
	PMC primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	PMC primary power supply, high (H) voltage	0.854	0.880	0.906	V
	PMC primary power supply, overdrive voltage for higher PMC performance at specific speed grades. See Available Speed Grades and Operating Voltages .	0.854	0.880	0.906	V
V _{CC_PSFP}	PS full-power domain power supply, low (L) voltage	0.676	0.700	0.724	V
	PS full-power domain power supply, mid (M) voltage	0.775	0.800	0.825	V
	PS full-power domain power supply, high (H) voltage	0.854	0.880	0.906	V
	PS full-power domain power supply, overdrive voltage for higher PS performance at specific speed grades. See Available Speed Grades and Operating Voltages .	0.854	0.880	0.906	V
V _{CC_PSLP}	PS low-power domain power supply, low (L) voltage	0.676	0.700	0.724	V
	PS low-power domain power supply, mid (M) voltage	0.775	0.800	0.825	V
	PS low-power domain power supply, high (H) voltage	0.854	0.880	0.906	V
	PS low-power domain power supply, overdrive voltage for higher PS performance at specific speed grades. See Available Speed Grades and Operating Voltages .	0.854	0.880	0.906	V
V _{CC_RAM}	PL RAM and clocking network power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	PL RAM and clocking network power supply, high (H) voltage	0.854	0.880	0.906	V
V _{CC_SOC} ⁸	Network on Chip (NoC) and integrated DDR memory controller power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	NoC and integrated DDR memory controller power supply, high (H) voltage	0.854	0.880	0.906	V
V _{GT_Y_AVCC} ¹¹	GT _Y transceiver primary analog power supply	0.854	0.880	0.906	V
V _{GT_P_AVCC} ¹¹	GT _P transceiver primary analog power supply (E or I temperature range)	0.892	0.920	0.948	V
	GT _P transceiver primary analog power supply (M or Q temperature range)	0.854	0.880	0.906	V
V _{GT_M_AVCC} ¹¹	GT _M transceiver primary analog power supply (E or I temperature range)	0.892	0.920	0.948	V
	GT _M transceiver primary analog power supply (M or Q temperature range)	0.854	0.880	0.906	V
V _{GT_Y_AVCCAUX} ¹¹ V _{GT_P_AVCCAUX} ¹¹ V _{GT_M_AVCCAUX} ¹¹	GT _Y and GT _P (or GT _M) transceiver auxiliary analog (PLL) power supply	1.455	1.500	1.545	V
V _{GT_Y_AVTT} ¹¹ V _{GT_P_AVTT} ¹¹ V _{GT_M_AVTT} ¹¹	GT _Y and GT _P (or GT _M) transceiver termination power supply	1.164	1.200	1.236	V
V _{GT_Y_AVTTRCAL} ¹¹ V _{GT_P_AVTTRCAL} ¹¹ V _{GT_M_AVTTRCAL} ¹¹	GT _Y and GT _P (or GT _M) transceiver analog resistor calibration power supply	1.164	1.200	1.236	V
V _{IN} ^{12, 13}	I/O input voltage for PSIO, HDIO, and XPIO banks	-0.200	-	V _{CCO} + 0.200	V
	I/O input voltage for X5IO banks	-0.100	-	V _{CCO} + 0.250	V
I _{IN} ¹⁴	Maximum current through any PL, PMC, or PS pin in a powered or unpowered bank when forward biasing the clamp diode	-	-	10	mA

Table 3: Recommended Operating Conditions (cont'd)

Symbol	Description ^{1, 2, 3}	Min	Typ	Max	Units
T_j ¹⁵	Junction temperature operating range for extended (E) temperature devices ¹⁶	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices ¹⁶	–40	–	100	°C
	Junction temperature operating range for military (M) temperature devices ¹⁶	–55	–	125	°C
	Junction temperature operating range for eFUSE programming	–40	–	125	°C

Notes:

- All voltages are relative to GND and in relation to the BGA package ball.
- For the design of the power distribution system consult the *Versal Adaptive SoC PCB Design User Guide* (UG863) and Power Design Manager (PDM) tool (download at www.amd.com/power).
- Each voltage listed requires decoupling as described in the *Versal Adaptive SoC PCB Design User Guide* (UG863). Refer to the Power Design Manager (PDM) tool (download at www.amd.com/power) for design specific decoupling recommendations.
- V_{CCAUX_SMON} must be connected to V_{CCAUX_PMC} . See *Versal Adaptive SoC System Monitor Architecture Manual* (AM006) for V_{CCAUX_SMON} information and filter considerations.
- When the battery-backed RAM and the real-time clock are not used, connect to GND.
- V_{CC_FUSE} must be within the recommended operating conditions during eFUSE programming. When V_{CC_FUSE} is not used, connect to GND.
- The -2LLI devices require the V_{CCINT} supply to power on at 0.725V and then use the PMC dynamic voltage scaling (DVS) drivers to change the voltage of the V_{CCINT} voltage regulator (using the I2C/PMBus) to 0.700V when the device temperature rises above 25°C or to 0.725V when the device temperature falls below 10°C.
- V_{CC_IO} must be connected to V_{CC_SOC} .
- For X5IO, XPIO, and HDIO operation, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010). PSIO includes PMC dedicated I/O banks, PMC MIO banks, and LPD MIO banks. For PSIO operation, see the *Versal Adaptive SoC Technical Reference Manual* (AM011).
- The physical unclonable function (PUF) is only supported when using a nominal V_{CC_PMC} of 0.70V on certain Versal devices. Refer to the *Versal Adaptive SoC Security Manual* (UG1508) in the [Design Security Lounge](#) for a list of affected devices and for detailed information on PUF usage, including a V_{CC_PMC} 0.70V solution for mid, high, and overdrive. When using a V_{CC_PMC} 0.70V solution, performance is reduced for functions based on the V_{CC_PMC} . The PUF is not supported in -3H devices.
- Each voltage listed requires filtering as described in the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002) or the *Versal Adaptive SoC GTM Transceivers Architecture Manual* (AM017). The noise beyond the recommended operating conditions at the power pins must not exceed 10 mVpp over the band from 10 kHz to 80 MHz.
- The lower absolute voltage specification always applies.
- In XPIO or X5IO banks, V_{IN} overshoot above V_{CCO} and undershoot below GND can reduce the performance of V_{REF} -based receivers within the same nibble.
- A total of 200 mA per bank should not be exceeded.
- Junction temperature specification is in relation to the absolute value reported by the PMC system monitor.
- Devices labeled with the -2E speed/temperature grade and all industrial (I) temperature grade devices can operate for a limited time at a junction temperature between 100°C and 110°C based on the temperature read from the SYSMON. Timing parameters adhere to the same speed file at up to 110°C as they do at up to 100°C. Operation up to $T_j = 110^\circ\text{C}$ is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of the device lifetime. For more information on excursion temperature see *Extending the Thermal Solution by Utilizing Excursion Temperatures* (WP517).

Available Speed Grades and Operating Voltages

The following table describes the speed grades per device and operating supply voltages for the PMC, PS low power, PS full power, and PL domains. For more information on selecting devices and speed grades, see the *Versal Architecture and Product Data Sheet: Overview* (DS950).

Table 4: Available Speed Grades and Operating Voltages

Speed Grade	Mode ^{1, 2}	Vivado Design Tools Device Code ³	V _{CCINT}	V _{CC_PSLP}	V _{CC_PSFP}	V _{CC_CPM5}	V _{CC_PMC} ⁴	V _{CC_SOC} and V _{CC_IO}	V _{CC_RAM}	Units
-3HSE	Standard	-3HP-e-S	0.88	0.88	0.88	0.88	0.88	0.88	0.88	V
-2HSI	Standard	-2HP-i-S	0.88	0.88	0.88	0.88	0.88	0.88	0.88	V
-2MSE	Standard	-2MP-e-S	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
	Overdrive	-2MHP-e-S	0.80	0.88	0.88	0.88	0.88	0.80	0.80	V
-2MSI	Standard	-2MP-i-S	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
	Overdrive	-2MHP-i-S	0.80	0.88	0.88	0.88	0.88	0.80	0.80	V
-2MLE	Standard	-2MP-e-L	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
	Overdrive	-2MHP-e-L	0.80	0.88	0.88	0.88	0.88	0.80	0.80	V
-2MLI	Standard	-2MP-i-L	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
	Overdrive	-2MHP-i-L	0.80	0.88	0.88	0.88	0.88	0.80	0.80	V
-2LSE	Standard	-2LP-e-S	0.70	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	-2LHP-e-S	0.70	0.88	0.88	0.88	0.88	0.80	0.80	V
-2LLE	Standard	-2LP-e-L	0.70	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	-2LHP-e-L	0.70	0.88	0.88	0.88	0.88	0.80	0.80	V
-2LLI	Standard	-2LLI-i-L	0.725 ⁵	0.70	0.70	0.70	0.70	0.80	0.80	V
-1MSM	Standard	-1MM-m-S	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
-1MSI	Standard	-1MP-i-S	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
-1MLI	Standard	-1MP-i-L	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
-1MSE	Standard	-1MP-e-S	0.80	0.80	0.80	0.80	0.80	0.80	0.80	V
-1LSI	Standard	-1LP-i-S	0.70	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	-1LHP-i-S	0.70	0.88	0.88	0.88	0.88	0.80	0.80	V
-1LLI	Standard	-1LP-i-L	0.70	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	-1LHP-i-L	0.70	0.88	0.88	0.88	0.88	0.80	0.80	V

Table 4: Available Speed Grades and Operating Voltages (cont'd)

Speed Grade	Mode ^{1, 2}	Vivado Design Tools Device Code ³	V _{CCINT}	V _{CC_PSLP}	V _{CC_PSPF}	V _{CC_CPM5}	V _{CC_PMC} ⁴	V _{CC_SOC} and V _{CC_IO}	V _{CC_RAM}	Units
-1LSE	Standard	-1LP-e-S	0.70	0.70	0.70	0.70	0.70	0.80	0.80	V

Notes:

1. The -2LLE, -2LSE, -2MLE, -2MSE, -2MLI, and -2MSI devices, that have a CPM5, allow dual-voltage operation of the PMC, PS, and CPM5 supplies in overdrive mode (0.88V) or standard drive mode (0.70V/0.80V).
2. -1LSI and -1LLI devices allow dual-voltage operation of the PMC, PS, and (when applicable) CPM5 supplies in overdrive mode (0.88V) or standard drive mode (0.70V).
3. The specified portion of the Vivado design tools device selection code includes speed grade (-3, -2, -1), operating voltages (HP, MP, MHP, MM, LP, LHP, LLI), temperature grade, (-i, -e, -m), and maximum static power screen (-S, -L).
4. The physical unclonable function (PUF) is only supported when using a nominal V_{CC_PMC} of 0.70V on certain Versal devices. Refer to the *Versal Adaptive SoC Security Manual* (UG1508) in the [Design Security Lounge](#) for a list of affected devices and for detailed information on PUF usage, including a V_{CC_PMC} 0.70V solution for mid, high, and overdrive. When using a V_{CC_PMC} 0.70V solution, performance is reduced for functions based on the V_{CC_PMC}. The PUF is not supported in -3H devices.
5. The -2LLI devices require the V_{CCINT} supply to power on at 0.725V and then use the PMC dynamic voltage scaling (DVS) drivers to change the voltage of the V_{CCINT} voltage regulator (using the I2C/PMBus) to 0.700V when the device temperature rises above 25°C or to 0.725V when the device temperature falls below 10°C. For more DVS implementation details, see *Temperature Dependent Dynamic Voltage Scaling Implementation* (XAPP1394).

DC Characteristics Over Recommended Operating Conditions

Table 5: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ¹	Max	Units
$C_{IN}^{2,3}$	HDIO and PSIO die input capacitance at the pad	–	–	3.50	pF
	XPIO die input capacitance at the pad	–	–	1.75	pF
	X5IO die input capacitance at the pad	–	–	1.50	pF
I_L	For XC devices, HDIO, XPIO, and PSIO input or output leakage current per pin (sample-tested)	–	–	15	μA
	For XQ devices, HDIO, XPIO, and PSIO input or output leakage current per pin (sample-tested)	–	–	20	μA
	X5IO input or output leakage current per pin (sample-tested)	–	–	100	μA
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 3.3V$	60	–	200	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 2.5V$	50	–	169	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.8V$	29	–	120	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.5V$	30	–	120	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.2V$	10	–	100	μA
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$	60	–	200	μA
	Pad pull-down (when selected) at $V_{IN} = 1.8V$	29	–	120	μA
I_{CC_FUSE}	V_{CC_FUSE} supply current during eFUSE programming	–	–	165	mA
Battery Supply Current					
$I_{CC_BATT}^{3,4}$	Battery supply current at $V_{CC_BATT} = 1.20V$, RTC disabled	–	–	160	nA
	Battery supply current at $V_{CC_BATT} = 1.50V$, RTC disabled	–	–	320	nA
	Battery supply current at $V_{CC_BATT} = 1.20V$, RTC enabled	–	–	1360	nA
	Battery supply current at $V_{CC_BATT} = 1.50V$, RTC enabled	–	–	1930	nA
Calibrated programmable on-die termination (DCI) in XPIO and X5IO banks⁵ (measured per JEDEC specification)					
R^7	Thevenin equivalent resistance of programmable input termination where x = target impedance of 40, 48, 60, 120, or 240	–20% ⁶	ODT = RTT_x	+20% ⁶	Ω
Uncalibrated programmable on-die termination in HDIO banks (measured per JEDEC specification)					
R^7	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
Differential Termination					
Differential termination	Programmable differential termination (TERM_100) for XPIO and X5IO banks	–35%	100	+35%	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Battery-backed RAM (BBRAM) is always enabled and included in I_{CC_BATT} .
- VR resistor tolerance is (240Ω ±1%).
- The tolerance limits are specified after calibration with stable voltage and temperature.
- On-die input termination resistance, for more information see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HDIO and PSIO Banks

AC Voltage Overshoot ¹	% of UI ² at -40°C to 100°C ³	AC Voltage Undershoot ¹	% of UI ² at -40°C to 100°C ³
$V_{CCO} + 0.20$	100%	-0.20	100%
$V_{CCO} + 0.25$	100%	-0.25	75%
$V_{CCO} + 0.30$	75%	-0.30	75%
$V_{CCO} + 0.35$	75%	-0.35	75%
$V_{CCO} + 0.40$	75%	-0.40	60%
$V_{CCO} + 0.45$	50%	-0.45	30%
$V_{CCO} + 0.50$	30%	-0.50	0%
$V_{CCO} + 0.55$	20%	-0.55	0%
$V_{CCO} + 0.60$	20%	-0.60	0%
$V_{CCO} + 0.65$	10%	-0.65	0%
$V_{CCO} + 0.70$	10%	-0.70	0%
$V_{CCO} + 0.75$	10%	-0.75	0%
$V_{CCO} + 0.80$	10%	-0.80	0%
$V_{CCO} + 0.85$	8%	-0.85	0%
$V_{CCO} + 0.90$	6%	-0.90	0%
$V_{CCO} + 0.95$	2%	-0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. For the -1MSM devices, the temperature limits are -55°C to 125°C.

Table 7: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for XPIO Banks

AC Voltage Overshoot ¹	% of UI ² at -40°C to 100°C ⁴	AC Voltage Undershoot ¹	% of UI ² at -40°C to 100°C ⁴
$V_{CCO} + 0.20$	100%	-0.20	100%
$V_{CCO} + 0.25$	100%	-0.25	100%
$V_{CCO} + 0.30$	100%	-0.30	10%
$V_{CCO} + 0.35$	100%	-0.35	0%
$V_{CCO} + 0.40$	96%	-0.40	0%
$V_{CCO} + 0.45$	2%	-0.45	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. In XPIO banks, V_{IN} overshoot above V_{CCO} and undershoot below GND can reduce the performance of V_{REF} -based receivers within the same nibble.
4. For the -1MSM devices, the temperature limits are -55°C to 125°C.

Table 8: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for X5IO Banks

AC Voltage Overshoot ¹	% of UI ² at -40°C to 100°C	AC Voltage Undershoot ¹	% of UI ² at -40°C to 100°C
$V_{CCO} + 0.10$	100%	-0.10	100%
$V_{CCO} + 0.15$	100%	-0.15	40%
$V_{CCO} + 0.20$	100%	-0.20	10%
$V_{CCO} + 0.25$	100%	-0.25	0%
$V_{CCO} + 0.30$	70%	-0.30	0%
$V_{CCO} + 0.35$	30%	-0.35	0%
$V_{CCO} + 0.40$	16%	-0.40	0%
$V_{CCO} + 0.45$	10%	-0.45	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.
3. In X5IO banks, V_{IN} overshoot above V_{CCO} and undershoot below GND can reduce the performance of V_{REF} -based receivers within the same nibble.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PSIO Levels

Table 9: PSIO DC Input and Output Levels

I/O Standard ^{1, 2}	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 3	Note 3
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	$V_{CCO} - 0.400$	Note 3	Note 3

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC Technical Reference Manual* (AM011).
3. Supported drive strengths of 4, 8, or 12 mA.

SelectIO Levels

Table 10: SelectIO DC Input and Output Levels For HDIO Banks

I/O Standard ^{1, 2}	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I_18	-0.300	50% $V_{CCO} - 0.100$	50% $V_{CCO} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 3	Note 3
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVTTL	-0.300	0.800	2.000	3.400	0.400	2.400	Note 3	Note 3
SSTL18_I	-0.300	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.0	-8.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).
3. Supported drive strengths of 4, 8, or 12 mA in HDIO banks.

Table 11: SelectIO DC Input and Output Levels for XPIO Banks

I/O Standard ^{1, 2, 3}	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$50\% V_{CCO} - 0.100$	$50\% V_{CCO} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	5.8	-5.8
HSTL_I_12	-0.300	$50\% V_{CCO} - 0.080$	$50\% V_{CCO} + 0.080$	$V_{CCO} + 0.300$	$25\% V_{CCO}$	$75\% V_{CCO}$	4.1	-4.1
HSUL_12	-0.300	$50\% V_{CCO} - 0.130$	$50\% V_{CCO} + 0.130$	$V_{CCO} + 0.300$	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	-0.1
LVC MOS12	-0.300	$35\% V_{CCO}$	$65\% V_{CCO}$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS15	-0.300	$35\% V_{CCO}$	$65\% V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVDCI_15	-0.300	$35\% V_{CCO}$	$65\% V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	7.0	-7.0
SSTL12	-0.300	$50\% V_{CCO} - 0.100$	$50\% V_{CCO} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.0	-8.0
SSTL135	-0.300	$50\% V_{CCO} - 0.090$	$50\% V_{CCO} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	9.0	-9.0
SSTL15	-0.300	$50\% V_{CCO} - 0.100$	$50\% V_{CCO} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	10.0	-10.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).
3. POD10 and POD12 DC input and output levels are shown in Table 12, Table 17, and Table 18.
4. Supported drive strengths of 2, 4, 6, or 8 mA in XPIO banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in XPIO banks.

Table 12: DC Input Levels for Single-ended POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards

I/O Standard ^{1, 2}	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	-0.300	$70\% V_{CCO} - 0.068$	$70\% V_{CCO} + 0.068$	$V_{CCO} + 0.300$
POD12	-0.300	$70\% V_{CCO} - 0.068$	$70\% V_{CCO} + 0.068$	$V_{CCO} + 0.300$
LVSTL06_12	-0.300	$V_{CCO}/8 - 0.100$	$V_{CCO}/8 + 0.100$	$V_{CCO} + 0.300$
LVSTL_11	-0.300	$V_{CCO}/6 - 0.100$	$V_{CCO}/6 + 0.100$	$V_{CCO} + 0.300$

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).

Table 13: Differential SelectIO DC Input and Output Levels for MIPI_DPHY

I/O Standard	V _{ICM} (V) ¹			V _{ID} (V) ²			V _{ILHS} ³	V _{IHHS} ³	V _{OCM} (V) ⁴			V _{OD} (V) ⁵		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
MIPI_DPHY for operation <1.5 GB/s ⁷	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270
MIPI_DPHY for operation at >1.5G GB/s ⁷	0.070	–	0.330	0.040	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS15 is specified in Table 26.
7. High-speed option for MIPI_DPHY. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 14: Complementary Differential SelectIO DC Input and Output Levels for HDIO Banks

I/O Standard	V _{ICM} (V) ¹			V _{ID} (V) ²		V _{OL} (V) ³	V _{OH} (V) ⁴	I _{OL}	I _{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V _{CCO} – 0.400	8.0	–8.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V _{CCO} /2) – 0.47	(V _{CCO} /2) + 0.47	8.0	–8.0
LVDS_25	0.300	1.200	1.425	0.100	0.600	–	–	–	–
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	–	–	–
LVPECL	0.300	1.200	1.425	0.100	0.600	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	0.450	–	–	–	–

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 15: Complementary Differential SelectIO DC Input and Output Levels for XPIO Banks

I/O Standard ¹	V _{ICM} (V) ²			V _{ID} (V) ³		V _{OL} (V) ⁴	V _{OH} (V) ⁵	I _{OL}	I _{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	0.400	V _{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V _{CCO}	V _{CCO} /2	0.600 x V _{CCO}	0.100	–	0.250 x V _{CCO}	0.750 x V _{CCO}	4.1	–4.1
DIFF_HSUL_12	(V _{CCO} /2) – 0.120	V _{CCO} /2	(V _{CCO} /2) + 0.120	0.100	–	20% V _{CCO}	80% V _{CCO}	0.1	–0.1
DIFF_SSTL12	(V _{CCO} /2) – 0.150	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	8.0	–8.0
DIFF_SSTL135	(V _{CCO} /2) – 0.150	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	9.0	–9.0
DIFF_SSTL15	(V _{CCO} /2) – 0.175	V _{CCO} /2	(V _{CCO} /2) + 0.175	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	10.0	–10.0

Notes:

1. DIFF_POD10 and DIFF_POD12 XPIO bank specifications are shown in [Table 16](#), [Table 17](#), and [Table 18](#).
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 16: DC Input Levels for Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards

I/O Standard ^{1, 2}	V _{ICM} (V)			V _{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.630	0.700	0.770	0.140	–
DIFF_POD12	0.756	0.840	0.924	0.160	–
DIFF_LVSTL06_12	0.143	0.150	0.157	0.140	–
DIFF_LVSTL_11	0.174	0.183	0.193	0.140	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* ([AM010](#)).

Table 17: DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards

I/O Standard	Symbol	Description ^{1, 2, 3}	V _{OUT}	Min	Typ	Max	Units
POD10 and POD12	R _{OL}	Pull-down resistance	V _{OM_DC} (as described in Table 18)	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OM_DC} (as described in Table 18)	32	40	48	Ω
LVSTL06_12	R _{OL}	Pull-down resistance	V _{OCM_DC_LOW}	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OCM_DC_HIGH}	32	40	48	Ω
LVSTL_11 (V _{OH} = 50)	R _{OL}	Pull-down resistance	V _{OM_DC} (as described in Table 18)	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OM_DC} (as described in Table 18)	32	40	48	Ω

Notes:

1. Tested according to relevant specifications.
2. The tolerance limits are specified after calibration with stable voltage and temperature.
3. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* ([AM010](#)).

Table 18: Definitions for DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards

I/O Standard	Symbol	Description	All Speed Grades	Units
POD10 and POD12	V _{OM_DC}	DC output mid measurement level (for IV curve linearity)	0.8 x V _{CCO}	V
LVSTL_11 (V _{OH} = 50)	V _{OM_DC}	DC output mid measurement level (for IV curve linearity)	V _{CCO} /2	V
LVSTL06_12	V _{OCM_DC_LOW}	DC output mid measurement level (for IV curve linearity), drive logic Low	V _{CCO} /2	V
	V _{OCM_DC_HIGH}	DC output measurement level (for IV curve linearity), drive logic High	V _{CCO} /2 to V _{CCO} /4	V

SelectIO Levels for X5IO Banks

Table 19: SelectIO DC Input and Output Levels for X5IO Banks

I/O Standard ^{1, 2, 3}	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I_12	-0.100	50% V _{CCO} - 0.080	50% V _{CCO} + 0.080	V _{CCO}	25% V _{CCO}	75% V _{CCO}	4.1	-4.1
HSUL_12	-0.100	50% V _{CCO} - 0.130	50% V _{CCO} + 0.130	V _{CCO}	20% V _{CCO}	80% V _{CCO}	0.1	-0.1
LVC MOS10	-0.100	35% V _{CCO}	65% V _{CCO}	V _{CCO}	0.400	V _{CCO} - 0.400	Note 4	Note 4
LVC MOS11	-0.100	35% V _{CCO}	65% V _{CCO}	V _{CCO}	0.400	V _{CCO} - 0.400	Note 4	Note 4
LVC MOS12	-0.100	35% V _{CCO}	65% V _{CCO}	V _{CCO}	0.400	V _{CCO} - 0.400	Note 4	Note 4
SSTL10	-0.100	50% V _{CCO} - 0.130	50% V _{CCO} + 0.130	V _{CCO}	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	6.0	-6.0
SSTL11	-0.100	50% V _{CCO} - 0.130	50% V _{CCO} + 0.130	V _{CCO}	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	7.0	-7.0
SSTL12	-0.100	50% V _{CCO} - 0.100	50% V _{CCO} + 0.100	V _{CCO}	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	8.0	-8.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).
3. POD10, POD11, and POD12 DC input and output levels are shown in Table 20, Table 24, and Table 25.
4. Supported drive strengths of 2, 4, 6, or 8 mA in X5IO banks.

Table 20: DC Input Levels for Single-ended POD10, POD11, POD12, LVSTL05_10, LVSTL06_12, and LVSTL_11 I/O Standards for X5IO Banks

I/O Standard ^{1, 3}	V _{IL}		V _{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	-0.100	70% V _{CCO} - 0.068	70% V _{CCO} + 0.068	V _{CCO}
POD11	-0.100	70% V _{CCO} - 0.068	70% V _{CCO} + 0.068	V _{CCO}
POD12	-0.100	70% V _{CCO} - 0.068	70% V _{CCO} + 0.068	V _{CCO}
LVSTL05_10	-0.100	V _{CCO} /8 - 0.100	V _{CCO} /8 + 0.100	V _{CCO}
LVSTL06_12	-0.100	V _{CCO} /8 - 0.100	V _{CCO} /8 + 0.100	V _{CCO}
LVSTL_11	-0.100	V _{CCO} /6 - 0.100	V _{CCO} /6 + 0.100	V _{CCO}

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).

Table 21: Differential SelectIO DC Input and Output Levels for MIPI_DPHY and MIPI_CPHY for X5IO Banks

I/O Standard	V_{ICM} (V) ¹			V_{ID} (V) ²			V_{ILHS} ³	V_{IHHS} ³	V_{OCM} (V) ⁴			V_{OD} (V) ⁵		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
MIPI_DPHY for operation <1.5 GB/s ⁶	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270
MIPI_DPHY for operation at >1.5G GB/s ⁶	0.070	–	0.330	0.040	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270
MIPI_CPHY	0.095	–	0.390	0.040	–	–	–0.040	0.535	0.175	0.225 – 0.250	0.310	0.090 ⁷	–	0.300 ⁸

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \bar{Q}$).
- High-speed option for MIPI_DPHY. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.
- Minimum for VOD weak.
- Maximum for VOD strong.

Table 22: Complementary Differential SelectIO DC Input and Output Levels for X5IO Banks

I/O Standard ¹	V_{ICM} (V) ²			V_{ID} (V) ³		V_{OL} (V) ⁴	V_{OH} (V) ⁵	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL10	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	6.0	–6.0
DIFF_SSTL11	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	7.0	–7.0
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0

Notes:

- DIFF_POD10, DIFF_POD11, and DIFF_POD12 X5IO bank specifications are shown in [Table 23](#), [Table 24](#), and [Table 25](#).
- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage.
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

Table 23: DC Input Levels for Differential POD10, POD11, POD12, LVSTL05_10, LVSTL06_12, and LVSTL_11 I/O Standards for X5IO Banks

I/O Standard ^{1, 2}	V _{ICM} (V)			V _{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.630	0.700	0.770	0.140	–
DIFF_POD11	0.693	0.77	0.847	0.150	–
DIFF_POD12	0.756	0.840	0.924	0.160	–
DIFF_LVSTL05_10	0.113	0.125	0.138	0.150	–
DIFF_LVSTL06_12	0.143	0.150	0.157	0.140	–
DIFF_LVSTL_11	0.174	0.183	0.193	0.140	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).

Table 24: DC Output Levels for Single-ended and Differential POD10, POD11, POD12, LVSTL05_10, LVSTL06_12, and LVSTL_11 I/O Standards for X5IO Banks

I/O Standard	Symbol	Description ^{1, 2, 3}	V _{OUT}	Min	Typ	Max	Units
POD10, POD11, POD12	R _{OL}	Pull-down resistance	V _{OM_DC} (as described in Table 25)	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OM_DC} (as described in Table 25)	32	40	48	Ω
LVSTL05_10	R _{OL}	Pull-down resistance	V _{OCM_DC_LOW}	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OCM_DC_HIGH}	32	40	48	Ω
LVSTL06_12	R _{OL}	Pull-down resistance	V _{OCM_DC_LOW}	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OCM_DC_HIGH}	32	40	48	Ω
LVSTL_11	R _{OL}	Pull-down resistance	V _{OM_DC} (as described in Table 25)	32	40	48	Ω
	R _{OH}	Pull-up resistance	V _{OM_DC} (as described in Table 25)	32	40	48	Ω

Notes:

1. Tested according to relevant specifications.
2. The tolerance limits are specified after calibration with stable voltage and temperature.
3. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010).

Table 25: Definitions for DC Output Levels for Single-ended and Differential POD10, POD 11, POD12, LVSTL05_10, LVSTL06_12, and LVSTL_11 I/O Standards for X5IO Banks

I/O Standard	Symbol	Description	All Speed Grades	Units
POD10, POD11, POD12	V _{OM_DC}	DC output mid measurement level (for IV curve linearity)	0.8 × V _{CCO}	V
LVSTL_11	V _{OM_DC}	DC output mid measurement level (for IV curve linearity)	V _{CCO} /3	V
LVSTL05_10	V _{OM_DC}	DC output mid measurement level (for IV curve linearity)	V _{CCO} /4	V
LVSTL06_12	V _{OCM_DC}	DC output mid measurement level (for IV curve linearity)	V _{CCO} /4	V

LVDS DC Specifications (LVDS15)

The LVDS15 standard is available in the XPIO banks. See the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010) for more information.

Table 26: LVDS15 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} ¹	Supply voltage		1.425	1.500	1.575	V
V_{ODIFF} ²	Differential output voltage: (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
V_{OCM} ²	Output common-mode voltage	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	1.000	1.20	1.320	V
V_{IDIFF} ³	Differential input voltage: (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High		100	350	600 ³	mV
V_{ICM_DC} ⁴	Input common-mode voltage (DC coupling)		0.300	1.200	1.320	V
V_{ICM_AC} ⁵	Input common-mode voltage (AC coupling)		200	–	330	mV

Notes:

1. In XPIO banks, when LVDS15 is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 3) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. AC coupling with external bias and external differential termination with EQUALIZATION settings enabled. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, or EQ_LEVEL4, any setting except EQ_NONE.

LVDS DC Specifications (LVDS12)

The LVDS12 standards are available in the X5IO banks. See the *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010) for more information.

Table 27: LVDS12 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} ¹	Supply voltage		1.14	1.20	1.26	V
V_{ODIFF} ²	Differential output voltage: (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	150	222	300	mV
V_{OCM} ²	Output common-mode voltage	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	0.75	–	1.1	V
V_{IDIFF} ³	Differential input voltage: (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High		100	350	600	mV
V_{ICM_DC} ^{3,4}	Input common-mode voltage (DC coupling)		0.300	–	1.15	V
V_{ICM_AC} ⁵	Input common-mode voltage (AC coupling)		200	–	330	mV

Notes:

1. In X5IO banks, when LVDS12 is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 3) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Not all combinations of V_{IDIFF} and V_{ICM_DC} levels are compatible. The V_{IN} recommended operating voltage takes priority over the LVDS12 DC specification. The following equation illustrates the relationship: $V_{ICM_DC(MAX)} = V_{IN(MAX)} - V_{IDIFF}/2$.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. AC coupling with external bias and external differential termination with EQUALIZATION settings enabled. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, or EQ_LEVEL4, any setting except EQ_NONE.

Power Supply Requirements

Versal Prime devices are powered by multiple power supply pins that must use specific rail combinations and power sequences. Only some combinations and sequences are supported. The combinations depend upon the selected device, speed specification, and power management options. The required sequencing, power delivery options, and decoupling requirements based on design are found in the Power Design Manager (PDM) tool (download at www.amd.com/power). See also *Simplified Power Sequencing Application Note* (XAPP1375) for specific power sequencing methods.

Table 28: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T _{VCCAUX}	Ramp time from GND to 95% of V _{CCAUX}	0.2	40	ms
T _{VCCAUX_PMC}	Ramp time from GND to 95% of V _{CCAUX_PMC}	0.2	40	ms
T _{VCCAUX_SMON}	Ramp time from GND to 95% of V _{CCAUX_SMON}	0.2	40	ms
T _{VCC_CPM5}	Ramp time from GND to 95% of V _{CC_CPM5}	0.2	40	ms
T _{VCC_FUSE}	Ramp time from GND to 95% of V _{CC_FUSE}	0.2	40	ms
T _{VCCINT}	Ramp time from GND to 95% of V _{CCINT}	0.2	40	ms
T _{VCCINT_GT}	Ramp time from GND to 95% of V _{CCINT_GT}	0.2	40	ms
T _{VCC_IO_VCC_SOC}	Ramp time from GND to 95% of V _{CC_IO} and V _{CC_SOC}	0.2	40	ms
T _{VCCO}	Ramp time from GND to 95% of V _{CCO}	0.2	40	ms
T _{VCC_PMC}	Ramp time from GND to 95% of V _{CC_PMC}	0.2	40	ms
T _{VCC_PSF}	Ramp time from GND to 95% of V _{CC_PSF}	0.2	40	ms
T _{VCC_PSLP}	Ramp time from GND to 95% of V _{CC_PSLP}	0.2	40	ms
T _{VCC_RAM}	Ramp time from GND to 95% of V _{CC_RAM}	0.2	40	ms
T _{GTY_AVCC}	Ramp time from GND to 95% of V _{GTY_AVCC}	0.2	40	ms
T _{GTY_AVCCAUX}	Ramp time from GND to 95% of V _{GTY_AVCCAUX}	0.2	40	ms
T _{GTY_AVTT}	Ramp time from GND to 95% of V _{GTY_AVTT}	0.2	40	ms
T _{GTYP_AVCC}	Ramp time from GND to 95% of V _{GTYP_AVCC}	0.2	40	ms
T _{GTYP_AVCCAUX}	Ramp time from GND to 95% of V _{GTYP_AVCCAUX}	0.2	40	ms
T _{GTYP_AVTT}	Ramp time from GND to 95% of V _{GTYP_AVTT}	0.2	40	ms
T _{GTM_AVCC}	Ramp time from GND to 95% of V _{GTM_AVCC}	0.2	40	ms
T _{GTM_AVCCAUX}	Ramp time from GND to 95% of V _{GTM_AVCCAUX}	0.2	40	ms
T _{GTM_AVTT}	Ramp time from GND to 95% of V _{GTM_AVTT}	0.2	40	ms

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the AMD Vivado™ Design Suite as outlined in the following table.

Table 29: Speed Specification Version by Device

2024.2.2	Device
2.13	XCVM1802, XQVM1802
2.07	XCVM2502
2.06	XCVM1502, XQVM1502
2.04	XCVM1302, XCVM1402, XQVM1402
2.03	XCVM1102, XQVM1102, XCVM2202, XCVM2302, VCVM2902
2.02	XCVM2152

Switching characteristics are specified on a per-speed-grade basis and can be designated as evaluation, engineering sample, pre-production, or production. Each designation is defined as follows:

- **Evaluation Product Specification:** These specifications are used for architecture evaluation only. They cannot be used for timing closure.
- **Engineering Sample Product Specification:** These specifications are based on simulations only and are typically available soon after dice design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Pre-production Product Specification:** These specifications are based on almost complete silicon characterization. Dice and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to engineering sample (ES) data.
- **Production Product Specification:** These specifications are released once enough production silicon of a particular dice family member has been characterized to provide full correlation between specifications and dices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Versal Prime devices.

Speed Grade Designations

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. The following table correlates the current status of the Versal Prime device on a per speed grade basis. See [Table 4: Available Speed Grades and Operating Voltages](#) for operating voltages listed by speed grade.

Table 30: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, Static Screen, and V_{CCINT} Operating Voltages			
	Evaluation	Engineering Sample	Pre-production	Production
XCVM1102				-2HSI ($V_{CCINT} = 0.88V$) -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -2LLI ($V_{CCINT} = 0.725V$) -2LSE, -2LLE ($V_{CCINT} = 0.70V$) -1MSE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$) -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)
XQVM1102				-2MSI ($V_{CCINT} = 0.80V$) -1MSM ($V_{CCINT} = 0.80V$) -1MSI ($V_{CCINT} = 0.80V$) -1LSI ($V_{CCINT} = 0.70V$)
XCVM1302				-2HSI ($V_{CCINT} = 0.88V$) -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -2LSE, -2LLE ($V_{CCINT} = 0.70V$) -2LLI ($V_{CCINT} = 0.725V$) -1MSE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$) -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)
XCVM1402				-2HSI ($V_{CCINT} = 0.88V$) -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -2LSE, -2LLE ($V_{CCINT} = 0.725V$) -2LLI ($V_{CCINT} = 0.725V$) -1MSE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$) -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)
XQVM1402				-2MSI ($V_{CCINT} = 0.80V$) -1MSI, -1MSM ($V_{CCINT} = 0.80V$) -1LSI ($V_{CCINT} = 0.70V$)
XCVM1502				-2HSI ($V_{CCINT} = 0.88V$) -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -2LSE, -2LLE ($V_{CCINT} = 0.70V$) -2LLI ($V_{CCINT} = 0.725V$) -1MSE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$) -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)
XQVM1502				-2MSI ($V_{CCINT} = 0.80V$) -1MSM, -1MSI ($V_{CCINT} = 0.80V$) -1LSI ($V_{CCINT} = 0.70V$)
XCVM1802				-2HSI ($V_{CCINT} = 0.88V$) -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -2LSE, -2LLE ($V_{CCINT} = 0.70V$) -2LLI ($V_{CCINT} = 0.725V$) -1MSE, -1MLE, -1MLI ($V_{CCINT} = 0.80V$) -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)

Table 30: Speed Grade Designations by Device (cont'd)

Device	Speed Grade, Temperature Ranges, Static Screen, and V _{CCINT} Operating Voltages			
	Evaluation	Engineering Sample	Pre-production	Production
XQVM1802				-2MSI (V _{CCINT} = 0.80V) -1MSM (V _{CCINT} = 0.80V) -1MSI (V _{CCINT} = 0.80V) -1LSI (V _{CCINT} = 0.70V)
XCVM2152				-2HSI (V _{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V _{CCINT} = 0.80V) -2LSE, -2LLE (V _{CCINT} = 0.70V) -1MSE, -1MSI, -1MLI (V _{CCINT} = 0.80V) -1LSE, -1LSI, -1LLI (V _{CCINT} = 0.70V)
XCVM2202				-2HSI (V _{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V _{CCINT} = 0.80V) -2LLI (V _{CCINT} = 0.725V) -2LSE, -2LLE (V _{CCINT} = 0.70V) -1MSE, -1MSI, -1MLI (V _{CCINT} = 0.80V) -1LSE, -1LSI, -1LLI (V _{CCINT} = 0.70V)
XCVM2302				-3HSE (V _{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V _{CCINT} = 0.80V) -1MSE, -1MSI, -1MLI (V _{CCINT} = 0.80V) -2LSE, -2LLE (V _{CCINT} = 0.70V) -1LSE, -1LSI, -1LLI (V _{CCINT} = 0.70V)
XCVM2502				-3HSE (V _{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V _{CCINT} = 0.80V) -2LSE, -2LLE (V _{CCINT} = 0.70V) -1MSE, -1MSI, -1MLI (V _{CCINT} = 0.80V) -1LSE, -1LSI, -1LLI (V _{CCINT} = 0.70V)
XCVM2902				-3HSE (V _{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V _{CCINT} = 0.80V) -1MSE, -1MSI, -1MLI (V _{CCINT} = 0.80V) -2LSE, -2LLE (V _{CCINT} = 0.70V) -1LSE, -1LSI, -1LLI (V _{CCINT} = 0.70V)

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (engineering sample, pre-production, production). Any labeling discrepancies are corrected in subsequent speed specification releases.

The following table lists the production released Versal Prime device, speed grade, and the minimum corresponding supported speed specification version and Vivado software versions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 31: Production Software and Speed Specification Release

Device	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT}) ^{1, 2}						
	0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)	
	-3	-2	-2	-1	-2LLI	-2LSE -2LLE	-1
XCVM1102	N/A	Vivado tools 2024.1 v2.01	Vivado tools 2023.2.1 v2.00		Vivado tools 2024.1 v2.01	Vivado tools 2023.2.1 v2.00	
XQVM1102	N/A	N/A	Vivado tools 2024.1.2 v2.03		N/A	N/A	Vivado tools 2024.1.2 v2.03
XCVM1302	N/A	Vivado tools 2022.1.1 v2.01	Vivado tools 2022.1 v2.00		Vivado tools 2023.2 v2.03	Vivado tools 2022.1 v2.00	Vivado tools 2022.1.1 v2.01 ³
XCVM1402	N/A	Vivado tools 2022.1.1 v2.01	Vivado tools 2022.1 v2.00		Vivado tools 2023.2 v2.03	Vivado tools 2022.1 v2.00	Vivado tools 2022.1.1 v2.01 ³
XQVM1402	N/A	N/A	Vivado tools 2022.2.1 v2.02		N/A	N/A	Vivado tools 2022.2.1 v2.02
XCVM1502	N/A	Vivado tools 2022.2.2 v2.02	Vivado tools 2022.2.1 v2.01		Vivado tools 2023.2 v2.04	Vivado tools 2022.2 v2.00	
XQVM1502	N/A	N/A	Vivado tools 2023.1.1 v2.03		N/A	N/A	Vivado tools 2023.1.1 v2.03
XCVM1802	N/A	Vivado tools 2022.1.1 v2.10	Vivado tools 2021.2.1 v2.05 ⁴		Vivado tools 2022.2.1 v2.11	Vivado tools 2021.2.1 v2.05 ^{4, 5}	
XQVM1802	N/A	N/A	Vivado tools 2022.1 v2.08		N/A	N/A	Vivado tools 2022.1 v2.08
XCVM2152	N/A	Vivado tools 2024.2.2 v2.02	Vivado tools 2024.2.1 v2.01		N/A	Vivado tools 2024.2.2 v2.02	
XCVM2202	N/A	Vivado tools 2023.2.2 v2.01	Vivado tools 2023.2.1 v2.00		Vivado tools 2024.1 v2.02	Vivado tools 2023.2.1 v2.00	
XCVM2302	Vivado tools 2023.1.1 v2.01	N/A	Vivado tools 2023.1.1 v2.01		N/A	Vivado tools 2023.1 v2.00	
XCVM2502	Vivado tools 2023.1.2 v2.01	N/A	Vivado tools 2023.1.2 v2.01		N/A	Vivado tools 2023.1.2 v2.01	
XCVM2902	Vivado tools 2023.1.1 v2.01	N/A	Vivado tools 2023.1.1 v2.01		N/A	Vivado tools 2023.1 v2.00	

Notes:

- See [Table 4: Available Speed Grades and Operating Voltages](#) for the complete list of operating voltages by speed grade and mode (standard or overdrive).
- Blank entries indicate a device and/or speed grade in engineering sample or pre-production status.
- The minimum production version of the Vivado tools is 2022.1.1 v2.01 for -1L (0.70V) designs using overdrive mode. The minimum production version of the Vivado tools is 2022.1 v2.00 for -1L (0.70V) designs using standard mode.
- The minimum production version of the Vivado tools is 2021.2.1 for designs using XPLL deskew (CLKIN_DESKEW, CLKFB_DESKEW) while CLKIN_DESKEW is connected to CLKIN, MMCM deskew (CLKIN_DESKEW, CLKFB_DESKEW), or CPM mode for PCI Express® with CPM4 to PL interfaces enabled. The minimum production version of the Vivado tools remains at 2020.3 v2.00 for 0.70V (L) devices and 2021.1 v2.01 for 0.80V (M) devices when the designs do not use XPLL deskew, MMCM deskew, or CPM mode for PCI Express with CPM4 to PL interfaces enabled.
- The minimum production version of the Vivado tools is 2022.2.1 for XCVM1802 devices with -2LLI speed grade.

Device Identification

The combined IDCODE and EXTENDED_IDCODE value provide the AMD device type identification as listed in the following table. For more information on the IDCODE and EXTENDED_IDCODE, see the *Versal Adaptive SoC Technical Reference Manual* ([AM011](#)).

Table 32: Device Identification

Device	IDCODE[31:0] (Hex) ¹	EXTENDED_IDCODE[31:0] (Binary) ²
XCVM1102	14CCA093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XQVM1102	14CCA093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1302	04C09093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1402	04C08093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XQVM1402	04C08093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1502	04C99093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XQVM1502	04C99093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1802	14CAA093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XQVM1802	14CAA093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2152	04C60093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2202	14CD4093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2302	04C24093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2502	14D01093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2902	04C23093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX

Notes:

1. An x at the location of the IDCODE[31:28] revision field is a placeholder until the production revision is defined.
2. Only the EXTENDED_IDCODE[27:14] bit values are relevant to device identification. The x in other bit positions indicate that they can be any value and must be ignored during device identification.

Processing System Performance Characteristics

Table 33: Processor Performance

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{APUMAX}	Maximum APU clock frequency where the operating voltage = V _{CC_PSEF}	1700	1650	1400 ¹	1300	1080 ¹	1000 ²	MHz
F _{RPUMAX}	Maximum RPU clock frequency where the operating voltage = V _{CC_PSLP}	800	800	600 ³	600	450 ³	400 ⁴	MHz

Notes:

1. The -2LLE, -2LSE, -2MLE, -2MSE, -2MLI, and -2MSI devices support an overdrive voltage V_{CC_PSF} = 0.88V where the maximum APU reference clock frequency is 1650 MHz.
2. The -1LLI and -1LSI devices support an overdrive voltage of V_{CC_PSF} = 0.88V where the maximum APU reference clock frequency is 1600 MHz.
3. The -2LLE, -2LSE, -2MLE, -2MSE, -2MLI, and -2MSI devices support an overdrive voltage V_{CC_PSLP} = 0.88V where the maximum RPU reference clock frequency is 800 MHz.
4. The -1LLI and -1LSI devices support an overdrive voltage of V_{CC_PSLP} = 0.88V where the maximum RPU reference clock frequency is 800 MHz.

Table 34: PS-PL Interface Performance

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{AXI_CLK}	Maximum AXI4 and ACE-LITE interface frequency	400	400	350	350	300	300	250 ¹	MHz
F _{PLAT_CLK}	Maximum PL address translation (AT) interface frequency	400	400	350	350	300	300	250 ¹	MHz
F _{PLATB_CLK}	Maximum PL-PS advanced trace bus (ATB) interface frequency	400	400	350	350	300	300	250 ¹	MHz
F _{PSACE_CLK}	Maximum AXI4 coherency extensions (ACE) interface frequency	400	400	350	350	300	300	250 ¹	MHz
F _{PSACP_CLK}	Maximum accelerator coherency port (ACP) interface frequency	400	400	350	350	300	300	250 ¹	MHz
F _{PSFCIDMA_CLK}	Maximum DMA flow-control interface (FCI) frequency	400	400	350	350	300	300	250 ¹	MHz

Notes:

- The -1LLI and -1LSI devices support an overdrive voltage ($V_{CC_PSFP} = 0.88V$ or $V_{CC_PSLP} = 0.88V$) where the maximum clock frequency is 280 MHz.

PS and PMC Switching Characteristics

Clocks and Reset

Table 35: Reference Clock Requirements

Symbol	Description	Min	Max	Units
F_{REFCLK}	Reference clock (REF_CLK) frequency	27	60	MHz
T_{RMSJ_REFCLK}	REF_CLK input RMS clock jitter	–	3	ps
T_{INPJ_REFCLK}	REF_CLK input period jitter (peak-to-peak) Number of clock cycles = 10,000	–	50	ps
T_{DC_REFCLK}	REF_CLK duty cycle	45	55	%
T_{REFCLK}	REF_CLK rise time (20%–80%) and fall time (80%–20%) at 3.3V	–	3	ns
	REF_CLK rise time (20%–80%) and fall time (80%–20%) at 1.8V or 2.5V	–	3.5	ns
	REF_CLK rise time (10%–90%) and fall time (90%–10%) at 3.3V	–	4	ns
	REF_CLK rise time (10%–90%) and fall time (90%–10%) at 1.8V or 2.5V	–	4.66	ns

Notes:

- The F_{REFCLK} clock frequency range and T_{DC_REFCLK} duty cycle specifications also apply to the PL alternative reference clock inputs (PL_PMC_ALT_REF_CLK, PL_LPD_ALT_REF_CLK, and PL_FPD_ALT_REF_CLK).
- See [Table 37: Power-on Reset Assertion Timing Requirements](#) for REF_CLK operating requirements with respect to the POR_B input.

Table 36: RTC Crystal Requirements

Symbol	Description	Min	Typ	Max	Units
F _{XTAL}	Parallel resonance crystal frequency	–	32.768	–	kHz
T _{FTXTAL}	Frequency tolerance	–20	–	20	ppm
C _{XTAL}	Load capacitance for crystal parallel resonance	–	12.5	–	pF
R _{ESR}	Crystal ESR (16.8 and 19.2 MHz)	–	70	–	kΩ
C _{SHUNT}	Crystal shunt capacitance	–	1.4	–	pF

Table 37: Power-on Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T _{POR_B}	Required POR_B assertion time ^{1,2}	10	–	–	μs
T _{MODEPOR}	MODE[3:0] setup time to POR_B rising edge	74	–	–	ns
T _{PORMODE}	POR_B rising edge to MODE[3:0] hold time	74	–	–	ns

Notes:

1. The POR_B input must be asserted Low during the power-on sequence and continue to be asserted for a duration T_{POR_B} after all the required supplies of the PMC have reached minimum voltage levels. The PS, system, and PL domains can be independently powered on or off with additional power management. If the PS, system, and/or PL domains are expected to be functional at initial power-on without additional power management, then the POR_B input must be held Low until all required domain power supplies have also reached minimum voltage levels. For additional power-on sequence information, refer to the *Power Design Manager User Guide* (UG1556). For additional power management information, see the *Versal Adaptive SoC Technical Reference Manual* (AM011) or the *Versal Adaptive SoC System Software Developers Guide* (UG1304).
2. Before the deassertion of POR_B, the REF_CLK must be operating within specification.

Table 38: PS FPD Clocks Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSF})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{FPD_LSBUS_CLK}	Maximum FPD LSBUS clock frequency	150	150	150 ¹	150	100 ¹	100 ⁴	MHz
F _{FPD_TOPSW_CLK}	Maximum FPD top-switch clock frequency	1000	950	825 ²	800	600 ²	550 ⁵	MHz
F _{DBG_FPD_CLK}	Maximum debug FPD clock frequency	400	400	400 ³	400	400 ³	333 ⁶	MHz

Notes:

1. The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum FPD LSBUS clock frequency is 150 MHz when V_{CC_PSF} = 0.88V.
2. The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum FPD top-switch clock frequency is 950 MHz when V_{CC_PSF} = 0.88V.
3. The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum debug FPD clock frequency is 400 MHz when V_{CC_PSF} = 0.88V.
4. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum FPD LSBUS clock frequency is 150 MHz when V_{CC_PSF} = 0.88V.
5. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum FPD top-switch clock frequency is 800 MHz when V_{CC_PSF} = 0.88V.
6. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug FPD clock frequency is 400 MHz when V_{CC_PSF} = 0.88V.

Table 39: PS LPD Clocks Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{RPLL_TO_XPD_CLK}	Maximum RPU PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz
F _{LPD_TOPSW_CLK}	Maximum LPD top-switch clock frequency ¹	750	700	600 ²	600	450 ²	400 ³	MHz
F _{LPD_LSBUS_CLK}	Maximum LPD LSBUS clock frequency ¹	150	150	150 ⁴	150	100 ⁴	100 ⁵	MHz
F _{IOP_SW_CLK}	Maximum I/O peripherals (IOP) switch clock frequency	250	250	250	250	250	250	MHz
F _{TS_REFCLK}	Maximum time-stamp reference clock frequency	100	100	100	100	100	100	MHz
F _{PSM_REFCLK}	Maximum PS manager (PSM) reference clock frequency	460	460	460 ⁶	460	368 ⁶	368 ⁷	MHz
F _{DBG_LPD_CLK}	Maximum debug LPD clock frequency	400	400	400 ⁸	400	400 ⁸	333 ⁹	MHz
F _{DBG_TS_CLK}	Maximum debug time-stamp clock frequency	400	400	400 ¹⁰	400	400 ¹⁰	333 ¹¹	MHz
F _{USB_REFCLK}	Maximum USB reference clock frequency	60	60	60	60	60	60	MHz
F _{CPM_TOPSW_CLK}	Maximum CPM top-switch clock frequency	1000	950	825 ¹²	800	600 ¹²	550	MHz
F _{CPM5_TOPSW_CLK}	Maximum CPM5 top-switch clock frequency	1050	1000	825 ¹³	800	600 ¹³	550	MHz

Notes:

- The LPD_TOPSW_CLK operating frequency must be greater than the LPD_LSBUS_CLK operating frequency.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum LPD top-switch clock frequency is 700 MHz when $V_{CC_PSLP} = 0.88V$.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum LPD top-switch clock frequency is 600 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum LPD LSBUS clock frequency is 150 MHz when $V_{CC_PSLP} = 0.88V$.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum LPD LSBUS clock frequency is 150 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum PSM reference clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum PSM reference clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum debug LPD clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug LPD clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum debug time-stamp clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug time-stamp clock frequency is 400 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum CPM top-switch clock frequency is 950 MHz when $V_{CC_PSLP} = 0.88V$.
- The -2MSE, -2MLE, -2MSI, -2MLI, -2LSE, and -2LLE devices support an overdrive voltage where the maximum CPM5 top-switch clock frequency is 1000 MHz when $V_{CC_PSLP} = 0.88V$.

Table 40: PMC IRO Clock Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{PMC_IRO_CLK}	PMC internal clock source typical frequency	400	400	400	400	320	320	MHz
	PMC internal clock source tolerance	+10/-17	+10/-17	+10/-17	+10/-17	+10/-17	+10/-17	%

Table 41: PMC Clocks Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{EFUSE_REFCLK}	Maximum eFUSE reference clock frequency for reading	115	115	115	115	92	92	MHz
	Maximum eFUSE reference clock frequency for programming	60	60	60	60	60	60	MHz
F _{SMON_REFCLK}	Maximum system monitor reference clock frequency	300	300	300	300	300	300	MHz
F _{USB_SREFCLK}	Maximum USB suspend reference clock frequency	115	115	115	115	92	92	MHz
F _{AXI_TO_REFCLK}	Maximum AXI4 timeout reference clock frequency	115	115	115	115	92	92	MHz
F _{CFU_REFCLK}	Maximum configuration frame unit (CFU) reference clock frequency ¹	400	400	400	400	320	320	MHz
	Minimum CFU reference clock frequency	20	20	20	20	20	20	MHz
F _{LSBUS_REFCLK}	Maximum PMC LSBUS reference clock frequency	150	150	150	150	100	100	MHz
F _{NPI_REFCLK}	Maximum NoC programming interface (NPI) reference clock frequency	300	300	300	300	300 ²	300 ²	MHz
F _{HSM1_REFCLK}	Maximum horizontal super module (HSM1) reference clock frequency used with XPIO ³	200	200	200	200	200	200	MHz
F _{PL0_REFCLK}	Maximum PL0 reference clock frequency	400	400	350	350	300	250 ⁴	MHz
F _{PL1_REFCLK}	Maximum PL1 reference clock frequency	400	400	350	350	300	250 ⁴	MHz
F _{PL2_REFCLK}	Maximum PL2 reference clock frequency	400	400	350	350	300	250 ⁴	MHz
F _{PL3_REFCLK}	Maximum PL3 reference clock frequency	400	400	350	350	300	250 ⁴	MHz
F _{PPLL_TO_XPD_CLK}	Maximum PMC PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz
F _{NPPLL_TO_XPD_CLK}	Maximum NoC PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz

Notes:

1. The maximum configuration frame interface (CFI) clock frequency is the same as the CFU reference clock. When the programmable device image (PDI) is compressed, the compressed data rate through the CFU decompressor is limited to half of the CFI data rate.
2. The maximum NoC programming interface (NPI) reference clock frequency is 250 MHz for the XCVM1302, XCVM1402, XQVM1402, XCVM1502, XQVM1502, and XQVM1802 devices in the -1L ($V_{CCINT} = 0.70V$) speed grades and for the XCVM1302, XCVM1402, and XCVM1502 devices in the -2LLI ($V_{CCINT} = 0.725V$) speed grade.
3. When the HSM1 reference clock is used as the source clock to the XPLL, the frequency range is limited from 100 MHz to 200 MHz.
4. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum PL0, PL1, PL2, and PL3 reference clock frequency is 280 MHz when $V_{CC_PMC} = 0.88V$.

Table 42: PMC PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{PMCPLL}	PMC PLL output frequency	2000	2000	1800	1600	1300	1300 ¹	MHz, Max
		270	270	270	270	270	270	MHz, Min
F _{PMCPLLVC0}	PMC PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
T _{PMCPLLLOCK}	PMC PLL lock time	100	100	100	100	100	100	μs, Max

Notes:

- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when $V_{CC_PMC} = 0.88V$.

Table 43: NoC PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{NOCPLL}	NoC PLL output frequency	2000	2000	1800	1600	1300	1300	MHz, Max
		270	270	270	270	270	270	MHz, Min
F _{NOCPLLVC0}	NoC PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
T _{NOCPLLLOCK}	NoC PLL lock time	100	100	100	100	100	100	μs, Max

Table 44: PS APU PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSPF})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{PSAPLL}	APU PLL output frequency	2000	2000	1800	1600	1300	1300 ¹	MHz, Max
		270	270	270	270	270	270	MHz, Min
F _{PSAPLLVCO}	APU PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
T _{PSAPLLLOCK}	APU PLL lock time	100	100	100	100	100	100	μs, Max

Notes:

- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when $V_{CC_PSFP} = 0.88V$.

Table 45: PS RPU PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{PSRPLL}	RPU PLL output frequency	2000	2000	1800	1600	1300	1300 ¹	MHz, Max
		270	270	270	270	270	270	MHz, Min
F _{PSRPLLVC0}	RPU PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
T _{PSRPLLLOCK}	RPU PLL lock time	100	100	100	100	100	100	μs, Max

Notes:

- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when $V_{CC_PSLP} = 0.88V$.

Table 46: CPM4 PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{CPM4PLL}	CPM4 PLL output frequency	1200	1080	900	900	810	810	720	MHz, Max
		270	270	270	270	270	270	270	MHz, Min
F _{CPM4PLLVCO}	CPM4 PLL VCO frequency	4320	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	2160	MHz, Min
T _{CPM4PLLLOCK}	CPM4 PLL lock time	100	100	100	100	100	100	100	μs, Max

Table 47: CPM5 PLL Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_CPM5})					Units
		0.88V (H)		0.80V (M)		0.70V (L)	
		-3	-2	-1	-2	-1	
$F_{CPM5PLL}$	CPM5 PLL output frequency	1200	900	900	725	725	MHz, Max
		270	270	270	270	270	MHz, Min
$F_{CPM5PLLVC0}$	CPM5 PLL VCO frequency	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	MHz, Min
$T_{CPM5PLLLOCK}$	CPM5 PLL lock time	100	100	100	100	100	μs, Max

PMC JTAG and SelectMAP

Table 48: JTAG/Boundary-Scan Port Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{TCK} ¹	JTAG clock frequency	70	70	70	70	60	60	60	MHz, Max
T _{TCKL} ¹	TCK Low pulse time	5.5	5.5	5.5	5.5	6.0	6.0	6.0	ns, Min
T _{TCKH}	TCK High pulse time	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns, Min
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup and hold	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	5.5	5.5	5.5	5.5	6.0	6.0	6.0	ns, Max

Notes:

- When using AC-JTAG, the maximum F_{TCK} frequency is 40 MHz and the minimum T_{TCKL} low pulse time is 7 ns.

Table 49: SelectMap Interface Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{SMAPCLK}	SelectMap clock frequency, write	200	200	200	200	200	200	200	MHz, Max
	SelectMap clock frequency, read	120	120	120	120	120	120	120	MHz, Max
T _{SMAPCLKL}	SelectMAP clock Low time	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns, Min
T _{SMAPCLKH}	SelectMAP clock High time	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns, Min
T _{SMAPDCLK} /SMAPCLKD	SelectMAP data (SMAP_IO[31:0]) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.5/0.0	4.5/0.0	4.5/0.0	ns, Min
T _{SMAPCSCLK} /SMAPCLKCS	SelectMAP chip select (SMAP_CS_b) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMAPRWCLK} /SMAPCLKRW	SelectMAP read write (SMAP_RDWR_b) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMAPCLKO}	SelectMAP clock to data output	13.0	13.0	13.0	13.0	13.0	13.0	13.0	ns, Max
C _{SMAPBUSYCS}	SelectMAP busy assertion to chip select deassertion	24	24	24	24	24	24	24	clock cycles, Max

PS and PMC Interface Specifications

PMC Quad-SPI Controller Interface

Table 50: Quad-SPI Interface

Symbol	Description ^{1, 2}	Min	Max	Units
Quad-SPI device clock frequency operating at >100 MHz up to 150 MHz. Loopback enabled.³				
F _{QSPI_CLK}	Quad-SPI device clock frequency	100	150	MHz
F _{QSPI_REFCLK} ⁴	Quad-SPI reference clock frequency	$2 \times F_{QSPI_CLK}$		MHz
T _{QSPIDCK}	Setup time, all inputs	0.77	–	ns
T _{QSPICKD}	Hold time, all inputs	1.0	–	ns
T _{QSPICKO}	Clock to output delay, all outputs	2.9	4.5	ns
T _{QSPICSLK} ⁵	Chip select asserted to next clock edge	5.0	–	ns
T _{QSPICLKCS}	Clock edge to chip select deasserted	5.0	–	ns
T _{DCQSPICLK}	Quad-SPI clock duty cycle	45	55	%
Quad-SPI device clock frequency operating at >37.5 MHz up to 100 MHz. Loopback enabled.³				
F _{QSPI_CLK}	Quad-SPI device clock frequency	37.5	100	MHz
F _{QSPI_REFCLK} ⁴	Quad-SPI reference clock frequency	$2 \times F_{QSPI_CLK}$		MHz
T _{QSPIDCK}	Setup time, all inputs	2.0	–	ns
T _{QSPICKD}	Hold time, all inputs	0.0	–	ns
T _{QSPICKO}	Clock to output delay, all outputs	3.2	7.8	ns
T _{QSPICSLK} ⁵	Chip select asserted to next clock edge	5.0	–	ns
T _{QSPICLKCS}	Clock edge to chip select deasserted	5.0	–	ns
T _{DCQSPICLK}	Quad-SPI clock duty cycle	45	55	%
Quad-SPI device clock frequency operating at ≤37.5 MHz. Loopback disabled.				
F _{QSPI_CLK}	Quad-SPI device clock frequency		37.5	MHz
F _{QSPI_REFCLK} ⁴	Quad-SPI reference clock frequency		300	MHz
T _{QSPIDCK}	Setup time, all inputs	19.1	–	ns
T _{QSPICKD}	Hold time, all inputs	0.0	–	ns
T _{QSPICKO}	Clock to output delay, all outputs	5.2	21.5	ns
T _{QSPICSLK}	Chip select asserted to next clock edge	9.0	–	ns
T _{QSPICLKCS} ⁵	Clock edge to chip select deasserted	9.0	–	ns
T _{DCQSPICLK}	Quad-SPI clock duty cycle	45	55	%

Notes:

1. The test conditions are configured for the generic Quad-SPI interface with a 12 mA drive strength, fast slew rate, and load conditions (15 pF/30 pF for a Quad-SPI device clock frequency up to 100 MHz and 15 pF for a Quad-SPI device clock frequency > 100 MHz), tested at 3.3V and 1.8V.
2. 30 pF loads are for QSPI dual-stacked or QSPI dual-parallel modes.
3. When the Quad-SPI device clock frequency is >37.5 MHz, the Quad-SPI loopback clock output (QSPI_LPBK_CLK) must be enabled in the control, interface, and processing system (CIPS), and the associated MIO[6] pin must be left unconnected on the board.
4. The Quad-SPI reference clock frequency must be 2x the Quad-SPI device clock frequency when it is >37.5 MHz.
5. T_{QSPICSLK} is only valid when two reference clock cycles are programmed between the chip select and clock.

PMC Octal-SPI Controller Interface

Table 51: Octal-SPI Interface

Symbol	Description ¹	Min	Max	Units
Octal-SPI device clock frequency operating at DDR 50 MHz up to 200 MHz.				
F _{OSPI_CLK}	Octal-SPI device clock frequency	50	200 ¹	MHz
F _{OSPI_REFCLK}	Octal-SPI reference clock frequency	= F _{OSPI_CLK} ²		MHz
T _{OSPI200IVW}	Input valid data window	0.5	–	UI
T _{OSPICKO}	Clock to output delay, all outputs	0.6	1.9	ns
T _{OSPICSLK}	Chip select asserted to next clock edge	3.375	–	ns
T _{OSPICLKCS}	Clock edge to chip select deasserted	3.375	–	ns
T _{OSPIDCCLK}	Octal-SPI clock duty cycle	45	55	%
Octal-SPI device clock frequency operating at SDR 50 MHz to 166 MHz.				
F _{OSPI_CLK}	Octal-SPI device clock frequency	50	166	MHz
F _{OSPI_REFCLK}	Octal-SPI reference clock frequency	= F _{OSPI_CLK} ²		MHz
T _{OSPI166IVW}	Input valid data window	0.4	–	UI
T _{OSPICKO}	Clock to output delay, all outputs	1.8	3.9	ns
T _{OSPICSLK}	Chip select asserted to next clock edge	3.375	–	ns
T _{OSPICLKCS}	Clock edge to chip select deasserted	3.375	–	ns
T _{OSPIDCCLK}	Octal-SPI clock duty cycle	45	55	%
Octal-SPI device clock frequency operating at SDR <50 MHz.				
F _{OSPI_CLK}	Octal-SPI device clock frequency	–	50	MHz
F _{OSPI_REFCLK}	Octal-SPI reference clock frequency	4 × F _{OSPI_CLK}	200	MHz
T _{OSPIDCK}	Setup time, all inputs	11	–	ns
T _{OSPICKD}	Hold time, all inputs	1.0	–	ns
T _{OSPICKO}	Clock to output delay, all outputs	2.0	18	ns
T _{OSPICSLK}	Chip select asserted to next clock edge	3.375	–	ns
T _{OSPICLKCS}	Clock edge to chip select deasserted	3.375	–	ns
T _{OSPIDCCLK}	Octal-SPI clock duty cycle	45	55	%

Notes:

1. The test conditions are configured for the Octal-SPI interface with a 12 mA drive strength, fast slew rate, and 12 pF load. The maximum Octal-SPI device clock frequency under different load conditions are 166 MHz for a 20 pF load and 100 MHz for a 40 pF load.
2. The Octal-SPI reference clock frequency must be equal to F_{OSPI_CLK} when the Octal-SPI device clock frequency is ≥50 MHz.

PS SPI Controller Interface

Table 52: SPI Controller Interface

Symbol	Description ¹	Min	Max	Units
SPI Master Interface				
F _{MSPI_CLK}	SPI master device clock frequency (MIO)	–	50	MHz
	SPI master device clock frequency (EMIO)	–	25	MHz
F _{SPI_REFCLK}	SPI reference clock frequency	–	200	MHz
T _{DCMSPICLK}	SPI master mode clock duty cycle	45	55	%
T _{MSPISSELCK}	Master select asserted to first active clock edge ²	1	–	SPI_REFCLK cycles
T _{MSPISCLKSS}	Last active clock edge to slave select deasserted ²	1	–	SPI_REFCLK cycles
T _{MSPIDCK}	Input setup time for master in/slave out (MISO)	9.9	–	ns
T _{MSPICKD}	Input hold time for MISO	0.0	–	ns
T _{MSPICKO}	Master out/slave in (MOSI) and slave select clock-to-out delay	–3.7	5.0	ns
SPI Slave Interface				
F _{SSPI_CLK}	SPI slave device clock frequency	–	25	MHz
F _{SPI_REFCLK}	SPI reference clock frequency	–	200	MHz
T _{SSPISSELCK}	Slave select asserted to first active clock edge	1	–	SPI_REFCLK cycles
T _{SSPISCLKSS}	Last active clock edge to slave select deasserted	1	–	SPI_REFCLK cycles
T _{SSPIDCK}	Input setup time for MISO	5.0	–	ns
T _{SSPICKD}	Input hold time for MISO	5.0	–	ns
T _{SSPICKO}	MOSI clock-to-out delay	0.0	13	ns

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and 15 pF load.
- The test conditions use the SPI delay register where XSPIPS_DR_OFFSET[xspips_dr_init_mask] = 2 and XSPIPS_DR_OFFSET[xspips_dr_after_mask] = 2.

PS USB Controller Interface

Table 53: ULPI Interface

Symbol	Description ¹	Min	Max	Units
T _{ULPIDCK}	Input setup to ULPI clock, all inputs	4.5	–	ns
T _{ULPICKD}	Input hold to ULPI clock, all inputs	0.5	–	ns
T _{ULPICKO}	ULPI clock to output valid, all outputs	2.0	8.9	ns
F _{ULPICLK}	ULPI clock frequency	–	60	MHz

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Gigabit Ethernet MAC Controller Interface

Table 54: RGMII Interface

Symbol	Description ¹	Min	Max	Units
F _{GEMTXCLK}	RGMII_TX_CLK transmit clock frequency	–	125	MHz
F _{GEMRXCLK}	RGMII_RX_CLK receive clock frequency	–	125	MHz
F _{GEMREFCLK}	Gigabit Ethernet MAC (GEM) reference clock frequency	–	125	MHz
F _{GEMTSUREFCLK} ²	Gigabit Ethernet MAC time-stamp unit reference clock frequency	–	250	MHz
T _{DCGEMTXCLK}	Transmit clock duty cycle	45	55	%
T _{GEMTXCKO}	TXD output clock to out time	–0.5	0.5	ns
T _{GEMRXDCK}	RXD input setup time	0.8	–	ns
T _{GEMRXCKD}	RXD input hold time	0.8	–	ns
T _{MDIOCLK}	MDC output clock period	400	–	ns
T _{MDIOCKL}	MDC Low time	160	–	ns
T _{MDIOCKH}	MDC High time	160	–	ns
T _{MDIODCK}	MDIO input data setup time	80	–	ns
T _{MDIOCKD}	MDIO input data hold time	0.0	–	ns
T _{MDIOCKO}	MDIO output data delay time	–3.0	15.0	ns

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
- The APB interface (LPD_LSBUS_CLK) operating frequency must be greater than or equal to the GEM_TSU_CLK operating frequency.

PMC SD/SDIO Controller Interface

Table 55: SD/SDIO Interface

Symbol	Description ¹	Min	Max	Units
F _{SD_REFCLK}	SD reference clock frequency	–	200	MHz
F _{SDDL_REFCLK}	SD DLL reference clock frequency	–	1200	MHz
SD/SDIO Interface Default Speed Mode				
F _{SDS_CLK} ²	SD standard device clock frequency	–	20	MHz
F _{SDID_CLK}	Clock frequency in identification mode	–	400	kHz
T _{SDDC_CLK}	SD standard device clock duty cycle	45	55	%
T _{SDCKO}	Clock to output delay, all outputs	–2.0	4.5	ns
T _{SDDC}	Input setup time, all inputs	2.0	–	ns
T _{SDCKD}	Input hold time, all inputs	2.0	–	ns
SD/SDIO Interface High-speed Mode				
F _{SDHS_CLK}	SD high-speed device clock frequency	25	50	MHz
T _{SDHSDC_CLK}	SD high-speed device clock duty cycle	45	55	%
T _{SDHSCKO}	Clock to output delay, all outputs	2.2	13.8	ns
T _{SDHSDIVW}	Input valid data window	0.4	–	UI
SD/SDIO Interface SDR12 Mode				
F _{SDSDR12_CLK} ²	SD SDR12 device clock frequency	–	25	MHz
T _{DCSDSDR12_CLK}	SD SDR12 device clock duty cycle	30	70	%

Table 55: SD/SDIO Interface (cont'd)

Symbol	Description ¹	Min	Max	Units
T _{SDSDR12CKO}	Clock to output delay, all outputs	1.0	36.8	ns
T _{SDSDR12DCK}	Input setup time, all inputs	10.0	–	ns
T _{SDSDR12CKD}	Input hold time, all inputs	1.5	–	ns
SD/SDIO Interface SDR25/SDR50 Mode				
F _{SDSDR_CLK}	SDR25 device clock frequency	25	50	MHz
	SDR50 device clock frequency	25	100	MHz
T _{SDSDRDC_CLK}	SD SDR50/SDR25 device clock duty cycle	30	70	%
T _{SDSDRCKO}	Clock to output delay, all outputs	1.0	6.8	ns
T _{SDDDRCKD}	Input valid data window	0.4	–	UI
SD/SDIO Interface SDR104 Mode				
F _{SDSDR104_CLK}	SDR104 device clock frequency	25	200	MHz
T _{DCSDSDR104_CLK}	SD SDR104 device clock duty cycle	30	70	%
T _{SDSDR104CKO}	Clock to output delay, all outputs	1.0	3.2	ns
T _{SDSDR104CKD}	Input valid data window	0.5	–	UI
SD/SDIO Interface DDR50 Mode				
F _{SDDDR_CLK}	SD DDR50 device clock frequency	25	50	MHz
T _{DCSDDDR_CLK}	SD DDR50 device clock duty cycle	45	55	%
T _{SDDDRCKO}	Clock to output delay, data	1.0	6.8	ns
T _{SDDDRDCK}	Input valid data window	0.5	–	UI
T _{SDDDRCKD}	Input setup time, command	4.7	–	ns
T _{SDDDRIDCLK}	Input hold time, command	1.5	–	ns
T _{SDDDRCLK}	Clock to output delay, command	1.0	13.8	ns

Notes:

- The test condition settings for SD/SDIO modes are: 12 mA drive strength, fast slew rate, and a 15 pF load. The OTAP delay (OTAP_DLY[5:0]) test condition settings are: SD high-speed mode = 0x04, SD SDR25/50 mode = 0x03, SD SDR104 mode = 0x02, and SD DDR50 mode = 0x03.
- EMIO is supported in SD default speed mode and SDR12 mode.

PMC eMMC Controller Interface

Table 56: eMMC Controller Interface

Symbol	Description ¹	Min	Max	Units
eMMC Interface Standard Mode				
F _{EMMCCLK}	eMMC standard device clock frequency ²	–	25	MHz
T _{DCEMMCCLK}	eMMC clock duty cycle	45	55	%
T _{EMMCCKO}	Clock to output delay, all outputs	–2.0	4.5	ns
T _{EMMCDCK}	Input setup time, all inputs	2.0	–	ns
T _{EMMCCKD}	Input hold time, all inputs	2.0	–	ns
eMMC Interface High-speed SDR Mode				
F _{EMMCSRCLK}	eMMC high-speed SDR device clock frequency	25	50	MHz
T _{DCEMMCSRCLK}	eMMC high-speed SDR clock duty cycle	45	55	%
T _{EMMCSRCKO}	Clock to output delay, all outputs ³	3.2	16.8	ns

Table 56: eMMC Controller Interface (cont'd)

Symbol	Description ¹	Min	Max	Units
T _{EMMCSDRDIVW}	Input valid data window ⁴	0.4	–	UI
eMMC Interface High-speed DDR Mode				
F _{EMMCDDRCLK}	eMMC high-speed DDR device clock frequency	25	50	MHz
T _{DCEMMCDRCLK}	eMMC high-speed DDR clock duty cycle	45	55	%
T _{EMMCDDRCKO1}	Data clock to output delay ³	2.7	7.3	ns
T _{EMMCDDRDIW}	Input valid data window ⁴	0.35	–	UI
T _{EMMCDDRCKO2}	Command clock to output delay	3.2	16	ns
T _{EMMCDDRCK2}	Command input setup time	3.9	–	ns
T _{EMMCDDRCKD2}	Command input hold time	2.5	–	ns
eMMC Interface HS200 Mode				
F _{EMMCHS200CLK}	eMMC HS200 device clock frequency	25	200	MHz
T _{DCEMMCHS200CLK}	eMMC HS200 clock duty cycle	30	70	%
T _{EMMCHS200CKO}	Clock to output delay, all outputs ³	1.0	3.4	ns
T _{EMMCHS200DIW}	Input valid data window ⁴	0.5	–	UI

Notes:

1. The test condition settings for the eMMC modes are: 12 mA drive strength, fast slew rate, and a 15 pF load. The OTAP delay (OTAP_DLY[5:0]) test condition settings are: eMMC high-speed SDR mode = 0x05, eMMC high-speed DDR mode = 0x05, and eMMC HS200 mode = 0x02.
2. EMIO is supported in the eMMC standard mode.
3. This specification is achieved using predetermined DLL tuning.
4. This specification is required for capturing input data using DLL tuning.

PS and PMC I2C Controller Interface

Table 57: I2C Controller Interface

Symbol	Description ¹	Min	Max	Units
I2C Fast-mode Interface				
F _{I2CF_CLK}	Serial clock line (SCL) clock frequency	–	400	kHz
F _{I2C_REFCLK} ²	I2C reference clock frequency	–	100	MHz
T _{I2CFCKL}	SCL Low time	1.3	–	μs
T _{I2CFCKH}	SCL High time	0.6	–	μs
T _{I2CFCKO}	Serial data line (SDA) clock-to-out delay	–	900	ns
T _{I2CFDCK}	SDA input setup time	100	–	ns
T _{I2CFCKD}	SDA input data hold time	0	–	ns
I2C Standard-mode Interface				
F _{I2CS_CLK}	SCL clock frequency	–	100	kHz
F _{I2C_REFCLK} ²	I2C reference clock frequency	–	100	MHz
T _{I2CSCKL}	SCL Low time	4.7	–	μs
T _{I2CSCKH}	SCL High time	4.0	–	μs
T _{I2CSCKO}	SDA clock-to-out delay	–	3450	ns
T _{I2CSDCK}	SDA input setup time	250	–	ns
T _{I2CSCKD}	SDA input data hold time	0	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. F_{I2C_REFCLK} specification applies to PMC_I2C_REFCLK, LPD_I2C0_REFCLK, LPD_I2C1_REFCLK, and SYSMON_I2C_REFCLK.

PS CAN FD Controller Interface

Table 58: CAN FD Controller Interface

Symbol	Description ¹	Min	Max	Units
F _{CAN_FD_REFCLK} ²	CAN FD reference clock frequency 1x	–	80	MHz
	CAN FD reference clock frequency 2x	–	160	MHz
T _{CAN_FD_PWRX}	Receive pulse width	125	–	ns
T _{CAN_FD_PWTX}	Transmit pulse width	125	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. The APB interface (LPD_LSBUS_CLK) operating frequency must be greater than or equal to the CAN FD operating frequency (which is the CAN_FD_REFCLK frequency divided by the CAN[0]1_REF_CTRL[DIVISOR]).

PS UART Controller Interface

Table 59: UART Controller Interface

Symbol	Description ¹	Min	Max	Units
$F_{UART_REF_CLK}$	UART reference clock frequency	–	100	MHz
$BAUD_{TXMAX}$	Transmit baud rate	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate	–	6.25	Mb/s

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 60: General Purpose I/O (GPIO) Interface

Symbol	Description ¹	Min	Max	Units
T_{GPIOH}	LPD GPIO input High pulse width	$10 \times 1/F_{LPD_LSBUS_CLK}$	–	μs
	PMC GPIO input High pulse width	$10 \times 1/F_{PMC_LSBUS_CLK}$	–	μs
T_{GPIOH}	LPD GPIO input Low pulse width	$10 \times 1/F_{LPD_LSBUS_CLK}$	–	μs
	PMC GPIO input Low pulse width	$10 \times 1/F_{PMC_LSBUS_CLK}$	–	μs

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and 15 pF load.

PS Trace Interface

Table 61: Trace Interface

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSPF})												Units
		0.88V (H)				0.80V (M)				0.70V (L)				
		-3		-2		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{TCECLK}	Trace clock frequency (MIO)	–	200	–	200	–	200	–	200	–	200	–	167 ²	MHz
	Trace clock frequency (EMIO)	–	400	–	400	–	350	–	350	–	300	–	250 ³	MHz
F _{DBGTCECLK}	Trace debug (DBG_TRACE) clock frequency	–	400	–	400	–	400	–	400	–	400	–	333 ⁴	MHz
T _{TCECKO}	Trace clock to output delay, all outputs	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	ns
T _{TCECKO}	Trace clock duty cycle	45	55	45	55	45	55	45	55	45	55	45	55	%

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace clock frequency (MIO) is 200 MHz when V_{CC_PSLP} = 0.88V or V_{CC_PMC} = 0.88V.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace clock frequency (EMIO) is 280 MHz when V_{CC_PSLP} = 0.88V.
- The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace debug clock frequency is 400 MHz when V_{CC_PSLP} = 0.88V.

PS Triple-timer Counter Interface

Table 62: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
F _{TTCX_REF_CLK}	Triple-timer counter input clock frequency (TTCX_REF_CLK) ¹	–	See Note 1	MHz
F _{TTCX_IO_REF_CLKX}	Triple-timer counter MIO-EMIO input clock frequency (TTCX_IO_REF_CLKX) ²	–	50 ³	MHz
T _{TTCCLK}	Triple-timer counter MIO-EMIO input clock High pulse width	2/F _{TTCX_IO_REF_CLKX} ²	–	µs
	Triple-timer counter MIO-EMIO input clock Low pulse width	2/F _{TTCX_IO_REF_CLKX} ²	–	µs
F _{TTCCLK}	Triple-timer counter output clock frequency	–	F _{TTCX_REF_CLK} /2 ¹	MHz
			F _{TTCX_IO_REF_CLKX} /2 ²	MHz
T _{TTCCLK}	Triple-timer counter output clock period	2/F _{TTCX_REF_CLK} ¹	–	µs
		2/F _{TTCX_IO_REF_CLKX} ²	–	µs

Notes:

- TTCX_REF_CLK source is used. TTCX_REF_CLK source can be the REF_CLK (F_{REFCLK}), LPD_LSBUS_CLK (F_{LPD_LSBUS_CLK}), or the RPU_REF_CLK (F_{RPU_MAX}).
- TTCX_IO_REF_CLKX source is used. TTCX_IO_REF_CLKX source can be MIO or EMIO.
- The maximum F_{TTCX_IO_REF_CLKX} is the lesser of the specified maximum F_{TTCX_IO_REF_CLKX} or F_{TTCX_REF_CLK}/2.

PS System Watchdog Timer Interface

Table 63: System Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F _{SWDTCLK}	System watchdog timer input clock frequency	–	100	MHz

PMC System Monitor Specifications

Table 64: PMC System Monitor Specifications

Parameter ¹	Symbol	Conditions ²	Min	Typ	Max	Units
V _{CCAUX_SMON} = 1.5V ±3%, V _{REFP} = 1.024V ³ , V _{REFN} = 0V, T _j = -40°C to 100°C, typical values at T _j = 40°C						
ADC Accuracy ⁴						
Resolution			10	-	-	Bits
Integral nonlinearity	INL		-1	-	1	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	-1	-	1	LSBs
Offset error		Calibrated	-2	-	2	LSBs
Gain error		Calibrated	-0.4	-	0.4	%
Sample rate				0.25		MS/s
RMS code noise		External 1.024V reference	-	-	1	LSBs
		On-chip reference	-	-	1	LSBs
Analog Inputs						
ADC input ranges (V _P -V _N)		Unipolar operation	0		1	V
		Bipolar operation	-0.5	-	0.5	V
ADC input common mode ranges		Unipolar common mode range (FS input)	0	-	0.25	V
		Bipolar common mode range (FS input)	0.5	-	0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	-0.1	-	V _{CCAUX_SMON}	V
On-Chip Sensors						
Supply sensor error		Measurement range up to V _{CCAUX_SMON} ±3% T _j = -55°C to 125°C, internal or external reference	-1	-	1	%
System Monitor Reference ⁵						
External reference	V _{REFP}	Externally supplied reference voltage	0.973	1.024	1.075	V
On-chip reference		Tie V _{REFP} to AGND, T _j = -40°C to 125°C	1.019	1.024	1.029	V

Notes:

- For more information, see the *Versal Adaptive SoC System Monitor Architecture Manual* (AM006).
- All the reference voltages required by the Versal device cannot sleep.
- All the accuracy specs are at $V_{REFP} = 1.024V$ (precisely). Variation in V_{REFP} will cause a proportional gain error which should be added to see the true accuracy. The temperature range is in Kelvin so the gain error is proportional.
- Gross offset and gain errors are removed by automatic calibration. The specification quotes the net error.
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.024V$ and $V_{REFN} = 0V$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric-type applications allowing the reference to vary by $\pm 5\%$ is permitted. On-chip reference variation is $\pm 0.5\%$.

Network on Chip Switching Characteristics

Table 65: Network on Chip Switching Characteristics

Symbol	Description	Devices	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_SOC})						Units
			0.88V (H)		0.80V (M)		0.80V (L) ¹		
			-3	-2	-2	-1	-2	-1	
F _{MAX}	Network on Chip (NoC) clock maximum frequency	VM2152	N/A	986	950	875	950	875	MHz
		All other devices	1080	1080	1000	960	1000	960	MHz
F _{MAX_NMU}	NoC master unit clock maximum frequency	All devices	540	540	500	480	500	480	MHz
F _{MAX_BLI_NMU}	NoC master unit clock maximum frequency using BLI resources	VM2152	N/A	450	425	400	425	350	MHz

Notes:

1. The NoC is powered by the V_{CC_SOC} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).

Programmable Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Versal Prime devices. These values are subject to the same guidelines as the [AC Switching Characteristics](#) section.

In each of the following performance tables, the I/O bank type is either XPIO, HDIO, or X5IO.

Table 66: I/O Logic Performance

Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})														Units
	0.88V (H)				0.80V (M)				0.725V (L)		0.70V (L)				
	-3		-2		-2		-1		-2LLI		-2		-1		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
TX DDR	0	250	0	250	0	250	0	250	0	200	0	200	0	200	Mb/s
TX SDR	0	125	0	125	0	125	0	125	0	100	0	100	0	100	Mb/s
RX DDR	0	250	0	250	0	250	0	250	0	200	0	200	0	200	Mb/s
RX SDR	0	125	0	125	0	125	0	125	0	100	0	100	0	100	Mb/s

Table 67: XPHY I/O Performance

Description ^{1, 2}	Data Width	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})														Units
		0.88V (H)				0.80V (M)				0.725V (L)		0.70V (L)				
		-3		-2		-2		-1		-2LLI		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
TX DDR	8	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	Mb/s
	4	200	1600	200	1600	200	1468	200	1468	200	1332 ³	200	1332 ³	200	1332 ³	Mb/s
	2	200	800	200	800	200	734	200	734	200	666 ⁴	200	666 ⁴	200	666 ⁴	Mb/s
RX DDR ⁵	8	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	Mb/s
	4	200	1600	200	1600	200	1468	200	1468	200	1332 ³	200	1332 ³	200	1332 ³	Mb/s
	2	200	800	200	800	200	734	200	734	200	666 ⁴	200	666 ⁴	200	666 ⁴	Mb/s

Notes:

1. XPHY I/O is supported through the Advanced I/O Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface. For asynchronous interfaces, see the *Advanced I/O Wizard LogiCORE IP Product Guide* (PG320).
2. Package skews are not included and should be removed through PCB routing.
3. For multi-bank interfaces, the performance is specified at 1066.5 Mb/s.
4. For multi-bank interfaces, the performance is specified at 533.25 Mb/s.
5. SDR specifications are a subset of the DDR specifications.

Table 68: MIPI D-PHY Performance

Description	I/O Bank Type	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
MIPI D-PHY transmitter or receiver	XP	3200	3200	3200	3200	3200	3200	3200	Mb/s

Table 69: X5IO Performance

Description ^{1, 2}	Data Width	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})												Units
		0.88V (H)		0.80V (M)				0.725V (L)		0.70V (L)				
		-2		-2		-1		-2LLI		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
TX DDR	16	400	1800	400	1800	400	1800	400	1800	400	1800	400	1800	Mb/s
	8	400	1800	400	1800	400	1800	400	1800	400	1800	400	1800	Mb/s
	4	400	1600	400	1468	400	1468	400	1332	400	1332	400	1332	Mb/s
	2	400	800	400	734	400	734	400	666	400	666	400	666	Mb/s
RX DDR ³	16	400	1800	400	1800	400	1800	400	1800	400	1800	400	1800	Mb/s
	8	400	1800	400	1800	400	1800	400	1800	400	1800	400	1800	Mb/s
	4	400	1600	400	1468	400	1468	400	1332	400	1332	400	1332	Mb/s
	2	400	800	400	734	400	734	400	666	400	666	400	666	Mb/s

Notes:

1. X5IO is supported through the X5IO I/O Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. Package skews are not included and should be removed through PCB routing.
3. SDR specifications are a subset of the DDR specifications.

Table 70: MIPI D-PHY/C-PHY Performance

Description	I/O Bank Type	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
		0.88V (H)		0.80V (M)		0.725V (L)		
		-2	-2	-1	-2LLI	-2	-1	
MIPI D-PHY/C-PHY transmitter or receiver	X5IO	4500	4500	4500	4500	4500	4500	Mb/s

The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists the devices that support the soft memory interface controller. The soft memory interface controller is only supported in XPIO banks and is not supported in X5IO banks.

Table 71: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller

Memory Standard	DRAM Type	DIMM Slots	XPIO Bank Performance ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
				0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
				-3	-2	-2	-1	-2LLI	-2	-1	
DDR4	Single rank component		All	3200	3200	2933	2667	2667	2667	2133	Mb/s
	1 rank RDIMM, DIMM ²	1	All	3200	3200	2933	2667	2133	2133	2133	Mb/s
	2 rank RDIMM, LRDIMM, DIMM ²	1	All	2933	2933	2667	2667	2133	2133	2133	Mb/s
	4 rank LRDIMM	1	All	2667	2667	2400	2400	2133	2133	2133	Mb/s
	1 rank RDIMM	2	All	2667	2667	2400	2400	2133	2133	2133	Mb/s
	1 rank DIMM ²	2	All	2400	2400	2133	2133	1867	1867	1867	Mb/s
	2 rank LRDIMM	2	All	2667	2667	2400	2400	2133	2133	2133	Mb/s
	2 rank RDIMM	2	All	2133	2133	2133	2133	2133	2133	2133	Mb/s
	2 rank DIMM ²	2	All	1866	1866	1866	1866	1866	1866	1866	Mb/s
RLDRAM3			All	1066	1066	1066	1066	1066 ⁴	1066 ⁴	1066 ⁴	MHz
QDRIV	HP		All	933	933	933	933	933	933	933	MHz
	XP ³		All	1066	1066	1066	1066	1066	1066	1066	MHz

Notes:

1. The Versal device package pinout files specify XPIO bank performance (XPIOperf). See ASCII package files information in the *Versal Adaptive SoC Packaging and Pinouts Architecture Manual* (AM013).
2. Dual in-line memory module (DIMM) includes SODIMM and UDIMM.
3. The QDRIV XP performance values are for 18-bit interfaces, for 36-bit interfaces the maximum performance is 933 MHz.
4. The RLDRAM3 maximum performance with burst length 2 (BL2) interfaces is 933 MHz in the -2L and -1L speed grades.

Programmable Logic Switching Characteristics

Block RAM Switching Characteristics

Table 72: Block RAM Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM})								Units
		0.88V (H)		0.80V (M)			0.80V (L) ¹			
		-3	-2	-2	-1	-1MM	-2LLI	-2LSE -2LLE	-1	
Maximum Frequency										
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes)	1000	1000	850	800	650	650	615	MHz	
F _{MAX_RF}	Block RAM (READ_FIRST mode)	850	850	725	675	550	550	510	MHz	
Block RAM Clock-to-Out Delays										
T _{RCKO_DO}	Clock CLK to DOUT output (without output register)	0.797	0.797	0.901	0.967	1.141	1.141	1.233	ns, Max	
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register)	0.234	0.234	0.262	0.280	0.333	0.333	0.362	ns, Max	

Notes:

1. The block RAM is powered by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).

UltraRAM Switching Characteristics

Table 73: UltraRAM Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L) ¹		
		-3	-2	-2	-1	-2	-1	
Maximum Frequency								
F _{MAX}	UltraRAM maximum frequency with output register	738	738	664	645	530	500	MHz

Notes:

1. The UltraRAM is powered by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).

Accelerator RAM Switching Characteristics

The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists the Versal Prime devices that include the accelerator RAM (XRAM).

Table 74: Accelerator RAM Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F _{MAX_XRAM}	Maximum accelerator RAM (XRAM) clock frequency	800	800	625	600	500	450 ¹	MHz
F _{PL_XRAM}	Maximum accelerator RAM PL interface frequency	390	375	325	300	270	250 ²	MHz

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 800 MHz when $V_{CC_PSLP} = 0.88V$.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 350 MHz when $V_{CC_PSLP} = 0.88V$.

Input/Output Delay Switching Characteristics

Table 75: Input/Output Delay Switching Characteristics

Symbol	Description	Devices	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units	
			0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
			-3	-2	-2	-1	-2LLI	-2		-1
T _{IDELAY_RESOLUTION/} T _{ODELAY_RESOLUTION}	X5IO IDELAY/ODELAY delay tap resolution for VM2152 only	VM2152	N/A	0.86 to 4.00 ¹		N/A	0.86 to 4.00 ¹		ps	
	XPHY IDELAY/ODELAY delay tap resolution	All other devices	1.22 to 4.00						ps	
T _{IDELAY_ERROR/} T _{ODELAY_ERROR}	X5IO calibrated delay line error (DELAY_VALUE) for VM2152 only	VM2152	N/A	-10 to +10		N/A	-10 to +10		Delay Taps	
	XPHY calibrated delay line error (DELAY_VALUE) (REFCLK_FREQUENCY = 500 to 1800 MHz) ²	All other devices	-10 to +10						Delay Taps	
T _{IOL_IDELAY_RESOLUTION/} T _{IOL_ODELAY_RESOLUTION}	IOL IDELAY/ODELAY uncalibrated delay tap resolution for IOL resources (HD or XP)	All devices	60 to 173						ps	

Notes:

1. For $800\text{ MHz} \leq \text{REFCLK_FREQUENCY} \leq 1600\text{ MHz}$, set the `PDL_CASCADE = TRUE`. For $\text{REFCLK_FREQUENCY} > 1600\text{ MHz}$, set the `PDL_CASCADE = FALSE`. Refer to the *Versal Adaptive SoC SelectIO Resources Architecture Manual* ([AM010](#)). IDELAY is used for alignment and ALIGN_DELAY effects the programmed DELAY_VALUE programming.
2. For $\text{REFCLK_FREQUENCY} < 500\text{ MHz}$, BISC calibration of the DELAY_VALUE <0-5> is not guaranteed. Use the $T_{IDELAY_RESOLUTION}/T_{ODELAY_RESOLUTION}$ for delay calculations. Refer to the *Versal Adaptive SoC SelectIO Resources Architecture Manual* ([AM010](#)). IDELAY is used for alignment and ALIGN_DELAY effects the programmed DELAY_VALUE programming.

DSP58 Switching Characteristics

Table 76: DSP58 Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})								Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)			
		-3	-2	-2	-1	-2LLI	-2	-1		
Fixed Point Arithmetic										
F _{MAX_INT_MULT}	27 × 24 two's complement multiply	1150	1150	1070	984	760	760	680	MHz	
F _{MAX_SIMD}	Single-instruction multiple-data (SIMD) arithmetic	1150	1150	1070	984	760	760	680	MHz	
Complex Arithmetic										
F _{MAX_COMPLEX_MULT}	18 × 18 two's complement complex multiply	984	984	909	850	646	646	578	MHz	
Floating Point Arithmetic										
F _{MAX_FP}	Floating-point operations	805	805	750	700	532	532	476	MHz	

Clock Buffers and Networks

Table 77: Clock Buffers Switching Characteristics

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL and MBUFGCTRL)									
F _{MAX}	Maximum frequency of a global clock tree (BUFG)	1150	1150	1070	984	800	800	680	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV and MBUFGCE_DIV)									
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability	1150	1150	1070	984	800	800	680	MHz
Global Clock Buffer with Clock Enable (BUFGCE)									
F _{MAX}	Maximum frequency of a global clock buffer with clock enable	1150	1150	1070	984	800	800	680	MHz
Global Clock Buffer for the Processing System (BUFG_PS and MBUFG_PS)									
F _{MAX}	Maximum frequency of a global clock buffer with clock enable	1150	1150	1070	984	800	800	680	MHz
GTY or GTM Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT and MBUFG_GT)									
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	1150	1150	1070	984	1000	1000	680	MHz

MMCM Switching Characteristics

Table 78: MMCM Specification

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L) ¹		
		-3	-2	-2	-1	-2	-1	
F _{INMAX_MMCM}	Maximum input clock frequency ²	1150	1150	1070	984	800	680	MHz
F _{INMIN_MMCM}	Minimum input clock frequency	10	10	10	10	10	10	MHz
F _{INJITTER_MMCM}	Maximum input clock period jitter ³	< 20% of clock input period or 1 ns Max						
F _{INDUTY_MMCM}	Input duty cycle range: 10–49 MHz	25–75						%
	Input duty cycle range: 50–199 MHz	30–70						%
	Input duty cycle range: 200–399 MHz	35–65						%
	Input duty cycle range: 400–499 MHz	40–60						%
	Input duty cycle range: >500 MHz	45–55						%
F _{MAX_PCLK_MMCM}	Maximum dynamic phase shift clock frequency	550	500	500	450	500	450	MHz
F _{MIN_PCLK_MMCM}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F _{VCOMAX_MMCM}	Maximum MMCM VCO frequency	4320	4320	4320	4320	4320	4320	MHz
F _{VCOMIN_MMCM}	Minimum MMCM VCO frequency	2160	2160	2160	2160	2160	2160	MHz
F _{BANDWIDTH_MMCM}	Low MMCM bandwidth at typical ⁴	1.00	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁴	4.00	4.00	4.00	4.00	4.00	4.00	MHz
T _{STATPHAOFFSET_MMCM}	Static phase offset of the MMCM outputs ⁵	0.12	0.12	0.12	0.12	0.12	0.12	ns
T _{OUTJITTER_MMCM}	MMCM output jitter	Note 6						
T _{OUTDUTY_MMCM}	MMCM output clock duty cycle precision ⁷	0.165	0.20	0.20	0.20	0.20	0.20	ns
T _{LOCKMAX_MMCM}	MMCM maximum lock time (non deskew mode)	100	100	100	100	100	100	μs
T _{LOCKDESKEWMAX_MMCM}	MMCM maximum lock time in deskew mode	Note 8						
F _{OUTMAX_MMCM}	MMCM maximum output clock frequency ²	1150	1150	1070	984	800	680	MHz
F _{OUTMIN_MMCM}	MMCM minimum output clock frequency	5	5	5	5	5	5	MHz
T _{EXTFDVAR_MMCM}	External clock feedback variation	< 20% of clock input period or 1 ns Max						
T _{PWRDWNMINPULSE_MMCM}	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F _{PFDMAX_MMCM}	Maximum frequency at the phase frequency detector with bandwidth set to High or optimized	550	500	500	450	500	450	MHz
	Maximum frequency at the phase frequency detector with bandwidth set to Low	550	500	500	450	500	450	MHz
F _{PFDMIN_MMCM}	Minimum frequency at the phase frequency detector	10	10	10	10	10	10	MHz
T _{FBDELAY_MMCM}	Maximum delay in the feedback path ⁹	3 ns Max or one clock cycle						

Table 78: MMCM Specification (cont'd)

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L) ¹		
		-3	-2	-2	-1	-2	-1	
T _{DESKEWTAPDELAY_MMCM}	Nominal tap-delay of the programmable delay in the PD based deskew scheme	Note 10						

Notes:

1. The MMCM is powered by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).
2. The maximum input and output clock frequencies are limited by the global clock buffers. See [Table 77: Clock Buffers Switching Characteristics](#).
3. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the MMCM. Input jitter above ~1 MHz is reduced by the filtering properties of the MMCM. The magnitude of the reduction is found in the Vivado timing report.
4. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
5. The static offset is measured between any MMCM outputs with identical phase.
6. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
7. Includes global clock buffer.
8. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in ms = (0.208 x (VCO_frequency in MHz) / (CLKIN_DESKEW_frequency in MHz)²) + 0.1.
9. The parameter only applies to analog compensation.
10. The value for this parameter is included in compensation delay calculations.

DPLL Switching Characteristics

Table 79: DPLL Specification

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM}) ²						Units
		0.88V (H)		0.80V (M)		0.80V (L) ²		
		-3	-2	-2	-1	-2	-1	
F _{INMAX_DPLL}	Maximum input clock frequency ³	1150	1150	1070	984	800	680	MHz
F _{INMIN_DPLL}	Minimum input clock frequency	50	50	50	50	50	50	MHz
F _{INJITTER_DPLL}	Maximum input clock jitter ⁴	< 20% of clock input period or 1 ns Max						
F _{INDUTY_DPLL}	Input duty cycle range: 50–399 MHz	35–65						%
	Input duty cycle range: 400–499 MHz	40–60						%
	Input duty cycle range: >500 MHz	45–55						%
F _{PSCLKMAX_DPLL}	Maximum dynamic phase shift clock frequency	550	500	500	450	500	450	MHz
F _{PSCLKMIN_DPLL}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F _{DCOMAX_DPLL}	Maximum DPLL DCO frequency	4000	4000	4000	4000	4000	4000	MHz
F _{DCOMIN_DPLL}	Minimum DPLL DCO frequency	2000	2000	2000	2000	2000	2000	MHz
F _{BANDWIDTH_DPLL}	DPLL bandwidth at typical ⁵	1.00	1.00	1.00	1.00	1.00	1.00	MHz
T _{STATPHAOFFSET_DPLL}	Static phase offset of the DPLL outputs ⁶	0.12	0.12	0.12	0.12	0.12	0.12	ns
T _{OUTJITTER_DPLL}	DPLL output jitter	Note ⁷						
T _{OUTDUTY_DPLL}	DPLL output clock duty cycle precision ⁸	0.165	0.20	0.20	0.20	0.20	0.20	ns
T _{LOCKMAX_DPLL}	DPLL maximum lock time (non-deskew mode)	Note ⁹						
T _{LOCKDESKEWMAX_DPLL}	DPLL maximum lock time in deskew mode ¹⁰	Note ¹¹						
F _{OUTMAX_DPLL}	DPLL maximum output clock frequency ³	1150	1150	1070	984	800	680	MHz
F _{OUTMIN_DPLL}	DPLL minimum output clock frequency	5	5	5	5	5	5	MHz
T _{PWRDWNMINPULSE_DPLL}	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F _{TDCMAX_DPLL}	Maximum frequency at the time to digital converter	200	200	200	200	200	200	MHz
F _{TDCMIN_DPLL}	Minimum frequency at the time to digital converter	50	50	50	50	50	50	MHz

Table 79: DPLL Specification (cont'd)

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_RAM}) ²						Units
		0.88V (H)		0.80V (M)		0.80V (L) ²		
		-3	-2	-2	-1	-2	-1	
T _{DESKEWTAPDELAY_DPLL}	Nominal tap-delay of the programmable delay in the PD based deskew scheme ¹⁰	Note ¹²						

Notes:

1. In the VM1802 device, the DPLLs (DPLL_X3Y7 and DPLL_X12Y7 sites) at the HDIO banks are not supported. Thus, DPLL ZHOLD mode for HDIO is not supported in these devices.
2. The DPLLs are powered by the V_{CC_RAM} supply, except for the DPLLs at HDIO banks are powered by the V_{CCINT} supply. The V_{CC_RAM} supply operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).
3. The maximum input and output clock frequencies are limited by the global clock buffers. See [Table 77: Clock Buffers Switching Characteristics](#).
4. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the DPLL. Input jitter above ~1 MHz is reduced by the filtering properties of the DPLL. The magnitude of the reduction is found in the Vivado timing report.
5. The DPLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
6. The static offset is measured between any DPLL outputs with identical phase.
7. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
8. Includes global clock buffer.
9. The maximum lock time in non-deskew mode is given by the given formula: Lock time in non-deskew mode in ms = 153.6 × DIVCLK_DIVIDE / (CLKIN_FREQUENCY in MHz).
10. In the VM1802 device, the DPLL deskew functions are not supported.
11. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in ms = (0.208 × (VCO_frequency in MHz) / (CLKIN_DESKEW_frequency in MHz)²) + (maximum lock time in non-deskew mode in ms from Note 9).
12. The value for this parameter is included in compensation delay calculations.

XPLL Switching Characteristics

Table 80: XPLL Specification

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_IO})						Units
		0.88V (H)		0.80V (M)		0.80V (L) ¹		
		-3	-2	-2	-1	-2	-1	
F _{INMAX_XPLL}	Maximum input clock frequency ²	1150	1150	1070	984	800	680	MHz
F _{INMIN_XPLL}	Minimum input clock frequency	100	100	100	100	100	100	MHz
F _{INJITTER_XPLL}	Maximum input clock jitter ³	< 20% of clock input period or 1 ns Max						
F _{INDUTY_XPLL}	Allowable input duty cycle: 100–399 MHz	35–65						%
	Allowable input duty cycle: 400–499 MHz	40–60						%
	Allowable input duty cycle: >500 MHz	45–55						%
F _{PSCLKMAX_XPLL}	Maximum dynamic phase shift clock frequency	300	300	300	300	300	300	MHz
F _{PSCLKMIN_XPLL}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F _{VCOMAX_XPLL}	Maximum XPLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz
F _{VCOMIN_XPLL}	Minimum XPLL VCO frequency	2160	2160	2160	2160	2160	2160	MHz
F _{BANDWIDTH_XPLL}	XPLL bandwidth at typical ⁴	14.00	14.00	14.00	14.00	14.00	14.00	MHz
T _{STATPHAOFFSET_XPLL}	Static phase offset of the XPLL outputs ⁵	0.12	0.12	0.12	0.12	0.12	0.12	ns
T _{OUTJITTER_XPLL}	XPLL output jitter	Note ⁶						
T _{OUTDUTY_XPLL}	XPLL CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3 duty-cycle precision ⁷	0.125	0.15	0.15	0.15	0.15	0.15	ns
T _{LOCKMAX_XPLL}	XPLL maximum lock time (in non-deskew mode)	100	100	100	100	100	100	μs
T _{LOCKDESKEWMAX_XPLL}	XPLL maximum lock time in deskew mode	Note ⁸						
F _{OUTMAX_XPLL}	XPLL maximum output frequency at CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3 ^{2,9}	1150	1150	1070	984	800	680	MHz
	XPLL maximum output frequency at CLKOUTPHY	4266	4266	3933	3733	3933	3733	MHz
F _{OUTMIN_XPLL}	XPLL minimum output frequency at CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3	16.875	16.875	16.875	16.875	16.875	16.875	MHz
	XPLL minimum output frequency at CLKOUTPHY	200	200	200	200	200	200	MHz
T _{PWRDWNMINPULSE_XPLL}	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F _{PFDMAX_XPLL}	Maximum frequency at the phase frequency detector with bandwidth set to High optimized	667.5	667.5	667.5	667.5	667.5	667.5	MHz
F _{PFDMIN_XPLL}	Minimum frequency at the phase frequency detector	100	100	100	100	100	100	MHz

Table 80: XPLL Specification (cont'd)

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_IO})						Units
		0.88V (H)		0.80V (M)		0.80V (L) ¹		
		-3	-2	-2	-1	-2	-1	
T _{DESKEWTAPDELAY_XPLL}	Nominal tap-delay of the programmable delay in the PD based deskew scheme	Note 10						

Notes:

1. The XPLL is powered by the V_{CC_IO} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).
2. The maximum input clock frequency and output clock frequency at CLKOUT0, CLKOUT1, CLKOUT2, and CLKOUT3 are limited by the global clock buffers. See [Table 77: Clock Buffers Switching Characteristics](#).
3. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the XPLL. Input jitter above ~1 MHz is reduced by the filtering properties of the XPLL. The magnitude of the reduction is found in the Vivado timing report.
4. The XPLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
5. The static offset is measured between any XPLL outputs with identical phase.
6. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
7. Includes global clock buffer.
8. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in μ s = $(208 \times (\text{VCO_frequency in MHz}) / (\text{CLKIN_DESKEW_frequency in MHz})^2 + 100)$.
9. XPLL CLKOUTs F_{MAX} is increased in the -1L/-2L speed grade when it directly drives the memory controller at a 1/4 x DDR bit rate. Refer to the DDR bit rate in [Table 84: Maximum Physical Interface \(PHY\) Rate for Integrated Memory Interface Controller](#).
10. The value for this parameter is included in compensation delay calculations.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 81: Global Clock Input to Output Delay With MMCM (Internal Mode)

Symbol	Description ^{1, 2}	Device	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})								Units
			0.88V (H)		0.80V (M)			0.725V (L)	0.70V (L)		
			-3	-2	-2	-1	-1MM	-2LLI	-2LSE -2LLE	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM											
T _{ICKOFFMMCM}	Global clock input and output flip-flop <i>with</i> MMCM	XCVM1102	N/A	6.08	6.60	7.06	N/A	7.27	7.33	7.94	ns
		XQVM1102	N/A	N/A	6.60	7.06	7.11	N/A	N/A	7.94	ns
		XCVM1302	N/A	6.29	6.82	7.27	N/A	7.48	7.49	8.08	ns
		XCVM1402	N/A	6.74	7.30	7.76	N/A	7.96	7.96	8.56	ns
		XQVM1402	N/A	N/A	7.30	7.76	7.83	N/A	N/A	8.56	ns
		XCVM1502	N/A	6.97	7.52	7.98	N/A	8.21	8.21	8.81	ns
		XQVM1502	N/A	N/A	7.52	7.98	8.04	N/A	N/A	8.81	ns
		XCVM1802	N/A	7.37	8.07	8.56	N/A	8.73	8.73	9.37	ns
		XQVM1802	N/A	N/A	8.07	8.56	8.67	N/A	N/A	9.37	ns
		XCVM2152	N/A	7.86	8.63	9.07	N/A	N/A	9.76	10.44	ns
		XCVM2202	N/A	6.73	7.31	7.78	N/A	8.00	8.00	8.61	ns
		XCVM2302	5.69	N/A	6.26	6.56	N/A	N/A	6.33	6.64	ns
		XCVM2502	5.87	N/A	6.52	6.87	N/A	N/A	6.52	6.89	ns
		XCVM2902	7.18	N/A	7.78	8.25	N/A	N/A	8.47	9.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 82: Global Clock Input Setup and Hold With MMCM (Internal Mode)

Symbol	Description	Device	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})									Units
			0.88V (H)		0.80V (M)			0.725V (L)	0.70V (L)			
			-3	-2	-2	-1	-1MM	-2LLI	-2LSE -2LLE	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. ^{1, 2, 3}												
T _{SUMMCM_VM1102}	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCVM1102	N/A	-0.49	-0.51	-0.51	N/A	-0.51	-0.48	-0.48	ns
T _{HMMCM_VM1102}		Hold		N/A	2.78	3.01	3.12	N/A	3.05	3.05	3.19	ns
T _{SUMMCM_XQ_VM1102}		Setup	XQVM1102	N/A	N/A	-0.51	-0.51	-0.48	N/A	N/A	-0.48	ns
T _{HMMCM_XQ_VM1102}		Hold		N/A	N/A	3.01	3.12	3.31	N/A	N/A	3.19	ns
T _{SUMMCM_VM1302}		Setup	XCVM1302	N/A	-0.62	-0.65	-0.65	N/A	-0.57	-0.59	-0.59	ns
T _{HMMCM_VM1302}		Hold		N/A	3.61	4.16	4.30	N/A	3.87	4.17	4.32	ns
T _{SUMMCM_VM1402}		Setup	XCVM1402	N/A	-0.65	-0.69	-0.69	N/A	-0.61	-0.63	-0.63	ns
T _{HMMCM_VM1402}		Hold		N/A	3.97	4.56	4.70	N/A	4.26	4.56	4.72	ns
T _{SUMMCM_XQ_VM1402}		Setup	XQVM1402	N/A	N/A	-0.69	-0.69	-0.65	N/A	N/A	-0.63	ns
T _{HMMCM_XQ_VM1402}		Hold		N/A	N/A	4.56	4.70	4.74	N/A	N/A	4.72	ns
T _{SUMMCM_VM1502}		Setup	XCVM1502	N/A	-0.67	-0.68	-0.68	N/A	-0.62	-0.64	-0.64	ns
T _{HMMCM_VM1502}		Hold		N/A	3.79	4.43	4.56	N/A	4.17	4.47	4.63	ns
T _{SUMMCM_XQ_VM1502}		Setup	XQVM1502	N/A	N/A	-0.68	-0.68	-0.64	N/A	N/A	-0.64	ns
T _{HMMCM_XQ_VM1502}		Hold		N/A	N/A	4.43	4.56	4.59	N/A	N/A	4.63	ns
T _{SUMMCM_VM1802}		Setup	XCVM1802	N/A	-0.90	-0.97	-0.97	N/A	-0.91	-0.93	-0.93	ns
T _{HMMCM_VM1802}		Hold		N/A	4.16	4.80	4.98	N/A	4.81	4.80	5.00	ns
T _{SUMMCM_XQ_VM1802}		Setup	XQVM1802	N/A	N/A	-0.97	-0.97	-0.93	N/A	N/A	-0.93	ns
T _{HMMCM_XQ_VM1802}		Hold		N/A	N/A	4.80	4.98	5.06	N/A	N/A	5.00	ns
T _{SUMMCM_VM2152}		Setup	XCVM2152	N/A	-0.43	-0.47	-0.47	N/A	N/A	-0.44	-0.44	ns
T _{HMMCM_VM2152}		Hold		N/A	4.01	4.41	4.55	N/A	N/A	4.64	4.83	ns

Table 82: Global Clock Input Setup and Hold With MMCM (Internal Mode) (cont'd)

Symbol	Description		Device	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})								Units
				0.88V (H)		0.80V (M)			0.725V (L)	0.70V (L)		
				-3	-2	-2	-1	-1MM	-2LLI	-2LSE -2LLE	-1	
T _{SUMMCM_VM2202}	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCVM2202	N/A	-0.62	-0.66	-0.66	N/A	-0.62	-0.62	-0.62	ns
T _{HMMCM_VM2202}		Hold		N/A	3.80	4.13	4.27	N/A	4.13	4.17	4.34	ns
T _{SUMMCM_VM2302}		Setup	XCVM2302	-0.94	N/A	-0.94	-0.94	N/A	N/A	-0.97	-0.97	ns
T _{HMMCM_VM2302}		Hold		4.04	N/A	4.40	4.57	N/A	N/A	4.47	4.65	ns
T _{SUMMCM_VM2502}		Setup	XCVM2502	-1.01	N/A	-1.02	-1.02	N/A	N/A	-1.02	-1.07	ns
T _{HMMCM_VM2502}		Hold		4.27	N/A	4.71	4.93	N/A	N/A	4.71	4.94	ns
T _{SUMMCM_VM2902}		Setup	XCVM2902	-0.98	N/A	-1.03	-1.03	N/A	N/A	-1.00	-1.00	ns
T _{HMMCM_VM2902}		Hold		4.54	N/A	4.93	5.12	N/A	N/A	5.00	5.20	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 83: Package Skew

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew ^{1, 2}	XCVM1102	SFVA784	103	ps
		XQVM1102	SSRA784	103	ps
		XCVM1302	NBVB1024	160	ps
			NSVF1369	135	ps
			VFVC1596	132	ps
			VSVD1760	289	ps
		XCVM1402	NBVB1024	165	ps
			NSVF1369	162	ps
			VFVC1596	132	ps
			VSVD1760	312	ps
		XQVM1402	VSRC1596	132	ps
			VSVD1760	312	ps
		XCVM1502	NFVB1369	254	ps
			VFVC1760	221	ps
			VSVA2197	137	ps
		XQVM1502	VSRA2197	137	PS
		XCVM1802	VFVC1760	214	ps
			VSVD1760	211	ps
			VSVA2197	111	ps
		XQVM1802	VSVD1760	211	ps
			VSRA2197	111	ps
		XCVM2152	NFVD1024	188	ps
			NFVM1369	165	ps
		XCVM2202	NSVH1369	164	ps
		XCVM2302	VFVF1760	83	ps
		XCVM2502	VSVI1760	229	ps
		XCVM2902	VFVF1760	85	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

DDR4 and LPDDR4/4X Memory Interface Controller

The following table provides the maximum data rates for applicable memory standards using the Versal Prime device memory PHY. Refer to *Versal Adaptive SoC Programmable Network on Chip and Integrated Memory Controller LogiCORE IP Product Guide* ([PG313](#)) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *Versal Adaptive SoC PCB Design User Guide* ([UG863](#)), electrical analysis, and characterization of the system.

Table 84: Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller

Memory Standard	DRAM Type	DIMM Slots	XPIO Bank Performance ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_SOC})						Units
				0.88V (H)		0.80V (M)		0.80V (L) ²		
				-3	-2	-2	-1	-2	-1	
DDR4	Single rank component ³		All	3200	3200	3200	3200	3200	3200	Mb/s
	1 rank DIMM ⁴ , LRDIMM ⁵	1	All	3200	3200	3200	3200	3200	3200	Mb/s
	2 rank DIMM ⁴	1	All	2933	2933	2933	2933	2933	2933	Mb/s
	1 rank RDIMM, 2 rank LRDIMM	2	All	2667	2667	2667	2667	2667	2667	Mb/s
	2 rank RDIMM	2	All	2133	2133	2133	2133	2133	2133	Mb/s
LPDDR4 LPDDR4X ⁶	Single rank component		High	4266	4266	3933	3733	3933	3733	Mb/s
			Medium	4266	4266	3933	3733	3933	3733	Mb/s
			Low	3200	3200	3200	3200	3200	3200	Mb/s
	Dual rank component		High	3733	3733	3733	3733	3733	3733	Mb/s
			Medium	3733	3733	3733	3733	3733	3733	Mb/s
			Low	2933	2933	2933	2933	2933	2933	Mb/s

Notes:

1. The Versal device/package pinout files specify XPIO bank performance (XPIOPerf). See the ASCII package files information in the *Versal Adaptive SoC Packaging and Pinouts Architecture Manual* ([AM013](#)).
2. The integrated DDRMC is powered by the V_{CC_SOC} supply that operates at 0.80V in low (L) voltage operation, see [Table 4: Available Speed Grades and Operating Voltages](#).
3. For DDR4 DDP deep components, the maximum data rate is 2933 Mb/s for five or less DDP devices across all speed grades and temperature grades. For six or more DDP deep devices, the maximum data rate is 2133 Mb/s across all speed grades and temperature grades. For DDR4 DDP wide components, use single rank component data rates.
4. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
5. Includes 2 and 4 rank LRDIMM.
6. For LPDDR4/4X, use the Vivado tool to determine the maximum performance by package and I/O bank combination.

DDR5 and LPDDR5 Memory Interface Controller for the XCVM2152 Only

The following table provides the maximum data rates for applicable memory standards using the Versal Prime device memory PHY. Refer to the *Programmable Network on Chip and Integrated DDR5/ LPDDR5 Memory Controller* (PG406) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *Versal Adaptive SoC PCB Design User Guide* (UG863), electrical analysis, and characterization of the system.

Table 85: Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller

Memory Standard	DRAM Type	DIMM Slots	Performance as a Function of Speed Grade and Operating Voltage (V _{CC_SOC})					Units
			0.88V (H)	0.80V (M)		0.80V (L) ¹		
			-2	-2	-1	-2	-1	
DDR5	Single rank component		5600	5600	5600	5600	5600	Mb/s
	1 rank DIMM ²	1	5600	5600	5600	5600	5600	Mb/s
	2 rank DIMM ²	1	5200	5200	5200	5200	5200	Mb/s
	1 rank RDIMM	2	5600	5600	5600	5600	5600	Mb/s
	2 rank RDIMM	2	5200	5200	5200	5200	5200	Mb/s
LPDDR5	Single rank component for VM2152		6400	6400	6400	6400	6400	Mb/s
	Single rank component for all other devices		6400	6400	5600	6400	5600	Mb/s
	Dual rank component for VM2152		6000	6000	6000	6000	6000	Mb/s
	Dual rank component		6000	6000	5200	6000	5200	Mb/s

Notes:

1. The integrated DDRMC is powered by the V_{CC_SOC} supply that operates at 0.80V in low (L) voltage operation, see [Table 4](#).
2. Dual in-line memory module (DIMM) includes SODIMM and UDIMM.

GTM Transceiver Specifications

The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists the Versal Prime devices that include the GTM transceivers.

GTM Transceiver DC Input and Output Levels

The following table summarizes the DC specifications of the GTM transceivers in Versal Prime devices. Consult the *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)) for further details.

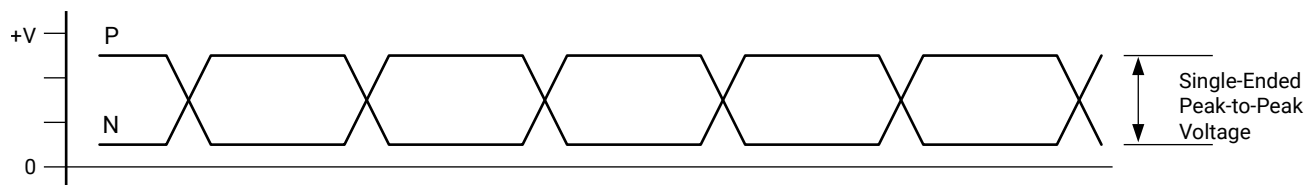
Table 86: GTM Transceiver DC Specifications

Symbol	DC Parameter	Conditions		Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	PAM4		600	–	900	mV
		NRZ		150	–	900	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ¹	Transmitter output swing is set to 1000100		800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC (equation based)	When remote RX is terminated to float	TX output swing ≥ 800 mV	$V_{AVCCAUX} - D_{VPPOUT}/2$			mV
			TX output swing < 800 mV	$V_{AVTT} - V_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ²	TX output swing ≥ 800 mV	$V_{AVCCAUX} - D_{VPPOUT}/4 - (V_{AVCCAUX} - V_{RX_TERM})/2$			mV
			TX output swing < 800 mV	$V_{AVTT} - D_{VPPOUT}/4 - (V_{AVTT} - V_{RX_TERM})/2$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based		$V_{AVCCAUX} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance			–	100	–	Ω
R _{OUT}	Differential output resistance			–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew			–	–	3.7	ps
C _{EXT}	Recommended external AC coupling capacitor ³			–	100	–	nF

Notes:

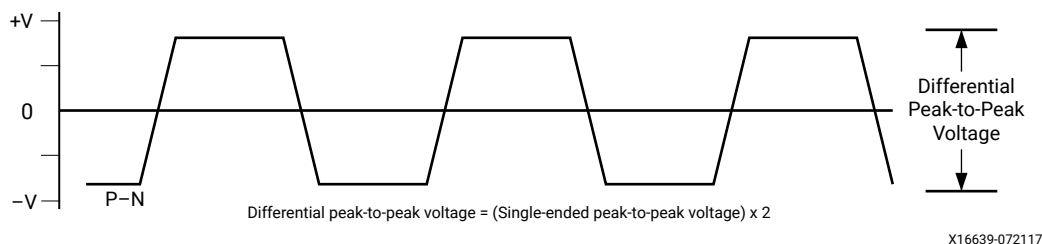
1. The output swing and pre-emphasis levels are programmable using the GTM transceiver attributes discussed in the *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage. The V_{RX_TERM} must be within 7% of the calculated value for V_{CMOUTDC} terminated to float.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 1: Single-Ended Peak-to-Peak Voltage



X16653-072117

Figure 2: Differential Peak-to-Peak Voltage



The following tables summarize the DC specifications of the clock input/output levels of the GTM transceivers in Versal Prime devices. Consult the *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)) for further details.

Table 87: GTM Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	1600	mV
V_{ICM}	REFCLK common-mode input voltage	–	V_{GTM_AVCC}	–	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 88: GTM Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

GTM Transceiver Switching Characteristics

Consult the *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)) for further information.

GTM Transceiver Performance

Table 89: GTM Transceiver Performance

Symbol	Description	Output Divider	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})								Units
			0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)			
			-3	-2	-2	-1	-2LLI	-2	-1		
			Max	Max	Max	Max	Max	Max	Max		
F _{GTMPAM41MAX}	GTM transceiver PAM4 maximum line rate for -3HSE, -2HSE, -2MSE, -2MLE, or -2LSE only. R _{XPPMTOL} = ±150 ppm. See Table 97 .	1 ²	112.00 ¹	112.00 ¹	112.00 ¹	N/A	N/A	112.00 ¹	N/A	Gb/s	
	GTM transceiver PAM4 maximum line rate. R _{XPPMTOL} = R _{XPPMTOL} = ±200 ppm. See Table 97 .		106.25	106.25	106.25	N/A	N/A	106.25	N/A	Gb/s	
F _{GTMPAM41MIN}	GTM transceiver PAM4 minimum line rate		76.00	76.00	76.00	N/A	N/A	76.00	N/A	Gb/s	
F _{GTMPAM42MAX}	GTM transceiver PAM4 maximum line rate	2 ^{3, 5}	58.00	56.42	56.42	53.125	56.42	56.42	53.125	Gb/s	
F _{GTMPAM42MIN}	GTM transceiver PAM4 minimum line rate		38.00	38.00	38.00	38.00	38.00	38.00	38.00	Gb/s	
F _{GTMPAM44MAX}	GTM transceiver PAM4 maximum line rate	4 ^{4, 5}	29.00	28.21	28.21	26.5625	28.21	28.21	26.5625	Gb/s	
F _{GTMPAM44MIN}	GTM transceiver PAM4 minimum line rate		19.00	19.00	19.00	19.00	19.00	19.00	19.00	Gb/s	
F _{GTMNRZ2MAX}	GTM transceiver NRZ maximum line rate	2 ⁶	29.00	28.21	28.21	26.5625	28.21	28.21	26.5625	Gb/s	
F _{GTMNRZ2MIN}	GTM transceiver NRZ minimum line rate		19.00	19.00	19.00	19.00	19.00	19.00	19.00	Gb/s	
F _{GTMNRZ4MAX}	GTM transceiver NRZ maximum line rate	4 ^{6, 7}	15.00	15.00	15.00	15.00	15.00	15.00	15.00	Gb/s	
F _{GTMNRZ4MIN}	GTM transceiver NRZ minimum line rate		9.50	9.50	9.50	9.50	9.50	9.50	9.50	Gb/s	

Notes:

1. Refer to the *Versal Adaptive SoC GTM Transceivers Architecture Manual (AM017)* and *Versal Adaptive SoC Packaging and Pinouts Architecture Manual (AM013)* for guidelines when using GTM transceivers targeting 112G long-reach (LR) applications.
2. Measured at BER of 10^{-5} .
3. For PAM4, data rates from F_{GTMPAM42MAX} to 76.00 Gb/s are not available.
4. For PAM4, data rates from F_{GTMPAM44MAX} to 38.00 Gb/s are not available.
5. Measured at BER of 10^{-6} .
6. Measured at BER of 10^{-12} .
7. For NRZ, data rates from F_{GTMNRZ4MAX} to 19 Gb/s are not available.

GTM Transceiver Configuration Interface Port Switching Characteristics

Table 90: GTM Transceiver Configuration Interface Port (APB3) Switching Characteristics

Symbol	Description	All Speed Grades		Units
		Min	Max	
F _{GTMAPB3}	GTMAPB3CLK maximum frequency	100	300	MHz

GTM Transceiver Reference Clock Switching Characteristics

Table 91: GTM Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK} ¹	Reference clock frequency range ¹		60	–	820	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Notes:

1. The frequency values apply when the reference clock buffer is configured as either an input or output.

GTM Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Table 92: GTM Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description ^{1, 2}	Offset Frequency	Min	Typ	Max	Units
LCPLL _{REFCLK} MASK	LCPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	LCPLL0 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	LCPLL0 reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol.

GTM Transceiver Digital Monitor Clock

Table 93: GTM Transceiver Digital Monitor Port Switching Characteristics

Symbol	Description	All Speed Grades		Units
		Min	Max	
F _{GTMDMONITORCLK_INPUT}	GTM transceiver digital monitor port input maximum frequency	100	500	MHz
F _{GTMDMONITORCLK_OUTPUT}	GTM transceiver digital monitor port output maximum frequency	100	500	MHz

GTM Transceiver PLL/Lock Time Adaptation

Table 94: GTM Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions		All Speed Grades			Units
				Min	Typ	Max	
T _{LOCK}	Initial PLL lock	Reference clock frequency ≥ 200 MHz		–	–	3	ms
		Reference clock frequency < 200 MHz		–	–	5.7	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time	PAM4 (<39 Gb/s)	Short reach (IL < 12db)	–	6.21×10 ¹⁰	–	UI
			Long reach (IL ≥ 12db)	–	7.71×10 ⁹	–	UI
		PAM4 (≥39 Gb/s)	Short reach (IL < 12db)	–	4×10 ¹⁰	–	UI
			Long reach (IL ≥ 12db)	–	1.54×10 ¹⁰	–	UI
		NRZ		–	1.54×10 ¹⁰	–	UI

GTM Transceiver User Clock Switching Characteristics

Table 95: GTM Transceiver User Clock Switching Characteristics

Symbol	Description ¹		Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units	
					0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
			Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2LLI	-2		-1
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA				906.25	881.56	881.56	830.08	881.56	881.56	830.08	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA				725.00	705.25	705.25	664.06	705.25	705.25	664.06	MHz
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK				906.25	881.56	881.56	830.08	881.56	881.56	830.08	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK				725.00	705.25	705.25	664.06	705.25	705.25	664.06	MHz
F _{TXIN}	TXUSRCLK maximum frequency	PAM4	128	64	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				80	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				128	664.063	664.063	664.063	415.039	440.781	664.063	415.039	MHz
				160	664.063	664.063	664.063	332.031	352.625	664.063	332.031	MHz
				256	437.500	437.500	437.500	207.520	220.391	437.500	207.520	MHz
				320	350.000	350.000	350.000	166.016	176.313	350.000	166.016	MHz
				512	218.750	218.750	218.750	103.760	110.195	218.750	103.760	MHz
		NRZ	64	32	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				40	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				64	453.125	440.781	440.781	415.039	440.781	440.781	415.039	MHz
				80	362.500	352.625	352.625	332.031	352.625	352.625	332.031	MHz
				128	226.563	220.391	220.391	207.520	220.391	220.391	207.520	MHz
				160	181.250	176.313	176.313	166.016	176.313	176.313	166.016	MHz
				256	113.281	110.195	110.195	103.760	110.195	110.195	103.760	MHz

Table 95: GTM Transceiver User Clock Switching Characteristics (cont'd)

Symbol	Description ¹		Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
					0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
			Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2LLI	-2	-1	
F _{RXIN}	RXUSRCLK maximum frequency	PAM4	160	64	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				80	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				128	664.063	664.063	664.063	415.039	440.781	664.063	415.039	MHz
				160	664.063	664.063	664.063	332.031	352.625	664.063	332.031	MHz
				256	437.500	437.500	437.500	207.520	220.391	437.500	207.520	MHz
				320	350.000	350.000	350.000	166.016	176.313	350.000	166.016	MHz
				512	218.750	218.750	218.750	103.760	110.195	218.750	103.760	MHz
		NRZ	80	32	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				40	664.063	664.063	664.063	664.063	664.063	664.063	664.063	MHz
				64	453.125	440.781	440.781	415.039	440.781	440.781	415.039	MHz
				80	362.500	352.625	352.625	332.031	352.625	352.625	332.031	MHz
				128	226.563	220.391	220.391	207.520	220.391	220.391	207.520	MHz
				160	181.250	176.313	176.313	166.016	176.313	176.313	166.016	MHz
				256	113.281	110.195	110.195	103.760	110.195	110.195	103.760	MHz

Notes:

- Clocking must be implemented as described in the *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)).

GTM Transceiver Transmitter and Receiver Switching Characteristics

Table 96: GTM Transceiver Transmitter Switching Characteristics

Symbol	Description	Conditions		Min	Typ	Max	Units
F _{GTMPAM4TX}	Transmitter PAM4 serial data rate range			19.0	–	F _{GTMPAM4MAX} ¹	Gb/s
F _{GTMNRZTX}	Transmitter NRZ serial data rate range			9.5	–	F _{GTMNRZMAX}	Gb/s
T _{SLEW}	TX slew rate			–	4.76×10 ⁴	–	V/μs
T _{J3U112_PAM4}	TX uncorrelated jitter ^{2,3} @10 ^{–3}	PAM4	112 Gb/s	–	–	0.125	UI
T _{J3U03112_PAM4}	TX uncorrelated jitter on edge 0–3 ^{2,3} @10 ^{–3}			–	–	0.115	UI
T _{EOJ112_PAM4}	TX even-odd jitter			–	0.015	–	UI
T _{J3U106.25_PAM4}	TX uncorrelated jitter ^{2,3} @10 ^{–3}	PAM4	106.25 Gb/s	–	–	0.125	UI
T _{J3U03106.25_PAM4}	TX uncorrelated jitter on edge 0–3 ^{2,3} @10 ^{–3}			–	–	0.115	UI
T _{EOJ106.25_PAM4}	TX even-odd jitter			–	–	0.025	UI
T _{J4U76_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	76 Gb/s	–	–	0.128	UI
T _{J4U0376_PAM4}	TX uncorrelated jitter on edge 0–3 @10 ^{–4}			–	–	0.118	UI
T _{EOJ76_PAM4}	TX even-odd jitter			–	–	0.025	UI
T _{J4U58_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	58 Gb/s	–	–	0.118	UI
T _{EOJ58_PAM4}	TX even-odd jitter			–	–	0.025	UI
T _{J4U56.5_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	56.5 Gb/s	–	–	0.118	UI
T _{EOJ56.5_PAM4}	TX even-odd jitter			–	–	0.019	UI
T _{J4U53.125_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	53.125 Gb/s	–	–	0.118	UI
T _{EOJ53.125_PAM4}	TX even-odd jitter			–	–	0.019	UI
T _{J4U28.21_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	28.21 Gb/s	–	–	0.118	UI
T _{EOJ28.21_PAM4}	Deterministic jitter			–	–	0.019	UI
T _{J4U19_PAM4}	TX uncorrelated jitter @10 ^{–4}	PAM4	19 Gb/s	–	–	0.118	UI
T _{EOJ19_PAM4}	Deterministic jitter			–	–	0.019	UI
T _{J29_NRZ}	Total jitter ⁴	NRZ	29 Gb/s	–	–	0.28	UI
D _{J29_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI
T _{J28.21_NRZ}	Total jitter ⁴	NRZ	28.21 Gb/s	–	–	0.28	UI
D _{J28.21_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI
T _{J26.5625_NRZ}	Total jitter ⁴	NRZ	26.5625 Gb/s	–	–	0.28	UI
D _{J26.5625_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI
T _{J25.78125_NRZ}	Total jitter ⁴	NRZ	25.78125 Gb/s	–	–	0.28	UI
D _{J25.78125_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI
T _{J24_NRZ}	Total jitter ⁴	NRZ	24 Gb/s	–	–	0.28	UI
D _{J24_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI
T _{J19.6_NRZ}	Total jitter ⁴	NRZ	19.6 Gb/s	–	–	0.28	UI
D _{J19.6_NRZ}	Deterministic jitter ⁴			–	–	0.17	UI

Table 96: GTM Transceiver Transmitter Switching Characteristics (cont'd)

Symbol	Description	Conditions		Min	Typ	Max	Units
T _{J9.5_NRZ}	Total jitter ⁴	NRZ	9.5 Gb/s	-	-	0.28	UI
D _{J9.5_NRZ}	Deterministic jitter ⁴			-	-	0.17	UI

Notes:

1. See [GTM Transceiver Performance](#) for maximum supported line rate.
2. Using LCPLL FBDIV = 32.
3. Setup with -11 dB channel loss at Nyquist.
4. NRZ jitter values are based on a bit-error ratio of 10⁻¹².

Table 97: GTM Transceiver Receiver Switching Characteristics

Symbol	Description	Conditions		Min	Typ	Max	Units
F _{GTMPAM4RX}	Receiver PAM4 serial data rate range			19.0	-	F _{GTMPAM4MAX} ¹	Gb/s
F _{GTMRZR}	Receiver NRZ serial data rate range			9.5	-	F _{GTMRZMAX}	Gb/s
R _{XRL}	Run length (CID)			-	-	128	UI
R _{XPMTOL}	Data/REFCLK PPM offset tolerance ≤106.25 Gb/s			-200	-	200	ppm
	Data/REFCLK PPM offset tolerance >106.25 Gb/s			-150	-	150	ppm
SJ Jitter Tolerance^{2, 3, 4}							
J _{T_SJ112_PAM4}	Sinusoidal jitter	PAM4	112 Gb/s ⁵	0.05	-	-	UI
J _{T_SJ106_PAM4}	Sinusoidal jitter	PAM4	106 Gb/s	0.05	-	-	UI
J _{T_SJ76_PAM4}	Sinusoidal jitter	PAM4	76 Gb/s	0.05	-	-	UI
J _{T_SJ58_PAM4}	Sinusoidal jitter	PAM4	58 Gb/s	0.05	-	-	UI
J _{T_SJ56.5_PAM4}	Sinusoidal jitter	PAM4	56.5 Gb/s	0.05	-	-	UI
J _{T_SJ53.125_PAM4}	Sinusoidal jitter	PAM4	53.125 Gb/s	0.05	-	-	UI
J _{T_SJ48_PAM4}	Sinusoidal jitter	PAM4	48 Gb/s	0.05	-	-	UI
J _{T_SJ39.2_PAM4}	Sinusoidal jitter	PAM4	39.2 Gb/s	0.05	-	-	UI
J _{T_SJ20.6_PAM4}	Sinusoidal jitter	PAM4	20.6 Gb/s	0.05	-	-	UI
J _{T_SJ29_NRZ}	Sinusoidal jitter	NRZ	29 Gb/s	0.3	-	-	UI
J _{T_SJ25.78125_NRZ}	Sinusoidal jitter	NRZ	25.78125 Gb/s	0.3	-	-	UI
J _{T_SJ19.6_NRZ}	Sinusoidal jitter	NRZ	19.6 Gb/s	0.3	-	-	UI
J _{T_SJ10.3_NRZ}	Sinusoidal jitter	NRZ	10.3 Gb/s	0.3	-	-	UI
J _{T_SJ9.5_NRZ}	Sinusoidal jitter	NRZ	9.5 Gb/s	0.3	-	-	UI

Notes:

1. See [GTM Transceiver Performance](#) for maximum supported line rate.
2. PAM4 values are measured at a bit error ratio of 10⁻⁶ for line rates ≤76 Gb/s and 10⁻⁵ for line rates >76 Gb/s.
3. NRZ values are based on a bit error ratio of 10⁻¹².
4. The frequency of the injected sinusoidal jitter is 20 MHz.
5. Only supported in -3HSE, -2MSE, -2MLE, -2LSE, and -2LLE devices.

GTM Transceiver Electrical Compliance

The *Versal Adaptive SoC GTM Transceivers Architecture Manual* ([AM017](#)) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 98: GTM Transceiver Protocol List

Protocol	Specification	Modulation	Serial Rate (Gb/s)	Electrical Compliance
400GAUI-4	IEEE 802.3ck 120F/120G D3.3	PAM4	106.25	Compliant
200GAUI-2	IEEE 802.3ck 120F/120G D3.3	PAM4	106.25	Compliant
100GAUI-1	IEEE 802.3ck 120F/120G D3.3	PAM4	106.25	Compliant
400GBASE-CR4/KR4	IEEE 802.3ck 162/163 D3.3	PAM4	106.25	Compliant
200GBASE-CR2/KR2	IEEE 802.3ck 162/163 D3.3	PAM4	106.25	Compliant
100GBASE-CR/KR	IEEE 802.3ck 162/163 D3.3	PAM4	106.25	Compliant
400GAUI-8	IEEE 802.3bs 120D/120E	PAM4	53.125	Compliant
200GAUI-4	IEEE 802.3bs 120D/120E	PAM4	53.125	Compliant
100GAUI-2	IEEE 802.3cd 135G/135F	PAM4	53.125	Compliant
50GAUI-1	IEEE 802.3cd 135G/135F	PAM4	53.125	Compliant
200GBASE-KR4	IEEE 802.3cd 137	PAM4	53.125	Compliant
200GBASE-CR4	IEEE 802.3cd 136A	PAM4	53.125	Compliant
100GBASE-KR2	IEEE 802.3cd 137	PAM4	53.125	Compliant
100GBASE-CR2	IEEE 802.3cd 136A	PAM4	53.125	Compliant
50GBASE-KR	IEEE 802.3cd 137	PAM4	53.125	Compliant
50GBASE-CR	IEEE 802.3cd 136A	PAM4	53.125	Compliant
CAUI-4	IEEE 802.3bm 83D/83E	NRZ	25.78125	Compliant
50GAUI-2	IEEE 802.3cd 135D/135E	NRZ	26.5625	Compliant
LAUI-2	IEEE 802.3cd 135B/135C	NRZ	25.78125	Compliant
25GAUI-1	IEEE 802.3cd 109A/109B	NRZ	27.78125	Compliant
100GBASE-KR4	IEEE 802.3bj 93.8	NRZ	25.78125	Compliant
100GBASE-CR4	IEEE 802.3bj 92A	NRZ	25.78125	Compliant
25GBASE-KR	IEEE 802.3by 111	NRZ	25.78125	Compliant
25GBASE-CR	IEEE 802.3by 110	NRZ	25.78125	Compliant
XLPP1	IEEE 802.3 86A	NRZ	10.3125	Compliant
40GBASE-CR4	IEEE 802.3 85A	NRZ	10.3125	Compliant
10GBASE-SR/LR	SFF8431	NRZ	10.3125	Compliant
10GBASE-KR	IEEE 802.3 72	NRZ	10.3125	Compliant
CEI-56G-VSR/MR/LR-PAM4	Common Electrical (I/O) CEI 4.0	PAM4	39.2-58	Compliant
CEI-25G/28G-VSR/MR/LR	Common Electrical (I/O) CEI 4.0	NRZ	19.9-28.1	Compliant
CEI-11G-SR/MR/LR	Common Electrical (I/O) CEI 4.0	NRZ	10.3-11.2	Compliant
10G-15G backplane capability	10G NRZ interfaces over backplanes that fall within the high-confidence region defined by IEEE 802.3 Clause 72	NRZ	15	Compliant
28.21G PAM4 backplanes	Insertion loss @ Nyquist (7.05 GHz) at BER < 10e ⁻¹⁷ with FEC	PAM4	28.21	Compliant
58G PAM4 backplanes	IEEE 802.3bj style backplanes and copper cables at 58 Gb/s (35 dB with RS (544, 514) FEC)	PAM4	58	Compliant
OTU4 optical modules NRZ optical 7% FEC	100G OTU4 and OTUCn requirements to CFP2, CFP4, and QSFP28 optics, OIF-CEI28-VSR	NRZ	28.21	Compliant
OTU4 optical module PAM4 optical 7% FEC	100G QSFP56, OIF-CEI56-VSR	PAM4	56.4	Compliant
Interlaken 25.78125G	OIF-CEI-25G-MR @ 20 dB loss	NRZ	25.78125	Compliant

Table 98: GTM Transceiver Protocol List (cont'd)

Protocol	Specification	Modulation	Serial Rate (Gb/s)	Electrical Compliance
Interlaken 12.5G	OIF-CEI-11G-SR (extended)	NRZ	12.5	Compliant
CPRI 48G PAM4	Fibre channel datapath and 1-lane FEC with customer alignment implemented in logic with 64b/66b encoding	PAM4	48	Compliant
CPRI 24G, 12G, and 10.1G NRZ	CPRI_v_6_1_2014-07-01	NRZ	24, 12	Compliant

Notes:

1. Requires lock to reference on a per-lane basis and oversampling logic in the device logic to capture the slower auto-negotiation.

GTY and GTYP Transceiver Specifications

The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists the Versal Prime devices that include the GTY and GTYP transceivers.

GTY and GTYP Transceiver DC Input and Output Levels

The following table summarizes the DC specifications of the GTY and GTYP transceivers in Versal Prime devices. Consult the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002) for further details.

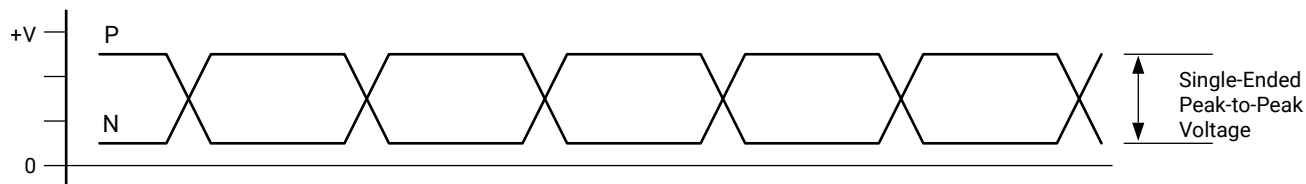
Table 99: GTY and GTYP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{GTY_AVTT} = 1.2V	–200	–	V _{GTY_AVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{GTY_AVTT} = 1.2V	–	2/3 V _{GTY_AVTT}	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ¹	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based) ²	When remote RX termination is floating	DV _{PPOUT} /2			mV
		When remote RX is terminated to V _{RX_TERM} ³	V _{RX_TERM} /2 + DV _{PPOUT} /4			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	DV _{PPOUT} /2			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁴		–	100	–	nF

Notes:

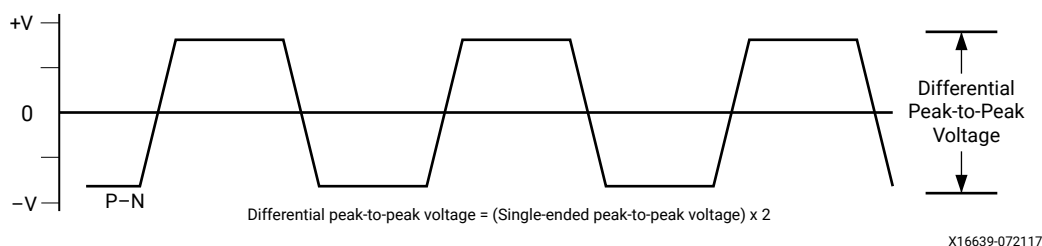
- The output swing and pre-emphasis levels are programmable using the GTY and GTYP transceiver attributes discussed in the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002) and can result in values lower than reported in this table.
- Remote RX termination = GND is not supported.
- V_{RX_TERM} is the remote RX termination voltage. V_{CMOUTDC_VRXTERM} should be less than 0.92V.
- Other values can be used as appropriate to conform to specific protocols and standards.

Figure 3: Single-Ended Peak-to-Peak Voltage



X16653-072117

Figure 4: Differential Peak-to-Peak Voltage



The following tables summarize the DC specifications of the clock input/output levels of the GTY and GTYP transceivers in Versal Prime devices. Consult the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* ([AM002](#)) for further details.

Table 100: GTY and GTYP Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	1600	mV
V_{ICM}	REFCLK common-mode input voltage	–	V_{GTY_AVCC} or V_{GTYP_AVCC}	–	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 101: GTY and GTYP Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

GTY and GTYP Transceiver Switching Characteristics

Consult the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* ([AM002](#)) for further information.

GTY and GTYP Transceiver Performance

Table 102: GTY Transceiver Performance

Symbol	Description	Subrate Divider	Output Divider	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})												Units
				0.88V (H)		0.80V (M)			0.725V (L)		0.70V (L)					
				-2		-2	-1		-2LLI		-2	-1				
F _{GTYMAX}	GTY maximum line rate			28.21		28.21		26.5625		28.21		28.21		25.78125		Gb/s
F _{GTYMIN}	GTY minimum line rate			1.2		1.2		1.2		1.2		1.2		1.2		Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYRRANGE}	RINGPLL line rate range ^{1,2}		1	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	Gb/s
			2	4	8	4	8	4	8	4	8	4	8	4	8	Gb/s
			4	2	4	2	4	2	4	2	4	2	4	2	4	Gb/s
			8	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYLRANGE}	LCPLL line rate range ³	1	1	16	28.21	16	28.21	16	26.5625	16	28.21	16	28.21	16	25.78125	Gb/s
		2		8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
		1	2	8	14.105	8	14.105	8	13.28125	8	14.105	8	14.105	8	12.891	Gb/s
		2		4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
		1	4	4	7.0525	4	7.0525	4	6.640625	4	7.0525	4	7.0525	4	6.4453125	Gb/s
		2		2	4.09375	2	4.09375	2	4.09375	2	4.0938	2	4.0938	2	4.09375	Gb/s
		1	8	2	3.52625	2	3.52625	2	3.3203125	2	3.5263	2	3.5263	2	3.2226563	Gb/s
		2		1.2	2.046875	1.2	2.046875	1.2	1.66015625	1.2	1.7631	1.2	1.7631	1.2	2.046875	Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{RPLLRANGE}	RINGPLL frequency range			4	8	4	8	4	8	4	8	4	8	4	8	GHz
F _{LCPLLRANGE}	LCPLL frequency range			8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	GHz

Notes:

- The values listed are the rounded results of the calculated equation $(2 \times \text{RINGPLL_Frequency}) / \text{Subrate_Divider}$.
- The highest supported line rate when using the RPLL to drive the datapath is 12.5 Gb/s.
- The values listed are the rounded results of the calculated equation $(2 \times \text{LCPLL_Frequency}) / (\text{Output_Divider} \times \text{Subrate_Divider})$.

Table 103: GTYP Transceiver Performance

Symbol	Description	Subrate Divider	Output Divider	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})														Units
				0.88V (H)				0.80V (M)				0.725V (L)		0.70V (L)				
				-3		-2		-2		-1		-2LLI		-2		-1		
FGTYPMAX	GTYP maximum line rate			32.75 (LPM)		32.00		32.00		26.5625		32.00		32.00		25.78125		Gb/s
		32 (DFE)																
FGTYPMIN	GTYP minimum line rate			1.2		1.2		1.2		1.2		1.2		1.2		1.2		Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
FGTYPRANGE	RINGPLL line rate range ^{1, 2}	1	1	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	Gb/s
		2	1	4	8	4	8	4	8	4	8	4	8	4	8	4	8	Gb/s
		4	1	2	4	2	4	2	4	2	4	2	4	2	4	2	4	Gb/s
		8	1	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
FGTYPLRANGE	LCPLL line rate range ³	1	1	16	32.75 (LPM)	16	32.00	16	32.00	16	26.5625	16	32.00	16	32.00	16	25.78125	Gb/s
					32 (DFE)													
		2	1	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
				2	1	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
		4	1	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
				2	1	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
		8	1	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	Gb/s
				2	1	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	Gb/s
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
FRPLLRange	RINGPLL frequency range			4	8	4	8	4	8	4	8	4	8	4	8	4	8	GHz
FLCPLLRange	LCPLL frequency range			8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	GHz

Notes:

- The values listed are the rounded results of the calculated equation $(2 \times \text{RINGPLL_Frequency}) / \text{Subrate_Divider}$.
- The highest supported line rate when using the RPLL to drive the datapath is 12.5 Gb/s.
- The values listed are the rounded results of the calculated equation $(2 \times \text{LCPLL_Frequency}) / (\text{Output_Divider} \times \text{Subrate_Divider})$.

GTY and GTYP Transceiver Configuration Interface Port Switching Characteristics

Table 104: GTY and GTYP Transceiver Configuration Interface Port (APB3) Switching Characteristics

Symbol	Description	All Speed Grades		Units
		Min	Max	
F _{GTYPB3}	GTYPB3CLK frequency	100	300	MHz

GTY and GTYP Transceiver Reference Clock Switching Characteristics

Table 105: GTY and GTYP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GTY_REFCLK} ¹	Reference clock frequency range		60	–	820	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Notes:

- The frequency values apply when the reference clock buffer is configured as either an input or output.

GTY and GTYP Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Table 106: GTY and GTYP Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description ^{1, 2}	Offset Frequency	Min	Typ	Max	Units
LCPLL _{REFCLKMASK}	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
RINGPLL _{REFCLKMASK}	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

GTY and GTYP Transceiver PLL/Lock Time Adaptation

Table 107: GTY and GTYP Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock	Reference clock frequency ≥ 150 MHz	–	–	3	ms
		Reference clock frequency < 150 MHz	–	–	5.7	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 × 10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3 × 10 ⁶	UI

GTY and GTYP Transceiver Digital Monitor Clock

Table 108: GTY and GTYP Transceiver Digital Monitor Port Switching Characteristics

Symbol	Description	All Speed Grades		Units
		Min	Max	
F _{GTYDMONITORCLK_INPUT}	GTY and GTYP transceiver digital monitor port input maximum frequency	100	500	MHz
F _{GTYDMONITORCLK_OUTPUT}	GTY and GTYP transceiver digital monitor port output maximum frequency	100	500	MHz

GTY and GTYP Transceiver User Clock Switching Characteristics

Table 109: GTY Transceiver User Clock Switching Characteristics

Symbol	Description ¹	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
				0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
		Internal Logic	Interconnect Logic	-2	-2	-1	-2LLI	-2	-1	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	664.063	664.063	664.063	644.531	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	664.063	664.063	664.063	644.531	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16	16	440.781	440.781	415.040	402.832	402.832	402.832	MHz
			32	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		32	32	440.781	440.781	415.040	402.832	402.832	402.832	MHz
			64	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		64	64	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			128	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		20	20	352.625	352.625	332.032	352.625	352.625	322.266	MHz
			40	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		80	80	352.625	352.625	332.032	352.625	352.625	322.266	MHz
			160	176.313	176.313	166.016	176.313	176.313	161.133	MHz

Table 109: GTY Transceiver User Clock Switching Characteristics (cont'd)

Symbol	Description ¹	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
				0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
		Internal Logic	Interconnect Logic	-2	-2	-1	-2LLI	-2	-1	
F _{RXIN}	RXUSRCLK maximum frequency	16	16	440.781	440.781	415.040	402.832	402.832	402.832	MHz
			32	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		32	32	440.781	440.781	415.040	402.832	402.832	402.832	MHz
			64	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		64	64	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			128	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		20	20	352.625	352.625	332.032	352.625	352.625	322.266	MHz
			40	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		80	80	352.625	352.625	332.031	352.625	352.625	322.266	MHz
			160	176.313	176.313	166.016	176.313	176.313	161.133	MHz

Notes:

1. Clocking must be implemented as described in the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002).

Table 110: GTYP Transceiver User Clock Switching Characteristics

Symbol	Description ¹	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
				0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2LLI	-2	-1	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	664.063	644.531	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	664.063	644.531	MHz
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	1000	664.063	664.063	644.531	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	1000	664.063	664.063	644.531	MHz

Table 110: GTYP Transceiver User Clock Switching Characteristics (cont'd)

Symbol	Description ¹	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
				0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2LLI	-2	-1	
F _{TXIN}	TXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		64	64	511.719 (LPM)	500	500	415.039	500	500	402.832	MHz
				500 (DFE)							
			128	255.859 (LPM)	250	250	207.520	250	250	201.416	MHz
				250 (DFE)							
		20	20	409.375	352.625	352.625	332.032	352.625	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		80	80	409.375 (LPM)	400	400	332.031	400	400	322.266	MHz
				400 (DFE)							
			160	204.688 (LPM)	200	200	166.016	200	200	161.133	MHz
				200 (DFE)							

Table 110: GTYP Transceiver User Clock Switching Characteristics (cont'd)

Symbol	Description ¹	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
				0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2LLI	-2	-1	
F _{RXIN}	RXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.039	402.832	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	201.416	MHz
		64	64	511.719 (LPM)	500	500	415.039	500	500	402.832	MHz
				500 (DFE)							
			128	255.859 (LPM)	250	250	207.520	250	250	201.416	MHz
				250 (DFE)							
		20	20	409.375	352.625	352.625	332.032	352.625	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	176.313	161.133	MHz
		80	80	409.375 (LPM)	400	400	332.031	400	400	322.266	MHz
				400 (DFE)							
			160	204.688 (LPM)	200	200	166.016	200	200	161.133	MHz
				200 (DFE)							

Notes:

- Clocking must be implemented as described in the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002).

GTY and GTYP Transceiver Transmitter and Receiver Switching Characteristics

Table 111: GTY and GTYP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		1.2	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ¹		–	–	500.00	ps
T _{J32.75}	Total jitter ^{2, 4}	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ^{2, 4}		–	–	0.19	UI
T _{J28.21}	Total jitter ^{2, 4}	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J16.375}	Total jitter ^{2, 4}	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J15.0}	Total jitter ^{2, 4}	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J14.1}	Total jitter ^{2, 4}	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J14.1}	Total jitter ^{2, 4}	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J13.1}	Total jitter ^{2, 4}	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J12.5_LCPLL}	Total jitter ^{2, 4}	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_LCPLL}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J12.5_RPLL}	Total jitter ^{3, 4}	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_RPLL}	Deterministic jitter ^{3, 4}		–	–	0.17	UI
T _{J11.3_LCPLL}	Total jitter ^{2, 4}	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_LCPLL}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J10.3125_LCPLL}	Total jitter ^{2, 4}	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_LCPLL}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J10.3125_RPLL}	Total jitter ^{3, 4}	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_RPLL}	Deterministic jitter ^{3, 4}		–	–	0.17	UI
T _{J9.953_LCPLL}	Total jitter ^{2, 4}	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_LCPLL}	Deterministic jitter ^{2, 4}		–	–	0.17	UI
T _{J9.953_RPLL}	Total jitter ^{3, 4}	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_RPLL}	Deterministic jitter ^{3, 4}		–	–	0.17	UI
T _{J8.0}	Total jitter ^{3, 4}	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ^{3, 4}		–	–	0.17	UI
T _{J6.6}	Total jitter ^{3, 4}	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ^{3, 4}		–	–	0.15	UI
T _{J5.0}	Total jitter ^{3, 4}	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ^{3, 4}		–	–	0.15	UI
T _{J4.25}	Total jitter ^{3, 4}	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ^{3, 4}		–	–	0.15	UI

Table 111: GTY and GTYP Transceiver Transmitter Switching Characteristics (cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ^{3, 4}	3.20 Gb/s	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ^{3, 4}		–	–	0.10	UI
T _{J2.5}	Total jitter ^{3, 4}	2.5 Gb/s	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ^{3, 4}		–	–	0.10	UI
T _{J1.25}	Total jitter ^{3, 4}	1.25 Gb/s	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ^{3, 4}		–	–	0.06	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY or GTYP Quad) at maximum line rate.
- Using LCPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using RPLL_FBDIV = 10, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².

Table 112: GTY and GTYP Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYRX}	Serial data rate		1.2	–	F _{GTYMAX}	Gb/s
R _{XSST}	Receiver spread-spectrum tracking	Modulated at 33 kHz	–5000	–	0	ppm
R _{XR} L	Run length (CID)		–	–	256	UI
R _{XP} PMTOL	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s and ≤ 16.3 Gb/s	–600	–	600	ppm
		Bit rates > 16.3 Gb/s and ≤ 24.0 Gb/s	–350	–	350	ppm
		Bit rates > 24.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance ¹						
J _{T_SJ} 32.75	Sinusoidal jitter (LCPLL) ²	32.75 Gb/s	0.25	–	–	UI
J _{T_SJ} 28.21	Sinusoidal jitter (LCPLL) ²	28.21 Gb/s	0.30	–	–	UI
J _{T_SJ} 16.375	Sinusoidal jitter (LCPLL) ²	16.375 Gb/s	0.30	–	–	UI
J _{T_SJ} 15.0	Sinusoidal jitter (LCPLL) ²	15.0 Gb/s	0.30	–	–	UI
J _{T_SJ} 14.1	Sinusoidal jitter (LCPLL) ²	14.1 Gb/s	0.30	–	–	UI
J _{T_SJ} 13.1	Sinusoidal jitter (LCPLL) ²	13.1 Gb/s	0.30	–	–	UI
J _{T_SJ} 12.5	Sinusoidal jitter (LCPLL) ²	12.5 Gb/s	0.30	–	–	UI
J _{T_SJ} 11.3	Sinusoidal jitter (LCPLL) ²	11.3 Gb/s	0.30	–	–	UI
J _{T_SJ} 10.32_LCPLL	Sinusoidal jitter (LCPLL) ²	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ} 10.32_RPLL	Sinusoidal jitter (RPLL) ²	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ} 9.953_LCPLL	Sinusoidal jitter (LCPLL) ²	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ} 9.953_RPLL	Sinusoidal jitter (RPLL) ²	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ} 8.0	Sinusoidal jitter (RPLL) ²	8.0 Gb/s	0.42	–	–	UI
J _{T_SJ} 6.6	Sinusoidal jitter (RPLL) ²	6.6 Gb/s	0.42	–	–	UI
J _{T_SJ} 5.0	Sinusoidal jitter (RPLL) ²	5.0 Gb/s	0.42	–	–	UI
J _{T_SJ} 4.25	Sinusoidal jitter (RPLL) ²	4.25 Gb/s	0.44	–	–	UI
J _{T_SJ} 3.2	Sinusoidal jitter (RPLL) ²	3.2 Gb/s	0.45	–	–	UI
J _{T_SJ} 2.5	Sinusoidal jitter (RPLL) ²	2.5 Gb/s	0.30	–	–	UI

Table 112: GTY and GTYP Transceiver Receiver Switching Characteristics (cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
J _{T_SJ1.25}	Sinusoidal jitter (RPLL) ²	1.25 Gb/s	0.30	-	-	UI

Notes:

1. All jitter values are based on a bit error ratio of 10⁻¹².
2. The frequency of the injected sinusoidal jitter is 10 MHz.

GTY and GTYP Transceiver Electrical Compliance

The *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* ([AM002](#)) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 113: GTY and GTYP Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25-28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25-25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ¹
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ¹
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ¹
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ¹
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ¹
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ¹
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493-32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18-13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ²	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328-11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555-9.956	Compliant
PCIe Gen1, 2, 3, 4	PCI Express 4.0 ³	2.5, 5.0, 8.0, and 16.0	Compliant
PCIe Gen1, 2, 3, 4, 5	PCI Express® 5.0 ⁴	2.5, 5.0, 8.0, 16.0, and 32.0	Compliant

Table 113: GTY and GTYP Transceiver Protocol List (cont'd)

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
SDI ⁵	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁵	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PH-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. For GTY transceivers, support is up to v4.0.
4. For GTYP transceivers, support is up to v5.0.
5. This protocol requires external circuitry to achieve compliance.

Integrated Block for MRMAC

More information and documentation on solutions using the multirate Ethernet MAC (MRMAC) can be found at *Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC) LogiCORE IP Product Guide* ([PG314](#)). The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists how many blocks are in each Versal Prime device.

Table 114: Maximum Performance for MRMAC Designs

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{RX_CORE_CLK}	Receive core clock	725.000	705.250	705.250	664.063	705.250	705.250	644.531	MHz
F _{TX_CORE_CLK}	Transmit core clock	725.000	705.250	705.250	664.063	705.250	705.250	644.531	MHz
F _{RX_AXIS_CLK}	Receive AXI4-Stream interface clock	431.762	420.000	420.000	420.000	420.000	420.000	322.266	MHz
F _{TX_AXIS_CLK}	Transmit AXI4-Stream interface clock	431.762	420.000	420.000	420.000	420.000	420.000	322.266	MHz
F _{RX_SERDES_CLK}	Serializer/deserializer clock	725.000	664.063	664.063	664.063	664.063	664.063	644.531	MHz
F _{RX_ALT_SERDES_CLK} ²	Receive alternate serializer/deserializer clock	362.500	352.625	352.625	332.031	352.625	352.625	322.266	MHz
F _{TX_ALT_SERDES_CLK} ²	Transmit alternate serializer/deserializer clock	362.500	352.625	352.625	332.031	352.625	352.625	322.266	MHz
F _{RX_TS_CLK}	Receive timestamp clock	350.000	350.000	350.000	350.000	350.000	350.000	350.000	MHz
F _{TX_TS_CLK}	Transmit timestamp clock	350.000	350.000	350.000	350.000	350.000	350.000	350.000	MHz
F _{RX_FLEXIF_CLK}	Receive flex interface clock	431.762	420.000	420.000	420.000	420.000	420.000	322.266	MHz
F _{TX_FLEXIF_CLK}	Transmit flex interface clock	431.762	420.000	420.000	420.000	420.000	420.000	322.266	MHz
F _{APB3_CLK}	AMBA® advance peripheral bus (APB3) clock	300.000	300.000	300.000	300.000	300.000	300.000	300.000	MHz

Notes:

- Overclocking is only supported in 100 GbE (with $F_{RX_CORE_CLK}$ and $F_{TX_CORE_CLK}$ running at 706 MHz, and the $F_{RX_SERDES_CLK}$ running at 353 MHz) by faster speed grade devices (-3H, -2M, -2L).
- The ALT_SERDES_CLKs run at half the speed of the primary SERDES_CLK. See *Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC) LogiCORE IP Product Guide* (PG314) for more information.

Integrated Block for DCMAC

More information and documentation on solutions using the 600G channelized multirate Ethernet MAC (DCMAC) can be found in the *Versal Adaptive SoC 600G Channelized Multirate Ethernet Subsystem (DCMAC) Product Guide* ([PG369](#)). The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists how many blocks are in each Versal Prime device.

Table 115: Maximum Performance for DCMAC Designs

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
		0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
		-2	-2	-1	-2LLI	-2	-1	
F _{RX_CORE_CLK}	Receive core clock	829.706	829.706	781.250	781.250	781.250	520.833	MHz
F _{TX_CORE_CLK}	Transmit core clock	829.706	829.706	781.250	781.250	781.250	520.833	MHz
F _{RX_AXIS_CLK}	Receive AXI4-Stream interface clock	456.338	456.338	390.625	429.688	429.688	260.417	MHz
F _{TX_AXIS_CLK}	Transmit AXI4-Stream interface clock	456.338	456.338	390.625	429.688	429.688	260.417	MHz
F _{RX_MAC_IF_CLK}	Receive MAC interface clock	414.853	414.853	390.625	390.625	390.625	260.417	MHz
F _{TX_MAC_IF_CLK}	Transmit MAC interface clock	414.853	414.853	390.625	390.625	390.625	260.417	MHz
F _{RX_SERDES_CLK}	Receiver serializer/deserializer clock	705.250	705.250	664.063	705.250	705.250	664.063	MHz
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	705.250	705.250	664.063	705.250	705.250	664.063	MHz
F _{RX_ALT_SERDES_CLK}	Receive alternate serializer/deserializer clock	352.625	352.625	332.031	352.625	352.625	332.031	MHz
F _{TX_ALT_SERDES_CLK}	Transmit alternate serializer/deserializer clock	352.625	352.625	332.031	352.625	352.625	332.031	MHz
F _{TS_CLK}	Timestamp clock	350.000	350.000	350.000	350.000	350.000	350.000	MHz
F _{RX_FLEXIF_CLK}	Receive flex interface clock	427.424	427.424	390.625	390.625	390.625	312.500	MHz
F _{TX_FLEXIF_CLK}	Transmit flex interface clock	427.424	427.424	390.625	390.625	390.625	312.500	MHz
F _{APB3_CLK}	APB3 clock	300.000	300.000	300.000	300.000	300.000	300.000	MHz

Notes:

- Overclock rates are supported by faster speed grade devices (-2H and -2M).

Programmable Logic Integrated Block for PCIe

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists how many blocks are in each Versal device.

Table 116: Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 4.0

Symbol	Description ^{1, 2}	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency	500	500	500	500	500	500	500	MHz
F _{CORECLK}	Core clock maximum frequency	500	500	500	500	500	500	500	MHz
F _{APBCLK}	APB clock maximum frequency	250	250	250	250	250	250	250	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. AMD LogiCORE™ IP solutions for PCIe that incorporate this block also integrate clocking, transceivers, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC Integrated Block for PCI Express LogiCORE IP Product Guide* ([PG343](#)) and *Versal Adaptive SoC DMA and Bridge Subsystem for PCI Express Product Guide* ([PG344](#)).
2. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.

Table 117: Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 5.0

Symbol	Description ^{1, 2, 3, 4}	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency	500	500	500	500	500	500	500	MHz
F _{CORECLK}	Core clock maximum frequency	500	500	500	500	500	500	500	MHz
F _{APBCLK}	APB clock maximum frequency	250	250	250	250	250	250	250	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, transceivers, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC Integrated Block for PCI Express LogiCORE IP Product Guide* ([PG343](#)) and *Versal Adaptive SoC DMA and Bridge Subsystem for PCI Express Product Guide* ([PG344](#)).
2. PCI Express Gen5 operation is supported for x1, x2, and x4 widths.
3. PCI Express Gen5 operation is supported in -3H, -2H, and -2M speed grades.
4. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.

Integrated Blocks for PCIe with DMA and Cache Coherent Interconnect (CPM)

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *Versal Architecture and Product Data Sheet: Overview* ([DS950](#)) lists how many blocks are in each Versal device.

Table 118: Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
PCIe Up To Gen3x16 With One Link With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz
PCIe Up To Gen4x8 With Two Links With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz
CCIX Up To Gen3x16 With One Link With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz
F _{CPM_CHICLK_MAX}	CPM AMBA® coherent hub interface (CHI) clock maximum frequency ²	390	390	390	312	312	312	250	MHz
CCIX Up To Gen4x8 With Two Links With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ²	390	390	390	312	312	312	250	MHz
CCIX Up To 20 Gb/s x8 With Two Links									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	156.125	156.125	156.125	156.125	156.125	156.125	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ²	390	390	390	312	312	312	N/A	MHz
CCIX Up To 25 Gb/s x8 With Two Links									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	195.312	195.312	195.312	N/A	N/A	N/A	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ²	390	390	390	N/A	N/A	N/A	N/A	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM Mode for PCI Express Product Guide* (PG346).
2. The CHI clock domain is for the CHI interface that connects the coherent hub to the programmable logic.

Table 119: Maximum Performance for DMA Streaming Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)

Symbol	Description ¹	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
PCIe Up To Gen3x16 With One Link With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz
PCIe Up To Gen4x8 With One Link With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM DMA and Bridge Mode for PCI Express Product Guide* (PG347).

Table 120: Maximum Performance for DMA Memory-Mapped AXI4 Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)

Symbol	Description ^{1, 2}	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})							Units
		0.88V (H)		0.80V (M)		0.725V (L)	0.70V (L)		
		-3	-2	-2	-1	-2LLI	-2	-1	
PCIe Gen4x16 With One Link									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	500	500	N/A	N/A	N/A	N/A	N/A	MHz
PCIe Up To Gen4x8 With One Link									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	250	250	250	250	250	250	250	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM DMA and Bridge Mode for PCI Express Product Guide* (PG347).
2. All clock frequencies shown are for informational purposes only. The CPM user clock is actually internal to the CPM block and cannot be set by the PL because the DMA is operating through hard memory-mapped AXI4 interfaces to the NoC.

Table 121: Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5)

Symbol	Description ¹	Mode	Performance as a Function of Speed Grade and V _{CCINT_CPM5} ² Operating Voltage					Units
			0.88V (H)	0.80V (M)		0.70V (L)		
			-2	-2	-1	-2	-1	
PCIe Up To Gen3x16 With One Link With 512-bit Interface								
FCPM_USERCLK_MAX	CPM user clock maximum frequency	Standard	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz

Table 121: Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5) (cont'd)

Symbol	Description ¹	Mode	Performance as a Function of Speed Grade and V _{CCINT_CPM5} ² Operating Voltage					Units
			0.88V (H)	0.80V (M)		0.70V (L)		
			-2	-2	-1	-2	-1	
PCIe Up To Gen4x8 With Two Links With 512-bit Interface								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
PCIe Up To Gen4x16 With One Link With 1024-bit Interface								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
Up to Gen5x8 With Two Links Up To 1024-bit Interface								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
CCIX Up To Gen3x16 With 512-bit Interface								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	390	312	312	250	MHz
		Overdrive	N/A	390	N/A	312	N/A	MHz
CCIX Up To Gen4x8 With One Link With 512-bit Interface								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	390	312	312	250	MHz
		Overdrive	N/A	390	N/A	312	N/A	MHz
CCIX Up To 20 Gb/s x8 With Two Links								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	156.125	156.125	156.125	156.125	N/A	MHz
		Overdrive	N/A	156.125	N/A	156.125	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	390	312	312	N/A	MHz
		Overdrive	N/A	390	N/A	312	N/A	MHz
CCIX Up To 25 Gb/s x8 With Two Links								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	195.312	195.312	N/A	N/A	N/A	MHz
		Overdrive	N/A	195.312	N/A	N/A	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	390	N/A	N/A	N/A	MHz
		Overdrive	N/A	390	N/A	N/A	N/A	MHz
CCIX Up To Gen4x16 With One Link								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	390	N/A	312	N/A	MHz
CCIX Up To Gen5x8 With Two Links								
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	N/A	MHz

Table 121: Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5) (cont'd)

Symbol	Description ¹	Mode	Performance as a Function of Speed Grade and V _{CCINT_CPM5} ² Operating Voltage					Units
			0.88V (H)	0.80V (M)		0.70V (L)		
			-2	-2	-1	-2	-1	
F _{CPM_CHICLK_MAX}	CPM CHI clock maximum frequency ³	Standard	390	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	390	N/A	312	N/A	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM Mode for PCI Express Product Guide* (PG346).
2. See the [Available Speed Grades and Operating Voltages](#) for further information on the dual-voltage operation CPM5 supplies in overdrive mode (0.88V) or standard drive mode (0.70V/0.80V).
3. The CHI clock domain is for the CHI interface that connects the coherent hub to the programmable logic.

Table 122: Maximum Performance for DMA Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5)

Symbol	Description ¹	Mode	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
			0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
			-2	-2	-1	-2LLI	-2	-1	
PCIe Up To Gen3x16 With One DMA instance With 512-bit Interface									
F _{CPM_DMACLK_MAX}	CPM DMA to PL user clock maximum frequency	Standard	433	400	300	250	250	250	MHz
		Overdrive	N/A	433	N/A	433	433	N/A	MHz
PCIe Up To Gen4x8 With Two DMA Instances With 512-bit Interface									
F _{CPM_DMACLK_MAX}	CPM DMA to PL (user) clock maximum frequency	Standard	433	400	300	250	250	250	MHz
		Overdrive	N/A	433	N/A	433	433	N/A	MHz
PCIe Up To Gen4x16 With One DMA Instance									
F _{CPM_DMACLK_MAX}	CPM DMA to PL (user) clock maximum frequency	Standard	433	N/A	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	433	N/A	433	433	N/A	MHz
CPM5 Configuration With Two Gen5x8 DMA Instances									
F _{CPM_DMACLK_MAX}	CPM DMA to PL (user) clock maximum frequency	Standard	433	N/A	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	433	N/A	433	433	N/A	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM DMA and Bridge Mode for PCI Express Product Guide* (PG347).

Table 123: Maximum Performance for DMA Memory-Mapped AXI4 Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5)

Symbol	Description ¹	Mode	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
			0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
			-2	-2	-1	-2LLI	-2	-1	
PCIe Up To Gen3x16 With One DMA Instance With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	250	N/A	MHz
PCIe Up To Gen4x8 With Two DMA Instances With 512-bit Interface									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	250	250	250	250	250	MHz
		Overdrive	N/A	250	N/A	250	250	N/A	MHz
PCIe Up To Gen4x16 With One DMA Instance									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	250	N/A	MHz
CPM5 Configuration With Two Gen5x8 Instances									
F _{CPM_USERCLK_MAX}	CPM user clock maximum frequency	Standard	250	N/A	N/A	N/A	N/A	N/A	MHz
		Overdrive	N/A	250	N/A	250	250	N/A	MHz

Notes:

1. This table only specifies the AC switching characteristics of the identified integrated block for PCIe. LogiCORE IP solutions for PCIe that incorporate this block also integrate clocking, logic, and block memory. LogiCORE IP solutions for PCIe must achieve timing closure during design implementation in the target device, including user-contributed application logic. For information and technical guidance on resource use and minimum device requirements, see the *Versal Adaptive SoC CPM DMA and Bridge Mode for PCI Express Product Guide* (PG347).

Integrated High-speed Channelized Cryptography Engine

This section describes the maximum performance for the integrated high-speed channelized cryptography (HSC) engine configurations.

Table 124: High-Speed Channelized Cryptography Engine Performance

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V _{CCINT})						Units
		0.88V (H)	0.80V (M)		0.725V (L)	0.70V (L)		
		-2	-2	-1	-2LLI	-2	-1	
F _{DEC_CORE_CLK}	Core clock for the decryption block	818.707	818.707	818.707	818.707	818.707	409.353	MHz
F _{ENC_CORE_CLK}	Core clock for the encryption block	818.707	818.707	818.707	818.707	818.707	409.353	MHz
F _{DEC_EGR_AXIS_CLK}	Egress AXI-S clock for the decryption block	409.353	409.353	409.353	409.353	409.353	204.677	MHz
F _{ENC_EGR_AXIS_CLK}	Egress AXI-S clock for the encryption block	409.353	409.353	409.353	409.353	409.353	204.677	MHz
F _{DEC_IGR_AXIS_CLK}	Ingress AXI-S clock for the decryption block	409.353	409.353	409.353	409.353	409.353	204.677	MHz
F _{ENC_IGR_AXIS_CLK}	Ingress AXI-S clock for the encryption block	409.353	409.353	409.353	409.353	409.353	204.677	MHz
F _{APB3_CLK}	APB3 clock	300.000	300.000	300.000	300.000	300.000	300.000	MHz

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
3/14/2025 Version 1.15	
General updates	Updated Table 29: Speed Specification Version by Device including production release of the XCVU2152 with speed grades -2HSI ($V_{CCINT} = 0.88V$), -2LSE, -2LLE, -1LSE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$) -1MSE, -1MSI, and -1MLI ($V_{CCINT} = 0.80V$) using the Vivado Design Suite 2024.2.2 v2.02. This includes updates to the following tables: Speed Grade Designations Production Silicon and Software Status
1/13/2025 Version 1.14	
General updates	Added VM2152 devices throughout. Updated Table 29: Speed Specification Version by Device including production release of the XCVU2152 with speed grades -2MSE, -2MSI, -2MLE, -2MLI, -1MSE, -1MSI, and -1MLI ($V_{CCINT} = 0.80V$) using the Vivado Design Suite 2024.2.1 v2.01. This includes updates to the following tables: Speed Grade Designations Production Silicon and Software Status Device Pin-to-Pin Output Parameter Guidelines Device Pin-to-Pin Input Parameter Guidelines Package Parameter Guidelines
Integrated High-speed Channelized Cryptography Engine	Added this table for the VM2152 devices only.

Section	Revision Summary
9/20/2024 Version 1.13	
General updates	Updated Table 29: Speed Specification Version by Device including production release of the XQVM1102 with speed grades -2MSI, -1MSM, -1MSI ($V_{CCINT} = 0.80V$) and -1LSI ($V_{CCINT} = 0.70V$) using the Vivado Design Suite 2024.1.2 v2.03. This includes updates to the following tables: Speed Grade Designations Production Silicon and Software Status Device Identification Device Pin-to-Pin Output Parameter Guidelines Device Pin-to-Pin Input Parameter Guidelines Package Parameter Guidelines
Video Decoder Engines Performance	Removed table because no Versal Prime devices support this feature.
7/24/2024 Version 1.12	
General updates	Updated Table 29: Speed Specification Version by Device including production release of the XCVM2202 with speed grade -2HSI ($V_{CCINT} = 0.88V$) using the Vivado Design Suite 2024.1 v2.01. This includes updates to the following tables: Speed Grade Designations Production Silicon and Software Status Device Pin-to-Pin Output Parameter Guidelines Device Pin-to-Pin Input Parameter Guidelines Package Parameter Guidelines
Absolute Maximum Ratings	Increased the maximum storage temperature to 150°C.
Table 34: PS-PL Interface Performance	Removed redundant Notes 1 and 2.
Clocks and Reset	Added $F_{CPM5_TOPSW_CLK}$ to Table 39: PS LPD Clocks Switching Characteristics and Table 13 .
Accelerator RAM Switching Characteristics	Corrected the -2L/-1L from 0.80V to 0.70V for V_{CC_PSLP} see the Available Speed Grades and Operating Voltages table.
GTM Transceiver Switching Characteristics	Removed the 58 Gb/s condition in the following tables: Table 96: GTM Transceiver Transmitter Switching Characteristics Table 97: GTM Transceiver Receiver Switching Characteristics
Programmable Logic Integrated Block for PCIe	Added a note to each table in this section to clarify that the specifications are only for the integrated blocks for PCIe.
Integrated Blocks for PCIe with DMA and Cache Coherent Interconnect (CPM)	Added a note to each table in this section to clarify that the specifications are only for the integrated blocks for PCIe.
4/30/2024 Version 1.11	
General updates	Updated Table 29: Speed Specification Version by Device including production release of the XCVM2202 with speed grade -2HSI ($V_{CCINT} = 0.88V$) using the Vivado Design Suite 2023.2.2 v2.01. This includes updates to the following tables: Speed Grade Designations Production Silicon and Software Status Device Pin-to-Pin Output Parameter Guidelines Device Pin-to-Pin Input Parameter Guidelines Package Parameter Guidelines
Absolute Maximum Ratings	Added V_{CCINT_GT} specification.
Recommended Operating Conditions	Updated V_{GTYP_AVCC} and V_{GTYP_AVCC} with voltages based upon temperature ranges (E, I, Q, or M).

Section	Revision Summary
Available Speed Grades and Operating Voltages	Updated Note 5.
Power Supply Requirements	Added reference links.
Device Identification	Updated IDCODE for XCVM1102.
DDR4 and LPDDR4/4X Memory Interface Controller	Updated Note 5.
GTM Transceiver DC Input and Output Levels	Revised V_{DIFF} maximum from 800 mV to 1600 mV.
GTY and GTYP Transceiver DC Input and Output Levels	Revised V_{DIFF} maximum from 800 mV to 1600 mV.
GTY and GTYP Transceiver Reference Clock Oscillator Selection Phase Noise Mask	Interchanged symbols LCPLL and RINGPLL.
2/29/2024 Version 1.10	
General updates	Updated Table 29: Speed Specification Version by Device including production release: - XCVM1102 with speed grades -2HSI and -2LLI using the Vivado Design Suite 2024.1 v2.01. - XCVM2202 with speed grade -2LLI using the Vivado Design Suite 2024.1 v2.02. This could include updates to the following tables: Speed Grade Designations Production Silicon and Software Status Device Pin-to-Pin Output Parameter Guidelines Device Pin-to-Pin Input Parameter Guidelines Package Parameter Guidelines
Absolute Maximum Ratings	Revised the transceiver REFCLK_AC maximum input voltage from 1.200V to 1.350V.
Block RAM Switching Characteristics	T_{RCKO_DO} and $T_{RCKO_DO_REG}$ values changed for -2LLI.
DDR4 and LPDDR4/4X Memory Interface Controller	Removed the LPDDR4/4X pin efficient component interface limitation.
Table 87: GTM Transceiver Clock Input Level Specification	Added the V_{ICM} specification. To support LVPECL clocks, changed the V_{DIFF} maximum (peak-to-peak) to 800 mV.
GTM Transceiver Performance	Updated to support all the AMD Versal™ Prime devices, added -2H specifications to Table 89: GTM Transceiver Performance and Table 95: GTM Transceiver User Clock Switching Characteristics .
GTM Transceiver PLL/Lock Time Adaptation	Update the T_{DLOCK} values for GTM PAM4.
Table 100: GTY and GTYP Transceiver Clock Input Level Specification	Added the V_{ICM} specification. To support LVPECL clocks, changed the V_{DIFF} maximum (peak-to-peak) to 800 mV.
GTY and GTYP Transceiver Performance	Updated Table 102: GTY Transceiver Performance and Table 109: GTY Transceiver User Clock Switching Characteristics to remove the -3H speed files to match the Versal Prime devices offered.
GTY and GTYP Transceiver User Clock Switching Characteristics	Updated the GTY transceiver -2H values.
11/08/2023 Version 1.9	
General updates	Updated Table 29: Speed Specification Version by Device including: - Production release of the XCVM1302 and XCVM1402 with speed grade -2LLI using the Vivado Design Suite 2023.2 v2.03. - Production release of the XCVM1502 with speed grade -2LLI using the Vivado Design Suite 2023.2 v2.04. - Added the XCVM2202. Includes updates to Speed Grade Designations, Production Silicon and Software Status, Device Pin-to-Pin Output Parameter Guidelines, Device Pin-to-Pin Input Parameter Guidelines, and Package Parameter Guidelines.
Recommended Operating Conditions	Updated Note 9 with PSIO operation information. Updated Note 10.
Available Speed Grades and Operating Voltages	Updated Note 4.

Section	Revision Summary
DDR4 and LPDDR4/4X Memory Interface Controller	Clarified the values for LPDDR4/4X XPIO bank performance.
GTM Transceiver Performance	Removed notes from $F_{GTMPAM42MAX}$ and $F_{GTMPAM44MAX}$ because they do not apply for the data rates listed.
GTM Transceiver Reference Clock Switching Characteristics	Added Note 1.
GTM Transceiver Digital Monitor Clock	Added table.
GTYP and GTYP Transceiver Reference Clock Switching Characteristics	Added Note 1.
GTYP and GTYP Transceiver Digital Monitor Clock	Added table.
9/08/2023 Version 1.8	
General updates	Updated the Table 29: Speed Specification Version by Device including: - Production release of the XCVM2302 and XCVM2902 with speed grades -2LSE, -2LLE, -1LSE, -1LSI, and -1LLI using the Vivado Design Suite 2023.1 v2.00 - Production release of the XCVM2302 and XCVM2902 with speed grades -3HSE, -2MSE, -2MLE, -2MSI, -2MLI, -1MSE, -1MSI, and -1MLI, using the Vivado Design Suite 2023.1.1 v2.01 - Production release of the XCVM2502 with speed grades -3HSE, -2MSE, -2MLE, -2MSI, -2MLI, -1MSE, -1MSI, -1MLI, -2LSE, -2LLE, -1LSE, -1LSI, and -1LLI using the Vivado Design Suite 2023.1.2 v2.01 - Production release of the XQVM1502 with speed grades -2MSI, -1MSM, -1MSI, and -1LSI using the Vivado Design Suite 2023.1.1 v2.03 Includes updates to Speed Grade Designations, Production Silicon and Software Status, Device Pin-to-Pin Output Parameter Guidelines, Device Pin-to-Pin Input Parameter Guidelines, and Package Parameter Guidelines.
GTYP and GTYP Transceiver Electrical Compliance	Clarified PCIe support for GTYP transceivers.
6/07/2023 Version 1.7	
General updates	Updated the Table 29: Speed Specification Version by Device including: Production release of the XCVM2302 and XCVM2902 with speed grades -2LSE, -2LLE, -1LSE, -1LSI, and -1LLI using the Vivado Design Suite 2023.1 v2.00 Includes updates to Speed Grade Designations, Production Silicon and Software Status, Device Pin-to-Pin Output Parameter Guidelines, Device Pin-to-Pin Input Parameter Guidelines, and Package Parameter Guidelines.
Summary	Clarified that the I and M temperature grades are also supported by the Versal Prime devices.
Recommended Operating Conditions	Updated T_j to add military (M) temperature specifications.
DC Characteristics Over Recommended Operating Conditions	Added I_L specifications.
V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot	Added Note 3 and Note 4 for -1MSM devices.
Table 38: PS FPD Clocks Switching Characteristics	Added Notes 1, 2, and 3.
Table 39: PS LPD Clocks Switching Characteristics	Added Notes 2, 4, 6, 8, 10, and 12.
PS Gigabit Ethernet MAC Controller Interface	Added Note 2 to $F_{GEMTSUREFCLK}$.
GTM Transceiver DC Input and Output Levels	Added $V_{CMOUTDC}$ to Table 86: GTM Transceiver DC Specifications . Updated the D_{VPPOUT} output swing setting to 1000100.
GTYP and GTYP Transceiver DC Input and Output Levels	Removed the row for $V_{CMOUTDC}$ when remote RX is terminated to GND and added Note 2. Updated Note 3.

Section	Revision Summary
3/28/2023 Version 1.6	
General updates	Updated the Table 29: Speed Specification Version by Device including: - Production release of the XCVM1502 with speed grades -2LSE, -2LLE, -1LSE, -1LSI, and -1LLI using the Vivado Design Suite 2022.2 v2.00 - Production release of the XCVM1502 with speed grades -2MSE, -2MLE, -2MSI, -2MLI, -1MSE, -1MSI, and -1MLI using the Vivado Design Suite 2022.2.1 v2.01 - Production release of the XCVM1502 with speed grades -2HSI using the Vivado Design Suite 2022.2.2 v2.02 - Production release of the XQVM1402 with speed grades -2MSI, -1MSI, -1MSM, and -1LSI using the Vivado Design Suite 2022.2.1 v2.02 - Production release of the XCVM1802 device in the -2LLI speed grade using the Vivado Design Suite 2022.2.1 v2.11. Includes updates to Speed Grade Designations, Production Silicon and Software Status, Device Pin-to-Pin Output Parameter Guidelines, Device Pin-to-Pin Input Parameter Guidelines, and Package Parameter Guidelines.
Absolute Maximum Ratings	Revised the $I_{DCIN_GTM_AVTT}$ and $I_{DCIN_GTM_GND}$ values from 12 mA to 16 mA.
Recommended Operating Conditions	Updated V_{CCINT} with values for -2LLI devices and added Note 7.
Available Speed Grades and Operating Voltages	Updated -2LLI device code and added Note 5. Updated V_{CC_CPM5} values because devices with CPM5 do not support the -2HSI or -2LLI speed grades. Updated Notes 1, 2, and 3.
Power Supply Requirements	Updated description to add references to the PDM tool.
Speed Grade Designations	Removed -2MLI, -2LLI, -1MLI, and -1LLI speed grades from the XQVM1102, XQVM1402, and XQVM1502.
Production Silicon and Software Status	Added Note 5 to Production Silicon and Software Status Added N/A to the columns for XQ devices that do not support low static-power grades.
Device Identification	Revised the VM1102 and VM1502 IDCODEs and added XQVM1402, XCVM2202, and XCVM2302 IDCODEs.
Processing System Performance Characteristics	Updated notes in Table 33: Processor Performance and Table 34: PS-PL Interface Performance .
PMC JTAG and SelectMAP	Updated Note 1 in Table 48: JTAG/Boundary-Scan Port Switching Characteristics .
PMC Quad-SPI Controller Interface	Updated the F_{QSPI_REFCLK} maximum for Quad-SPI device clock frequency operating at ≤ 37.5 MHz (Loopback disabled) from 150 MHz to 300 MHz.
Block RAM Switching Characteristics	To further delineate the specifications for block RAM clock-to-out delays, added a column for -2LLI and renamed -2L column to -2LSE, -2LLE.
Device Pin-to-Pin Output Parameter Guidelines	Added column for -2LLI and renamed column to -2LSE, -2LLE. Added XCVM2302 and XCVM2902 values.
Device Pin-to-Pin Input Parameter Guidelines	Added column for -2LLI and renamed column to -2LSE, -2LLE. Added XCVM2302 and XCVM2902 values.
Package Parameter Guidelines	Updated XQVM1102, added XQVM1502, XCVM2302 and XCVM2902 values.
GTM Transceiver DC Input and Output Levels	Updated the D_{VPPIN} PAM4 maximum specification in Table 86: GTM Transceiver DC Specifications . Added Table 88: GTM Transceiver Clock Output Level Specification .

Section	Revision Summary
GTM Transceiver Performance	Added notes to the output divider column for both measured BER and availability of certain data rates.
GTM Transceiver PLL/Lock Time Adaptation	Updated conditions for T_{LOCK} .
GTM Transceiver Transmitter and Receiver Switching Characteristics	Removed the PAM4 82.5 Gb/s sinusoidal jitter condition.
Table 97: GTM Transceiver Receiver Switching Characteristics	Updated $R_{XPPMTOL}$ conditions and Note 2, and added Note 1.
GTY and GTYP Transceiver DC Input and Output Levels	Revised $V_{CMOUTDC}$ and $V_{CMOUTAC}$ equations in GTU and GTYP Transceiver DC Input and Output Levels .
	Updated V_{OL} , V_{OH} , and V_{CMOUT} minimum/maximum values in Table 101: GTY and GTYP Transceiver Clock Output Level Specification .
GTU and GTYP Transceiver Performance	In Table 103: GTYP Transceiver Performance , revised the GTYP maximum line rate and the LCPLL line rate range.
GTU and GTYP Transceiver User Clock Switching Characteristics	Updated F_{TXIN} and F_{RXIN} values for some data width conditions.
8/02/2022 Version 1.5	
General updates	Updated the Table 29: Speed Specification Version by Device including production release of some of the devices/speed grade/operating voltages using the Vivado Design Suite 2022.1.1 v2.10 in Speed Grade Designations and Production Silicon and Software Status .
Speed Grade Designations	Moved the -2LLI ($V_{CCINT} = 0.70V$) speed file to Evaluation in some devices where it was listed as production. This speed file is not available in the software tools.
DC Characteristics Over Recommended Operating Conditions	Updated the I_{CC_BATT} conditions and values.
PMC SD/SDIO Controller Interface	Added T_{SDDC} and T_{SDCKD} minimum values and updated the $T_{SDSDR12DCK}$ minimum value.
PMC eMMC Controller Interface	Added $T_{EMMEDCK}$ and T_{EMMCKD} minimum values.
Device Pin-to-Pin Output Parameter Guidelines	Updated the XCVM1502 values and added the -2H values for XCVM1302, XCVM1402, and XCVM1802.
Device Pin-to-Pin Input Parameter Guidelines	Updated the XCVM1502 values and added the -2H values for XCVM1302, XCVM1402, and XCVM1802.
GTM Transceiver User Clock Switching Characteristics	Updated table values to match the maximum 58 Gb/s line rate.
Integrated Blocks for PCIe with DMA and Cache Coherent Interconnect (CPM)	Clarified that Overdrive support is not available on -1L (0.70V) devices in Table 121: Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5) , Table 122: Maximum Performance for DMA Streaming Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5) , and Table 123: Maximum Performance for DMA Memory-Mapped AXI4 Mode Interface of Integrated Block for PCIe Rev. 5.0 with DMA and CCIX Rev. 1.1 (CPM5) .
5/02/2022 Version 1.4	
General updates	Added XQ devices: XQVM1102, XQVM1402, XQVM1502, and XQVM1802.
Absolute Maximum Ratings	Revised the V_{GTU_AVCC} maximums from 0.97V to 1.01V. Revised the GT transceivers V_{IN} specifications and added unpowered and powered values for V_{IN_DC} and V_{IN_AC} . Revised the transceiver reference clock absolute input AC and DC voltages. Removed duplicate $I_{DCIN-FLOAT}$ rating and note. Removed note 9.
Available Speed Grades and Operating Voltages	Added the -1MSM speed grade for XQ devices (-1MP-m-S device code).
Power Supply Requirements	Updated the description.
AC Switching Characteristics	Updated the Table 29: Speed Specification Version by Device including production release of some of the devices/speed grade/operating voltages using the Vivado Design Suite 2022.1 v2.06 in Speed Grade Designations and Production Silicon and Software Status .
Clocks and Reset	Added note 2 to Table 35: Reference Clock Requirements .
PMC Octal-SPI Controller Interface	Added values to Table 51: Octal-SPI Interface and updated note 1.

Section	Revision Summary
PMC SD/SDIO Controller Interface	Added values to Table 55: SD/SDIO Interface and updated note 1.
PMC eMMC Controller Interface	Added values and notes 3 and 4 to Table 56: eMMC Controller Interface and updated note 1.
DDR4 and LPDDR4/4X Memory Interface Controller	Added note 7 to Table 84: Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller
GTM Transceiver Specifications	Added GTM transceiver specifications. Some Versal Prime devices have GTM transceivers, see the <i>Versal Architecture and Product Data Sheet: Overview</i> (DS950).
GTY and GTYP Transceiver Performance	Added the -2H column. Some XC devices offer a -2HSI device and others offer a -3SE device. See the <i>Speed and Temperature Grade</i> table in the <i>Versal Architecture and Product Data Sheet: Overview</i> (DS950).
Programmable Logic Integrated Block for PCIe	Updated Table 117: Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 5.0 .
1/06/2022 Version 1.3	
Summary and General Updates	Added the XCV2202, XCV2302, and removed XCV2602 devices.
	Added the GTM transceiver, PCIe 5.0, and CPM5 specifications where applicable.
Absolute Maximum Ratings	Revised the maximum V_{CCO} from 3.465V to 3.63V for certain HDIO and PSIO banks.
	Added V_{REF} specifications.
	Removed T_{SOL} guidelines. See <i>Versal Adaptive SoC Packaging and Pinouts Architecture Manual</i> (AM013) for appropriate specifications by package type.
DC Characteristics Over Recommended Operating Conditions	Updated the HDIO, PSIO, and XPIO maximum capacitance and added Note 2.
Available Speed Grades and Operating Voltages	Added the <i>Vivado Design Tools Device Code</i> column.
AC Switching Characteristics	Updated to Vivado Design Suite 2021.2.1 v2.05 for XCV1802 and v1.02 for XCV1302, XCV1402.
	Added the <i>Evaluation Product Specification</i> description.
Speed Grade Designations	Revised the available speed specifications by device.
Production Silicon and Software Status	Revised the production released version of the XCV1802 to Vivado Design Suite 2021.2.1 v2.05 and added Note 4.
PS USB Controller Interface	Revised $T_{ULPICKD}$ input hold time from 0 to 0.5 ns (500 ps).
Table 71: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller	Added Note 4 limiting the RDRAM3 maximum performance for -2L and -1L speed grades.
Device Pin-to-Pin Output Parameter Guidelines	Revised the XCV1802 speed specification values for Vivado Design Suite 2021.2.1 v2.05 and added the Vivado Design Suite 2021.2.1 v1.02 values for XCV1302 and XCV1402.
Device Pin-to-Pin Input Parameter Guidelines	Revised the XCV1802 speed specification values for Vivado Design Suite 2021.2.1 v2.05 and added the Vivado Design Suite 2021.2.1 v1.02 values for XCV1302 and XCV1402.
Package Parameter Guidelines	Added some XCV1302 and XCV1402 values.
7/01/2021 Version 1.2	
Recommended Operating Conditions	Added Note 10.
AC Switching Characteristics	Updated the speed file versions to Vivado Design Suite 2021.1 v2.01.
Speed Grade Designations	Moved the XCV1802 to production for the following speed grades: -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -1MSE, -1MLE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$)
Production Silicon and Software Status	Updated the software status for the following speed grades to Vivado Design Suite 2021.1 v2.01. -2MSE, -2MLE, -2MSI, -2MLI ($V_{CCINT} = 0.80V$) -1MSE, -1MLE, -1MSI, -1MLI ($V_{CCINT} = 0.80V$)

Section	Revision Summary
Processing System Performance Characteristics	In Table 33: Processor Performance , updated F_{RPUMAX} for the -3/-2 (0.88V (H)) speed grades. Added F_{PLATB_CLK} to Table 34: PS-PL Interface Performance .
PS CAN FD Controller Interface	Added Note 2.
PS Trace Interface	Updated Note 2 and added Note 4.
Programmable Logic Performance Characteristics	Updated Table 68: MIPI D-PHY Performance for -2/-1 (0.80V (M) and 0.70V (L)) speed grades. In Table 71: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller : - Removed Note 4: Maximum performance for interfaces using more than one bank. - Added Note 1. - Revised the -1 performance values for DRAM type DDR4 single rank component. - Revised the -1M performance value for DRAM type 1 rank RDIMM, DIMM.
Accelerator RAM Switching Characteristics	Added the section because the accelerator RAM is available in the VM1102 device.
Device Pin-to-Pin Output Parameter Guidelines	Updated the $T_{ICKOFMMCM}$ values to the speed specifications in Vivado Design Suite 2021.1.
Device Pin-to-Pin Input Parameter Guidelines	Updated the setup and hold values to the speed specifications in Vivado Design Suite 2021.1.
DDR4 and LPDDR4/4X Memory Interface Controller	Added Note 1 to Table 84: Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller , and updated Note 5.
GTY and GTYP Transceiver Configuration Interface Port Switching Characteristics	Reduced the maximum GTYAPB3CLK frequency in Table 104: GTY and GTYP Transceiver Configuration Interface Port (APB3) Switching Characteristics .
GTY and GTYP Transceiver User Clock Switching Characteristics	Updated values in Table 110: GTYP Transceiver User Clock Switching Characteristics .
4/14/2021 Version 1.1	
General updates	Added GTYP transceiver specifications.
Summary	Added V_{CC_PMC} overdrive support.
Table 1: Absolute Maximum Ratings—Power, Voltages, and Current	Updated the notes.
Table 3: Recommended Operating Conditions	Revised maximum V_{CCBATT} , added minimum CFU reference clock frequency to F_{CFU_REFCLK} , added overdrive conditions to V_{CC_PMC} , added Notes 2, 3, 4, 9, 13, and updated Note 16.
Available Speed Grades and Operating Voltages	Updated table with standard and overdrive modes. Added Note 4.
Table 5: DC Characteristics Over Recommended Operating Conditions	Added table.
V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot	Added note 3 to Table 7: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for XPIO Banks .
Table 12: DC Input Levels for Single-ended POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Updated V_{IL} maximum and V_{IH} minimum for LVSTL06_12 and LVSTL_11.
Table 17: DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Removed LVSTL_11 ($V_{OH} = 33$). Added Note 2.
Table 18: Definitions for DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Removed LVSTL_11 ($V_{OH} = 33$).
LVDS DC Specifications (LVDS15)	Added V_{ICM_AC} and Note 5.
AC Switching Characteristics	Updated the speed file versions and the definitions for engineering sample, pre-production, and production product specification.
Speed Grade Designations	Moved the XCVM1802 to production for the following speed grades: -2LSE, -2LLE ($V_{CCINT} = 0.70V$) -1LSE, -1LLE, -1LSI, -1LLI ($V_{CCINT} = 0.70V$)

Section	Revision Summary
Production Silicon and Software Status	The XCVM1802 is production released using Vivado Design Suite 2020.3 v2.00.
Device Identification	Updated the IDCODE for the XCVM1802, and added notes to explain the table fields.
Processing System Performance Characteristics	Updated Table 33: Processor Performance . Added F _{PSFCIDMA_CLK} and Note 1 to Table 34: PS-PL Interface Performance .
Clocks and Reset	Added T _{MODEPOR} and T _{PORMODE} to Table 37: Power-on Reset Assertion Timing Requirements . Added F _{FPD_LSBUS_CLK} and Note 4 to Table 38: PS FPD Clocks Switching Characteristics . Added F _{RPLL_TO_XPD_CLK} , F _{LPD_LSBUS_CLK} , F _{TS_REFCLK} , F _{PSM_REFCLK} , F _{DBG_LPD_CLK} , F _{USB_REFCLK} , F _{DBG_TS_CLK} , and Notes 1, 5, 7, and 11 to Table 39: PS LPD Clocks Switching Characteristics . In Table 40: PMC IRO Clock Switching Characteristics , updated the IRO tolerance range. In Table 41: PMC Clocks Switching Characteristics , added F _{FUSE_REFCLK} , F _{SMON_REFCLK} , F _{NP1_REFCLK} , F _{PPLL_TO_XPD_CLK} , F _{NPLL_TO_XPD_CLK} , F _{LSBUS_REFCLK} , F _{AXI_TO_REFCLK} , F _{USB_SREFCLK} , and F _{HSM0_REFCLK} . Revised the -3 specifications for F _{PLO_REFCLK} , F _{PL1_REFCLK} , F _{PL2_REFCLK} , and F _{PL3_REFCLK} . Updated the Notes 1 and 4. Added Note 1 to Table 42: PMC PLL Switching Characteristics .
PMC JTAG and SelectMAP	Extensive updates to Table 48: JTAG/Boundary-Scan Port Switching Characteristics and Table 49: SelectMap Interface Switching Characteristics .
PMC Quad-SPI Controller Interface	Extensive changes to the table. Updated Note 1 and added Note 2 and 5.
PMC Octal-SPI Controller Interface	Removed load condition column. Updated Note 1.
PS USB Controller Interface	Added T _{ULPIDCK} , T _{ULPICKD} , and T _{ULPICKO} .
PS Gigabit Ethernet MAC Controller Interface	Added F _{GEMTSUREFCLK} .
PS Trace Interface	Updated F _{TCECLK} and Note 3.
Network on Chip Switching Characteristics	Updated the performance values in the table.
Programmable Logic Performance Characteristics	Updated values in Table 66: I/O Logic Performance . Updated values in Table 67: XPHY I/O Performance and added Notes 3 and 4. Updated the values in Table 68: MIPI D-PHY Performance . Updated the values in Table 71: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller and added Note 4: Maximum performance for interfaces using more than one bank. Removed the <i>LVDS Native-Mode 100BASE-X Support</i> table.
Block RAM Switching Characteristics	Updated T _{RCKO_DO} and T _{RCKO_DO_REG} .
Input/Output Delay Switching Characteristics	Added T _{IOL_IDELAY_RESOLUTION} .
MMCM Switching Characteristics	Extensive updates to table and notes including removal of T _{DESKEWMISMATCH_MMCM} .
DPLL Switching Characteristics	Extensive updates to table and notes including removal of T _{DESKEWMISMATCH_DPLL} .
XPLL Switching Characteristics	Extensive updates to table and notes including removal of T _{DESKEWMISMATCH_XPLL} .
Device Pin-to-Pin Output Parameter Guidelines	Updated the XCVM1802 parameters in Vivado Design Suite 2020.3 v2.00.
Device Pin-to-Pin Input Parameter Guidelines	Updated the XCVM1802 parameters in Vivado Design Suite 2020.3 v2.00.
Package Parameter Guidelines	Updated the XCVM1802 package skew in Vivado Design Suite 2020.3 v2.00.
DDR4 and LPDDR4/4X Memory Interface Controller	Added Notes 2 and 3. Updated Note 6.

Section	Revision Summary
GTY and GTYP Transceiver DC Input and Output Levels	Revised V_{IN} in Table 99: GTY and GTYP Transceiver DC Specifications. Updated the specifications in Table 101: GTY and GTYP Transceiver Clock Output Level Specification.
GTY and GTYP Transceiver Performance	Updated the $F_{GTYLRANGE}$ values.
GTY and GTYP Transceiver PLL/Lock Time Adaptation	Added conditions to T_{LOCK} .
GTY and GTYP Transceiver Transmitter and Receiver Switching Characteristics	Removed legacy content and updated the applicable symbols, conditions, and values in both the Transmitter and Receiver tables.
GTY and GTYP Transceiver Electrical Compliance	Added the table.
PMC Quad-SPI Controller Interface	Added additional load information to the table.
Integrated Block for MRMAC	Changed title and added specifications.
Programmable Logic Integrated Block for PCIe	Added Table 116: Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 4.0.
7/16/2020 Version 1.0	
Initial release.	N/A

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