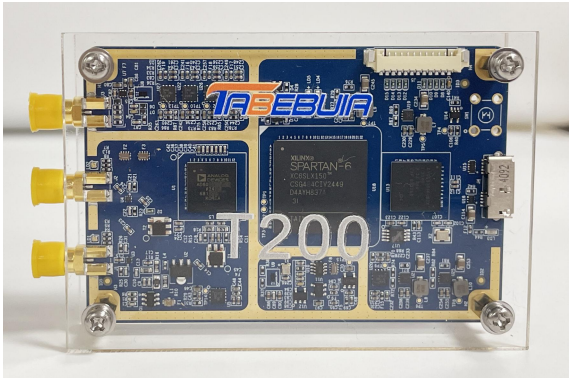
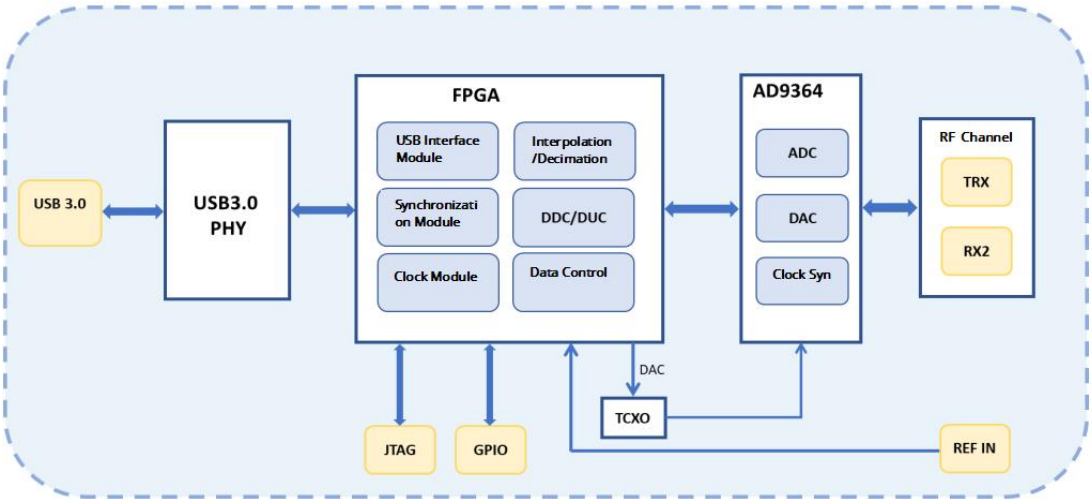
USRP T200 Datasheet

Overview

The USRP T200 is a compact industrial-grade software-defined radio (SDR) device with strong portability, making it ideal for mobile applications and field deployments. Equipped with an industrial-programmable optional Spartan 6 XC6SLX150 FPGA, Xilinx Artix 7 75T/100T/200T FPGA and featuring an ADI AD9364 RF integrated circuit in its transmit front-end, it is a cost-effective single-channel transceiver (1T1R).



Block Diagram



Features

- Compact size, highly integrated
- RF coverage from 70MHz to 6GHz
- Supports maximum real-time bandwidth of 56MHz with 61.44MSps base sampling rate
- Open-source UHD supports multiple frameworks (requires UHD 3.9.2 or newer driver version)
- Features high-speed USB 3.0 connection with USB power supply
- GPIO universal interface and JTAG debugging capability
- Supports 10MHz reference clock or PPS synchronization
- Compatible with GNU Radio open-source software framework

Specification

DC Voltage Input		**RF Performance Parameters**	
DC Voltage Input	5V	Input Third-Order Intercept Point (IIP3)	-21dBm
Converter Module Parameters		Maximum Output Power	>9dBm
ADC Sampling Rate (Max)	61.44 MSps	Noise Figure	<8dB
ADC Resolution	12 bits	LO Accuracy	±2.0ppm
DAC Sampling Rate	61.44 MSps	**Physical Characteristics**	
DAC Resolution	12 bits	Dimensions	10.4*5.7cm
Maximum Host Rate (16b)	61.44 MSps	Weight	0.04kg

Baseband Processor and RF Frontend

High-performance Baseband

Equipped with an industrial-grade programmable optional Spartan 6 XC6SLX150 FPGA, Xilinx Artix 7 75T/100T/200T FPGA, allowing users to program it according to their needs to implement various custom signal processing algorithms and functions, enhancing the device's flexibility and scalability.

High Bandwidth Capability

The RF frontend utilizes Analog Devices' AD9364 RFIC transceiver, supporting a maximum real-time bandwidth of 56MHz with a base sampling rate of 61.44 MSps, making it suitable for wideband signal processing (e.g., LTE, Wi-Fi).

Interfaces and Connectivity

High-Speed USB Interface

Powered via high-speed USB 3.0 bus and used for data transfer to the host, providing a fast and convenient data transmission channel capable of meeting high-bandwidth data transfer requirements.

Expansion and Debugging Capabilities

Offers 8 GPIO pins for controlling external devices and expanding functionality (e.g., sensors, triggers);

Supports JTAG debugging, facilitating FPGA program debugging and development.

Synchronization and Clock System

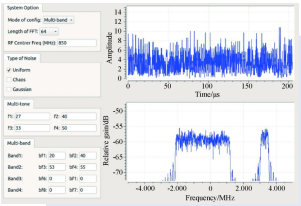
Supports external 10 MHz reference clock and PPS synchronization, enabling multi-device synchronization and control through shared clock/trigger signals.

Compatible Platforms

Applications

Wireless Communication Research

- Physical layer development & testing for 5G/6G, Wi-Fi, LTE protocols
- 2x2 MIMO system experiments (e.g. beamforming)



Portable Field Applications

- On-site spectrum monitoring & interference detection
- Mobile comms testing (drone communications, IoT nodes)

IoT & Sensor Networks

- Custom wireless protocol development (LoRa/ZigBee)
- Low-power communication system experiments

Education & Labs

- University communication engineering courses
- Open-source projects (GNU Radio signal processing workflows)