PCN Number:	PCN# 20251014001.2	**PCN Date:**	October 14, 2025

Title:	Qualification of CDAT as an additional Assembly/Test site for select devices

Customer Contact:	Change Management Team	**Dept:**	Quality Services
Proposed 1st Ship Date:	April 12, 2026	**Sample requests accepted until:**	December 13, 2025*

***Sample requests received after** December 13, 2025 **will not be supported.**

Change Type:

☒	Assembly Site	☐	Design	☐	Wafer Bump Material
☒	Assembly Process	☐	Data Sheet	☐	Wafer Bump Process
☒	Assembly Materials	☐	Part number change	☐	Wafer Fab Site
☐	Mechanical Specification	☒	Test Site	☐	Wafer Fab Material
☒	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of CDAT as an additional Assembly/Test site for the devices listed below. Construction differences are as follows:

	HFTF	HNA	TFME	CDAT
Mount Compound	4207123	SID#A-09	SID#A-09 SID# A-03	4207123 4226215
Bond wire diam/type	0.8mil Cu	1.0mil Au	1.0mil Au	0.8mil Cu
Mold Compound	SID#R-27	SID#450179	SID# R-07	4222198
Lead finish	NiPdAu	NiPdAu	NiPdAu	Matte Sn
Wafer thickness	6.0mil	7.5mil	7.5mil	6.0mil

Upon expiry of this PCN, TI will combine lead finish solutions in a single standard part number. For example, a customer order for 7500 units of a specific TI part number with 2500 units SPQ (Standard Pack Quantity per reel) may be fulfilled in the following ways:

- 3 reels of NiPdAu finish
- 3 reels of Matte Sn finish
- 2 reels of Matte Sn and 1 reel of NiPdAu finish
- 2 reels of NiPdAu and 1 reel of Matte Sn finish

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ

Qual details are provided in the Qual Data Section.

Reason for Change:

Supply continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

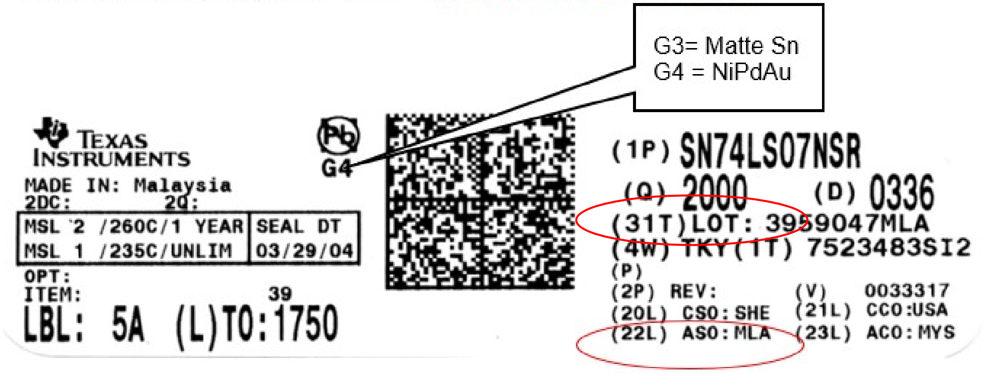
Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
HFTF	HFT	CHN	Hefei
HNA	HNT	THA	Ayutthaya
TFME	NFM	CHN	Economic Development Zone
CDAT	**CDA**	**CHN**	**Chengdu**

Sample product shipping label (not actual product label)



G3= Matte Sn
G4 = NiPdAu

TEXAS INSTRUMENTS
MADE IN: Malaysia
2DC: 2Q:
MSL 2 /260C/1 YEAR | SEAL DT
MSL 1 /235C/UNLIM | 03/29/04
OPT:
ITEM: 39
LBL: 5A (L)TO:1750
G4
(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T)LOT: 3959047MLA
(4W) TKY(1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CSO: SHE (21L) CCO:USA
(22L) ASO: MLA (23L) ACO: MYS

Product Affected:

INA186A1QDCKRQ1*	INA186A3QDCKRQ1*	TLV70030QDCKRQ1
INA186A2QDCKRQ1*	SN74LV1T34QDCKRQ1	TS5A3166QDCKRQ1

* G4 part numbers are available and will remain on NiPdAu flows. This PCN does not apply to existing G4 materials. Please visit TI’s labeling and symbolization page for more information on material designators

Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 06-December-2024

Product Attributes

Attributes	**Qual Device:** INA210BQDCKRTL	**QBS Process Reference:** INA215AQDCKRQ1	**QBS Package Reference:** TPS3840PH30DBVRQ1	**QBS Package Reference:** LM74703QDDFRQ1	**QBS Package Reference:** TXS0101QDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Power Management	Power Management	Logic
Wafer Fab Supplier	AIZU	AIZU	RFAB	RFAB	RFAB
Assembly Site	CDAT	TFME	CDAT	CDAT	CDAT
Package Group	SOT	SOT	SOT	SOT	SOT
Package Designator	DCK	DCK	DBV	DDF	DCK
Pin Count	6	6	5	8	6

QBS: Qual By Similarity, also known as Generic Data
Qual Device INA210BQDCKRTL is qualified at MSL1 260C
Note 1: Qual device and affected devices in PCN have justification to use Package QBS references for HAST, AC/UHAST and TC-BP based on AEC-100J A1.3 assembly site and package attributes were qualified.
Note 2: Qual device and affected devices in PCN have justification to use Process QBS references for HTOL and ELFR based on AEC-100J A1.2 silicon wafer fab and process attributes were qualified. Group B tests purpose is for silicon defects, they do not get influenced by assembly site or BOM differences.
Note 3: Qual device and affected devices in PCN have justification to use SD QBS based on AEC-100J A1.3 leadframe attributes are qualified.
Note 4: One lot is allowed per AEC-Q100J A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: INA210BQDCKRTL	QBS Process Reference: INA215AQDCKRQ1	QBS Package Reference: TPS3840PH30DBVRQ1	QBS Package Reference: LM74703QDDFRQ1	QBS Package Reference: TXS0101QDCKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	1/Pass Note 4	-	3/Pass	3/Pass	3/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	-	3/231/0	3/231/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	1/77/0 Note 4	-	-	3/231/0	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0 Note 4	-	3/231/0	3/231/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	Note 1	-	1/5/0	1/5/0	1/5/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	1/45/0 Note 4	-	3/135/0	1/45/0	3/135/0
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 2	3/231/0	3/231/0	-	1/77/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	Note 2	-	-	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 2	3/2400/0	-	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0 Note 4	1/30/0	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0 Note 4	1/30/0	3/90/0	3/90/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	Note 3	-	1/15/0	1/15/0	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	Note 3	-	1/15/0	1/15/0	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0 Note 4	-	3/30/0	3/30/0	3/30/0
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0 Note 4	-	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0 Note 4	-	-	-	-
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 4	-	-	-	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2405-062

Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)

Q006 SOT at CDAT

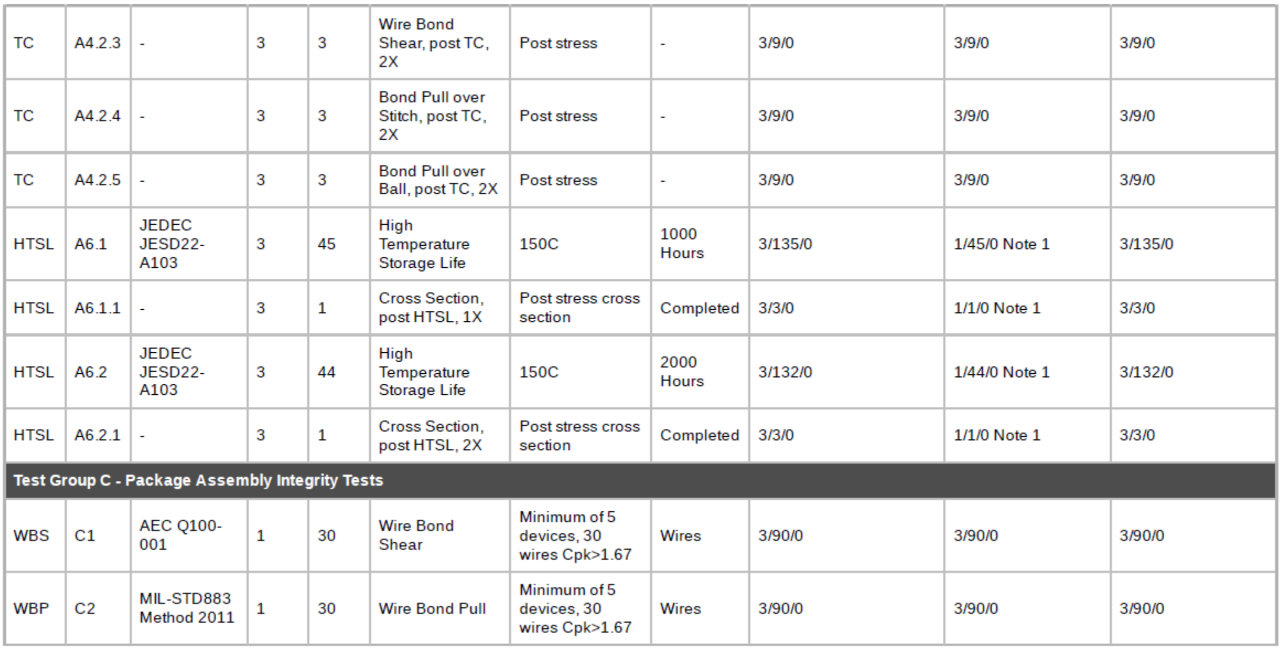
Approve Date 06-December-2024

Attributes	Q006 Reference: TPS3840PH30DBVRQ1	Q006 Reference: LM74703QDDFRQ1	Q006 Reference: TXS0101QDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Power Management	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB
Assembly Site	CDAT	CDAT	CDAT
Package Group	SOT	SOT	SOT
Package Designator	DBV	DDF	DCK
Pin Count	5	8	6

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Q006 Reference: TPS3840PH30DBVRQ1	Q006 Reference: LM74703QDDFRQ1	Q006 Reference: TXS0101QDCKRQ1
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	3/Pass	3/Pass
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0	3/66/0	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0	3/66/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	Note 1	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0	Note 1	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0	Note 1	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0	Note 1	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0	Note 1	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0	Note 1	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0	Note 1	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0	Note 1	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0	Note 1	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0	Note 1	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0	Note 1	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0	3/66/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0	3/3/0	3/3/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0	3/9/0	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0	3/9/0	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0	3/9/0	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0	3/210/0	3/210/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	3/66/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	3/3/0	3/3/0



TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0	3/9/0	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0	3/9/0	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0	3/9/0	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	1/45/0 Note 1	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0	1/1/0 Note 1	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/132/0	1/44/0 Note 1	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0	1/1/0 Note 1	3/3/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0

This report represents AEC-Q006 7.1 Family Data Usage using technology driver and lead products that are most representative of the technology family.
Note 1: LM74703QDDFRQ1 HAST and HTSL QBS'd to TPS3840PH30DBVRQ1 that has same Assembly site, package, bond pad metal, wire and mold attributes.
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2405-062

Automotive New Product Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 02-July-2025

Product Attributes

Attributes	Qual Device: CAHC1G125QDCKRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: TL331QDBVRQ1	QBS Package, Product Reference: CAHCT1G125QDBVRQ1	QBS Package Reference: TXS0101QDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain,Logic	Logic	Signal Chain	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB	RFAB	RFAB
Assembly Site	CDAT	MLA	CDAT	CDAT	CDAT
Package Group	SOT	TSSOP	SOT	SOT	SOT
Package Designator	DCK	PW	DBV	DBV	DCK
Pin Count	5	14	5	5	6

QBS: Qual By Similarity, also known as Generic Data
Qual Device CAHC1G125QDCKRQ1 is qualified at MSL1 260C
Per AEC-Q100J A1.3: The PCN devices are categorized as a qualification family and use generic data that has been qualified for the critical attributes in Die sizes, Package Type, Assembly Process and Site
Note 1: Qual Device and affected devices in PCN have justification to use Package and Process QBS references for Group A, Group B and Group C tests based on AEC-100J Appendix 1 A1.2 and A1.3. The fab, assembly site and package attributes were qualified.
Note 2: Other devices have passed HBM/CDM/LU with the final wafer/backgrind thickness. TI will not re-run HBM/CDM/LU for this change since backgrind removes bulk silicon and does not affect the active area of die. HBM/CDM/LU purpose is to test the active area of die, die circuit design and/or wafer fab defects that would result damage to dielectrics, junctions, metal.
Note 3: ED cannot use Generic data per AEC-Q100J but there is representation of passing Electrical Distributions in QBS Package devices with the same assembly site and package attributes.

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CAHC1G125QDCKRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: TL331QDBVRQ1	QBS Package, Product Reference: CAHCT1G125QDBVRQ1	QBS Package Reference: TXS0101QDCKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	Note 1	-	3/Pass	3/Pass	3/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	-	3/231/0	1/77/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	Note 1	-	3/231/0	1/77/0	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	Note 1	-	3/231/0	1/77/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	Note 1	-	1/6/0	1/5/0	1/5/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	Note 1	-	-	-	3/135/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	Note 1	-	1/45/0	1/45/0	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 1	3/231/0	-	-	3/231/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	Note 1	-	1/77/0	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 1	3/2400/0	-	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	3/90/0	1/30/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	3/90/0	1/30/0	3/90/0

SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	Note 1	1/15/0	1/15/0	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	Note 1	1/15/0	1/15/0	-	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	3/30/0	3/30/0	1/10/0	3/30/0
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	Note 2	-	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	Note 2	-	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	Note 2	-	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	Note 3	-	1/30/0	1/30/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2502-024

Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)

Q006 SOT at CDAT

Approve Date 02-July-2025

Attributes	QBS Package Reference: TXS0101QDCKRQ1
Automotive Grade Level	Grade 1
Operating Temp Range (C)	-40 to 125
Product Function	Logic
Wafer Fab Supplier	RFAB
Assembly Site	CDAT
Package Group	SOT
Package Designator	DCK
Pin Count	6

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	QBS Reference: TXS0101QDCKRQ1
Test Group A - Accelerated Environment Stress Tests								
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0

TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0
Test Group C - Package Assembly Integrity Tests								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0

This report represents AEC-Q006 7.1 Family Data Usage using technology driver and lead products that are most representative of the technology family.
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2502-024

ZVEI IDs: SEM-PW-03, SEM-PA-05, SEM-PA-07, SEM-PA-08, SEM-PA-11, SEM-PA-18, SEM-TF-01

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a ‘product qualification family’ for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled “QBS

Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to Change Management team or your local Field Sales Representative.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.