

DDR5 SDRAM RDIMM Addendum

MTC40F2046S1RC – 64GB

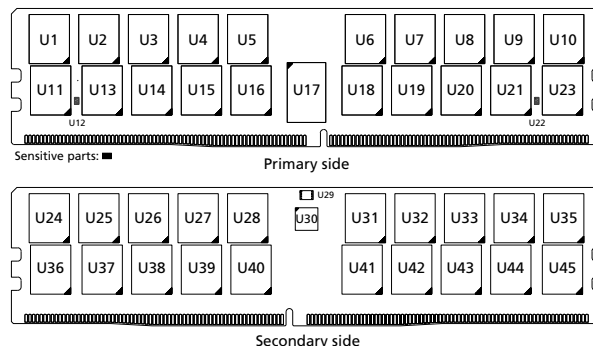
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800
- 64GB (8Gig x 80)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 RDIMM (R/C-A0)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.416ns @ CL = 40 (DDR5-4800)

Marking

C

48B

Table 1: Addressing

Parameter	64GB
Row address ¹	64K (R0-R15)
Column address ¹	2K (C0-C10)
Device bank group address ¹	8 (BG0-BG2)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (4Gb x 4), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 64GB Modules

Base device: MT60B4G4,¹ 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL _n RCD _n RP)
MTC40F2046S1RC48BA1	64GB	8Gb x 80 (EC8)	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on [micron.com](https://www.micron.com).



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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	7A	161	U2	0	15A	172
	1	4A	14		1	12A	25
	2	6A	159		2	14A	170
	3	5A	16		3	13A	27
U3	0	23A	183	U4	0	31A	194
	1	20A	36		1	28A	47
	2	22A	181		2	30A	192
	3	21A	38		3	29A	49
U5	0	CB7A	205	U6	0	CB7B	236
	1	CB4A	58		1	CB4B	89
	2	CB6A	203		2	CB6B	234
	3	CB5A	60		3	CB5B	91
U7	0	3B	247	U8	0	11B	258
	1	0B	100		1	8B	111
	2	2B	245		2	10B	256
	3	1B	102		3	9B	113
U9	0	19B	269	U10	0	27B	280
	1	16B	122		1	24B	133
	2	18B	267		2	26B	278
	3	17B	124		3	25B	135
U11	0	3A	154	U13	0	11A	165
	1	0A	7		1	8A	18
	2	2A	152		2	10A	163
	3	1A	9		3	9A	20
U14	0	19A	176	U15	0	27A	187
	1	16A	29		1	24A	40
	2	18A	174		2	26A	185
	3	17A	31		3	25A	42
U16	0	CB3A	198	U18	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB2A	196		2	CB2B	241
	3	CB1A	53		3	CB1B	98



64GB (x80, ECC, DR) 288-Pin DDR5 RDIMM DQ Map

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	7B	254	U20	0	15B	265
	1	4B	107		1	12B	118
	2	6B	252		2	14B	263
	3	5B	109		3	13B	120
U21	0	23B	276	U23	0	31B	287
	1	20B	129		1	28B	140
	2	22B	274		2	30B	285
	3	21B	131		3	29B	142
U24	0	24B	133	U25	0	16B	122
	1	27B	280		1	19B	269
	2	25B	135		2	17B	124
	3	26B	278		3	18B	267
U26	0	8B	111	U27	0	0B	100
	1	11B	258		1	3B	247
	2	9B	113		2	1B	102
	3	10B	256		3	2B	245
U28	0	CB4B	89	U31	0	CB4A	58
	1	CB7B	236		1	CB7A	205
	2	CB5B	91		2	CB5A	60
	3	CB6B	234		3	CB6A	203
U32	0	28A	47	U33	0	20A	36
	1	31A	194		1	23A	183
	2	29A	49		2	21A	38
	3	30A	192		3	22A	181
U34	0	12A	25	U35	0	4A	14
	1	15A	172		1	7A	161
	2	13A	27		2	5A	16
	3	14A	170		3	6A	159
U36	0	28B	140	U37	0	20B	129
	1	31B	287		1	23B	276
	2	29B	142		2	21B	131
	3	30B	285		3	22B	274
U38	0	12B	118	U39	0	4B	107
	1	15B	265		1	7B	254
	2	13B	120		2	5B	109
	3	14B	263		3	6B	252



Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U40	0	CB0B	96	U41	0	CB0A	51
	1	CB3B	243		1	CB3A	198
	2	CB1B	98		2	CB1A	53
	3	CB2B	241		3	CB2A	196
U42	0	24A	40	U43	0	16A	29
	1	27A	187		1	19A	176
	2	25A	42		2	17A	31
	3	26A	185		3	18A	174
U44	0	8A	18	U45	0	0A	7
	1	11A	165		1	3A	154
	2	9A	20		2	1A	9
	3	10A	163		3	2A	152

I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 64GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	345	mA
Operating four bank ACTIVATE-PRECHARGE current	I _{DD0F} ¹	436	mA
Precharge standby current	I _{DD2N} ²	313	mA
Precharge standby non-target command	I _{DD2NT} ¹	494	mA
Precharge power-down current	I _{DD2P} ²	289	mA
Active standby current	I _{DD3N} ²	356	mA
Active power-down current	I _{DD3P} ²	333	mA
Operating burst read current	I _{DD4R} ¹	798	mA
Operating burst write current	I _{DD4W} ¹	971	mA
Operating burst write with write CRC current	I _{DD4WC} ¹	993	mA
Burst refresh (normal refresh mode) current	I _{DD5B} ¹	660	mA
Burst refresh (fine granularity refresh mode) current	I _{DD5F} ¹	469	mA
Burst refresh (same bank refresh mode) current	I _{DD5C} ¹	382	mA
Self refresh current	I _{DD6N} ²	148	mA
Operating bank interleave read current	I _{DD7} ¹	899	mA
Maximum power saving deep power down mode current	I _{DD8} ²	169	mA

Notes: 1. One module rank in this I_{DD}/I_{DDQ}/I_{PP} condition, the other rank in I_{DD2N}/I_{DDQ2N}/I_{PP2N}.

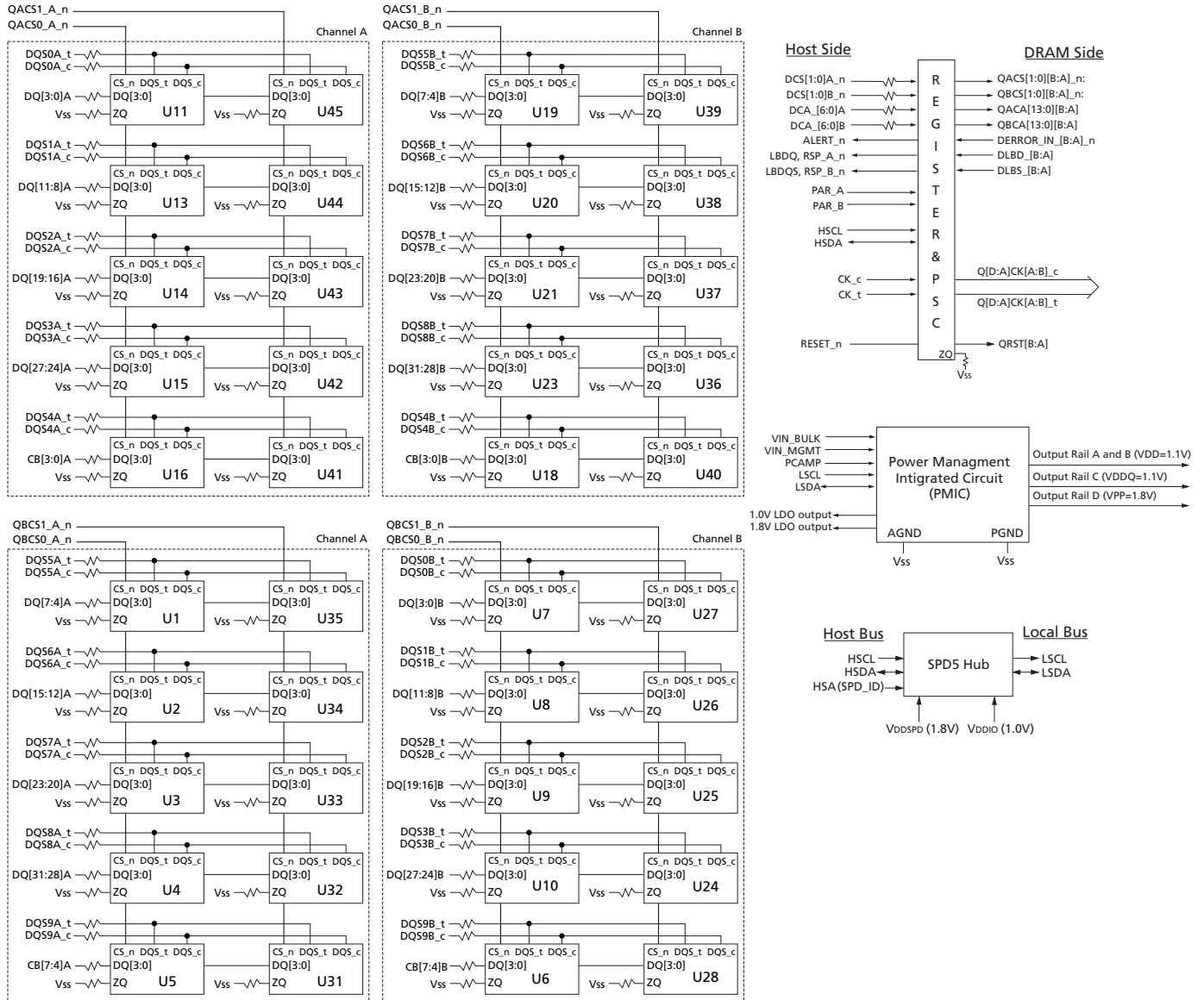
2. Both ranks in this I_{DD}/I_{DDQ}/I_{PP} condition.



64GB (x80, ECC, DR) 288-Pin DDR5 RDIMM Functional Block Diagram

Functional Block Diagram

Figure 2: Functional Block Diagram



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
 2. Functional block diagram is for reference only.



Revision History

Rev. D – 08/2021

- Production Release

Rev. C – 02/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.