Product Specification | Rev. 1.0 | 2022

IMM2G72D4DVD8AG (Die Revision B)

16GByte (2G x 72 Bit)

16GB DDR4 VLP ECC Unbuffered DIMM
RoHS Compliant Product

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Features

- 288-Pin Unbuffered Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- SPD Power Supply: V_{DDSPD} = 2.5 or 3.3V
- Power Supply: V_{DD}, V_{DDQ} = 1.2 ± 0.06V
- DRAM Activating Power Supply: V_{PP} = 2.5V(2.375V – 2.75V)
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - DDR4-3200: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
- Programmable CAS Write Latency (CWL):
  - DDR4-3200: 9, 10, 11, 12, 14, 16, 18, 20
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- Low Power Auto Self Refresh mode is supported
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Very Low Profile Module Height: 18.75mm (0.738inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D4DVD8AG-Bzzzy	16GB	2Gx72	2	16GB DDR4 VLP ECC Unbuffered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_{case}^{*}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade		
Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
062	DDR4-3200	1600MHz (0.625ns@CL=22)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G72D4DVD8AG-Bzzzy	IM	IM8G08D4GBBG	1.2V	1Gx8	Lead Free

Part Number Decoder

IM M 2G72 D4 DV D 8 A G - B 062 (I)

IM Module

DRAM Brand
M = IM

Module Configuration
2G72 = 2Gx72 (16GB)

Memory Type
D4 = DDR4

Module Form-Factor
DV = VLP Unbuffered DIMM (VLP UDIMM)

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
B = Revision B

Speed Grade
062 = DDR4-3200 CL22

Temperature Grade
Blank = Commercial Temperature
(0°C to 95°C T_{case})
I = Industrial Temperature
(-40°C to 95°C T_{case})

Table 5 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	4 BA[1:0]
Device bank group	4 BG[1:0]
Device configuration	8Gb (1Gx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	18

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	145	NC	73	V_{DD}	217	V_{DD}
2	V_{SS}	146	V_{REFCA}	74	CK0	218	CK1
3	D4	147	V_{SS}	75	/CK0	219	/CK1
4	V_{SS}	148	D5	76	V_{DD}	220	V_{DD}
5	D0	149	V_{SS}	77	V_{TT}	221	V_{TT}
6	V_{SS}	150	D1	78	/EVENT	222	PARITY
7	/DM0, /DBI0	151	V_{SS}	79	A0	223	V_{DD}
8	NC	152	/DQS0	80	V_{DD}	224	BA1
9	V_{SS}	153	DQS0	81	BA0	225	A10, AP
10	D6	154	V_{SS}	82	/RAS	226	V_{DD}
11	V_{SS}	155	D7	83	V_{DD}	227	NC
12	D2	156	V_{SS}	84	/CS0	228	A14, /WE
13	V_{SS}	157	D3	85	V_{DD}	229	V_{DD}
14	D12	158	V_{SS}	86	A15, /CAS	230	NC
15	V_{SS}	159	D13	87	ODT0	231	V_{DD}
16	D8	160	V_{SS}	88	V_{DD}	232	A13
17	V_{SS}	161	D9	89	/CS1	233	V_{DD}
18	/DM1, /DBI1	162	V_{SS}	90	V_{DD}	234	NC
19	NC	163	/DQS1	91	ODT1	235	NC
20	V_{SS}	164	DQS1	92	V_{DD}	236	V_{DD}
21	D14	165	V_{SS}	93	NC	237	NC
22	V_{SS}	166	D15	94	V_{SS}	238	SA2
23	D10	167	V_{SS}	95	D36	239	V_{SS}
24	V_{SS}	168	D11	96	V_{SS}	240	D37
25	D20	169	V_{SS}	97	D32	241	V_{SS}
26	V_{SS}	170	D21	98	V_{SS}	242	D33
27	D16	171	V_{SS}	99	/DM4, /DBI4	243	V_{SS}
28	V_{SS}	172	D17	100	NC	244	/DQS4
29	/DM2, /DBI2	173	V_{SS}	101	V_{SS}	245	DQS4
30	NC	174	/DQS2	102	D38	246	V_{SS}
31	V_{SS}	175	DQS2	103	V_{SS}	247	D39
32	D22	176	V_{SS}	104	D34	248	V_{SS}
33	V_{SS}	177	D23	105	V_{SS}	249	D35
34	D18	178	V_{SS}	106	D44	250	V_{SS}
35	V_{SS}	179	D19	107	V_{SS}	251	D45
36	D28	180	V_{SS}	108	D40	252	V_{SS}
37	V_{SS}	181	D29	109	V_{SS}	253	D41
38	D24	182	V_{SS}	110	/DM5, /DBI5	254	V_{SS}
39	V_{SS}	183	D25	111	NC	255	/DQS5
40	/DM3, /DBI3	184	V_{SS}	112	V_{SS}	256	DQS5
41	NC	185	/DQS3	113	D46	257	V_{SS}
42	V_{SS}	186	DQS3	114	V_{SS}	258	D47
43	D30	187	V_{SS}	115	D42	259	V_{SS}
44	V_{SS}	188	D31	116	V_{SS}	260	D43
45	D26	189	V_{SS}	117	D52	261	V_{SS}
46	V_{SS}	190	D27	118	V_{SS}	262	D53
47	CB4	191	V_{SS}	119	D48	263	V_{SS}
48	V_{SS}	192	CB5	120	V_{SS}	264	D49
49	CB0	193	V_{SS}	121	/DM6, /DBI6	265	V_{SS}
50	V_{SS}	194	CB1	122	NC	266	/DQS6
51	/DM8, /DBI8	195	V_{SS}	123	V_{SS}	267	DQS6
52	NC	196	/DQS8	124	D54	268	V_{SS}
53	V_{SS}	197	DQS8	125	V_{SS}	269	D55
54	CB6	198	V_{SS}	126	D50	270	V_{SS}
55	V_{SS}	199	CB7	127	V_{SS}	271	D51

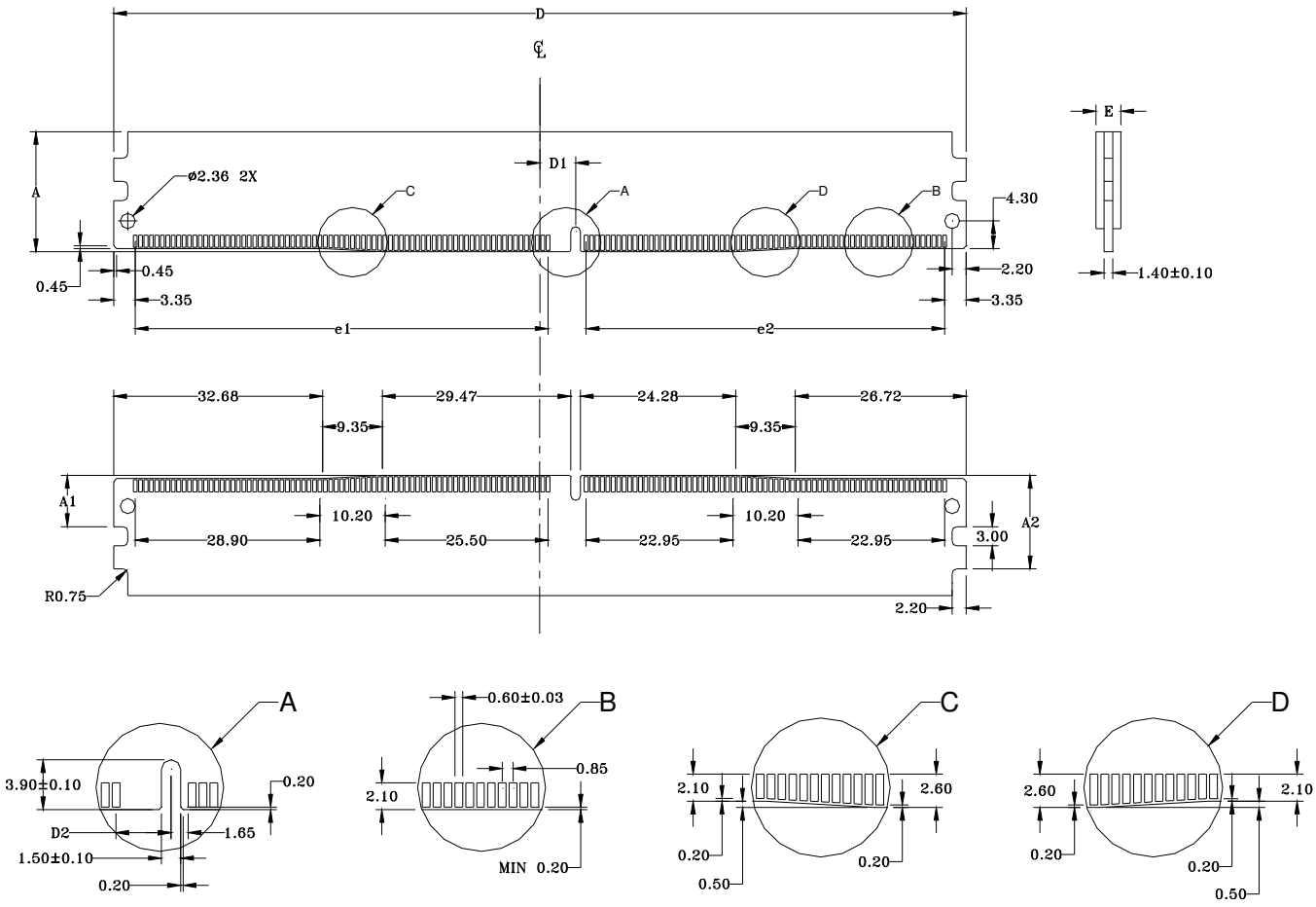
Pin	Name	Pin	Name	Pin	Name	Pin	Name
56	CB2	200	V_{SS}	128	D60	272	V_{SS}
57	V_{SS}	201	CB3	129	V_{SS}	273	D61
58	/RESET	202	V_{SS}	130	D56	274	V_{SS}
59	V_{DD}	203	CKE1	131	V_{SS}	275	D57
60	CKE0	204	V_{DD}	132	/DM7, /DBI7	276	V_{SS}
61	V_{DD}	205	NC	133	NC	277	/DQS7
62	/ACT	206	V_{DD}	134	V_{SS}	278	DQS7
63	BG0	207	BG1	135	D62	279	V_{SS}
64	V_{DD}	208	/ALERT	136	V_{SS}	280	D63
65	A12, /BC	209	V_{DD}	137	D58	281	V_{SS}
66	A9	210	A11	138	V_{SS}	282	D59
67	V_{DD}	211	A7	139	SA0	283	V_{SS}
68	A8	212	V_{DD}	140	SA1	284	V_{DDSPD}
69	A6	213	A5	141	SCL	285	SDA
70	V_{DD}	214	A4	142	V_{PP}	286	V_{PP}
71	A3	215	V_{DD}	143	V_{PP}	287	V_{PP}
72	A1	216	A2	144	NC	288	V_{PP}

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM I/O & core power supply	V_{SS}	Power supply return (ground)
V_{REFCA}	SDRAM command/address reference supply	V_{PP}	SDRAM activating power supply
V_{TT}	SDRAM I/O termination supply	V_{DDSPD}	EEPROM positive power supply
A0-A15	Address input	BA0-BA1	Bank select input
BG0-BG1	Bank group select input	/RAS	Row address strobe input
/CAS	Column address strobe input	/WE	Write enable input
/CS0-/CS1	DIMM rank select lines input	CKE0-CKE1	Clock enable lines input
ODT0-ODT1	On-die termination control lines input	/ACT	Input for activate input
D0-D63	Memory data bus	CB0-CB7	ECC check bit
/DM0-/DM8	Data mask	/DBI0-/DBI8	Data bus inversion
DQS0-DQS8	Data strobe (Positive line of differential pair)	/DQS0-/DQS8	Data buffer strobe (Negative line of differential pair)
CK0-CK1	Clock input (Positive line of differential pair)	/CK0-/CK1	Clock input (Negative line of differential pair)
PARITY	Register parity input	/RESET	Set register and SDRAMs to a known state
/ALERT	Register /ALERT output	/EVENT	Temperature event
SDA	EEPROM data line	SCL	EEPROM clock
SA0-SA2	EEPROM address input	NC	Spare pin (no connect)

Module Dimension

Figure 1 – 288 Pin DDR4 VLP ECC Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	18.60	18.75	18.90
A1	7.85	8.00	8.15
A2	14.45	14.60	14.75
D	133.20	133.35	133.50
D1		5.575 BSC	
D2		4.30 BSC	
e1		64.60 BSC	
e2		56.10 BSC	
E			4.10

Notes:

1 All dimensioning and tolerancing conform to ASME Y14.5M–1994.
2 Tolerance on all dimensions ± 0.15 unless otherwise specified.
3 All dimensions are in millimeters.

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	May, 2022