# M21004

## 3G/HD/SD-SDI Low Power Backplane Equalizer and Redriver with 2x2 Crosspoint Switch

Rev V3

### Applications

- 3G/HD/SD-SDI switchers and routers
- SMPTE 259M, 292M, 344M, 424M, DVB ASI 270Mb/s

### Features

- Dual FR4 equalizer and output de-emphasis
- Robust operation up to 3.2Gbps
- Input equalization for up to 40" of FR4 + 2 connectors
- Output de-emphasis for up to 40" of FR4 + 2 connectors
- 2x2 crosspoint switch
- Integrated 50Ω input termination
- Loss of Signal detection at the input
- Very low power consumption (38 mW per channel @1.2V)
- On-chip regulators for operation from 1.2V to 3.3V DC supply
- Universal DC coupling at the input and output with integrated level shifter
- Industrial operating temperature range of -40°C to 85°C
- 4mm x 4mm, 24-pin QFN package

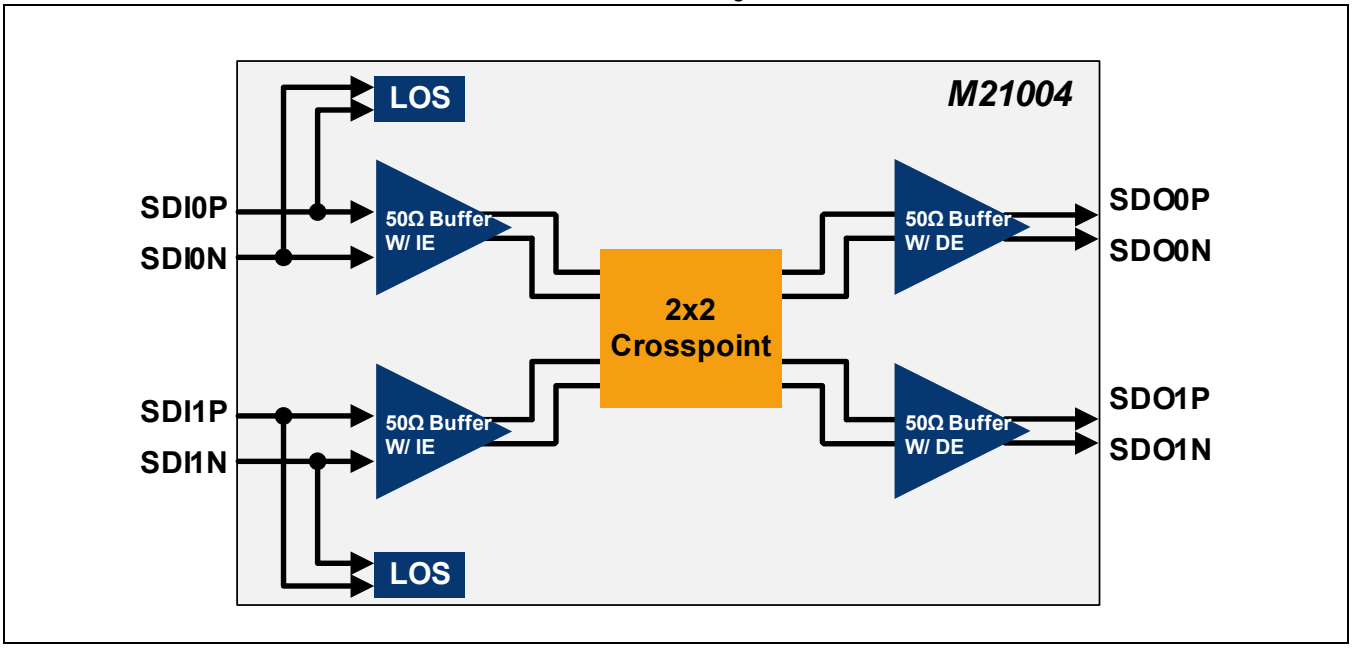
The M21004 is a very low power, highly integrated, dual backplane equalizer and redriver with optimized power and performance for Serial Digital Interface (SDI) video applications. It can also be used in non-SDI systems for data rates up to 3.2Gbps.

Each of the two independent channels has a 50Ω input buffer with configurable input equalizer, capable of compensating for losses across 40" of FR4 and two connectors. Each channel also includes a 50Ω output buffer with configurable de-emphasis to aid transmission of the signal across an additional 40" of FR4 trace and two connectors. In addition, the M21004 features a non-blocking 2x2 crosspoint switch. The switch allows either input to be routed to any or both of the outputs.

The device has integrated internal supply regulators, allowing it to be powered from a single 1.2V, 1.8V, 2.5V, or 3.3V supply voltage. The power rails for the input and output circuitry are electrically independent from each other and the core supply and thus may be connected to a different voltage rail on the board. This feature enables the M21004 to be DC coupled to any upstream and downstream device in the 1.2V to 3.3V range without level shifting.

The M21004 is offered in a green and RoHS compliant 24-pin QFN package.

**M21004 Block Diagrams**



## Ordering Information

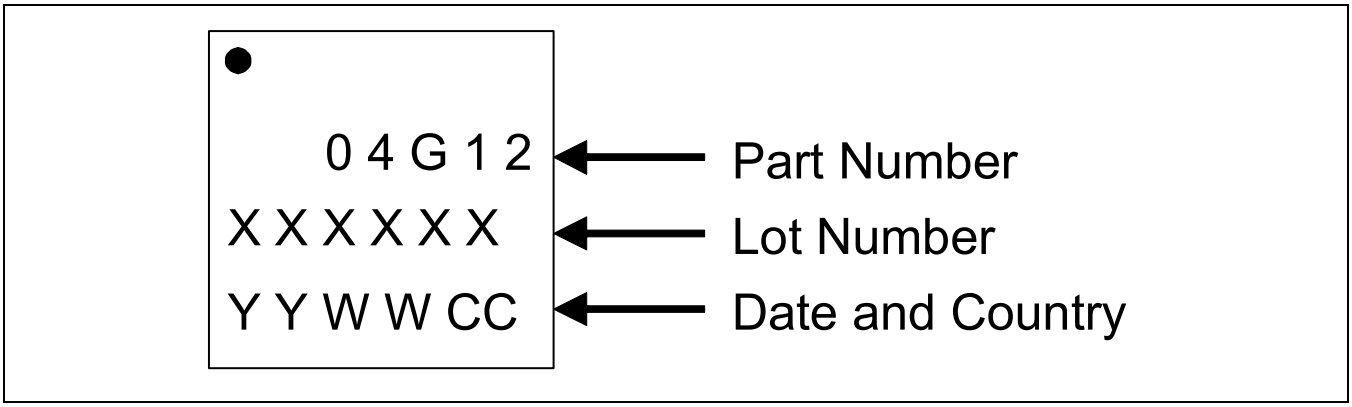
| Part Number | Package | Operating Temperature |
|---|---|---|
| M21004G-12* | 4 mm, 24-pin QFN (RoHS compliant) | –40 °C to 85 °C |

* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

## Revision History

| Revision | Level | Date | Description |
|---|---|---|---|
| V3 | Release | October 2017 | Added Tables 1-5 Logic output Characteristic<br>Updated Tables 4-5 XPT Control<br>Updated Tables 1-4 Output Characteristic |
| V2 | Release | December 2015 | Updated Package Drawing, Figure 3-9 and Figure 3-10.<br>Package effective as of July 2014. |
| C (V1) | Release | March 2010 | Added Marking Diagram.<br>Added final characterization figures to Tables 1-3, 1-4, 1-5.<br>Added Figures 3-2 to 3-8.<br>Added $\theta_{JA}$ to Table 1-3.<br>Added recommended 10 µF input caps in Section 4.1 and 4.3.<br>Added Figures 2-3, 2-4 and Section 4.2 and 4.3. |
| B (V2A) | Advance | November 2009 | Updated power, added jitter, DCD rise/fall time figures.<br>Add Section 4.6.4, 4.6.5, 4.6.6. |
| A (V1A) | Advance | July 2009 | Initial Release |

**Marking Diagram**



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# 1.0 Electrical Characteristics

Unless noted otherwise, specifications in this section apply to nominal power supply, 25 °C ambient temperature, 800 mVpp input data swing, default output data swing, PRBS $2^{15}$ – 1 test pattern, RL = 50Ω. voltages are referenced to $AV_{SS}$.

***Table 1-1. Absolute Maximum Ratings***

| Symbol | Parameter | Note | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $AV_{DD}0,1$ | Analog Core power supply voltage | 1 | -0.5 | — | 1.5 | V |
| $AV_{DD}OUT$ | Analog power Output supply voltage | 1 | -0.5 | — | 3.6 | V |
| $AV_{DD}IN$ | Analog power Input supply voltage | 1 | -0.5 | — | 3.6 | V |
| $V_{IN,PCML}$ | DC input voltage (PCML) | 1 | -0.5 | — | $AV_{DD}OUT$ + 0.5 | V |
| $V_{IN,CMOS}$ | DC input voltage (CMOS) | 1 | -0.5 | — | $AV_{DD}OUT$ + 0.5 | V |
| $T_{STORE}$ | Storage temperature | 1 | -65 | — | 150 | °C |
| $T_{JUNC}$ | Junction temperature | 1 | -40 | — | 125 | °C |
| $V_{ESD,HBM}$ | Electrostatic discharge voltage (HBM) | 1, 2 | — | — | 4 | kV |
| $V_{ESD,CDM}$ | Electrostatic discharge voltage (CDM) | 1, 2 | — | — | 500 | V |

***NOTES:***

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).

***Table 1-2. Recommended Operating Conditions***

| Symbol | Parameter | Note | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $AV_{DD}0,1$ | Analog Core supply voltage | — | 1.14 | 1.2 | 1.26 | V |
| $AV_{DD}OUT$ | Analog Output supply voltage | — | 1.14 | 1.2/1.8/2.5/3.3 | 3.47 | V |
| $AV_{DD}IN$ | Analog Input supply voltage | — | 1.14 | 1.2/1.8/2.5/3.3 | 3.47 | V |
| $T_{CASE}$ | Operating temperature | 1 | -40 | — | 85 | °C |

***NOTES:***

1. Case temperature.

***Table 1-3. Power Consumption Specifications***

| Symbol | Parameter | Note | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$CORE | Core current consumption | 1 | — | 35 | 50 | mA |
| $I_{DD}$OUT | Output current consumption | 1 | — | 30 | 40 | mA |
| $I_{DD}$IN | Input current consumption | 1, 5 | — | 0.7 | 1 | mA |
| $I_{DD}$TOTAL | Total current consumption | 1, 5 | — | 65 | 86 | mA |
| $P_{TOTAL}$ | Power consumption | 1, 5 | — | 75 | 108 | mW |
| $I_{DD}$CORE | Core Current consumption | 2 | — | 35 | 50 | mA |
| $I_{DD}$OUT | Output Current consumption | 2 | — | 40 | 50 | mA |
| $I_{DD}$IN | Input current consumption | 2, 5 | — | 0.7 | 1 | mA |
| $I_{DD}$TOTAL | Total current consumption | 2, 5 | — | 75 | 101 | mA |
| $P_{TOTAL}$ | Power consumption | 2, 5 | — | 90 | 128 | mW |
| $I_{DD}$CORE | Core Current consumption | 3 | — | 40 | 60 | mA |
| $I_{DD}$OUT | Output Current consumption | 3 | — | 60 | 80 | mA |
| $I_{DD}$IN | Input current consumption | 3, 5 | — | 8 | 10 | mA |
| $I_{DD}$TOTAL | Total current consumption | 3, 5 | — | 108 | 150 | mA |
| $P_{TOTAL}$ | Power consumption | 3, 5 | — | 272 | 388 | mW |
| $I_{DD}$OUT | Output Current consumption | 4 | — | 100 | 140 | mA |
| $I_{DD}$IN | Input current consumption | 4, 5 | — | 8 | 10 | mA |
| $I_{DD}$TOTAL | Total current consumption | 4, 5 | — | 108 | 150 | mA |
| $P_{TOTAL}$ | Power consumption | 4, 5 | — | 356 | 520 | mW |
| $\theta_{JA}$ | Junction to ambient thermal resistance | 6 | — | 60 | — | °C/W |

***NOTES:***

1. $AV_{DD}$CORE = 1.2V, $AV_{DD}$IN, $AV_{DD}$OUT = 1.2V and low output swing setting.
2. $AV_{DD}$CORE = 1.2V, $AV_{DD}$IN, $AV_{DD}$OUT = 1.2V and med output swing setting.
3. $AV_{DD}$CORE = 1.2V, $AV_{DD}$IN, $AV_{DD}$OUT = 3.3V and high output swing setting.
4. $AV_{DD}$IN, $AV_{DD}$OUT = 3.3V, Regulator Enabled and high output swing setting.
5. See Section 4.3 for additional current drawn by the input termination.
6. Airflow = 0 m/s.

### Table 1-4. PCML Input/Output Electrical Characteristics

| Symbol | Parameter | Note | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| DR | NRZ data rate | — | 143 | — | 3200 | Mbps |
| $V_{IN}$ | Differential Input Voltage | 1 | 250 | 800 | 1600 | mVppd |
| IE | Input equalization | — | — | 6, 4, 0 | — | dB |
| $R_{IN}$ | Input termination resistance | 2 | — | 50 | — | Ω |
| $V_{LOSA}$ | LOS level, assert | 1 | 70 | 75 | 85 | mVpp |
| $V_{LOSD}$ | LOS level, deassert | 1 | — | 145 | 160 | mVpp |
| $V_{OUT}$ | PCML differential output swing - low | 5 | 485 | 600 | 720 | mVppd |
| | PCML differential output swing - med | 5, 6 | 680 | 800 | 960 | mVppd |
| | PCML differential output swing - high | 4, 5 | 1000 | 1200 | 1440 | mVppd |
| $R_{OUT}$ | Output termination resistance | 3 | — | 50 | — | Ω |
| DE | Output de-emphasis settings | 7 | — | 6, 4, 0 | — | dB |
| $J_{OUT}$ | Total Output Jitter | 8, 9 | — | 95 | 170 | mUI |
| $DCD_O$ | Output Duty Cycle distortion | 8 | — | — | 16 | ps |
| tr/tf | Rise/Fall Time | — | — | 80 | 135 | ps |

***NOTES:***

1. Value specified at the device pins.
2. Internal termination to $AV_{DD}$IN.
3. Internal termination to $AV_{DD}$OUT.
4. To achieve high swing; $AV_{DD}$OUT must be > =1.8V.
5. Measured into 50Ω load.
6. Default output swing level.
7. Measured with 16 ones and 16 zeros pattern.
8. Measured at 3.2 Gbps
9. Measured point blank, BER = $10^{-12}$

### Table 1-5. Control/Interface Logic Input/Output Characteristics

| Symbol | Parameter | Note | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input logic high | | 0.85 x $AV_{DD}$OUT | — | $AV_{DD}$OUT | V |
| $V_{IF}$ | Input logic float | | 0.25 x $AV_{DD}$OUT | — | 0.75 x $AV_{DD}$OUT | V |
| $V_{IL}$ | Input logic low | | 0 | — | 0.15 x $AV_{DD}$OUT | V |
| $V_{OH}$ | Output logic high | | 0.8 x $AV_{DD}$OUT | $AV_{DD}$OUT | — | V |
| $V_{OL}$ | Output logic low | | — | 0 | 0.2 x $AV_{DD}$OUT | V |
| $I_{IL}$ | Input Current logic low | | 100 | — | | uA |
| $I_{IH}$ | Input Current logic high | | — | — | -100 | uA |

# 2.0 Typical Performance Characteristics

*Figure 2-1. Eye Diagram @ 0" FR4, 3.2 Gbps, $AV_{DD}$_CORE = $AV_{DD}$_IN = $AV_{DD}$_OUT = 1.2V, Medium Swing*

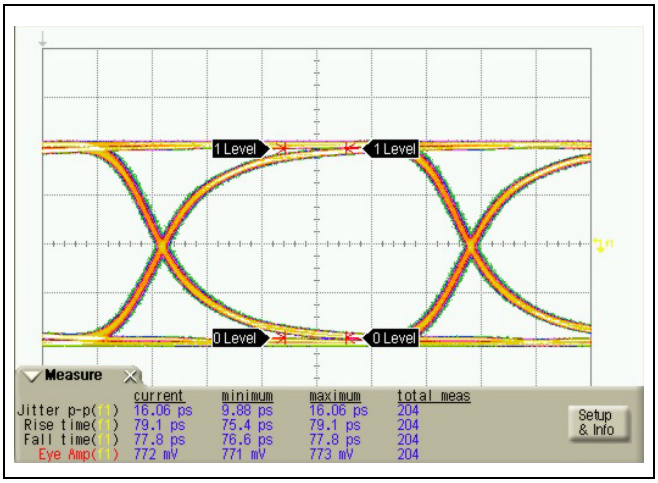



*Figure 2-2. Eye Diagram @ 40" FR4, 3.2 Gbps, $AV_{DD}$_CORE = $AV_{DD}$_IN = $AV_{DD}$_OUT = 1.2V, Medium Swing*

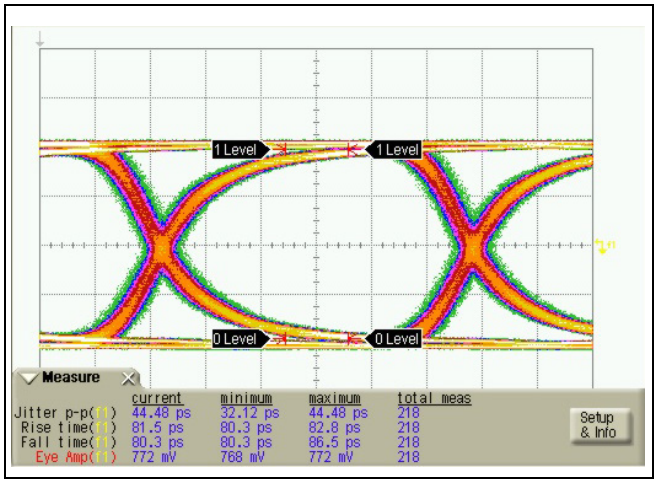



*Figure 2-3. Eye Diagram @ 0" FR4, 3.2 Gbps, $AV_{DD}$_CORE = $AV_{DD}$_IN = 1.2V, $AV_{DD}$_OUT = 1.8V, Medium Swing*

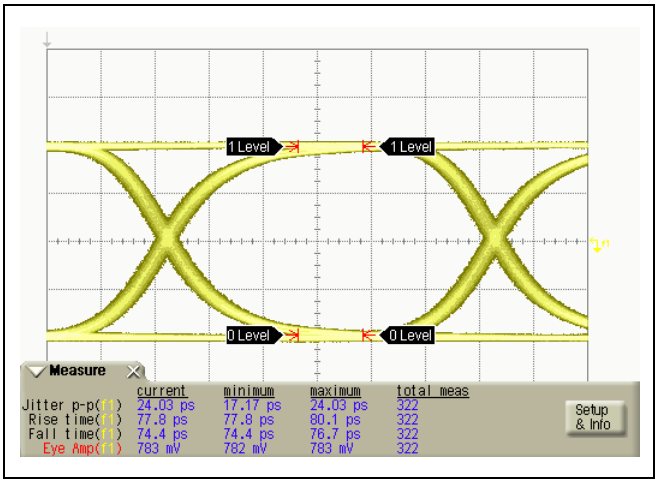
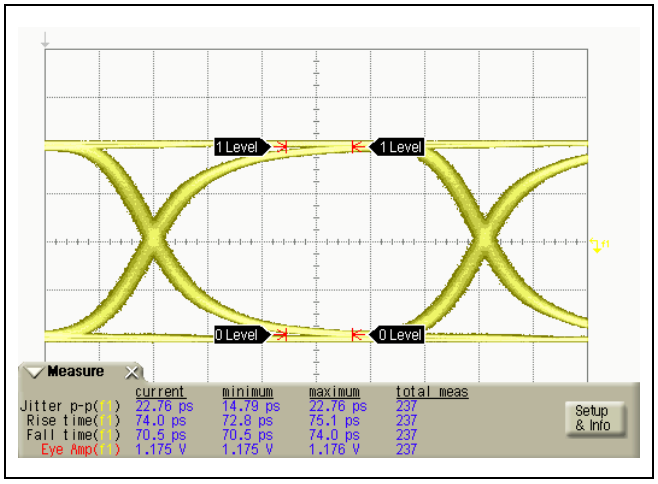



*Figure 2-4. Eye Diagram @ 0" FR4, 3.2 Gbps, $AV_{DD}$_CORE = $AV_{DD}$_IN = 1.2V, $AV_{DD}$_OUT = 1.8V, High Swing*



# 3.0 Pinout Diagram, Pin Descriptions, and Packaging Outline Drawing

***Figure 3-1. M21004 Pinout Diagram (Top View)***

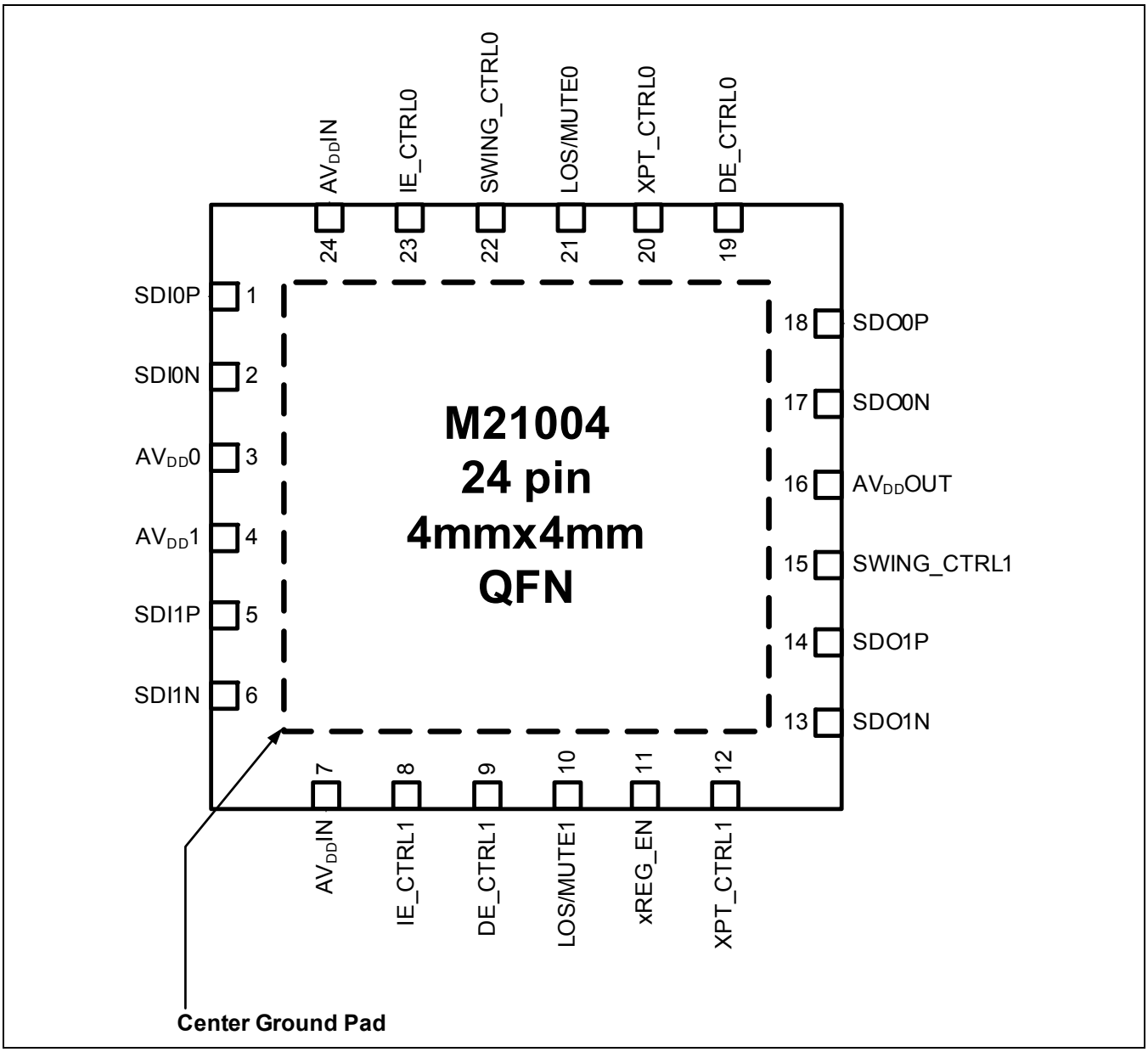


***Table 3-1. M21004 Pin Descriptions (1 of 2)***

| Pin Name | Pin Number(s) | Type | Description |
|---|---|---|---|
| $AV_{SS}$ | Center Pad | Power | Ground |
| $AV_{DD}0$ | 3 | Power | Analog Core positive supply for channel 0 |
| $AV_{DD}1$ | 4 | Power | Analog Core positive supply for channel 1 |
| $AV_{DD}OUT$ | 16 | Power | Analog positive supply for output circuitry |
| $AV_{DD}IN$ | 24, 7 | Power | Analog positive supply for input circuitry |
| xREG_EN | 11 | I–Digital with pull up | Internal regulator disable<br>L = Enable integrated regulator<br>H = disable integrated regulator (default) |
| XPT_CTRL[1:0] | 12, 20 | I–Digital: XPT_CTRL1 with pull up, XPT_CTRL0 with pull down | Input Crosspoint Control<br>L L = Broadcast SDI0; SDI0 to SDO0, SDI0 to SDO1<br>L H= Crossover; SDI1 to SDO0, SDI0 to SDO1<br>H L = Feedthrough; SDI0 to SDO0, SDI1 to SDI1 (default)<br>H H = Broadcast SDI1; SDI1 to SDO0, SDI1 to SDI1 |
| SWING_CTRL0, 1 | 22, 15 | 3-state/<br>I–Digital | Output swing control for channel 0 and channel 1<br>L = Low<br>F = Medium (default)<br>H = High |
| DE_CTRL0, 1 | 19, 9 | 3-state/<br>I–Digital | Output de-emphasis control for channel 0 and channel 1<br>L = DE off<br>F = Medium DE (default)<br>H = High DE |
| IE_CTRL0, 1 | 23, 8 | 3-state/<br>I–Digital | Input Equalization control for channel 0 and channel 1<br>L = IE off<br>F = Medium IE (default)<br>H = High IE |
| LOS/MUTE0, 1 | 21, 10 | O-Digital/<br>I–Digital | Configured as output (> 50 kΩ resistive load):<br>LOS alarm output (active high) for channel 0 and channel 1<br>Configured as input (driven with R < 0.25 kΩ)<br>L = never mute the output<br>H = force mute the output |
| SDI0P | 1 | I-Analog | Serial Data video input0, true |
| SDI0N | 2 | I-Analog | Serial Data video input0, complement |
| SDI1P | 5 | I-Analog | Serial Data video input1, true |
| SDI1N | 6 | I-Analog | Serial Data video input1, complement |
| SDO0P | 18 | O-Analog | Serial Data output0, true |

*Table 3-1. M21004 Pin Descriptions (2 of 2)*

| Pin Name | Pin Number(s) | Type | Description |
|---|---|---|---|
| SDO0N | 17 | O-Analog | Serial Data output0, complement |
| SDO1P | 14 | O-Analog | Serial Data output1, true |
| SDO1N | 13 | O-Analog | Serial Data output1, complement |
| ***NOTE:*** The default state is controlled by pull up/pull down resistors of 100kΩ to $AV_{DD}OUT$ or $AV_{SS}$. | | | |

*Figure 3-2. I-Analog*

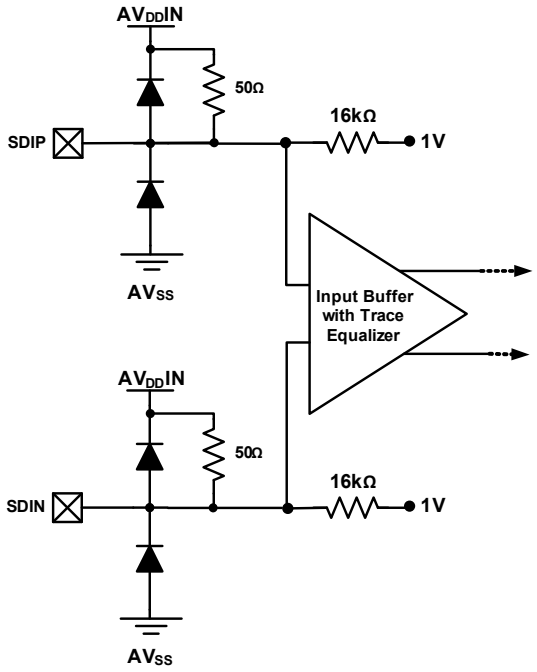


*Figure 3-3. O-Analog*

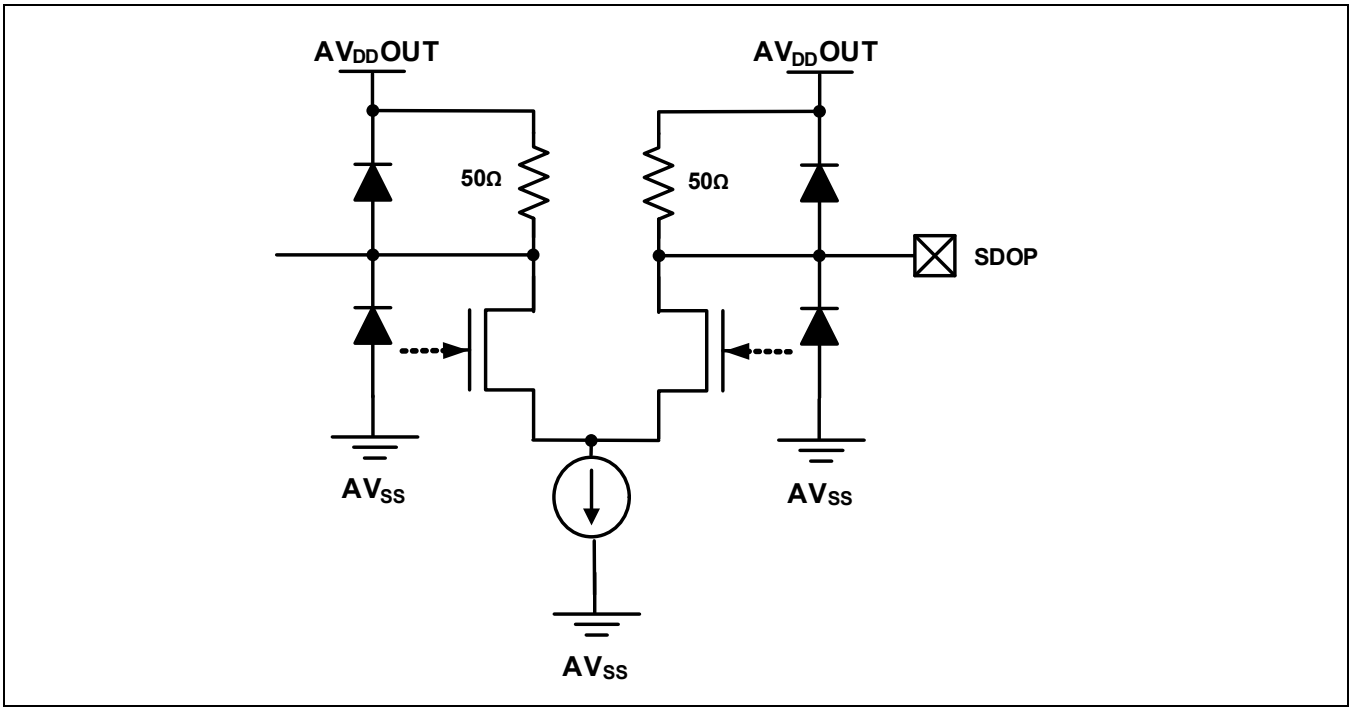


*Figure 3-4. I-Digital With Pull-up*

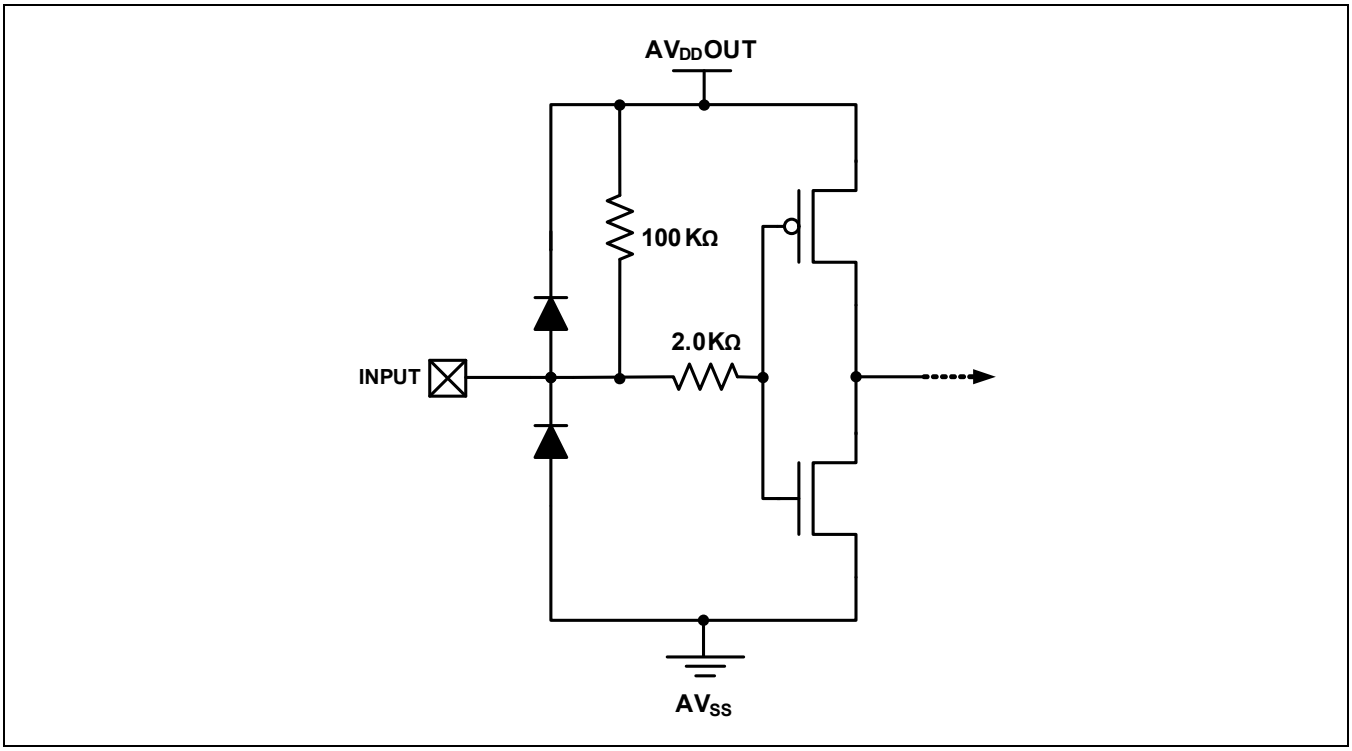


*Figure 3-5. I-Digital With Pull-down*

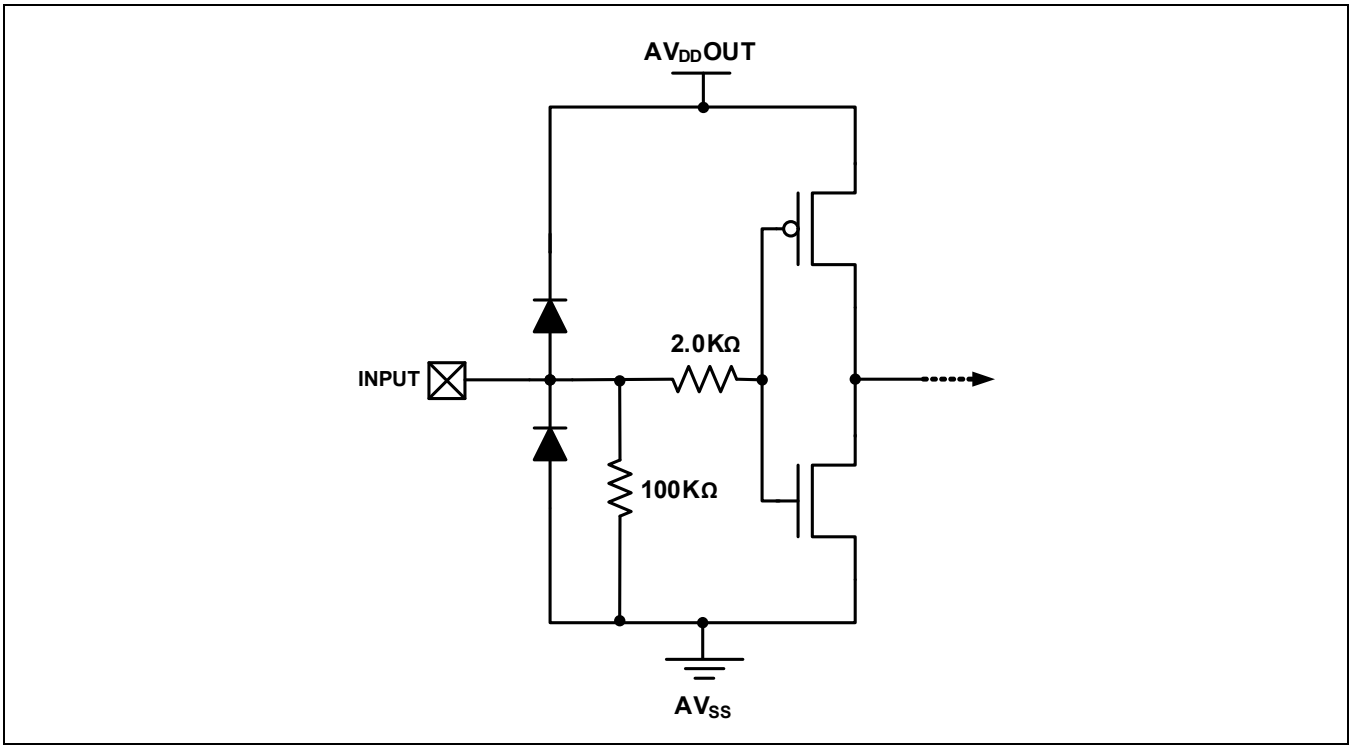


*Figure 3-6. 3-State/I-Digital*

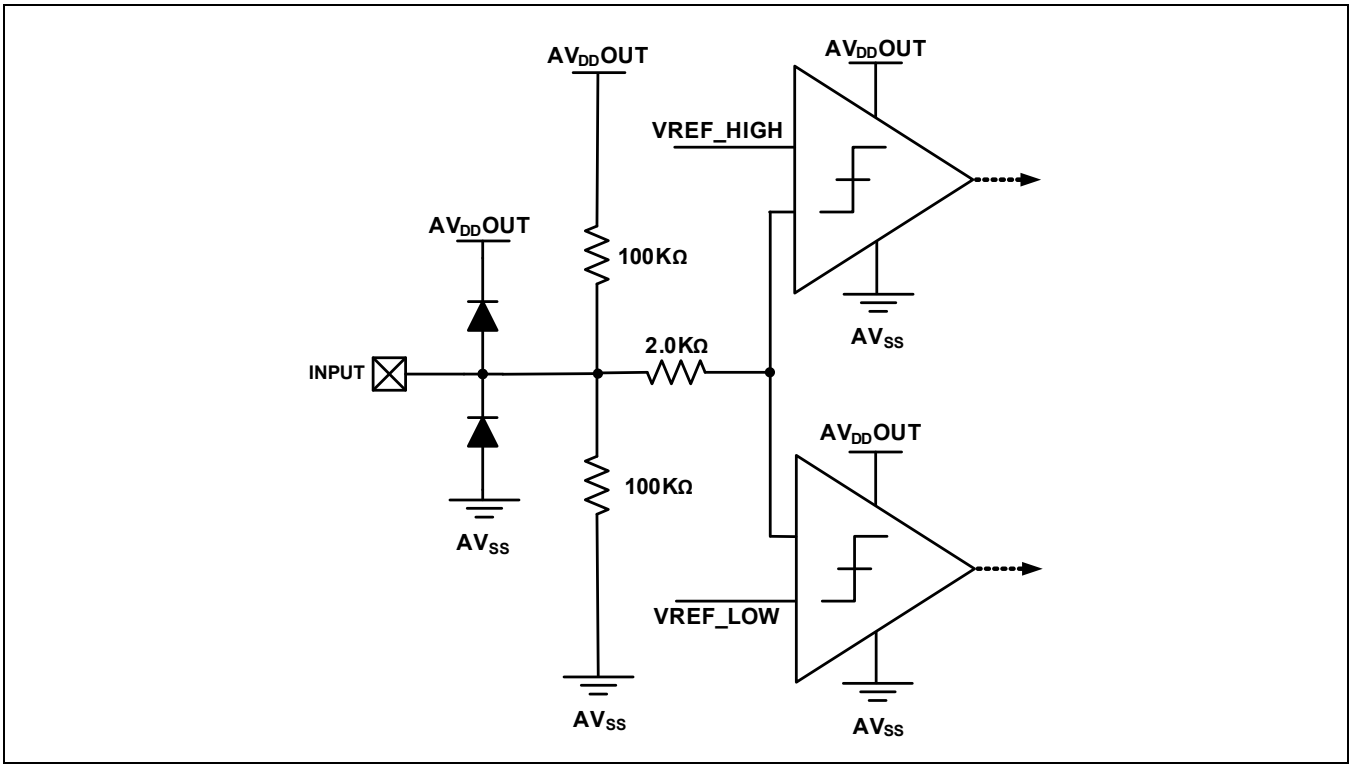
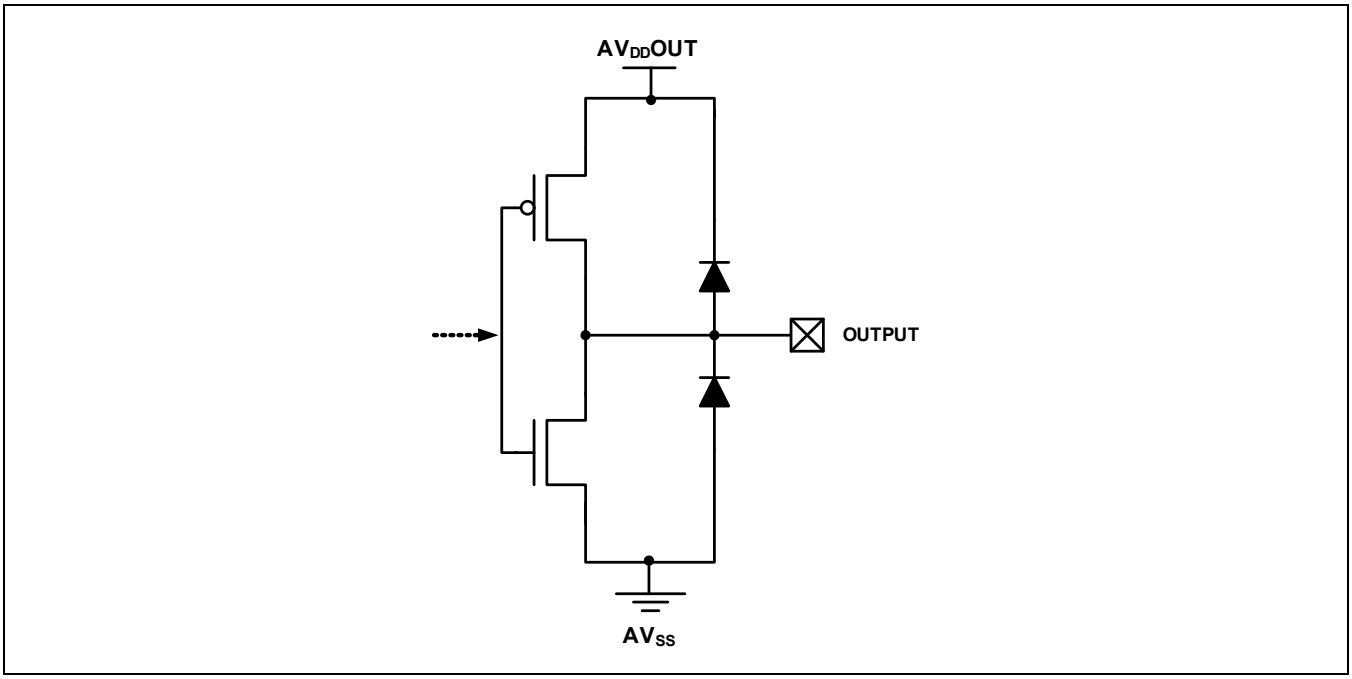


*Figure 3-7. O-Digital*



# 3.1 Package Drawings and Surface Mount Details

The M21004 is assembled in a 24-pin, 4 mm x 4 mm Quad Flat No-Lead (QFN) package. The exposed die paddle serves as the IC ground ($AV_{SS}$), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB ground. A cross-section of the QFN package can be found in Figure 3-8.

***Figure 3-8. QFN Package Cross Section***

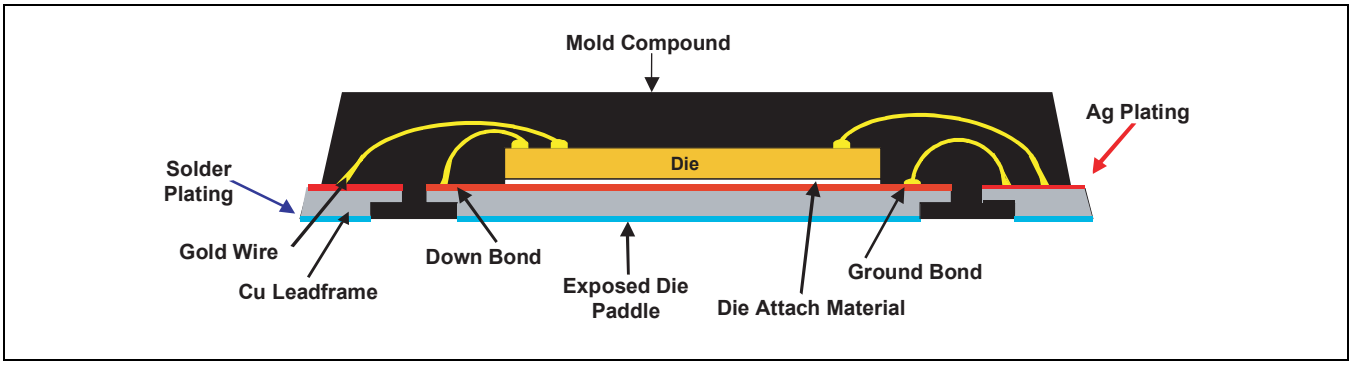
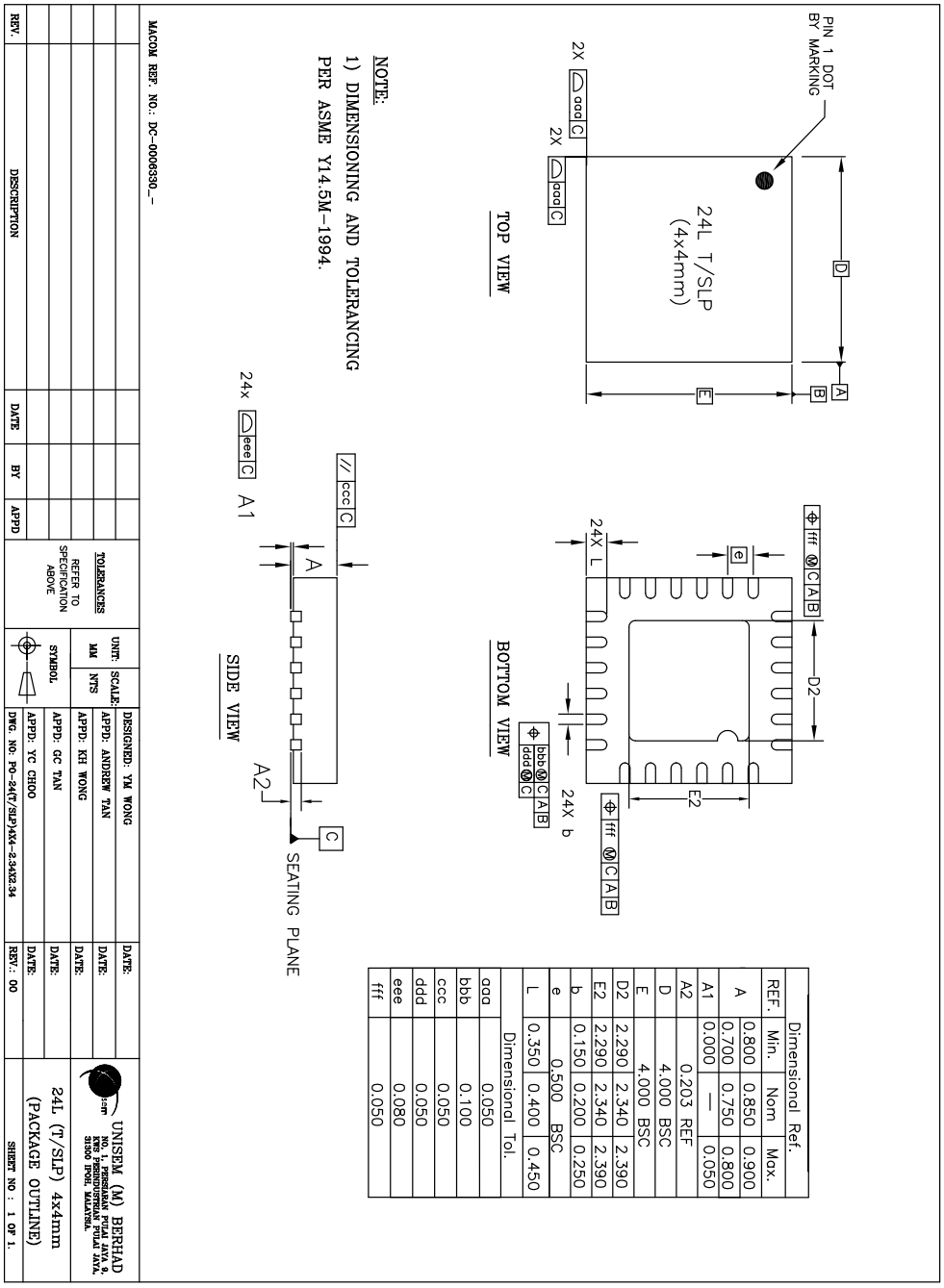


***Figure 3-9. M21004 Package Drawing***




| Dimensional Ref. | | | |
|---|---|---|---|
| REF. | Min. | Nom | Max. |
| A | 0.800 | 0.850 | 0.900 |
| | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | — | 0.050 |
| A2 | | 0.203 REF | |
| D | | 4.000 BSC | |
| E | | 4.000 BSC | |
| D2 | 2.290 | 2.340 | 2.390 |
| E2 | 2.290 | 2.340 | 2.390 |
| b | 0.150 | 0.200 | 0.250 |
| e | | 0.500 BSC | |
| L | 0.350 | 0.400 | 0.450 |

| Dimensional Tol. |
|---|
| aaa 0.050 |
| bbb 0.100 |
| ccc 0.050 |
| ddd 0.050 |
| eee 0.080 |
| fff 0.050 |

1. For dimension reference A, Min. is 0.800, Nom. is 0.850 and Max. is 0.900.
2. New Unisem package and the old Amkor package have the same footprint.

***Figure 3-10. M21004 24-Pin Package Dimensions***

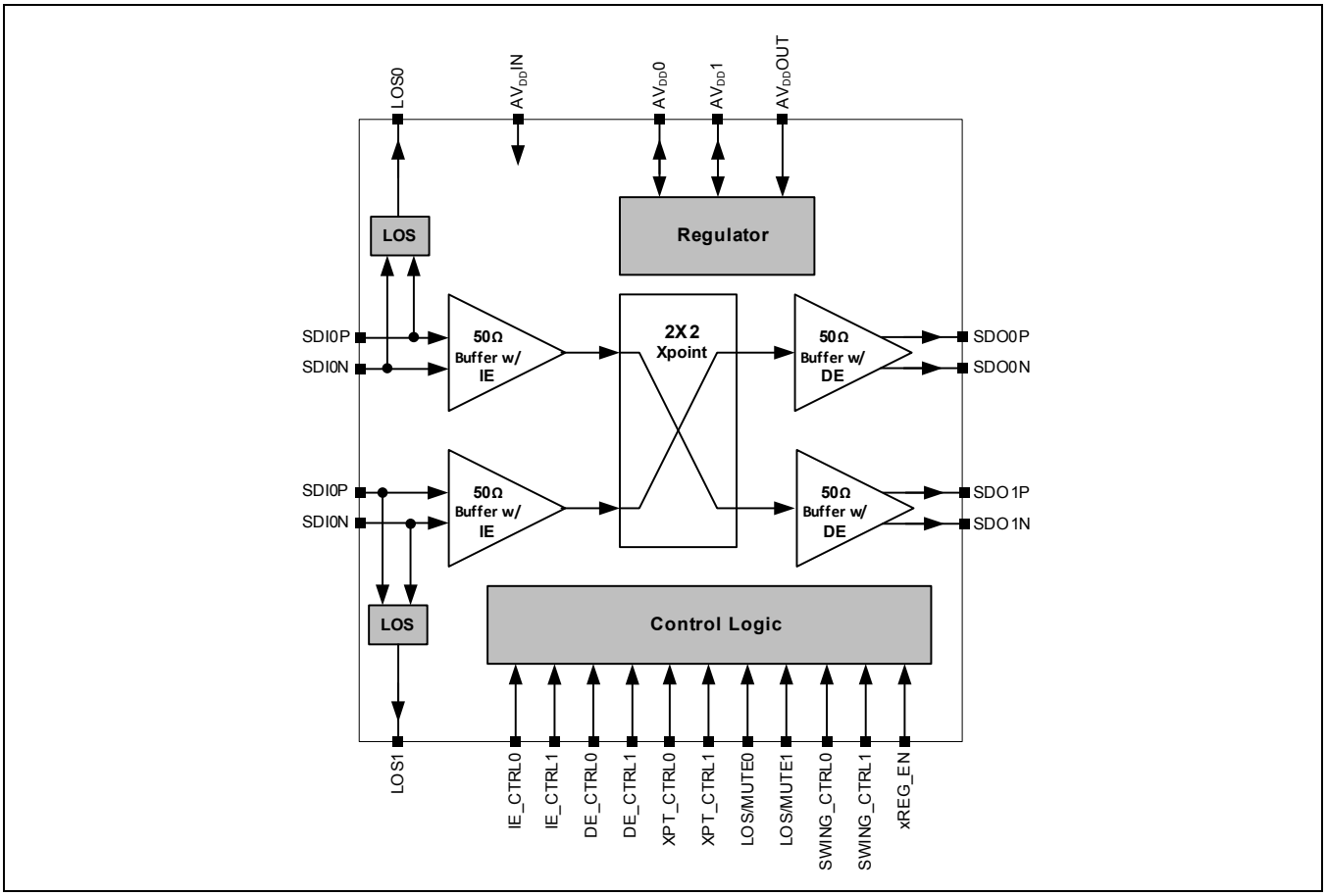
| Dimensional Ref. | | | |
|---|---|---|---|
| REF. | Min. | Nom | Max. |
| A | 0.800 | 0.850 | 0.900 |
| | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | — | 0.050 |
| A2 | 0.203 REF | | |
| D | 4.000 BSC | | |
| E | 4.000 BSC | | |
| D2 | 2.290 | 2.340 | 2.390 |
| E2 | 2.290 | 2.340 | 2.390 |
| b | 0.150 | 0.200 | 0.250 |
| e | 0.500 BSC | | |
| L | 0.350 | 0.400 | 0.450 |
| Dimensional Tol. | | | |
| aaa | 0.050 | | |
| bbb | 0.100 | | |
| ccc | 0.050 | | |
| ddd | 0.050 | | |
| eee | 0.080 | | |
| fff | 0.050 | | |

1. For dimension reference A, Min. is 0.800, Nom. is 0.850 and Max. is 0.900.
2. New Unisem package and the old Amkor package have the same footprint.

# 4.0 Functional Description

Figure 4-1 illustrates the functional block diagram of the M21004. The subsequent sections provide additional detail on the operation of the device.

***Figure 4-1. M21004 Functional Block Diagram***



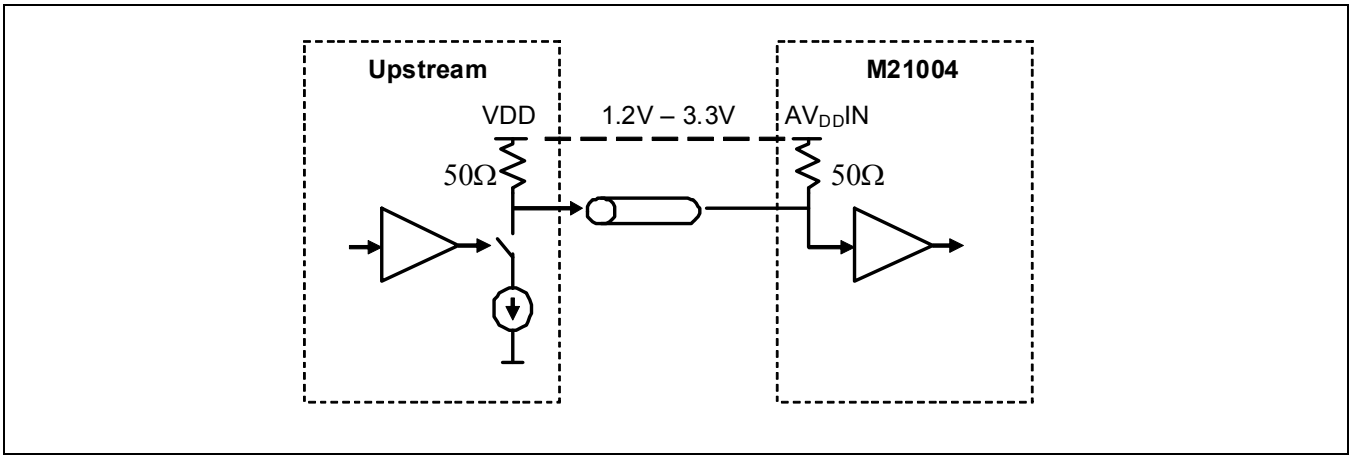
## 4.1 High Speed Input Description

The M21004 features two inputs with a 50Ω termination to $AV_{DD}IN$. $AV_{DD}IN$ can be supplied from any voltage ranging from 1.2V to 3.3V.

In order to improve signal integrity when used in large systems, each input also comes equipped with programmable input equalization (IE) for FR4 trace. There are three settings for input equalization: 6 dB, 4 dB and 0 dB (or no equalization). The IE for each input channel is controlled through the corresponding three state control pin: IE_CTRL0 or IE_CTRL1.

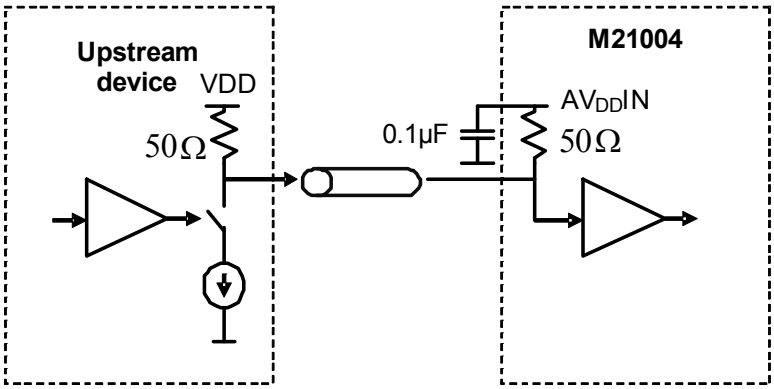
In most SDI applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the upstream device, the $AV_{DD}IN$ power domain of the M21004 is electrically independent from all other power domains allowing it to be tied to the VDD of the upstream device. This is demonstrated in Figure 4-2 below.

***Figure 4-2. M21004 $AV_{DD}IN$ Connected to the VDD of the Upstream Device***




Alternatively and provided that the internal regulators are not used, the M21004 allows for the input to be self biased, eliminating the need for an electrical connection between the supply voltages of the upstream device and M21004. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M21004 completely isolated, while still allowing DC coupling. This self biasing scheme is demonstrated in Figure 4-3 below.

*Figure 4-3. Self Biasing the Input of M21004*




In this configuration, the minimum input common mode that can be tolerated is 600 mV. If AC coupling is desired or necessary, Because of the low frequency content of 3G level B pathological patterns, the coupling capacitor should be at least 10 µF, when used for SDI applications.

## 4.2 Input Circuit Power

Due to the unique architecture of the M21004 front end, its current draw is dependent on the input configuration, as well as swing and common mode voltages.

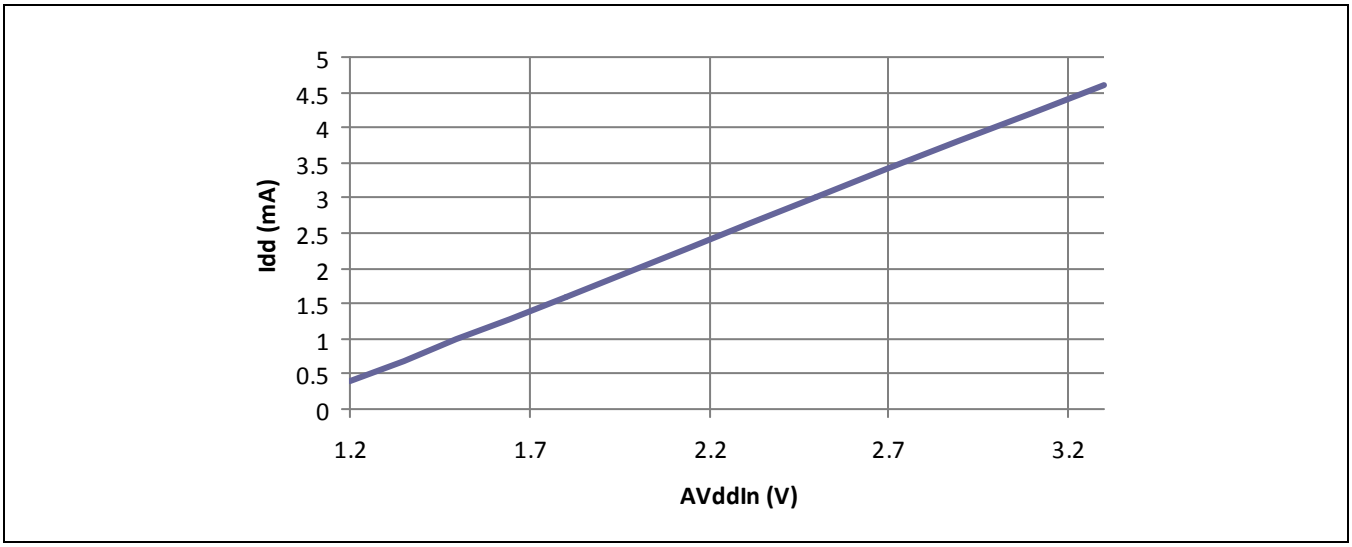
### 4.2.1 AC Coupled Configuration

In this configuration, the current is drawn from $AV_{DD}IN$:

$$I_{DC} = 2(AV_{DD}IN - 1)mA$$

$I_{DC}$ is the current drawn per differential input used, also see graph in Figure 4-4.

***Figure 4-4. Current drawn per differential input, when AC Coupled***




## 4.2.2 DC Coupled Configuration

In this configuration, the current drawn is the sum of the AC Coupled case current drawn plus an additional bias current bias current from the upstream driver. Note that the input common mode voltage $VCM_{IN}$ needs calculating first and this depends on the input signal swing:

$$VCM_{IN} = (AV_{DD}IN + Vswing / 4)V$$

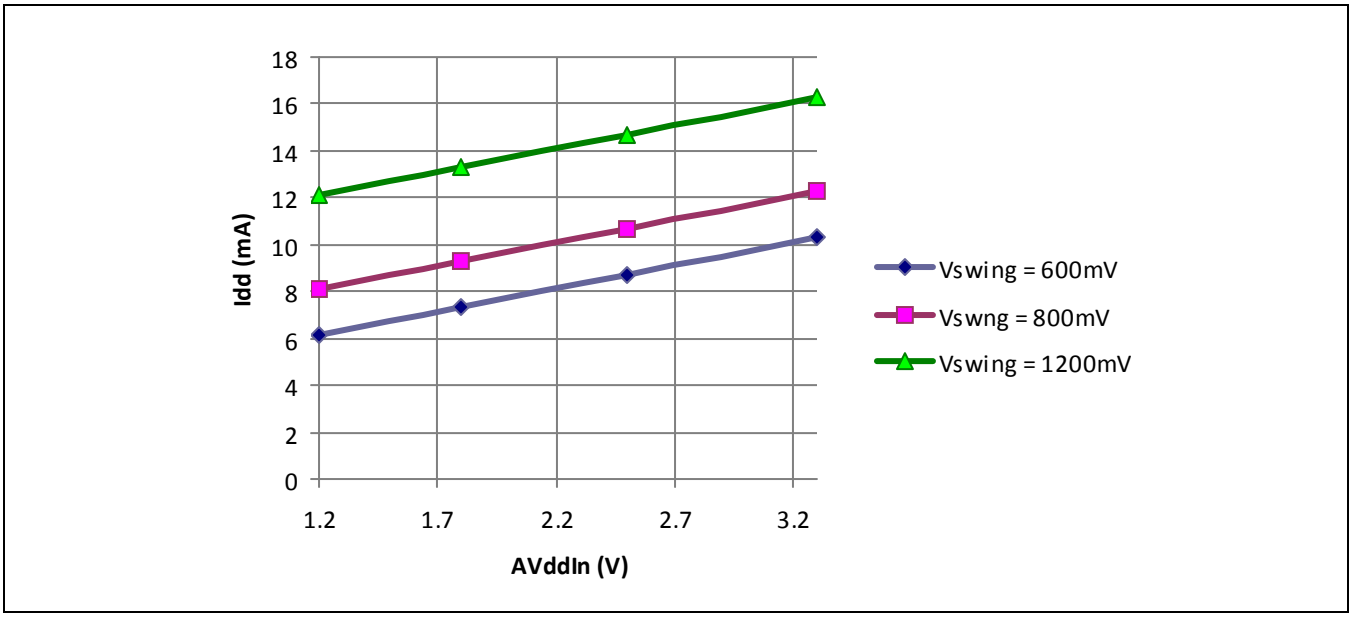
where *Vswing* is the differential input voltage peak to peak

This assumes that the upstream output driver has its 50Ω termination to the same voltage level as $AV_{DD}IN$.

$$I_{DC} = 2(VCM_{IN} - 1) + 10(Vswing)mA$$

$I_{DC}$ is the current drawn per differential input used, also see graph in see Figure 4-5.

*Figure 4-5. Current drawn per differential input, when DC Coupled*




### 4.2.3 Self Biased Configuration

In this configuration the DC current draw is the same as the AC coupled configuration. However, as no voltage is applied to $A_{VDD}$IN, the current is drawn from the VDD of the upstream driver device, see Figure 4-4.

## 4.3 High-Speed Output Description

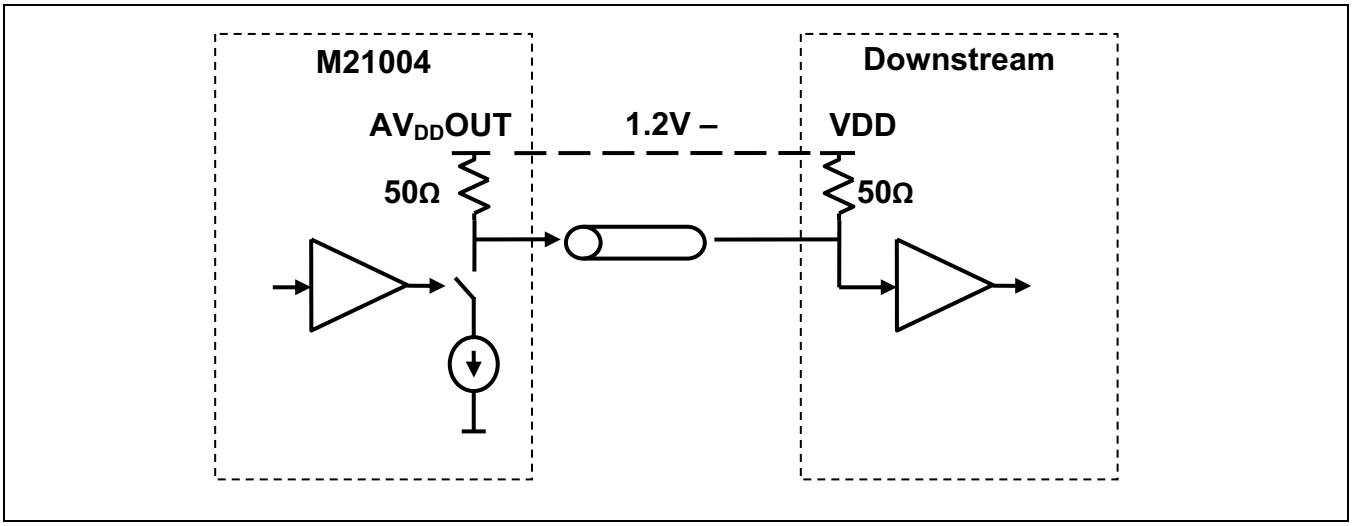
The M21004 features differential positive current mode logic (PCML) drivers with integrated 50Ω pull ups to $AV_{DD}$OUT. $AV_{DD}$OUT may be supplied from any voltage ranging from 1.2V to 3.3V.

The differential, peak-to-peak output swing for each PCML driver is selectable and may be set to low, medium, or high through the SWING_CTRL pin. Please note that the high output swing setting is only available when $AV_{DD}$OUT is supplied from a voltage of 1.8V or greater.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 trace. There are three settings for output de-emphasis: 0 dB (or no DE), 4 dB, and 6 dB. The de-emphasis level for each output is set through the DE_CTRL0 and DE_CTRL1 pins.

In most SDI applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the downstream device, the $AV_{DD}$OUT power domain of the M21004 is electrically independent from all other power domains, therefore allowing it to be tied to the VDD of the downstream device. This is demonstrated in Figure 4-6 below.

*Figure 4-6. M21004 $AV_{DD}OUT$ Connected to the VDD of the Downstream Device*




If AC coupling is desired or necessary, then the capacitor should be at least 10 µF.

## 4.4 Power Supply Description

The device core is designed to operate from a nominal 1.2V supply. However, if a 1.2V supply is not available locally then the internal regulator can be used to create a 1.2V domain from $AV_{DD}OUT$.

Note that as $AV_{DD}IN$ is electrically independent, it must always be supplied with a voltage within the specified range regardless of whether the regulator is enabled or not.

The regulator is controlled through the active low xREG_EN pin. Setting the pin LOW by connecting it to $AV_{SS}$ enables the regulator. The xREG_EN signal is referenced to $AV_{DD}OUT$, so in order to set it HIGH it must be connected to that supply rail. However, the pin features an integrated pull-up resistor, so it may be left floating if the regulator is not used.

When using the internal regulator the total power consumption will increase, the amount of increase depends on supply voltage used. This occurs because the voltage dropped across the regulator (supply voltage - 1.8) is dissipated within the M21004.

Figure 4-7 to Figure 4-10 illustrate the connection for four different supply configurations. Note that the decoupling capacitors must be 0.1 µF or greater.

***Figure 4-7. Supply Configuration Example #1***

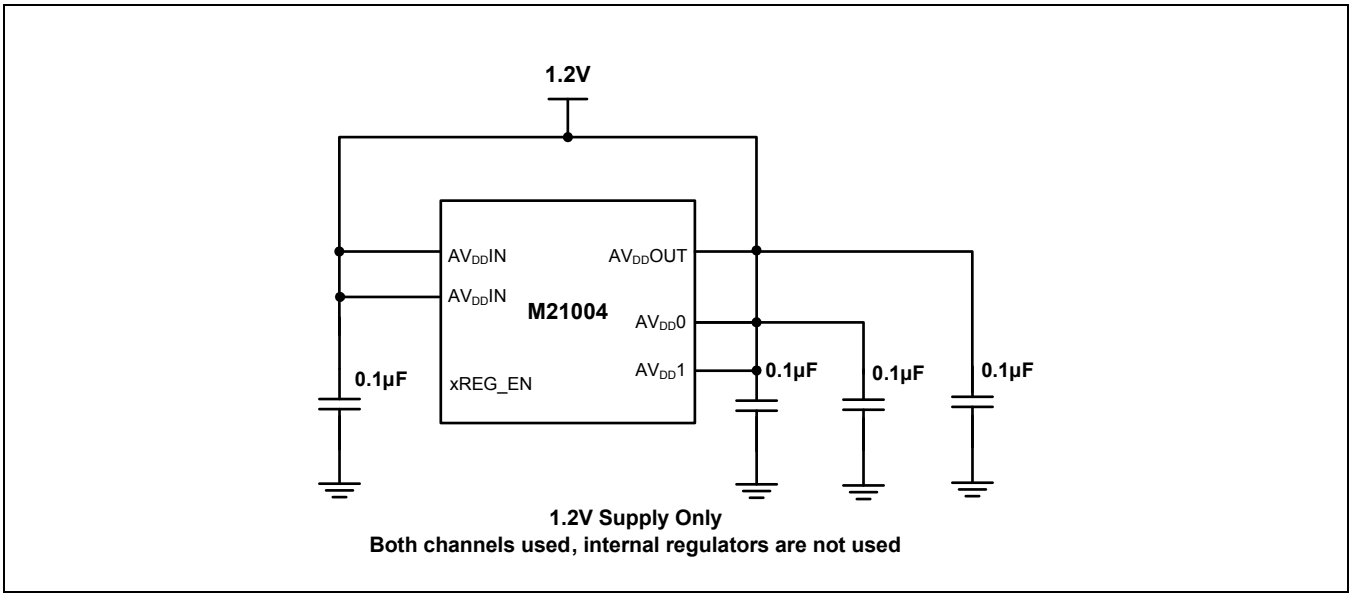
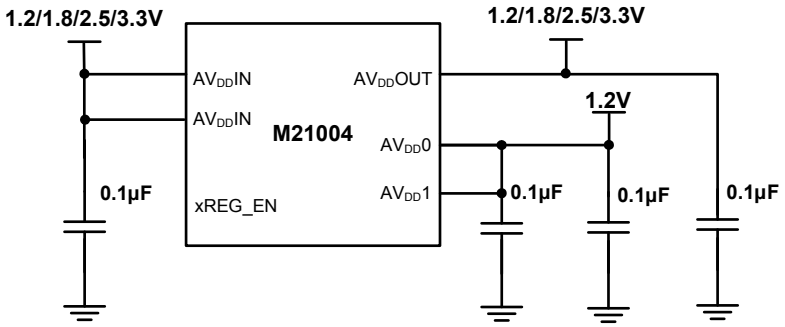
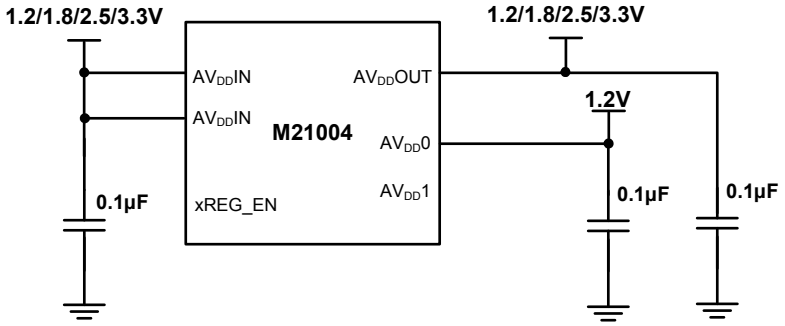


*Figure 4-8. Supply Configuration Example #2*



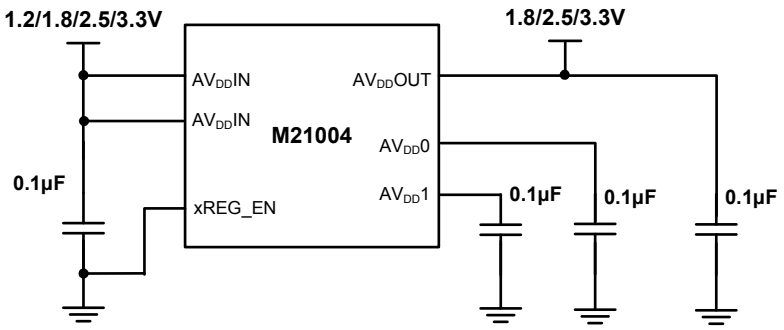

**1.2V used for Core, 1.8V/2.5V/3.3V used for Input and Output**
**Both channels used, internal regulators are not used**

*Figure 4-9. Supply Configuration Example #3*




**1.2V used for Core, 1.8V/2.5V/3.3V used for Input and Output**
**Channel 1 not used, internal regulators are not used**

*Figure 4-10. Supply Configuration Example #4*




**1.8V/2.5V/3.3V used for Core, Input and Output**
**Both channels used, internal regulators are used for Core**

# 4.5 Power Up Sequence

For most applications the supply power up sequence does not matter. However if the supply to $AV_{DD}OUT$ is low impedance when powered down then current can be diverted from the core supply to $AV_{DD}OUT$. To prevent these current surges from $AV_{DD}0,1$ to the output stage, the power up sequence should be as follows:

$AV_{DD}OUT$ first followed by $AV_{DD}IN$ and $AV_{DD}0$, 1.

# 4.6 Logic Control Signals

The M21004 may be configured through several digital control pins. In order to allow interfacing to logic levels other than the 1.2V core voltage, the digital control signals are referenced to $AV_{DD}OUT$.

Some digital control pins have three states: HIGH (H), LOW (L), or FLOATING (F). In order to assert the F state, the pin must be left unconnected or undriven.

## 4.6.1 Input Equalizer Control

The IE_CTRL pins in the M21004 set the equalizer level for the corresponding inputs.

*Table 4-1. Operation of IE_CTRL Pins (Input Equalizer)*

| Pin | Level | Function |
|---|---|---|
| IE_CTRL0, IE_CTRL1 | L | Input equalization disabled |
| | F | Medium equalization (default) |
| | H | High equalization |

### 4.6.2 Output De-emphasis Control

The DE_CTRL pins in the M21004 set the de-emphasis level for the corresponding outputs.

***Table 4-2. Operation of DE_CTRL Pins (De-emphasis)***

| Pin | Level | Function |
|---|---|---|
| DE_CTRL0, DE_CTRL1 | L | De-emphasis disabled |
| | F | Medium de-emphasis (default) |
| | H | High de-emphasis |

### 4.6.3 Output Swing Control

The SWING_CTRL pin in the M21004 sets the PCML swing level for the corresponding output.

***Table 4-3. Operation of SWING_CTRL Pin***

| Pin | Level | Function |
|---|---|---|
| SWING_CTRL0, SWING_CTRL1 | L | Output swing set to low |
| | F | Output swing set to medium (default) |
| | H | Output swing set to high |

### 4.6.4 LOS/Mute Control

The LOS/Mute pins are dual purpose:

*LOS Output*

If left floating the pin is a loss of signal detect output, when the input signal goes below the LOS assert level the output will go high, when the input signal goes above the de-assert level the output will go low. Note that the impedance of the load attached to LOS/MUTE should be > 50 kΩ to either ground or Vdd, this will prevent false activation of Mute Control.

In this state the M21004 automatically squelches the relevant channels data outputs when LOS is asserted.

*Mute Control*

When LOS_MUTE is forced high externally, the squelch circuit is overridden and high speed data output for that channel will be forced to mute.

***Table 4-4. Operation of DE_CTRL pin***

| Pin | Level | Function |
|---|---|---|
| LOS/MUTE0, LOS/MUTE1 | L | Output is never muted |
| | F | LOS output indicator with Squelch enabled |
| | H | Output muted |

### 4.6.5 XPT Control

The XPT_CTRL1:0 pins control the internal 2x2 crosspoint switch, this is situated between the input IE block and the output DE block, see Figure 4-1. All four modes; feed-through, crossover and broadcast from input 0 or input 1 are supported as shown in Table 4-5 below:

***Table 4-5. XPT Control***

| XPT_CTRL1 | XPT_CTRL0 | Connections | Function |
|---|---|---|---|
| LOW (L) | LOW (L) | SDI0 to SDO0, SDI0 to SDO1 | Broadcast 0 |
| LOW (L) | HIGH (H) | SDI1 to SDO0, SDI0 to SDO1 | Crossover |
| HIGH (H) | LOW (L) | SDI0 to SDO0, SDI1 to SDO1 (default) | Feed-through |
| HIGH (H) | HIGH (H) | SDI1 to SDO0, SDI1 to SDO1 | Broadcast 1 |

### 4.6.6 Regulator Enable

Setting the xREG_EN pin low enables the internal regulator, see Section 4.4 for description.

## 4.7 Typical Application Circuit