50 V, 800 mA, 2.2 MHz, Synchronous Buck Regulator with Internal Compensation, Frequency Dithering, Adjustable Current Limit, Synchronization, and Power Good

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Wide operating range: 3.5 to 46 V_{IN}, 50 V_{IN} maximum
- 2.1 MHz PWM switching frequency, avoids AM band
- Selectable outputs: 5.0 V, 3.3 V, 2.5 V
- Minimal external components and extremely small package make the ARG81880 easy to use and save PCB area
- Output voltage accuracy is 53% better than regulators requiring external resistor divider: ±1.8% versus ±3.8%
- Outstanding minimum on-time: typically 20 ns
- PWM frequency dithering and controlled SW node slew rate significantly reduce EMI signature
- Internal loop compensation and internal soft-start lower cost, require less PCB area, and minimize design time
- Compensation automatically adjusts to selected output voltage to maintain high bandwidth and good stability
- Power Good output with rising threshold accuracy (98%) not found in competing regulators
- Selectable current limits allow reduction of output filter component ratings, size, and cost for lower current designs
- Synchronizes to external clock (overrides dithering)
- High-voltage compatible enable input (EN/UV)
- EN/UV input can be used to raise V_{IN} UVLO threshold
- Pin-to-pin and pin-to-ground short circuit tolerant at every pin
- Internal 700 mΩ / 425 mΩ N-channel MOSFETs
- Operating junction temperature range −40°C to 150°C

APPLICATIONS

- Underhood
- Infotainment
- Center Stack
- Clusters
- Telematics
- ADAS, HUD, AVN

DESCRIPTION

The ARG81880 is a fixed-frequency synchronous buck regulator complete with control, diagnostics, and protections that efficiently converts automotive battery voltages into tightly regulated output voltages. The ARG81880 does not require an external resistor divider to select V_{OUT}, which lowers cost, minimizes PCB area, and tightens output voltage tolerance over regulators that must use an external resistor divider to determine V_{OUT}. The ARG81880 is designed to deliver up to 800 mA of output current, given an adequate thermal solution.

Internal loop compensation and soft-start minimize design effort—saving time, cost, and PCB area. An optional synchronization input allows the ARG81880 to increase or decrease its PWM frequency by ±10%. The ARG81880 can be enabled by its high-voltage compatible enable input (EN/UV). Also, the EN/UV input can be used to raise the V_{IN} UV thresholds for higher output voltage systems.

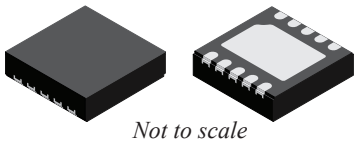
The ARG81880 uses frequency dithering, which has been shown to greatly reduce EMI/EMC. If necessary, frequency dithering may be disabled by applying a synchronization clock at the $I_{LIM}/SYNC_{IN}$ pin. The ARG81880 includes an open-drain Power Good output (PG) with a relatively short fixed delay.

Protection features include V_{IN} undervoltage lockout, V_{OUT} over- and undervoltage protections, PWM pulse-by-pulse current limit, hiccup mode short-circuit protection, SW short-circuit protection, BOOT capacitor protection, and thermal shutdown.

The ARG81880 is supplied in a low-profile 10-lead DFN package (suffix "EJ") with wettable flanks and an exposed power pad.

PACKAGE:

10-Pin, 3 × 3 mm
Wettable Flank DFN
with Exposed Thermal Pad
(Suffix EJ)



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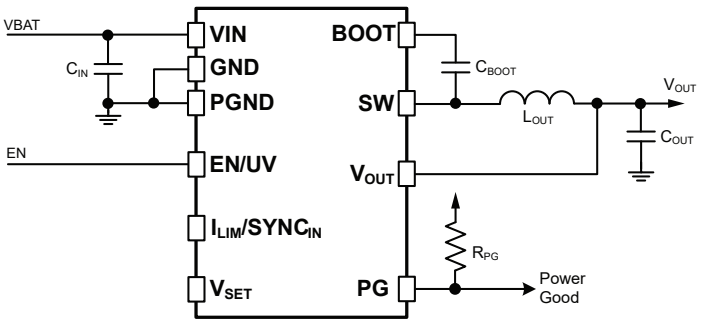

Figure 1: Typical Schematic, 5 V_{OUT}, 800 mA Synchronization not used

SELECTION GUIDE

Part Number	Temperature Range	Package	Packing*	Lead Frame
ARG81880KEJTR	–40°C to 150°C	10-pin DFN w/ thermal pad and wettable flank	1500 pieces per 7-inch reel	100% matte tin

*Contact Allegro for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN/UV	V_{IN}, $V_{EN/UV}$		−0.3 to 50	V
SW	V_{SW}	Continuous	−0.3 to 50	V
		t < 50 ns	54	V
		t < 250 ns	−1.5	V
BOOT	V_{BOOT}		−0.3 to V_{IN} + 8 V	V
VOUT, PG	V_{OUT}, V_{PG}		−0.3 to 26	V
VSET, ILIM/SYNCIN	V_{SET}, $V_{ILIM/SYNCIN}$		−0.3 to 5.5	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−55 to 150	°C

* Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	DFN 10-pin (EJ) package on 4-layer PCB based on JEDEC standard	45	°C/W

* Additional thermal information available on the Allegro website.

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FUNCTIONAL BLOCK DIAGRAM

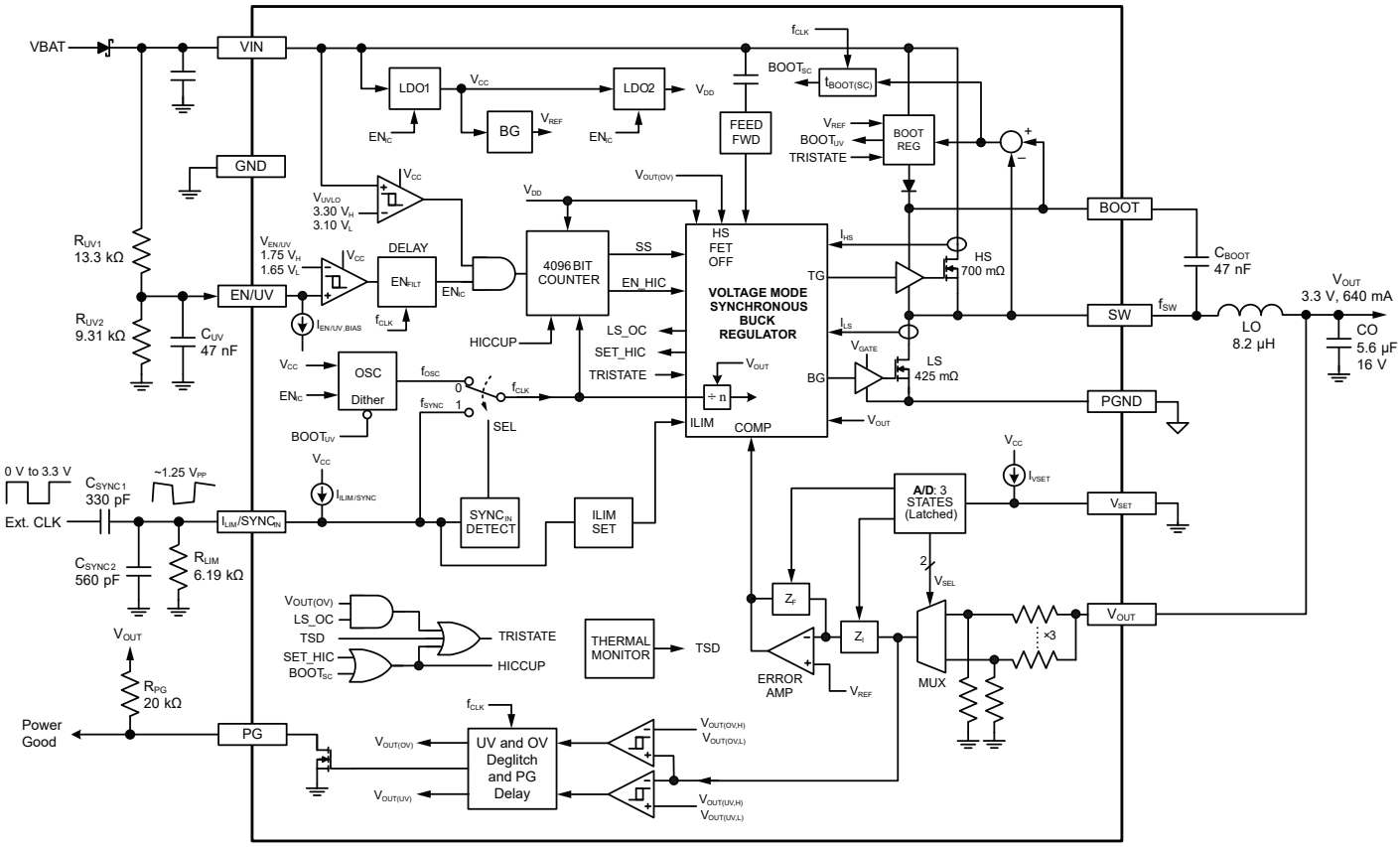

Figure 2: Block Diagram / Typical Schematic

Component values shown are for 12 V_{IN}, 3.3 V_{OUT} at 640 mA.

The V_{IN} Start/Stop thresholds raised to 4.25 V / 4.0 V using a resistor divider at the EN/UV pin

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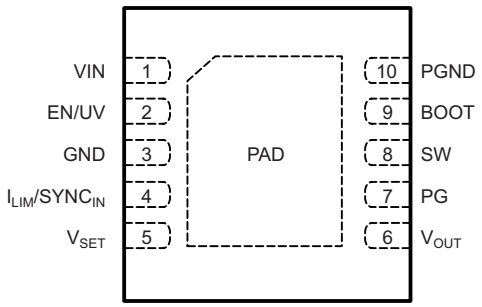
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package EJ, 10-Pin DFN Pinout Drawing

Terminal List

Pin Number	Pin Name	Description
1	VIN	Input voltage to the control circuit and drain of the high-side MOSFET. Connect several high quality ceramic capacitors from this pin directly to PGND. Do not use vias when connecting these capacitors.
2	EN/UV	High-voltage tolerant enable input: HIGH = ON, LOW = OFF. If a resistor divider is placed between this pin and VIN, it will increase the V_{IN} UVLO threshold.
3	GND	Analog ground for the control circuits.
4	I_{LIM}/$SYNC_{IN}$	Dual function pin: current limit selection and (optional) external synchronization input. This pin should be either open circuit or connected to ground through a resistor to set the current limit. An external clock may be AC-coupled to this pin via a capacitor-divider to raise or lower the switching frequency by about ±10%. The capacitor divider should be chosen to produce typically 1.25 V_{PP} at the I_{LIM}/$SYNC_{IN}$ pin. The functionality of this pin is detailed in Table 2.
5	V_{SET}	Output voltage selection pin. The functionality of this pin is detailed in Table 1.
6	V_{OUT}	Output voltage sense and feedback pin to the error amplifier.
7	PG	Open-drain Power Good (PG) output. An external pull-up resistor must be connected to this pin. This signal will be high if V_{OUT} is in regulation. This pin will transition low if V_{OUT} is out of regulation—undervoltage or overvoltage. See Figure 13 for a state diagram showing the operation of the PG pin.
8	SW	Switching node for the synchronous buck regulator. Connect this pin to the output inductor.
9	BOOT	Bootstrap supply input for the high-side gate driver. Connect a high quality 47 nF / 16 V_{MIN} ceramic capacitor from this pin to the SW node.
10	PGND	Source of the low-side MOSFET and ground for its gate driver.
–	PAD	Exposed thermal pad; tie to ground

ELECTRICAL CHARACTERISTICS [1]: Unless otherwise noted, specifications are valid at 3.5 V ≤ V_{IN} ≤ 46 V, −40°C ≤ T_J ≤ 150°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{IN}	After V_{IN} > $V_{INSTART}$, EN/UV = 1	3.5	–	46	V
V_{IN} UVLO Start	$V_{IN(START)}$	V_{IN} rising	3.15	3.30	3.45	V
V_{IN} UVLO Stop	$V_{IN(STOP)}$	V_{IN} falling	2.95	3.10	3.25	V
Supply Quiescent Current [1]	I_Q	EN/UV = 1, No PWM or BOOT switching	–	5.7	–	mA
	$I_{Q(SLEEP)}$	V_{IN} = 12 V, T_J ≤ 85°C [2], EN/UV = 0, V_{SW} = 0 V	–	2.5	5	µA
OUTPUT VOLTAGE						
Output Voltage Accuracy [3]	V_{OUT}	V_{IN} = 12 V	–1.8	±1.3 [2]	+1.8	%
PULSE WIDTH MODULATION (PWM) TIMING						
Buck Minimum On-Time [2]	$t_{ON(MIN)}$	V_{IN} = 12 V, Measure pulse width from 10% of rising edge to 90% of falling edge	–	20	40	ns
Buck Minimum Off-Time	$t_{OFF(MIN)}$		–	65	100	ns
PWM FREQUENCY AND DITHERING						
Oscillator Frequency (no $SYNC_{IN}$)	f_{OSC}	RSET = GND, OPEN, 15.4 kΩ	1.98	2.20	2.44	MHz
Frequency Dithering Range	Δf_{OSC}	No $SYNC_{IN}$	–	±9	–	% of f_{OSC}
Dithering Modulation Frequency	f_{MOD}	No $SYNC_{IN}$	–	11	–	kHz
Minimum PWM Frequency	$f_{PWM(MIN)}$	$f_{OSC(MIN)} - \Delta f_{OSC(MAX)}$	1.81	–	–	MHz
Operational Frequency Foldback	$f_{SW(FB)}$	f_{OSC} = 2.1 MHz and V_{OUT} < 1.1 V	–	f_{CLK} / 4	–	—
MOSFET CHARACTERISTICS						
High-Side MOSFET On-Resistance	$R_{ds(ON,HS)}$	T_J = 25°C [2], $V_{BOOT} - V_{SW}$ = 4.5 V, I_{DS} =400 mA	–	700	–	mΩ
		T_J = 150°C, $V_{BOOT} - V_{SW}$ = 4.5 V, I_{DS} = 400 mA	–	–	1790	mΩ
Low-Side MOSFET On-Resistance	$R_{ds(ON,LS)}$	T_J = 25°C [2], V_{IN} > 6 V, I_{DS} = 400 mA	–	425	–	mΩ
		T_J = 150°C, V_{IN} > 6 V, I_{DS} = 400 mA	–	–	875	mΩ
MOSFET Non-Overlap Time [2]	t_{NO}		–	8	–	ns
SW Node Rising Slew Rate [2]	SR_{SW}	12 V < V_{IN} < 16 V	–	4.0	–	V/ns
PWM PULSE-BY-PULSE CURRENT LIMITS						
High-Side MOSFET Current Limit	$I_{LIM(HS)}$	R_{LIM} = OPEN	1275	1500	1725	mA
		R_{LIM} = 6.19 kΩ	1010	1190	1370	mA
		R_{LIM} = 17.8 kΩ	770	910	1050	mA
SW Short Circuit Current Limit (hiccup mode after 2 consecutive detections)	$I_{LIM(SC)}$	R_{LIM} = OPEN	–	3.8	–	A
		R_{LIM} = 6.19 kΩ	–	3.4	–	A
		R_{LIM} = 17.8 kΩ	–	2.8	–	A
Low-Side MOSFET Current Limit	$I_{LIM(LS)}$		0.5	0.7	0.9	A

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ELECTRICAL CHARACTERISTICS [1] (continued): Unless otherwise noted, specifications are valid at 3.5 V ≤ V_{IN} ≤ 46 V, −40°C ≤ T_J ≤ 150°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
HICCUP MODE PROTECTION						
V_{OUT} Hiccup Enable Delay	$t_{HIC(EN)}$		–	512	–	f_{CLK} cycles
Hiccup Recovery Time	$t_{HIC(REC)}$	HICCUP = 1	–	4096	–	f_{CLK} cycles
PWM Overcurrent Counts	$t_{PWM(OC)}$	V_{OUT} < 25%	–	30	–	OC Counts @ f_{SW}
		V_{OUT} > 25%	–	120	–	OC Counts @ f_{SW}
V_{BOOT} Short Circuit Counts	$t_{BOOT(SC)}$		–	64	–	f_{CLK} cycles
SOFT-START TIME AND FREQUENCY						
Soft-Start Ramp Time	t_{SS}		–	4096	–	f_{CLK} cycles
Soft-Start Frequency Foldback	$f_{SW(SS)}$	T_J = 150°C, V_{OUT} = 0 V	–	f_{CLK} / 8	–	–
		T_J = 150°C, V_{OUT} = 11%	–	f_{CLK} / 4	–	–
		T_J = 150°C, V_{OUT} = 20%	–	f_{CLK} / 2	–	–
		T_J = 150°C, V_{OUT} = 35%	–	f_{CLK}	–	–
ENABLE/UNDER-VOLTAGE INPUT (EN/UV) AND DEGLITCH						
EN/UV Thresholds	$V_{EN/UV(H)}$	$V_{EN/UV}$ rising	1.58	1.75	1.92	V
	$V_{EN/UV(L)}$	$V_{EN/UV}$ falling	1.49	1.65	1.81	V
EN/UV Hysteresis	$V_{EN/UV(HYS)}$	$V_{EN/UV(H)} - V_{EN/UV(L)}$	–	100	–	mV
EN/UV Bias Current [1]	$I_{EN/UV(BIAS)}$	$V_{EN/UV}$ = 1.4 V	–	4.5	–	µA
		$V_{EN/UV}$ ≥ 12 V	–	10	–	µA
ENABLE FILTER/DEGLITCH TIME						
Enable Filter/Deglitch Time	EN_{FILT}		–	32	–	f_{CLK} cycles
V_{SET} AND I_{LIM}/$SYNC_{IN}$ PINS						
V_{SET} Bias Current [1]	I_{VSET}	V_{SET} = 2 V	–94	–104	–114	µA
I_{LIM}/$SYNC_{IN}$ Bias Current [1]	$I_{ILIM/SYNC}$	V_{ILIM}/V_{SYNCIN} = 2 V	–92	–104	–116	µA
SYNCHRONIZATION INPUT						
Synchronization Frequency Range	f_{SYNC}		1.89	–	2.4	MHz
Synchronization Voltage Sensitivity	ΔV_{SYNC}	V_{SYNC} = 3.0 V_{DC}	1.0	1.25	1.5	V_{PP}
Synchronization Transition Time [2]	t_{SYNC}		–	20	100	µs
Synchronization CLK Duty Cycle	D_{SYNC}		40	50	60	%
Synchronization CLK Rise and Fall Time [2]	$t_{R/F(SYNC)}$		–	–	15	ns

Continued on next page...

ELECTRICAL CHARACTERISTICS [1] (continued): Unless otherwise noted, specifications are valid at 3.5 V ≤ V_{IN} ≤ 46 V, −40°C ≤ T_J ≤ 150°C

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER GOOD (PG) RISING DELAY, FILTER/DEGLITCH TIMES, AND UV/OV THRESHOLDS						
PG Rising Delay	t_{dPG}	V_{OUT} rising	–	256	–	f_{CLK} cycles
UV Filter/Deglitch Times	t_{dUV}	V_{OUT} rising or falling	–	64	–	f_{CLK} cycles
V_{OUT} UV Thresholds	$V_{OUT(UV,H)}$	V_{OUT} rising	–	98	–	%
	$V_{OUT(UV,L)}$	V_{OUT} falling	94	95	96	%
V_{OUT} UV Hysteresis	$V_{OUT(UV,HYS)}$	$V_{OUT(UV,H)} – V_{OUT(UV,L)}$	–	3	–	%
OV Filter/Deglitch Times	t_{dOV}	V_{OUT} rising only	–	128	–	f_{CLK} cycles
V_{OUT} OV Thresholds	$V_{OUT(OV,H)}$	V_{OUT} rising	106	107	108	%
	$V_{OUT(OV,L)}$	V_{OUT} falling	–	104	–	%
V_{OUT} OV Hysteresis	$V_{OUT(OV,HYS)}$	$V_{OUT(OV,H)} – V_{OUT(OV,L)}$	–	3	–	%
POWER GOOD (PG) INITIALIZATION AND OUTPUT VOLTAGES						
PG Initialization at Low V_{IN}	$V_{PG(INIT)}$	V_{IN} = 1.5 V, I_{PG} = 330 µA, EN/UV = 0	–	–	400	mV
PG Low Output Voltage	$V_{PG(LOW)}$	EN/UV = 1, V_{IN} ≥ 2.5 V, I_{PG} = 4 mA	–	150	400	mV
PG Leakage Current	$I_{PG,LKG}$	V_{PG} = 5 V, T_J ≤ 85°C [2]	–	–	1	µA
		V_{PG} = 5 V	–	–	6	µA
THERMAL SHUTDOWN PROTECTION (TSD)						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	160	175	190	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Typical specification applies from 0°C < T_J < 85°C. Min/max specifications apply from –40°C < T_J < 150°C.

FUNCTIONAL DESCRIPTION

Overview

The ARG81880 is a wide input voltage range, high performance synchronous buck regulator designed specifically for demanding automotive and industrial applications. The device requires minimal external components, and combined with its very small footprint, is easy to use, reduces system cost, and saves PCB area.

The ARG81880 provides excellent output voltage accuracy (±1.8%) compared to regulators needing an external resistor divider (±3.8%). The device uses a proprietary voltage mode control algorithm to deliver exceptional minimum on-times, as low as 20 ns, and is capable of jitter-free operation. It employs PWM frequency dithering to reduce its EMI/EMC signature as much as 16 dB, and provides an adjustable current limit, so the rating and size of the output filter components (L and C) can be optimized to each application, saving cost and PCB area. The ARG81880 has internal compensation that automatically adjusts for each output voltage to maintain high bandwidth and good stability. It provides a Power Good output with a typical rising threshold of 98%, an accuracy not found in competing regulators.

The ARG81880 operates at a fixed frequency of 2.1 MHz, above the AM band, and delivers 5.0 V, 3.3 V, or 2.5 V from input voltages as high as 46 V. The ARG81880 can accept an external clock, so multiple regulators can be synchronized in-phase (same clock) or 180° out-of-phase (clock and inverted clock) to reduce input capacitor requirements. The ARG81880 has a high-voltage tolerant enable input and an internally fixed soft-start time.

Protection features of the ARG81880 include V_{IN} undervoltage lockout, cycle-by-cycle current limit, hiccup mode short-circuit protection, overvoltage protection, and thermal shutdown.

Output Voltage Accuracy and Selection

The ARG81880 provides a DC output voltage accuracy of ±1.3% when its junction temperature is 0°C < T_J < 85°C, and ±1.8% when –40°C < T_J < 150°C. It also monitors V_{OUT} directly so its accuracy is not compromised by an external resistor divider between V_{OUT} and a feedback pin. Traditional regulators using a ±1% reference and an external resistor divider created with two ±1%, 50 ppm resistors can only offer output voltage accuracies of ±3.8%.

The ARG81880 offers three output voltages: 5.0 V, 3.3 V, and 2.5 V. The output voltage is selected by setting the state of the V_{SET} pin according to the following table. The V_{SET} pin is sampled at power-up and the output voltage is internally latched at that time. This means the output voltage cannot change during operation. This prevents noise or transients from erroneously altering the output voltage.

Table 1: Output Voltage Selections

V_{OUT} (V)	V_{SET} Pin State
5.0	OPEN
3.3	GND
2.5	15.4 kΩ ± 1%

Adjustable Current Limit

The ARG81880 supports three possible load currents: 800 mA, 640 mA, or 480 mA. The load current is selected by setting the state of the $I_{LIM}/SYNC_{IN}$ pin according to the following table. The pulse-by-pulse current limit scales with the load current selected. Providing multiple current settings allows the designer to reduce the saturation current, physical size, and cost of the output inductor for lower current applications.

Table 2: Current Selection

I_{OUT} (mA)	High-Side Current Limit, $I_{LIM(HS)}$ (mA)	$I_{LIM}/SYNC_{IN}$ State or R_{LIM} Value
800	1500	OPEN
640	1190	GND if $SYNC_{IN}$ is not used; otherwise 6.19 kΩ, ±1% or 6.2 kΩ, ±5%
480	910	17.8 kΩ, ±1% or 18 kΩ, ±5%

Note, for the 640 mA design, if synchronization is not needed, the R_{LIM} resistor can be omitted and the $I_{LIM}/SYNC_{IN}$ pin can be connected directly to ground. This reduces the component count by one resistor which saves cost and PCB area.

PWM Control and Internal Loop Compensation

The ARG81880 uses a proprietary voltage mode control algorithm. This control scheme provides excellent noise immunity, incredibly low minimum on-times, and is capable of delivering pulse-widths that are virtually jitter free. Also, the ARG81880 incorporates V_{IN} feed-forward compensation to supplement the control loop during fast line transients. Figure 2 shows repeatable, closed-loop control producing on-times of only 25 ns—not just a single short pulse during startup or while pulse skipping. Figure 3 shows pulse-width jitter of less than 1 ns while using $SYNC_{IN}$.

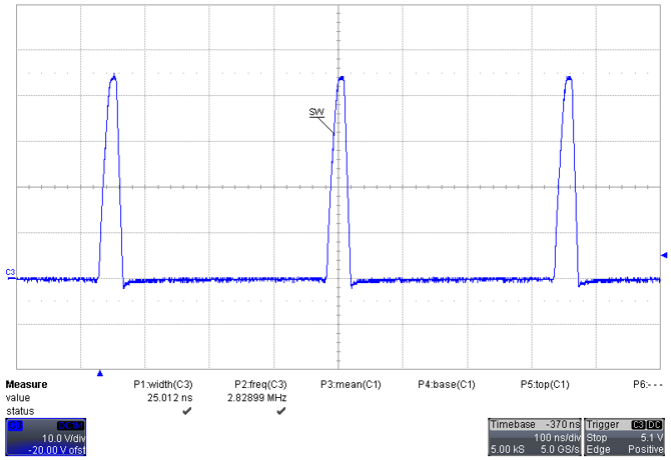


Figure 3: Repeatable, Controlled On-Times of only 25 ns. 46 V_{IN}, 2.5 V_{OUT}, 2.8 MHz at 400 mA load.

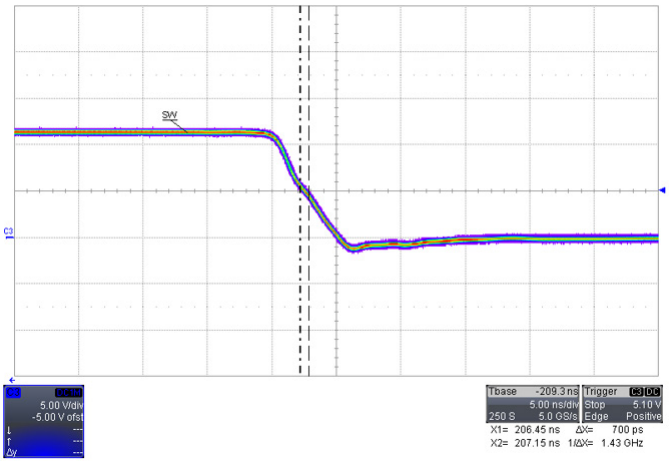


Figure 4: Less than 1 ns of Pulse Width Jitter, (5 ns/DIV). Trace captured with infinite oscilloscope persistence. 12 V_{IN}, 5 V_{OUT} at 800 mA.

The ARG81880 employs internal compensation. This makes it very easy to use, reduces PCB area, and lowers cost. However, unlike other internally compensated regulators, the ARG81880 stores specific compensation values for each of its output voltage settings. When the output voltage is selected, the ARG81880 compensates itself to maintain high bandwidth, fast transient response, and good gain and phase margins.

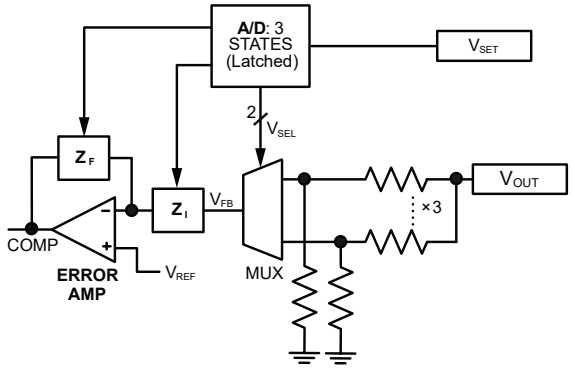


Figure 5: The Error Amplifier Compensation (Z_F, Z_I) is modified when the output voltage is programmed.

PWM Frequency and Dithering

The ARG81880 includes two state-of-the-art techniques to help reduce EMI/EMC for demanding automotive applications.

First, the ARG81880 performs dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the nominal frequency. A typical fixed-frequency PWM regulator will create distinct “spikes” of energy at the switching frequency, and at multiples of the switching frequency. Conversely, the ARG81880 spreads the spectrum around the switching frequency, thus creating a lower magnitude at any comparative frequency. Frequency dithering is disabled if an external clock is applied to $SYNC_{IN}$.

Second, the ARG81880 controls the rising slew rate of the SW node to approximately 4 V/ns. A controlled SW rise time reduces high frequency ringing and harmonics of the regulator.

The dithering sweep is internally set at Δf_{OSC} (±9%). This means the PWM switching frequency will ramp from 0.91 to 1.09 times the base frequency (f_{OSC}). However, the lowest PWM frequency, $f_{OSC} - \Delta f_{OSC}$, is guaranteed not to fall below $f_{PWM(MIN)}$ (1.81 MHz), thus keeping harmonics out of the AM band. The rate or modulation frequency sweeps a triangular pattern operating at f_{MOD} (11 kHz).

The following two figures compare the conducted and radiated emissions of the ARG81880 with dithering disabled (a trim option) to the ARG81880 employing PWM dithering. The external components, operating conditions, and PCB layouts of the two setups were identical. From these plots, it is clear that PWM dithering significantly reduces the peak levels of energy produced by a traditional, non-dithering regulator.

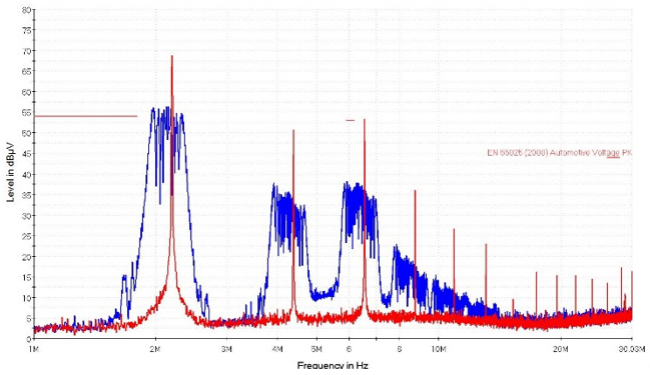


Figure 6: Comparison with Dithering (blue) and Non-Dithering (red) Conducted Emissions (Peak) in dBµV.

Table 3: Sample Values from Conducted Emissions Testing

Freq.	Typical PWM	ARG81880	Improvement
2.1 MHz	69	56	–13 dB
4.2 MHz	51	35	–16 dB
10.5 MHz	26	12	–14 dB

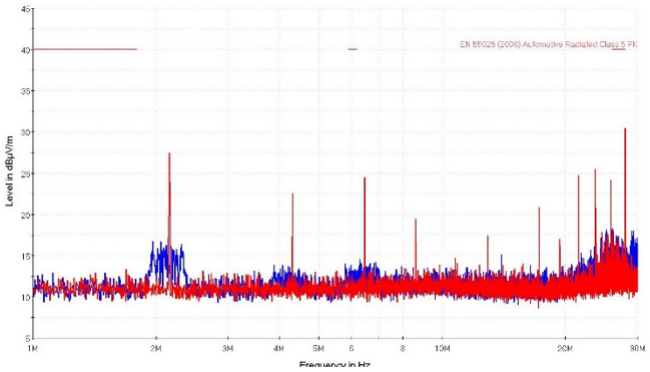


Figure 7: Comparison with Dithering (blue) and Non-Dithering (red) Radiated Emissions (Peak) in dBµV/m.

Table 4: Sample Values from Radiated Emissions Testing

Freq.	Typical PWM	ARG81880	Improvement
2.1 MHz	28	16	–12 dB
4.2 MHz	23	14	–11 dB
21 MHz	25	15	–10 dB

Frequency dithering has obvious benefits, but combined with the control algorithm can produce nontraditional output voltage ripple that increases slightly at higher V_{IN}. The peak-to-peak ripple is relatively low, but may have a random appearance as shown in the following figure. The output voltage ripple can increase further if the junction temperature exceeds the absolute maximum rating of 150°C, just prior to TSD.

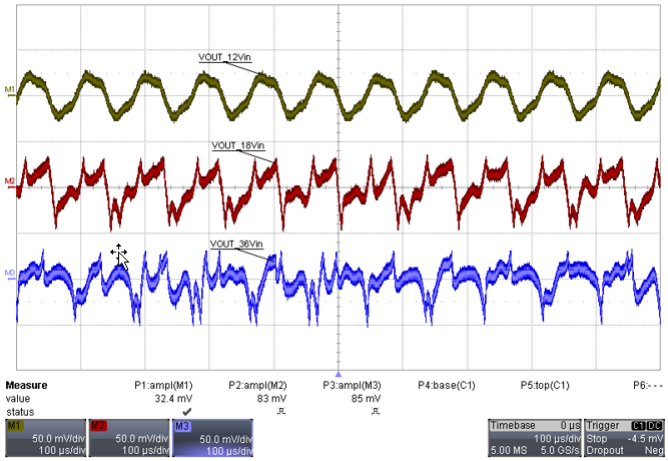


Figure 8: Output Voltage Ripple at 12 V, 18 V, and 36 V Input. 5 V Output, 800 mA Loading (50 mV/DIV, 100 µs/DIV).

Internal Clock and Soft-Starting

The clock frequency, f_{CLK}, is derived from either the internal 2.1 MHz oscillator (f_{OSC}) or the external clock frequency (f_{SYNC}), if one is applied to the $I_{LIM}/SYNC_{IN}$ pin. Timing functions within the ARG81880 (soft-start, deglitch, delays, etc.) are relative to f_{CLK}.

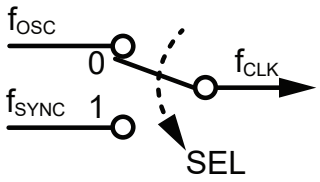


Figure 9: The main clock frequency, f_{CLK}, is derived from either the internal oscillator (f_{OSC}) or external clock (f_{SYNC}).

Soft-start of the ARG81880 is internally fixed at 4096 clock cycles (f_{CLK}). Based on f_{OSC} (2.1 MHz), the typical soft-start time is about 1.95 ms. If no faults exist and EN/UV transitions high, the ARG81880 will begin its soft-start routine.

At the beginning of soft-start, the PWM switching frequency (f_{SW}) is temporarily folded back to $f_{CLK}/8$ while V_{OUT} is very low. Folding back the frequency extends the PWM off-time which allows the inductor current to decay much further than it would otherwise. Thus, longer off-times significantly limit the peak current in the inductor when the regulator output is shorted to ground. Also, folding back the PWM frequency results in a longer time period which enables the control loop to achieve

much lower duty cycles and better regulation.

As V_{OUT} rises, the switching frequency (f_{SW}) increases to $f_{CLK}/4$, $f_{CLK}/2$, and finally f_{CLK} at about 35% of the steady-state output.

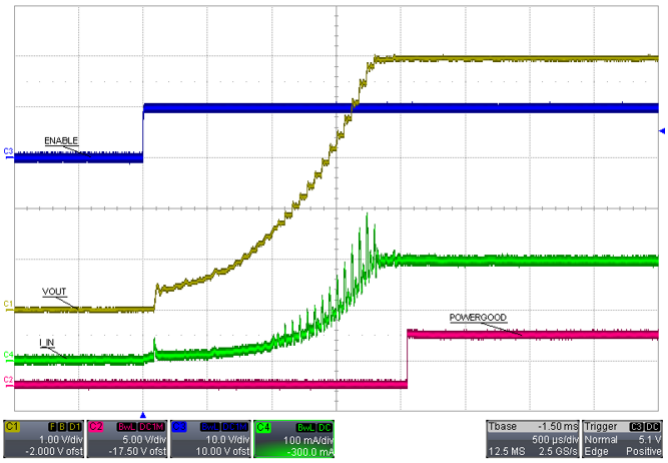


Figure 10: Typical Soft-Start Triggered by the Enable Input. Power Good transitions high only after V_{OUT} achieves 100%.

Current Limit and Synchronization Input

The $I_{LIM}/SYNC_{IN}$ input provides two functions. First, if this pin is open or has a resistor connected to ground, the current limit can be set to one of the three values shown in Table 2. Second, an external clock can be applied to this pin to synchronize two or more regulators either in phase (same clock) or 180° out of phase (clock and inverted clock). The ARG81880 can be synchronized from 1.89 to 2.4 MHz.

The external clock must be AC-coupled to this pin via a capacitor divider, as shown below. The capacitor values must be chosen to produce at least 1.0 V_{PP} but not more than 1.5 V_{PP} at the $SYNC_{IN}$ pin, given the lowest and highest peak-to-peak voltages of the external clock.

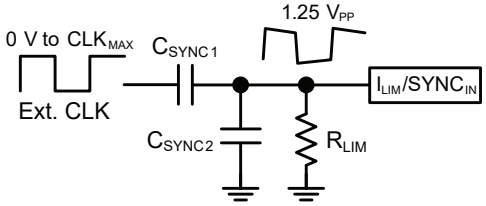


Figure 11: AC-Coupling of an External Clock to $SYNC_{IN}$

The synchronization capacitors should be relatively low value ceramic capacitors (100 to 1000 pF) with tight initial tolerances (±5% initial tolerance) and good stability across temperature (COG/NPO type, 30 ppm). The ratio of the synchronization capacitors can be calculated using the following formula.

Equation 1:

$$\frac{C_{SYNC1}}{C_{SYNC2}} = \frac{1.25\ \text{V}}{CLK_{MAX} - 1.25\ \text{V}}$$

Table 5: Recommended Synchronization Capacitor Values

External Clock	CSYNC1	CSYNC2
0 to 3.3 V	330 pF	560 pF
0 to 5.0 V	180 pF	560 pF

Enable/Undervoltage Function

The enable/undervoltage input (EN/UV) allows the system to selectively enable and disable the ARG81880. Also, the EN/UV pin is rated to 50 V, so the ARG81880 can be automatically controlled from an analog voltage, for example, directly from V_{IN} or from another regulators output. In addition, the enable input can be used as a programmable UVLO. Connecting a resistor divider from VIN to enable implements this feature as shown in the following figure.

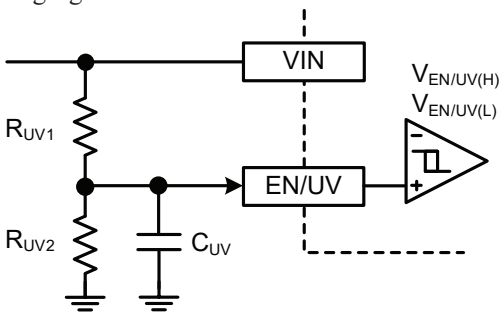


Figure 12: Using EN/UV as a Programmable UVLO. C_{UV} filters transients on VIN and is strongly recommended.

The programmed UVLO thresholds can be calculated using the following formulas.

Equation 2:

$$V_{IN(START)} = \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \times V_{EN/UV(H)}$$

Equation 3:

$$V_{IN(STOP)} = \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \times V_{EN/UV(L)}$$

If the EN/UV pin is floating, an internal current sink will pull the voltage down and disable the regulator. When the ARG81880 is disabled, it will draw less than 5 µA from the input provided $T_J \leq 85°C$. When EN transitions low, the device waits 32 f_{CLK} cycles (EN_{FILT}) before shutting down. The shutdown delay prevents the device from prematurely entering Sleep mode due to noisy events like line or load transients.

Power Good Function

The ARG81880 has a Power Good (PG) output with a fixed delay of 256 f_{CLK} cycles (t_{dPG}) on its rising edge. This relatively short delay on the rising edge (122 µs at 2.1 MHz) allows the ARG81880 to complete soft-start, so V_{OUT} can achieve 100% regulation before PG transitions high. The benefit of the rising edge delay on PG is shown in Figure 10. The PG output is an open-drain output, so an external pull-up resistor must be used, as shown in the applications schematic. If Power Good is not used, the PG pin can be left floating or grounded.

Basically, Power Good is high if V_{OUT} is within regulation and low if V_{OUT} is out of regulation. The control algorithm in the ARG81880 allows the Power Good function to have a much tighter window of detection than competing regulators: 98% to 107% of the desired value. The Power Good function incorporates hysteresis ($V_{OUT(UV,HYS)}$), $V_{OUT(OV,HYS)}$) to prevent chattering and deglitch filtering (t_{dUV}, t_{dOV}) to eliminate false triggering. The following flow chart shows the operation of Power Good.

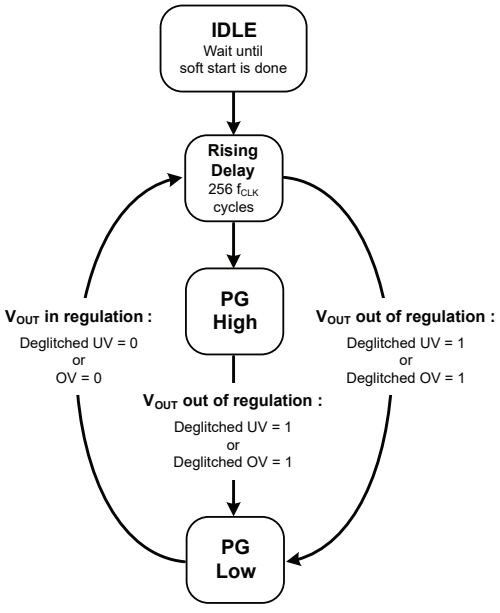


Figure 13: Power Good Operation

At power-up, Power Good must be initialized (set to a logic low) when V_{IN} is relatively low. The following figure shows V_{IN} ramping up and PG being set to a logic low when V_{IN} is only 620 mV. Most competing regulators cannot initialize PG at this level of V_{IN}. For this test, PG is pulled up by an external 3.3 V supply via a 10 kΩ resistor (I_{PG} = 330 μA_{DC}).

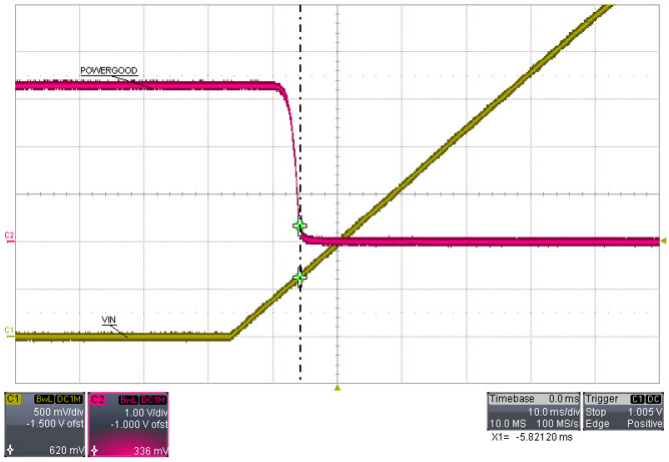


Figure 14: Power Good is fully initialized at V_{IN} = 620 mV during power-up, 10 ms/DIV.

At power-down, Power Good should be held in the logic low state as long as possible. The following figure shows V_{IN} ramping down and PG being held low until V_{IN} is only 570 mV. Most competing regulators cannot maintain PG low down to this level of V_{IN}. For this test, PG is pulled up by an external 3.3 V supply via a 10 kΩ resistor (I_{PG} = 330 μA_{DC}).

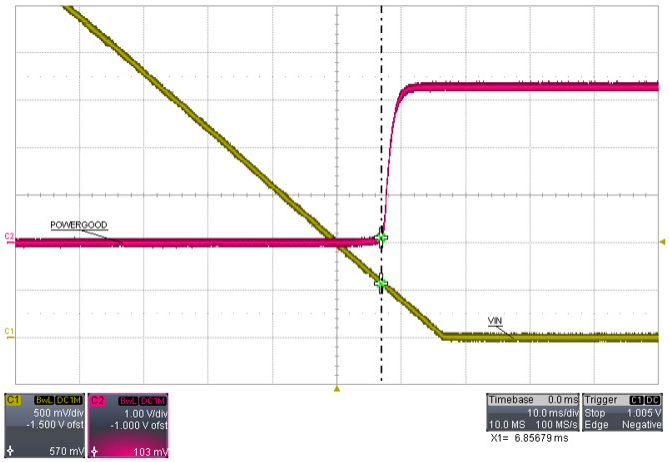


Figure 15: Power Good maintains a low state until V_{IN} = 570 mV at power-down, 10 ms/DIV.

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{IN(START)}$). The UVLO comparator incorporates enough hysteresis, about 200 mV, to prevent on/off cycling of the regulator due to I_R drops in the V_{IN} path during heavy loading or during startup.

Pulse-by-Pulse Current Limit

The current in the high-side MOSFET is monitored on a cycle-by-cycle basis. If the high-side current exceeds $I_{LIM(HS)}$, the high-side MOSFET is turned off. This protects the high-side MOSFET from excessive current, overheating, and possible damage. The high-side current limit scales with the load current selection as shown in Table 2.

In a synchronous regulator, the inductor current is allowed to go negative. If the negative current in the low-side MOSFET exceeds $I_{LIM(LS)}$, the low-side MOSFET is turned off. This protects the low-side MOSFET from excessive current, overheating, and possible damage. The low-side current limit is fixed at approximately 700 mA ($I_{LIM(LS)}$).

Output Short-Circuit Protection and Hiccup Mode

An overcurrent (OC) counter and hiccup mode logic protect the regulator when its output is shorted to ground or when the load is too high.

For the first 512 of 4096 f_{CLK} cycles during soft-start, the OC counter and hiccup mode are disabled. However, pulse-by-pulse current limit is always enabled. This approach gives high priority to startup but still protects the regulator. After 512 f_{CLK} cycles, the OC counter and the hiccup mode are enabled. At this instant, given the level of V_{OUT}, the regulator will allow an additional fixed number of overcurrent counts before activating hiccup mode:

- If $V_{OUT} < 25\%$, allow only 30 consecutive OC counts, or
- If $V_{OUT} > 25\%$, allow 120 consecutive OC counts.

If the OC counter reaches its limit, a hiccup latch is set and PWM switching is suspended for 4096 f_{CLK} cycles (1.95 ms, $t_{HIC(REC)}$). This provides time for the regulator to cool down. After the hiccup timer expires, the hiccup latch is cleared, and a new soft-start routine begins, as described earlier. If the short circuit at the regulator output remains, another hiccup cycle will occur as explained previously. Hiccup cycles repeat until the short circuit is removed or the regulator is disabled. If the short circuit is removed and the 4096 f_{CLK} recovery time expires, the regulator will soft-start normally and the output voltage will automatically recover to the target level. Hiccup mode operation and recovery are shown in the following figure.

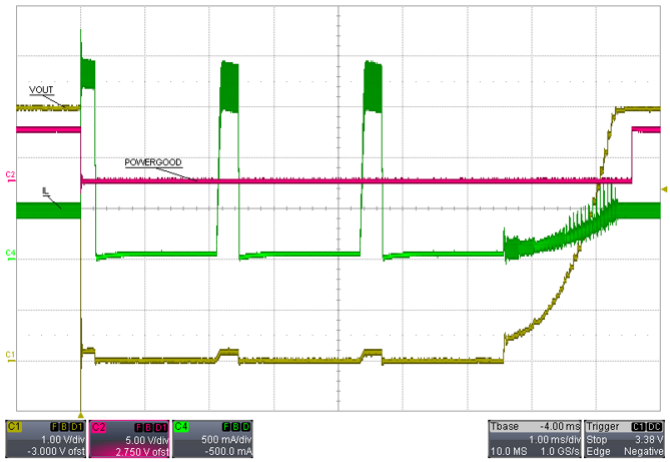


Figure 16: Output Short Circuit Transient and Recovery

SW Pin Protection

Unlike most regulators, the ARG81880 protects itself even when the SW pin is shorted to ground.

If the SW pin is shorted to ground, there will be a very high current in the high-side MOSFET when it is turned on. When the ARG81880 detects this unusually high current ($I_{LIM(SC)}$), it instantly turns off the high-side MOSFET. If the regulator detects two consecutive instances where the current exceeds $I_{LIM(SC)}$, it will set the hiccup mode latch and stop switching. After 4096 f_{CLK} cycles ($t_{HIC(REC)}$), the regulator will attempt to restart. If the SW pin remains shorted to ground, another hiccup will occur. If the short to ground is removed, the ARG81880 will automatically recover. Unlike other hiccup mode protections, the SW pin protection does not observe the hiccup mode enable delay of 512 f_{CLK} cycles ($t_{HIC(EN)}$).

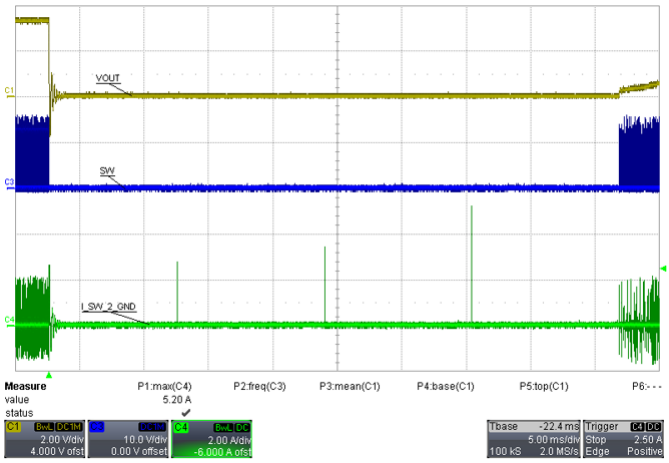


Figure 17: SW short-to-ground protection and recovery hiccup mode after two detections.

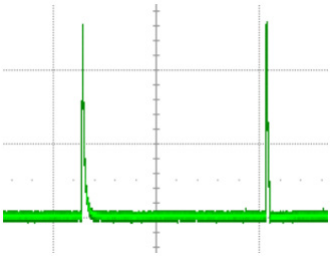


Figure 18: Each of the SW-to-ground transients shown in the previous figure is actually 2 events.

BOOT Pin Protections

The ARG81880 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited.

If the BOOT capacitor is missing, the BOOT voltage appears adequate due to stray capacitance between the BOOT and the SW pins (10 to 20 pF). However, there is not enough charge to enhance the high-side MOSFET. Therefore, at the start of every PWM cycle, the BOOT voltage drops the instant the gate driver attempts to turn on the high-side MOSFET. This causes $BOOT_{UV}$ to occur and the high-side MOSFET is turned off (it never actually turns on). The regulator is unable to raise V_{OUT} so Power Good remains low. The ARG81880 repeats this process until the BOOT capacitor is replaced.

If the BOOT capacitor is short-circuited, $BOOT_{UV}$ persists during soft-start and the BOOT charger is purposely shut down after only 64 f_{CLK} cycles ($t_{BOOT(SC)}$). After the Hiccup Enable Delay (512 f_{CLK} cycles, $t_{HIC(EN)}$) plus the minimum OC count (30 f_{SW} cycles or 240 f_{CLK} cycles), the regulator will set the hiccup latch. After waiting 4096 f_{CLK} cycles ($t_{HIC(REC)}$), the regulator will clear the hiccup latch and attempt another soft-start. The regulator will continue in hiccup mode until the short circuit is removed from the BOOT capacitor.

Overvoltage Protection (OVP)

The ARG81880 provides a fundamental level of overvoltage protection. If V_{OUT} is above the overvoltage threshold (107%, $V_{OUT(OV,H)}$) for longer than the deglitch time (128 f_{CLK} cycles, t_{dOV}), the high-side MOSFET is shut off. Also, to correct the overvoltage condition, the low-side MOSFET is turned on and sinks current from V_{OUT}. Each PWM cycle, the low-side MOSFET is allowed to be on until the inductor current reaches the low-side MOSFET negative current limit (700 mA, $I_{LIM(LS)}$).

Thermal Protection

The ARG81880 protects itself from overheating by means of an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, 175°C typical), both high-side and low-side MOSFETs are shut off, the BOOT charger is shut down, and the internal control circuits are reset. The regulator automatically restarts when the junction temperature decreases more than the thermal shutdown hysteresis (T_{HYS}, 20°C typical).

Pin-to-Ground and Adjacent Pin Short Protections

The ARG81880 is designed to satisfy the most demanding automotive applications. For example, the device is designed to withstand a short circuit to ground at each pin without suffering damage. In addition, care was taken when defining the device pin-out to optimize protection against adjacent pin-to-pin short circuits. For example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low voltage pins are located adjacent to high voltage pins, but in these instances the low voltage pins are designed to withstand unusually high voltages—with clamps and/or series input resistance to prevent damage to the device.

Table 6 is a comprehensive summary of all fault conditions and the response of the ARG81880 in each case.

Table 6: Summary Of Fault Mode Operation

Fault Condition	Response To Fault	V_{OUT}	Boot Regulator	PG	Latched Fault?	Reset Method
V_{OUT} overvoltage (OV)	If OV exists for t > t_{dOV}, stop PWM switching, turn on the low-side FET, and set PG low. Turn off the low-side FET if it exceeds its current limit.	V_{OUT} > $V_{OUT(OV,H)}$	Off when MOSFETs are tristated	Low if OV for t > t_{dOV}	No	Remove the cause of OV
V_{OUT} undervoltage (UV)	If UV exists for t > t_{dUV}, set PG low.	V_{OUT} < $V_{OUT(UV,L)}$	On	Low if UV for t > t_{dUV}	No	Check V_{OUT} for overload or a short to ground.
V_{OUT} pin open circuit	If V_{OUT} is open circuit its voltage will be near 0 V. If V_{OUT} is this low, the frequency is limited to f_{OSC}/8 and the duty cycle is limited to 1/8.	0 V to V_{IN}/8	On	Low if V_{OUT} < $V_{OUT(UV,L)}$	No	Connect the V_{OUT} pin
V_{OUT} overcurrent (OC)	The high-side MOSFET is shut off when the current is higher than the pulse-by-pulse current limit. Hiccup mode after the Hiccup Enable Delay (512 f_{CLK} cycles) and too many consecutive OC counts, 30 or 120, depending on the level of V_{OUT}.	Depends on V_{IN} and load	On	Low if V_{OUT} < $V_{OUT(UV,L)}$	No	Reduce the load
V_{OUT} short to ground	High-side MOSFET shuts off when the current is higher than the pulse-by-pulse limit ($I_{LIM(HS)}$). Enters hiccup mode after 30 consecutive OC counts.	0 V	On	Low	No	Remove the short circuit at V_{OUT}
SW pin open circuit	The regulator will be unable to charge the BOOT capacitor so the high-side FET will not switch.	0 V	On	Low	No	Connect the SW pin
SW pin short to ground	High-side MOSFET shuts off when the current is higher than the SW short-circuit limit ($I_{LIM(SC)}$). Immediately enters Hiccup mode after 2 consecutive detections—does not wait for the Hiccup Enable delay ($t_{HIC(EN)}$).	0 V	On	Low	No	Remove the short circuit at SW
BOOT pin open circuit	The voltage at the BOOT pin appear OK due to stray capacitance (10 to 20 pF). However, there is not enough charge to enhance the upper FET, so the BOOT voltage falls below the $BOOT_{UV}$ threshold at the start of every PWM cycle.	0 V	On	Low	No	Connect the BOOT pin
BOOT pin short to ground	The BOOT regulator cannot charge C_{BOOT}. The BOOT regulator remains on for only 64 f_{CLK} cycles ($t_{BOOT(SC)}$). Hiccup mode occurs after 752 f_{CLK} cycles ($t_{HIC(EN)}$ + 30/f_{SW}, where f_{SW} = f_{CLK}/8).	0 V	Off after 64 f_{CLK} cycles	Low	No	Remove the short circuit from BOOT to ground
BOOT pin short to SW	The low-side MOSFET turns on as part of the BOOT charging routine but C_{BOOT} cannot charge. The BOOT regulator remains on for only 64 f_{CLK} cycles ($t_{BOOT(SC)}$). Hiccup mode occurs after 752 f_{CLK} cycles ($t_{HIC(EN)}$ + 30/f_{SW}, where f_{SW} = f_{CLK}/8).	0 V	Off after 64 f_{CLK} cycles	Low	No	Remove the short circuit from BOOT to SW
EN/UV pin short to ground	The EN/UV voltage is at 0V so the regulator is disabled.	0V	Off when the IC is disabled	Low	No	Remove the short circuit from EN/UV to ground
EN/UV pin open circuit	The EN/UV voltage is pulled low by an internal current sink. The pin is stuck at 0 V and the regulator is disabled.	0 V	Off when the IC is disabled	Low	No	Connect the EN/UV pin
I_{LIM}/$SYNC_{IN}$ short to ground	This is a valid state for this pin resulting in current limits to support 640 mA.	Set by V_{SET} pin status	On	High if V_{OUT} > $V_{OUT(UV,H)}$	No	Remove the short circuit from I_{LIM}/$SYNC_{IN}$ to ground
I_{LIM}/$SYNC_{IN}$ open circuit	This is a valid state for this pin resulting in current limits to support 800mA.	Set by VSET pin status	On	High if V_{OUT} > $V_{OUT(UV,H)}$	No	Connect the I_{LIM}/$SYNC_{IN}$ pin

Continued on next page...

Table 6: Summary Of Fault Mode Operation (continued)

Fault Condition	Response To Fault	V_{OUT}	Boot Regulator	PG	Latched Fault?	Reset Method
V_{SET} short to ground	This is a valid state for this pin resulting in an output voltage of 3.3 V.	3.3 V	On	High if $V_{OUT} > V_{OUT(UV,H)}$	No	Remove the short circuit from V_{SET} to ground
V_{SET} open circuit	This is a valid state for this pin resulting in an output voltage of 5.0 V.	5.0 V	On	High if $V_{OUT} > V_{OUT(UV,H)}$	No	Connect the V_{SET} pin
PG open circuit	PG pulled high via external pull-up resistor.	Normal, Set by V_{SET}	On	Stuck high	No	Connect the PG pin
PG short to ground	PG stuck at 0 V.	Normal, Set by V_{SET}	On	Stuck low	No	Remove the short circuit from PG to ground
PG short to SW	PG unable to show correct state. PG will follow SW, toggling between 0 V and V_{IN}.	Normal, Set by V_{SET}	On	Follows SW voltage	No	Remove the short circuit from PG to SW
Thermal Shutdown (TSD)	The regulator will shut down when $T_J > T_{TSD}$.	0 V	Off when MOSFETs are tristated	Low	No	Automatic, resets after $T_J < T_{TSD} - T_{HYS}$

COMPONENT SELECTIONS

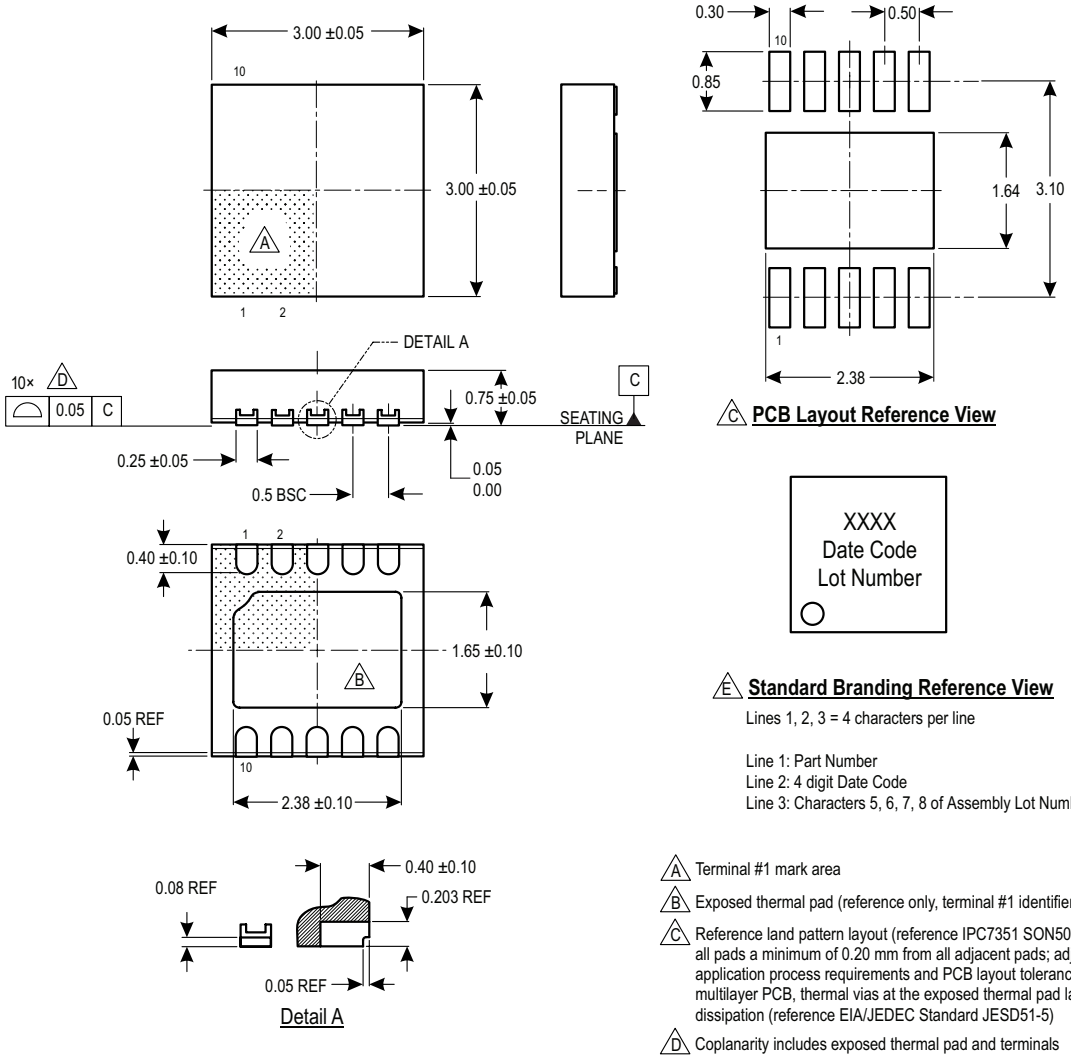
Table 7: Recommended Component Values for a 12 V_{IN} System

V_{OUT} (V)	R_{SET} ±1%	Recommended Power Components					
		I_{OUT} = 800 mA		I_{OUT} = 640 mA		I_{OUT} = 480 mA	
5.0	OPEN	8.2 µH	4.7 µF	10 µH	3.3 µF	12 µH	2.2 µF
3.3	GND	6.8 µH	6.8 µF	8.2 µH	5.6 µF	10 µH	3.3 µF
2.5	15.4kΩ	5.6 µH	8.2 µF	6.8 µH	6.8 µF	8.2 µH	5.6 µF

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-229)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 19: Package EJ, Wettable Flank DFN-10 with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	March 20, 2018	Initial release
1	June 20, 2018	Corrected Thermal Characteristics table (page 2)

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