CS2600

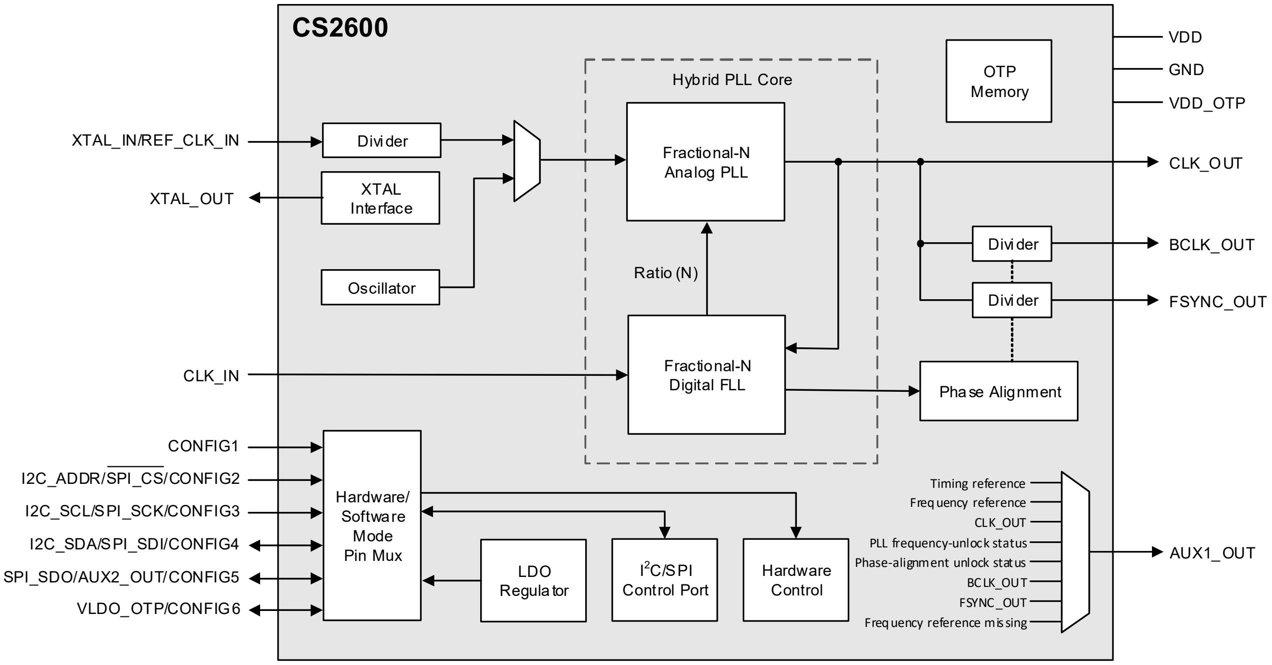
Fractional-N Clock Synthesizer and Multiplier

Features

- Clock frequency synthesizer incorporating delta-sigma fractional-N analog PLL
  - Generates low-jitter 6–75 MHz clock (CLK_OUT) from 8–75 MHz timing reference (REF_CLK_IN)
- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - Generates low-jitter 6–75 MHz clock (CLK_OUT), synchronized to a 150 Hz–30 MHz low-quality or intermittent frequency reference (CLK_IN)
- Flexible timing reference source
  - External clock, external crystal, or built-in oscillator
- High resolution PLL ratio (1 PPM)
- 18 ps_{RMS} period jitter (external timing reference), 18 ps_{RMS} period jitter (oscillator reference)
- Glitchless clock output generated from intermittent input
- BCLK and FSYNC outputs (derived from CLK_OUT) for digital audio applications
  - Phase alignment with CLK_IN frequency reference
- Automatic rate control (ARC) for digital audio applications
  - Seamless transitions through changes in CLK_IN frequency reference
- Customer-programmable startup configuration, using integrated one-time programmable (OTP) memory
- Hardware and software control modes
  - I²C/SPI control port
  - Hardware control with no host processor required
- Configurable auxiliary clock/status output
- Minimal board space required
  - No external analog loop-filter components
- Single-supply operation at 1.8 V or 3.3 V

Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



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General Description

The CS2600 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2600 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 150 Hz. An internal oscillator can provide the timing reference clock, enabling a reduction in external component requirements. The CS2600 can be configured using a control interface supporting I^{2}C and SPI modes of operation. The device can also be configured in Hardware Control Mode using pull-up/pull-down resistors, reducing system software overhead.

The CS2600 supports BCLK and FSYNC outputs, derived from the PLL output signal. All of the clock outputs can be phase-aligned with the clock input source. The automatic rate control (ARC) function detects the clock input frequency and configures the PLL ratio for the required output. The ARC supports seamless transitions through changes in the reference frequency; the BCLK and FSYNC outputs are automatically adjusted to maintain the applicable ratios.

The CS2600 provides a built-in OTP memory to configure the default operating settings, loaded at boot-up. The OTP memory is optimized and managed to support multiple programming cycles.

The CS2600 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2600 is available in commercial-grade 16-pin QFN package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C. See Section 12 for ordering information.

Table of Contents

1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 QFN Pin Assignments (Top View, Through Package)

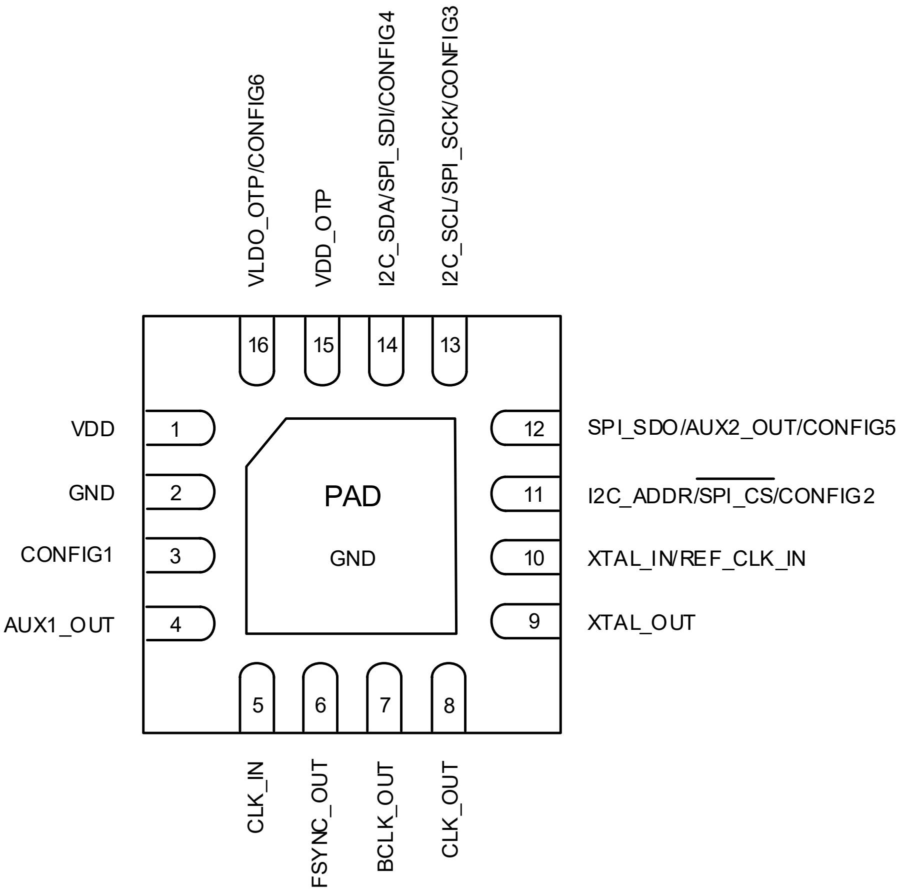


Figure 1-1. QFN 16-Pin Diagram (Top View, Through-Package)

1.2 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
VDD	1	—	—	**Power Supply.** 3.3 V/1.8 V supply for the digital and analog blocks.
GND	2, PAD	—	—	**Ground and Pad.** The paddle must be connected to ground plane directly underneath the CS2600.
CONFIG1	3	VDD	I	**Hardware Configuration 1.** Hardware Control Mode configuration connection. Connect to GND for Software Control Mode.
AUX1_OUT	4	VDD	O	**Auxiliary Output.** Configurable clock output or status output.
CLK_IN	5	VDD	I	**Clock Input.** Frequency reference input for the digital FLL.
FSYNC_OUT	6	VDD	O	**FSYNC Output.** PLL frame sync clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.
BCLK_OUT	7	VDD	O	**BCLK Output.** PLL bit clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.
CLK_OUT	8	VDD	O	**Clock Output.** PLL clock output.

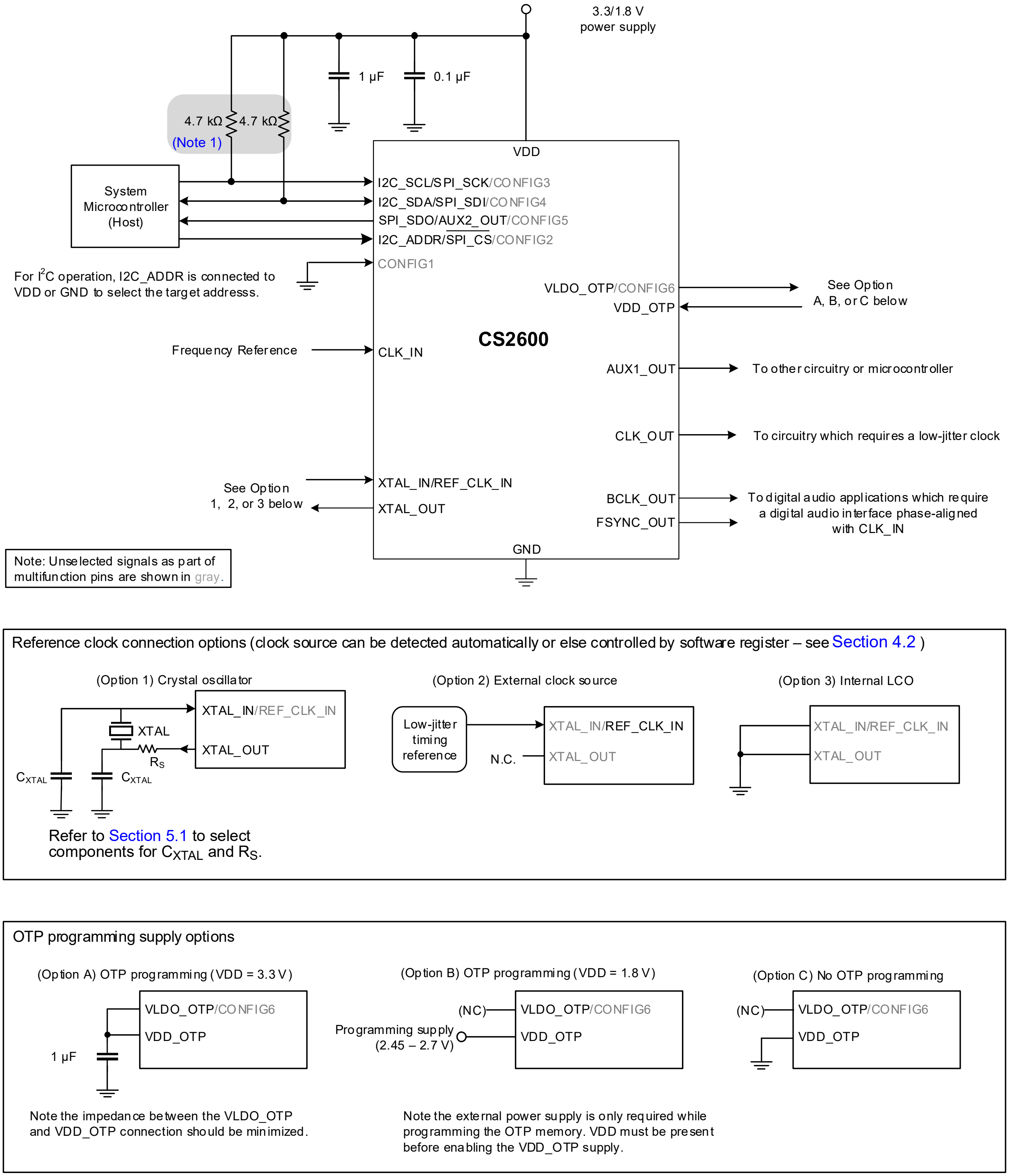
Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
XTAL_OUT	9	VDD	O	**Crystal Connection.** Output for an external crystal. Connect to GND for internal oscillator reference clock.
XTAL_IN/REF_CLK_IN	10	VDD	I	**Crystal Connection.** Input for an external crystal. **Reference Clock.** External low-jitter timing reference clock input. Connect to GND for internal oscillator reference clock.
I2C_ADDR/$\overline{\text{SPI\_CS}}$/CONFIG2	11	VDD	I	**I^{2}C Control-Port Address.** Chip address input for the I^{2}C interface. **SPI Control-Port Chip Select.** Active-low chip select input for the SPI interface. **Hardware Configuration 2.** Hardware Control Mode configuration connection.
SPI_SDO/AUX2_OUT/CONFIG5	12	VDD	I/O	**SPI Control-Port Serial Data Out.** SPI data output. **Auxiliary Output 2.** Configurable status output. **Hardware Configuration 5.** Hardware Control Mode configuration connection.
I2C_SCL/SPI_SCK/CONFIG3	13	VDD	I	**I^{2}C Control-Port Clock.** Clock input for the I^{2}C interface. **SPI Control-Port Clock.** Clock input for the SPI interface. **Hardware Configuration 3.** Hardware Control Mode configuration connection.
I2C_SDA/SPI_SDI/CONFIG4	14	VDD	I/O	**I^{2}C Control-Port Data.** Data input/output for the I^{2}C interface. **SPI Control-Port Serial Data In.** SPI data input. **Hardware Configuration 4.** Hardware Control Mode configuration connection.
VDD_OTP	15	—	—	**OTP Programming Supply (Input).** If VDD = 1.8 V, an external programming supply is required when writing to the OTP memory. This supply can be generated internally if VDD = 3.3 V.
VLDO_OTP/CONFIG6	16	VDD	I/O	**OTP Programming Supply (Output).** OTP programming regulator output (VDD = 3.3 V). **Hardware Configuration 6.** Hardware Control Mode configuration connection.

1.3 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS2600 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

2 Typical Connections



For I²C operation, I2C_ADDR is connected to VDD or GND to select the target addresss.

Note: Unselected signals as part of multifunction pins are shown in gray.

Reference clock connection options (clock source can be detected automatically or else controlled by software register – see Section 4.2)

Refer to Section 5.1 to select components for C_{XTAL} and R_S.

Note the impedance between the VLDO_OTP and VDD_OTP connection should be minimized.

Note the external power supply is only required while programming the OTP memory. VDD must be present before enabling the VDD_OTP supply.

Figure 2-1. Typical Connection Diagram—Software Control Mode

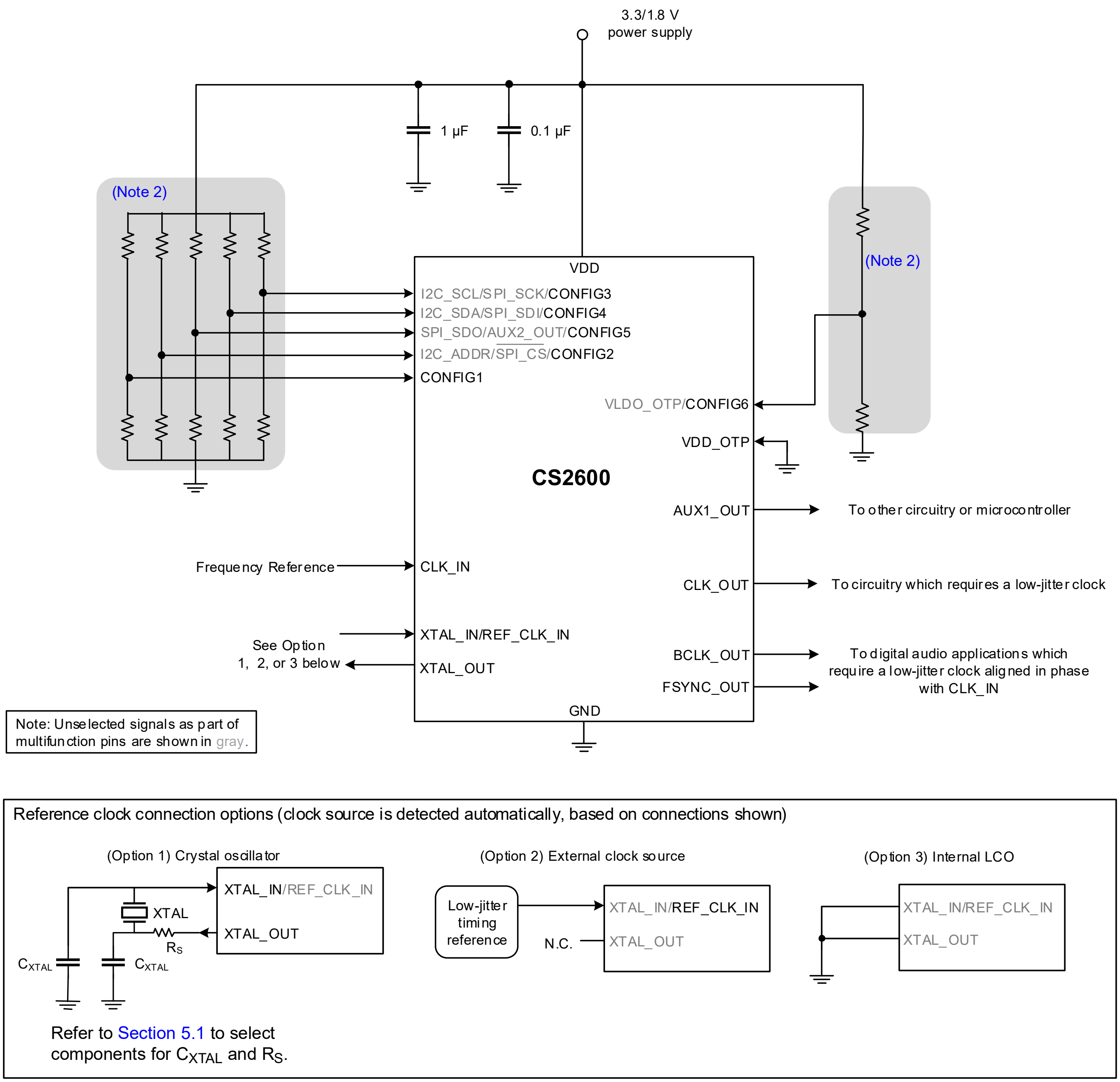

3.3/1.8 V
power supply
1 µF
0.1 µF
(Note 2)
(Note 2)
VDD
I2C_SCL/SPI_SCK/CONFIG3
I2C_SDA/SPI_SDI/CONFIG4
SPI_SDO/AUX2_OUT/CONFIG5
I2C_ADDR/SPI_CS/CONFIG2
CONFIG1
VLDO_OTP/CONFIG6
VDD_OTP
CS2600
AUX1_OUT
To other circuitry or microcontroller
Frequency Reference
CLK_IN
CLK_OUT
To circuitry which requires a low-jitter clock
XTAL_IN/REF_CLK_IN
See Option
1, 2, or 3 below
XTAL_OUT
BCLK_OUT
FSYNC_OUT
To digital audio applications which
require a low-jitter clock aligned in phase
with CLK_IN
GND
Note: Unselected signals as part of
multifunction pins are shown in gray.
Reference clock connection options (clock source is detected automatically, based on connections shown)
(Option 1) Crystal oscillator
XTAL
XTAL_IN/REF_CLK_IN
XTAL_OUT
Rs
CXTAL
CXTAL
(Option 2) External clock source
Low-jitter
timing
reference
XTAL_IN/REF_CLK_IN
N.C.
XTAL_OUT
(Option 3) Internal LCO
XTAL_IN/REF_CLK_IN
XTAL_OUT
Refer to Section 5.1 to select
components for CXTAL and RS.

Figure 2-2. Typical Connection Diagram—Hardware Control Mode

Notes referenced in the typical connection diagrams:

1. The pull-up resistors are required only for I2C operation. The diagram shows 4.7 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.
2. Each hardware pin is configured using a pull-up to VDD or pull-down to GND, supporting up to eight configuration options per pin. See Section 4.9 for further detail.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
DC power supply	Nominal 3.3 V Nominal 1.8 V	VDD	3.1 1.71	3.3 1.8	3.5 1.89	V V
OTP programming supply [1,2]		VDD_OTP	2.45	—	2.7	V
Supply ramp up/down (all supplies)		t_{PWR_UD}	0.01	—	10	ms
Ambient temperature	Commercial Grade AEC-Q100 Grade 2	T_A	–40 –40	— —	85 105	°C °C

[1] The OTP programming supply can be generated by an internal LDO, or else powered externally. To use the internal LDO, the VDD_OTP pin must be connected to VLDO_OTP. If VDD < 3.1 V, the OTP programming supply must be powered externally. If OTP programming is not required, VDD_OTP should be connected to GND.

[2] VDD must be present before enabling the VDD_OTP supply. VDD_OTP supply must be removed before powering down VDD.

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	–0.3	4.32	V
OTP programming supply	VDD_OTP	–0.3	2.75	V
External voltage applied to digital input/output	V_{INDI}	–0.3	VDD + 0.3	V
Input current	I_{in}	—	±10	mA
Ambient temperature	T_A	–55	125	°C
Storage temperature	T_{STG}	–65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = 25°C; timing reference = 12 MHz (external clock or crystal).

Parameters		Symbol	Min	Typ	Max	Units
Power supply current—unloaded [1]		I_{VDD}	—	4	—	mA
OTP programming supply current		I_{VDD_OTP}	—	—	25	mA
Input leakage current (per pin)		I_{IN}	—	—	±10	µA
Input capacitance (per pin)		I_C	—	—	5	pF
High-level input voltage		V_{IH}	0.70 × VDD	—	—	V
Low-level input voltage		V_{IL}	—	—	0.30 × VDD	V
High-level output voltage		V_{OH}	0.90 × VDD	—	—	V
Low-level output voltage		V_{OL}	—	—	0.10 × VDD	V
VDD power-on reset (POR) threshold	VDD rising VDD falling	V_{POR}	1.40 1.38	— —	1.59 1.55	V V
VDD power-on reset duration [2]		t_{POR}	100	—	—	ms

[1] To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).

[2] To trigger a power-on reset, VDD must be held below the reset threshold for longer than this duration. Note that VDD interruption shorter than this duration may result in incorrect device behavior.

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	f_{XTAL}	8 16 32	— — —	18.75 37.50 50	MHz MHz MHz
Crystal interface transconductance (T_A = 25°C)	VDD = 3.3 V VDD = 1.8 V	—	— —	26 43	— —	mS mS
Reference clock input frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	$f_{REF\_CLK\_IN}$	8 16 32	— — —	18.75 37.50 75	MHz MHz MHz
Reference clock input duty cycle		$D_{REF\_CLK\_IN}$	45	—	55	%
Clock input frequency		f_{CLK_IN}	150	—	30×10^6	Hz
Clock input pulse width	$f_{CLK\_IN} < f_{SYSCLK} / 96$ [1] $f_{CLK\_IN} > f_{SYSCLK} / 96$ [1]	pw_{CLK_IN}	2 10	— —	— —	UI [2] ns
CLK_OUT frequency range		f_{CLK_OUT}	6	—	75	MHz
BCLK frequency range		f_{BCLK_OUT}	f_{CLK_OUT} / 48	—	f_{CLK_OUT}	MHz
FSYNC frequency range		f_{FSYNC_OUT}	f_{CLK_OUT} / 1536	—	f_{CLK_OUT} / 16	MHz
Clock output duty cycle	measured at VDD / 2	t_{OD}	45	50	55	%
Clock output rise time	10% to 90% of VDD	t_{OR}	—	1.8	—	ns
Clock output fall time	90% to 10% of VDD	t_{OF}	—	1.8	—	ns
CLK_OUT period jitter [3,4]	external timing reference internal oscillator reference	t_{JIT}	— —	18 18	25 25	ps_{RMS} ps_{RMS}
CLK_OUT baseband TIE jitter [3,5]	external timing reference internal oscillator reference	—	— —	21 170	70 350	ps_{RMS} ps_{RMS}
CLK_OUT wideband TIE jitter [3,6]	external timing reference internal oscillator reference	—	— —	90 200	160 380	ps_{RMS} ps_{RMS}
PLL lock time—Multiplier Mode	150 Hz ≤ f_{CLK_IN} < 600 Hz 600 Hz ≤ f_{CLK_IN} < 200 kHz f_{CLK_IN} ≥ 200 kHz	t_{LC}	— — —	160 100 1	700 200 3	UI [7] UI [7] ms
PLL lock time—Synthesizer Mode	$f_{REF\_CLK\_IN}$ = 8 to 75 MHz	t_{LR}	—	1	3	ms
CLK_OUT frequency resolution [3,8]	high resolution high multiplication	—	— —	1 244	— —	ppm ppm
Oscillator frequency	at 25°C	—	11.76	12.0	12.24	MHz
Oscillator frequency thermal sensitivity	at 25°C	—	—	90	—	ppm/°C
Oscillator frequency stability (relative to 25°C)	–40 to 85°C –40 to 105°C	—	–1.0 –1.3	— —	0.8 0.8	% %
Phase alignment error	CLK_IN to FSYNC	—	—	±0.5	—	UI [9]
Clock output skew	CLK_OUT, BCLK, and FSYNC	—	—	—	±0.5	ns
Clock output frequency deviation	CLK_IN stopped, holdover enabled	—	—	—	0.1	%
Start-up time [10]	from VDD applied	—	—	—	20	ms

[1] The internal timing reference clock (SYSCLK) is derived from REF_CLK_IN (see Section 4.2).

[2] UI (unit interval) corresponds to t_{SYSCLK} or 1 / f_{SYSCLK}.

[3] REF_CLK_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz.

[4] Sample size is 10000.

[5] Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.

[6] Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.

[7] UI (unit interval) corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.

[8] The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.

[9] UI (unit interval) corresponds to t_{CLK_OUT} or 1 / f_{CLK_OUT}.

[10] The time to first locked clock output, assuming OTP configuration for f_{CLK_IN} = 48 kHz.

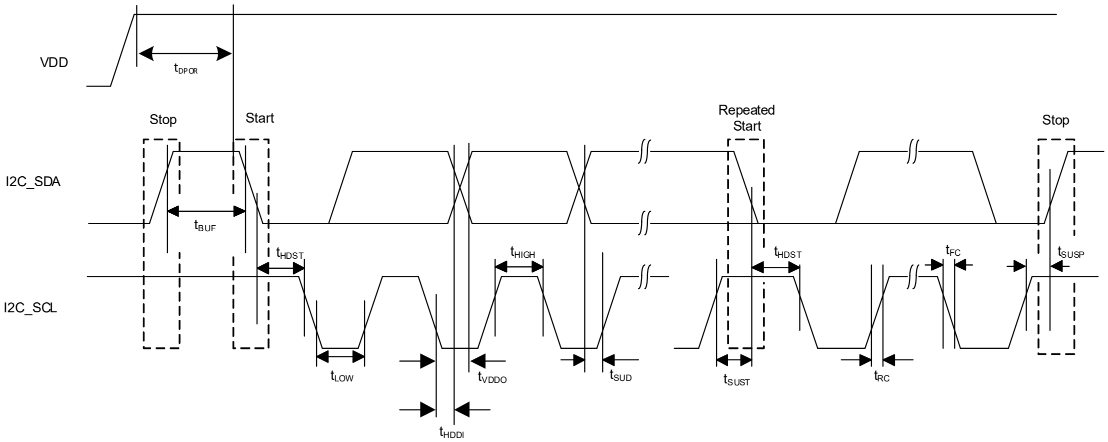
Table 3-5. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]	Symbol	Min	Max	Units
SCL clock frequency	f_{SCL}	—	1000	kHz
Clock low time	t_{LOW}	500	—	ns
Clock high time	t_{HIGH}	260	—	ns
Start condition hold time (before first pulse clock)	t_{HDST}	260	—	ns
Setup time for repeated start	t_{SUST}	260	—	ns
Rise time of SCL and SDA $f_{SCL} \le 100$ kHz 100 kHz $< f_{SCL} \le 400$ kHz 400 kHz $< f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time SCL and SDA $f_{SCL} \le 100$ kHz 100 kHz $< f_{SCL} \le 400$ kHz 400 kHz $< f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL	—	—	1.67	x
Fall time variation between SDA and SCL $f_{SCL} \le 100$ kHz 100 kHz $< f_{SCL} \le 400$ kHz 400 kHz $< f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition	t_{SUSP}	260	—	ns
SDA setup time to SCL rising	t_{SUD}	50	—	ns
SDA input hold time from SCL falling	t_{HDDI}	0	—	ns
Output data valid (Data/ACK) $f_{SCL} \le 100$ kHz 100 kHz $< f_{SCL} \le 400$ kHz 400 kHz $< f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions	t_{BUF}	500	—	ns
SDA bus capacitance	C_B	—	400	pF
SCL/SDA pull-up resistance	R_P	500	—	Ω
Pulse width of spikes to be suppressed	t_{ps}	0	50	ns
Start-up time from power-up/software reset to control port ready [3]	t_{DPOR}	—	5	ms

[1] The I²C control port uses a 16-bit register address and 16-bit data words.

[2] I²C control-port timing.



[3] Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

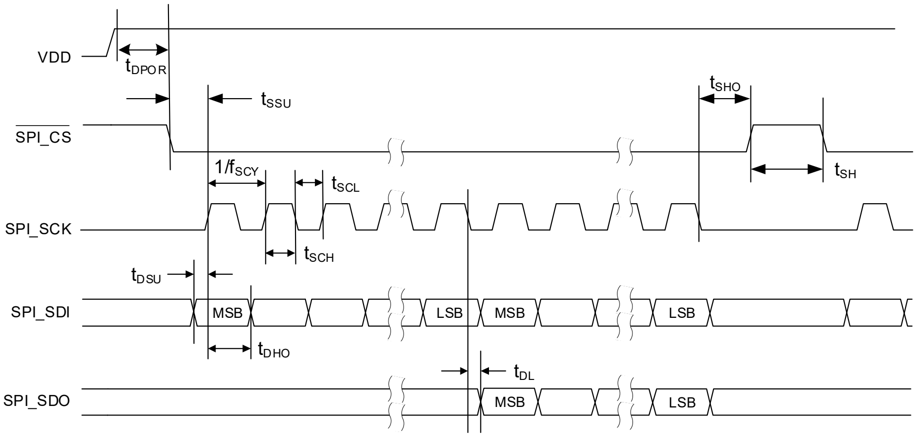
Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]		Symbol	Min	Max	Units
SCK clock frequency	Access to OTP registers (0x2300–0x232F) Access to all other registers	f_{SCL}	— —	4.5 17.5	MHz MHz
$\overline{\text{CS}}$ falling edge to SCK rising edge		t_{SSU}	5	—	ns
SCK falling edge to $\overline{\text{CS}}$ rising edge		t_{SHO}	0.5	—	ns
SCK pulse width low		t_{SCL}	18.5	—	ns
SCK pulse width high		t_{SCH}	18.5	—	ns
SDI to SCK rising setup time		t_{DSU}	5	—	ns
SDI to SCK hold time		t_{DHO}	2.5	—	ns
SCK falling edge to SDO transition		t_{DL}	0	15	ns
$\overline{\text{CS}}$ rising edge to SDO output high-Z		—	0	20	ns
Bus free time between active $\overline{\text{CS}}$		t_{SH}	110	—	ns
Delay from supply voltage stable to control port ready [3]		t_{DPOR}	—	5	ms

[1] The SPI control port uses a 15-bit register address and 16-bit data words.

[2] SPI control-port timing.



[3] The supply voltage is considered stable when VDD is within the recommended operating conditions (see Table 3-1).

4 Functional Description

4.1 Device Architecture

The CS2600 is a highly versatile clock generator. It combines an analog PLL and digital FLL to provide high-resolution clock multiplier and clock synthesizer capability. The delta-sigma architecture enables low-jitter clock generation across a wide range of fractional operating ratios; it also supports fast transitions between different ratios and output frequencies. Configurable bandwidth of the digital FLL enables optimized behavior under dynamic operating conditions.

The analog PLL generates the main clock output (CLK_OUT), using the timing reference as its input. The timing reference is a stable low-jitter clock source, derived from the REF_CLK_IN input, external crystal, or the internal oscillator. The timing reference is used to ensure the time and phase stability of the PLL output. The PLL frequency ratio determines the multiplier ratio between the timing-reference input and the clock output.

The digital FLL provides input to the analog PLL to configure the frequency ratio. The digital FLL uses the frequency reference (CLK_IN) as its input and generates the PLL frequency ratio as a control signal to the analog PLL. The capability of the digital FLL is enhanced by its configurable bandwidth; a wide bandwidth is used to achieve lock in a short time, while a narrow bandwidth is used to provide optimal jitter performance.

The CS2600 can be configured in Multiplier Mode or Synthesizer Mode.

- In Multiplier Mode, the user-selected ratio is an input to the digital FLL and defines the CLK_OUT:CLK_IN frequency ratio. The FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required CLK_OUT frequency. The frequency ratio is dynamically controlled to maintain the required output ratio.
- In Synthesizer Mode, the user-selected ratio is an input to the analog PLL and defines the CLK_OUT:REF_CLK_IN frequency ratio (or CLK_OUT:oscillator frequency ratio). The analog PLL frequency ratio is configured directly by the respective control fields. The output clock is generated from the timing reference alone, with no other clock input required. Note that the digital FLL is not used in Synthesizer Mode.

The hybrid analog/digital PLL is illustrated in Fig. 4-1. In Multiplier Mode, the user-defined ratio is defined by the *M_Ratio* parameter. In Synthesizer Mode, the user-defined ratio is defined by the *S_Ratio* parameter.

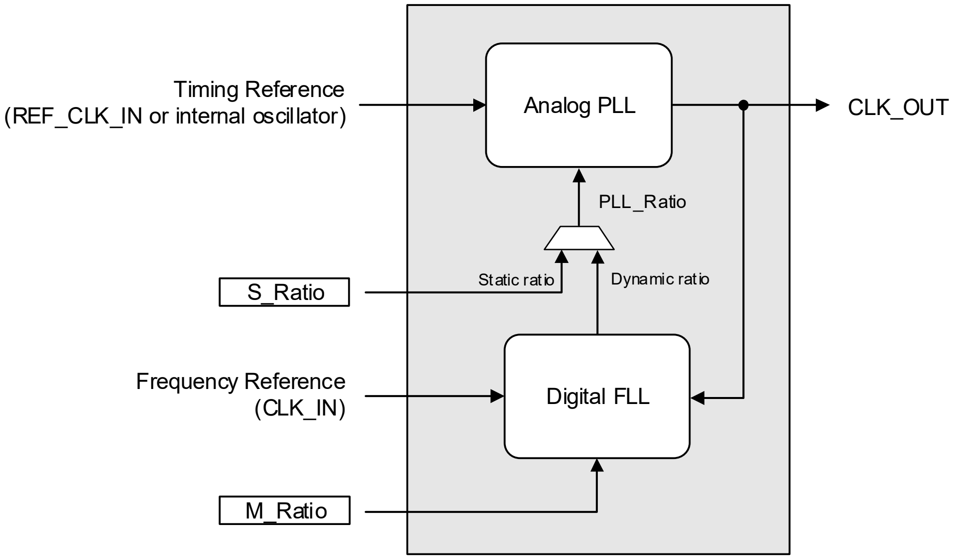


Figure 4-1. Hybrid Analog/Digital PLL

4.2 Timing Reference Configuration

The low-jitter timing reference is provided either by an external source (clock input or crystal), or by the internal oscillator. By default, the timing reference is selected automatically depending on the external pin connections, as shown Section 2. It is recommended to use SYSCLK_SRC to select the internal or external source, as shown in Fig. 4-2.

The frequency range for the external timing reference is described in Table 3-4. Note that the supported frequency range differs depending on the applicable source.

The internal timing reference, SYSCLK, is derived from the selected timing source. A programmable divider is provided for the external timing reference; the divider must be configured using REF_CLK_IN_DIV to bring the reference frequency within the valid SYSCLK range of 8–18.75 MHz.

The timing reference configuration is shown in Fig. 4-2.

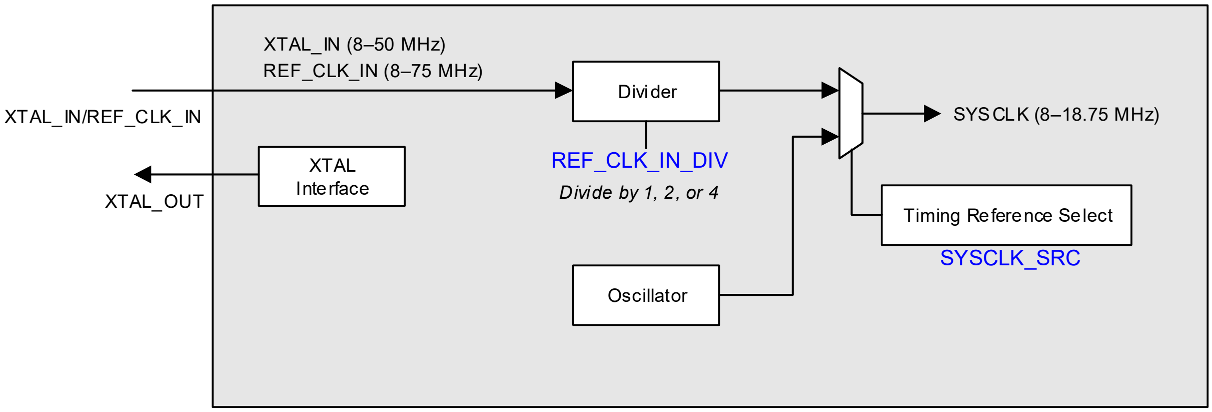


Figure 4-2. Timing Reference Configuration

Note that, in Synthesizer Mode, the PLL ratio defines the CLK_OUT:REF_CLK_IN frequency ratio (or CLK_OUT:oscillator frequency ratio, if the oscillator is selected as the timing reference). The timing-reference divider has no effect on this, and does not need to be considered when calculating the desired frequency ratio.

4.2.1 REF_CLK_IN Detection and Indication

The REF_CLK_IN signal is monitored to confirm the timing reference is present.

The REF_CLK_IN presence is indicated using ERR_STS3. This bit is a latching bit—it is set when REF_CLK_IN is not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if REF_CLK_IN is not present.

4.2.2 Crystal Oscillator

The crystal oscillator uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 4-3. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

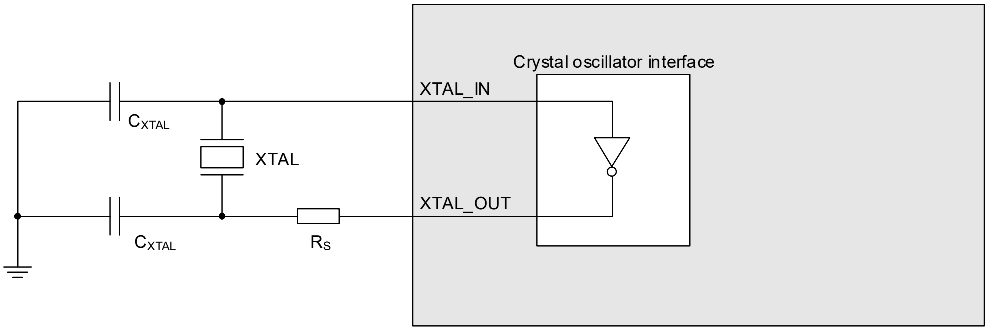


Figure 4-3. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.1. The suitability of the external crystal is calculated as a function of the operating voltage (VDD) and the transconductance of the crystal interface, as defined in Table 3-4.

4.3 Hybrid PLL Configuration

The PLL is enabled and configured as described in the following sections.

4.3.1 Enable and Lock Status

The PLL is enabled by setting PLL_EN1 and PLL_EN2 (both bits must be set in order to enable the PLL). Note there are no sequencing requirements—the bits may be set or cleared in any order.

Note: The device should be fully configured by writing to the applicable control registers before enabling the PLL. When changing the configuration, it is recommended to disable the PLL before updating the register fields; this ensures there is no unexpected transient behavior. See Section 4.7.3 for further details of configuration restrictions.

The PLL lock status is dependent on the clock inputs and the device configuration. Changes in the clock inputs or to the configuration registers can cause the PLL to lose lock. If the PLL loses lock, the quality of the clock outputs cannot be assured.

The PLL lock status is indicated using F_UNLOCK. This bit is set if the PLL is not frequency locked (including if the PLL is disabled). The lock status can be indicated on an auxiliary output pin as described in Section 4.6. The lock status can be used to automatically disable the clock outputs—see Section 4.5.4 for further details.

The PLL lock status is also indicated using F_UNLOCK_STICKY. This is a latching bit—it is set when F_UNLOCK is set, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if F_UNLOCK is set.

4.3.2 Ratio Configuration

The PLL is configured using a ratio that determines the output frequency as a function of either the timing reference, REF_CLK_IN, (in Synthesizer Mode) or the frequency reference, CLK_IN, (in Multiplier Mode).

- In Synthesizer Mode, the output frequency is defined by the following equation:

  $$f_{CLK\_OUT} = f_{REF\_CLK\_IN} \times \text{PLL Ratio}$$

  For example, to generate a 24.576 MHz output from a 12 MHz timing reference, a ratio of 2.048 is required.
- In Multiplier Mode, the output frequency is defined by the following equation:

  $$f_{CLK\_OUT} = f_{CLK\_IN} \times \text{PLL Ratio}$$

  For example, to generate a 24.576 MHz output from a 48 kHz frequency reference, a ratio of 512 is required.

The PLL ratio is a 32-bit value, configured using the RATIOn fields. A maximum of four different ratios can be configured, allowing the device to switch easily between different use cases. The applicable ratio is selected using S_RATIO_SEL (in Synthesizer Mode) or M_RATIO_SEL (in Multiplier Mode).

In Multiplier Mode, the PLL ratio can be defined in high-resolution (12.20) or high-multiplication (20.12) format; the format is selected using RATIO_CFG. In Synthesizer Mode, the high-resolution (12.20) format is used.

- In high-resolution (12.20) format, the 12 MSBs represent the integer portion of the ratio, and the remaining 20 bits represent the fractional portion. This format supports a maximum multiplication factor of ~4096, with a resolution of 0.954 ppm.
- In high-multiplication (20.12) format, the 20 MSBs represent the integer portion of the ratio, and the remaining 12 bits represent the fractional portion. This format supports a maximum multiplication factor of ~1,048,576, with a resolution of 244 ppm.

Note: If the desired ratio is less than 4096, the 12.20 format is recommended, to ensure the accuracy of the PLL output.

The PLL ratio is also configured using RATIO_MOD, allowing additional multiplication/division factors to be applied to the RATIOn selection.

The ratio modifier can be used to simplify the selection of related frequency ratios, while using the same RATIOn value. It can also be used to support high multiplication ratios in 12.20 format (multiplying by 2, 4, or 8) or to enable greater precision in 20.12 format (dividing by 2, 4, 8, or 16).

Note that, regardless of the ratio format and the ratio modifier, the PLL ratio cannot exceed a multiplication factor of 1,048, 576 or a resolution of 0.954 PPM. If the configured parameters exceed these limits, the effective multiplication or resolution is truncated.

If the selected PLL ratio is invalid, the output clocks are disabled. Normal operation resumes when a valid ratio is detected (either due to register configuration or a change in CLK_IN frequency).

An invalid ratio is indicated using ERR_STS6. This bit is a latching bit—it is set when an invalid configuration is detected and remains set until a 1 is written to the bit. Note the bit cannot be cleared if the configuration is invalid.

The ratio configuration is illustrated in Fig. 4-4.

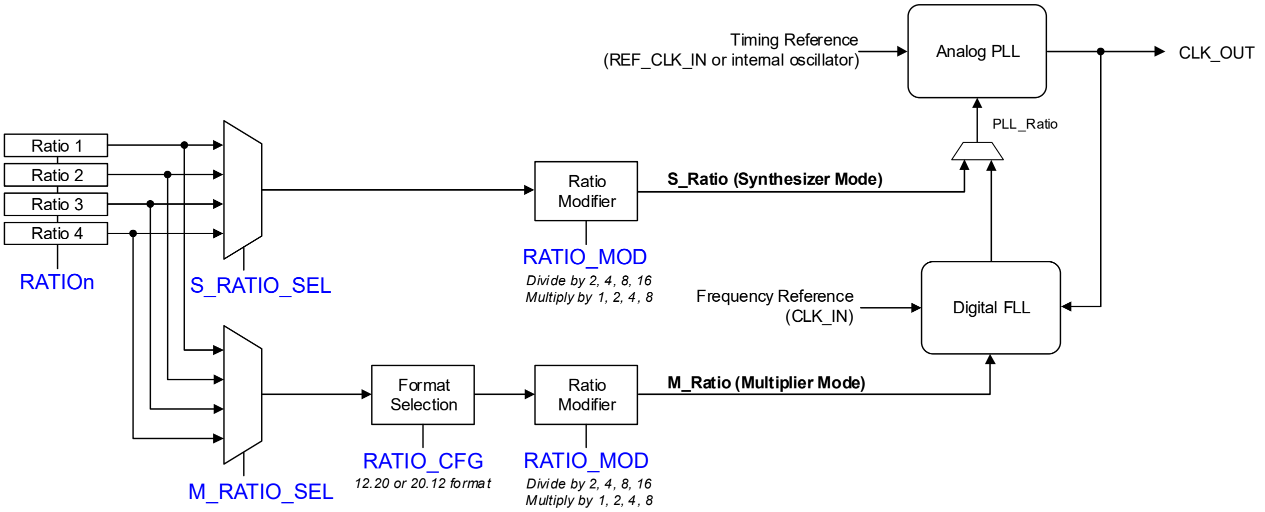


Figure 4-4. PLL Ratio Configuration

Notes: In Synthesizer Mode, the selected *S_Ratio* defines the CLK_OUT:REF_CLK_IN frequency ratio (or CLK_OUT:oscillator frequency ratio, if the oscillator is selected as the timing reference). The timing-reference divider (see Section 4.2) has no effect on this, and does not need to be considered when calculating the desired frequency ratio.

In Multiplier Mode, if automatic rate control (ARC) is enabled, the frequency ratio is configured automatically depending on the selected CLK_OUT frequency and the detected CLK_IN frequency. The RATIO_n and RATIO_MOD fields are not used if ARC is enabled. See Section 4.4.4 for details of the ARC function.

4.3.3 Mode Selection

The hybrid PLL architecture supports Multiplier Mode and Synthesizer Mode functions. The CS2600 can also be configured in Smart Multiplier Mode, with the ability to switch automatically between modes.

- In Multiplier Mode, the CLK_IN signal provides the frequency reference. The user-selected ratio defines the CLK_OUT:CLK_IN frequency ratio. The PLL is dynamically controlled to maintain the required output ratio.
- In Synthesizer Mode, the REF_CLK_IN signal provides the input reference. The user-selected ratio defines the CLK_OUT:REF_CLK_IN frequency ratio. The PLL is controlled using a static ratio derived from the respective control fields.
- In Smart Multiplier Mode, the CS2600 selects Multiplier Mode or Synthesizer Mode depending on the status of the CLK_IN frequency reference. The adaptive behavior can be used to accommodate periods where the frequency reference is unstable or not present.

The hybrid-PLL operating modes are illustrated in Fig. 4-5 and Fig. 4-6.

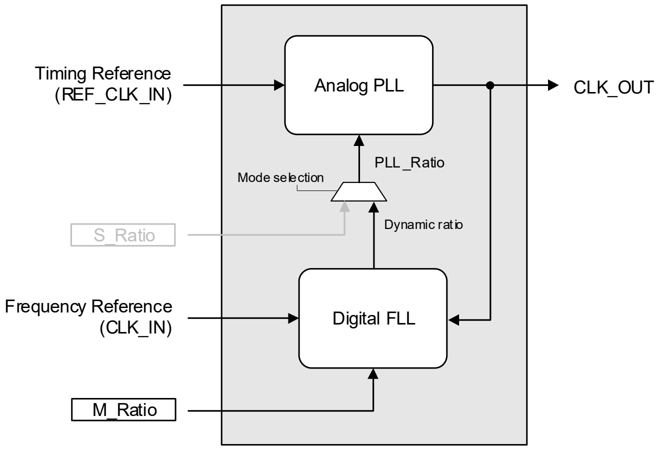


Figure 4-5. Multiplier Mode

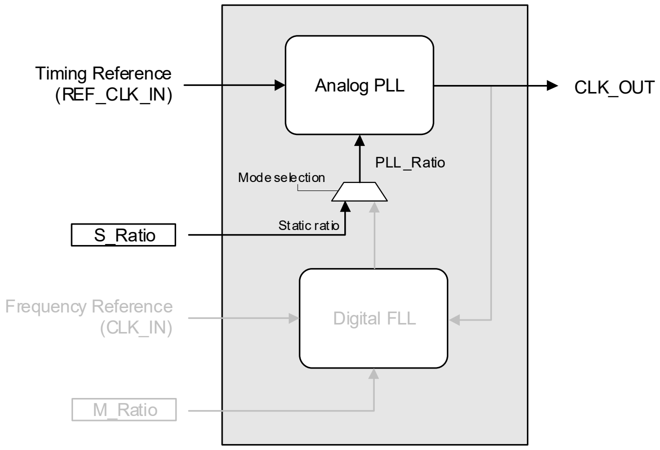


Figure 4-6. Synthesizer Mode

To select Synthesizer Mode or Multiplier Mode, the S_RATIO_SEL and M_RATIO_SEL fields must both be set to the same value. Under this condition, the operating mode is selected using PLL_MODE_SEL.

Smart Multiplier Mode is selected if S_RATIO_SEL and M_RATIO_SEL are set to different values. Under this condition, the operating mode is configured automatically.

In Smart Multiplier Mode, the device normally operates in Multiplier Mode. Synthesizer Mode may be used during PLL start-up, if CLK_IN is not present; the behavior is selectable using the ratio configuration fields.

- If the ratio selected by S_RATIO_SEL is zero, Synthesizer Mode is not valid. In this case, the clock output starts when a valid reference is present at CLK_IN; there is no clock output until CLK_IN is present. When CLK_IN is present, Multiplier Mode is enabled and is used thereafter, including if CLK_IN is subsequently interrupted.
- If the ratio selected by S_RATIO_SEL is nonzero, Synthesizer Mode is selected during PLL start-up, if CLK_IN is not present. When CLK_IN is present, the CS2600 makes a glitchless transition to Multiplier Mode and remains in this mode thereafter, including if CLK_IN is subsequently interrupted.

See Section 4.4 for further details of the CS2600 behavior when the CLK_IN input is missing or unstable.

4.4 Frequency Reference Configuration

The frequency reference (CLK_IN) is an input to the digital FLL, which is used to generate the dynamic ratio for the analog PLL. The digital FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required CLK_OUT frequency. The hybrid PLL/FLL architecture allows the low-jitter timing reference to be used to generate the clock output, while using a separate clock (CLK_IN) as a frequency reference. The frequency range for CLK_IN is defined in Table 3-4.

The CS2600 is tolerant of intermittent or unstable characteristics on the CLK_IN frequency reference. The behavior of the device is configurable as described in the following sections.

4.4.1 CLK_IN Detection and Indication

The CLK_IN signal is monitored to confirm the frequency reference is present and stable.

The CLK_IN presence is indicated using ERR_STS1. This bit is a latching bit—it is set when CLK_IN is not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if CLK_IN is not present.

The CLK_IN stability is indicated using ERR_STS2. This bit is a latching bit—it is set when CLK_IN is unstable or not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if CLK_IN is unstable or not present.

The CLK_IN status can be indicated on an auxiliary output pin as described in Section 4.6.

4.4.2 Holdover Mode

The CLK_IN signal is monitored to confirm the frequency reference is present and stable. The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. The holdover function is enabled automatically in Smart Multiplier Mode. See Section 4.3.3 to select Smart Multiplier Mode.

Notes: If Smart Multiplier Mode is selected, Synthesizer Mode may be used during PLL start-up, if CLK_IN is not present. The holdover function is not supported until a valid CLK_IN has been detected and the CS2600 automatically transitions to Multiplier Mode.

In Multiplier Mode (Smart Multiplier Mode not selected), the PLL remains unlocked indefinitely while CLK_IN is interrupted. When CLK_IN resumes, the PLL locks to CLK_IN and the valid CLK_OUT signal is restored.

If CLK_IN is missing or unstable, the CS2600 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK_OUT signal continues without any glitch or interruption.

When a valid CLK_IN is detected, the PLL resynchronizes to the frequency reference. If the frequency reference aligns with the previous CLK_IN frequency, the PLL remains locked and maintains a glitchless output.

4.4.3 Digital FLL Bandwidth

The bandwidth of the digital FLL can be configured to suit different operating conditions. The FLL bandwidth determines the extent to which any jitter on the CLK_IN signal is attenuated or is passed through to the output clocks. In some applications, it is desirable to reject all jitter as far as possible; in other applications, it may be preferable to preserve the low-frequency variations in the reference clock while attenuating jitter at higher frequencies.

The FLL bandwidth is configured using FLL_BW and FLL_BW_MOD. The FLL_BW field selects a value 1–128 Hz; the FLL_BW_MOD selects multiplication factor of ×1 or ×16. The combination of two fields allows bandwidth selections in the range 1–2048 Hz.

Notes: If the internal oscillator is used as the timing reference (see Section 4.2), or Smart Multiplier Mode is selected (see Section 4.3.3), the FLL bandwidth selection must be 16 Hz or greater.

The CS2600 automatically limits the FLL bandwidth to ensure optimal performance; the bandwidth is limited to a maximum of f_{CLK_IN} / 23.4 (rounded down to the nearest valid bandwidth selection).

The FLL bandwidth scales with the SYSCLK frequency; the nominal values selected using FLL_BW and FLL_BW_MOD are valid for 12 MHz SYSCLK.

A narrow bandwidth is typically recommended in applications where the CLK_OUT signal provides a new clock domain from which all other system clocks are derived. In these circumstances, the system benefits from maximum jitter rejection, as illustrated in Fig. 4-7.

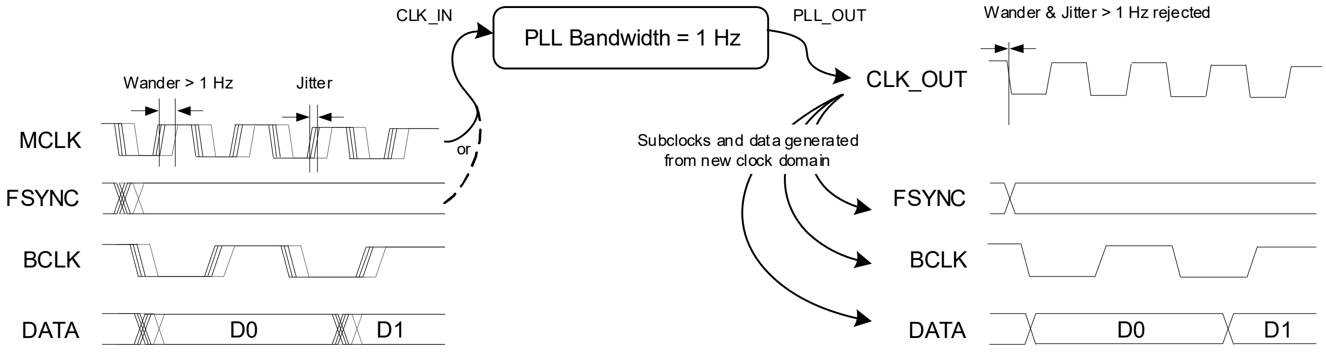


Figure 4-7. Narrow Bandwidth Application

A wide bandwidth is typically recommended in applications where some of the system clocks are referenced to CLK_OUT, while others are derived from CLK_IN. In these circumstances, it may be necessary to preserve some of the input reference variation in the clock output, in order to maintain phase alignment.

The FLL bandwidth should be set to the lowest setting that does not cause system-timing errors between the CLK_IN and CLK_OUT domains. The wide bandwidth use case is illustrated in Fig. 4-8.

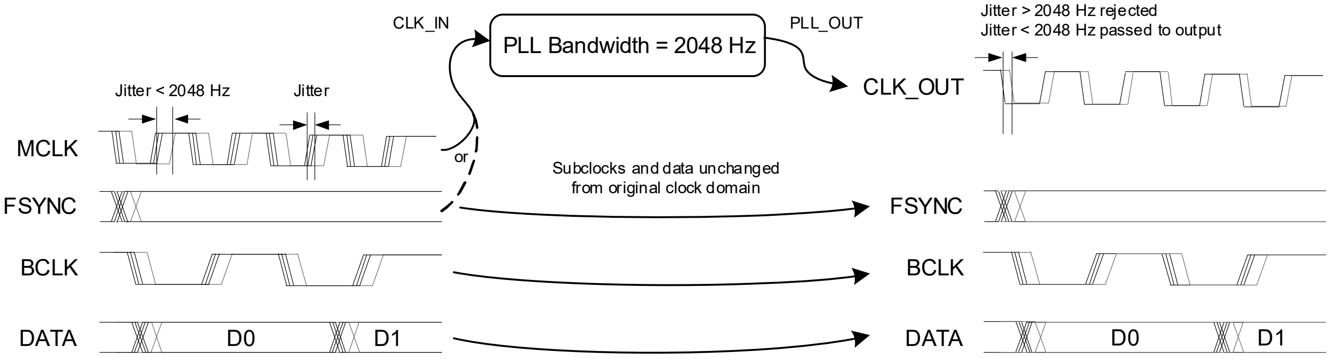

CLK_IN
PLL Bandwidth = 2048 Hz
PLL_OUT
Jitter > 2048 Hz rejected
Jitter < 2048 Hz passed to output
CLK_OUT
Jitter < 2048 Hz
Jitter
MCLK
or
Subclocks and data unchanged from original clock domain
FSYNC
FSYNC
BCLK
BCLK
DATA
D0
D1
DATA
D0
D1

Figure 4-8. Wide Bandwidth Application

4.4.4 Automatic Rate Control (ARC)

The CS2600 supports an automatic rate control (ARC) function which detects the CLK_IN reference frequency and configures the PLL multiplier ratio for the required PLL output frequency. Auto-detection is supported across a range of sample-rate frequencies typically used in digital audio systems.

The ARC supports seamless transitions through changes in the reference frequency. The BCLK and FSYNC outputs (see Section 4.5.2) are controlled automatically to accommodate changes in CLK_IN frequency.

Note: Automatic rate control is supported in Multiplier Mode only (see Section 4.3.3). If Synthesizer Mode is selected, ARC should be disabled at all times. If Smart Multiplier Mode is selected, and the ratio selected by S_RATIO_SEL is nonzero, ARC should be disabled at all times.

Automatic rate control is enabled using ARC_EN. If ARC is enabled, the CS2600 automatically detects the CLK_IN reference as one of the valid input frequencies. The PLL output frequency is configured using ARC_MCLK; the PLL output (MCLK) frequency follows the same base frequency as the input reference, as described in Table 4-1.

Table 4-1. ARC Configuration

CLK_IN Frequency	ARC_MCLK	PLL Output Frequency
32 kHz, 48 kHz, 96 kHz, or 192 kHz	00	12.288 MHz
	01	24.576 MHz
	10	49.152 MHz
	11	—
44.1 kHz, 88.2 kHz, or 176.4 kHz	00	11.2896 MHz
	01	22.5792 MHz
	10	45.1584 MHz
	11	—

The ARC automatically adjusts for changing CLK_IN reference frequencies. The input reference can be stopped and then restarted at the new frequency, or the input reference can change frequency without interruption.

Detection of a new CLK_IN frequency takes a maximum of 24 stable CLK_IN periods. The PLL remains locked provided the CLK_IN frequency transition is an exact integer ratio (increasing or decreasing). The PLL output is stable to within 0.1% during these transitions. In the case of 32–48 kHz transitions, an exact 1.5 ratio transition is also supported without losing PLL lock. For example, the PLL remains locked for 48.2–96.4 kHz transitions, or 48.3–32.2 kHz transitions; seamless operation is not assured for 48.2–96.0 kHz transitions, or 48.0–44.1 kHz transitions.

Note that, if the CLK_IN reference changes frequency without interruption, the new frequency must be established within five CLK_IN periods to ensure stable operation. If the input reference is stopped when changing frequency, the CS2600 must be configured in Smart Multiplier Mode (see Section 4.3.3) to ensure uninterrupted PLL operation.

If ARC is enabled, the FSYNC output is automatically configured to align with the CLK_IN reference frequency. The duty cycle is configured using FSYNC_DUTY_CYCLE.

If ARC is enabled, the BCLK output is configured using ARC_BCLK_DIV. The frequency can be configured as a ratio of the PLL output (MCLK) or else as a multiple of the FSYNC rate.

Note: BCLK output is only supported for valid divisions of the MCLK frequency (valid divisions of the MCLK frequency are defined by the BCLK_DIV field options). If the ratio calculated by the ARC is not supported, the output clocks are disabled. Normal operation resumes when a valid configuration is detected (due to register write or change in CLK_IN frequency).

An invalid configuration is indicated using ERR_STS6. This bit is a latching bit—it is set when an invalid configuration is detected and remains set until a 1 is written to the bit. Note the bit cannot be cleared if the configuration is invalid.

The CS2600 provides a glitchless transition following a change in CLK_IN frequency; the FSYNC and BCLK outputs are reconfigured seamlessly at the end of a FSYNC period.

4.5 Output Configuration

The CS2600 provides three clock outputs. The main output from the PLL is provided on the CLK_OUT pin. Two additional clock signals, BCLK_OUT and FSYNC_OUT, are derived from the main PLL output and are intended to support digital-audio applications.

The clock outputs are illustrated in Fig. 4-9.

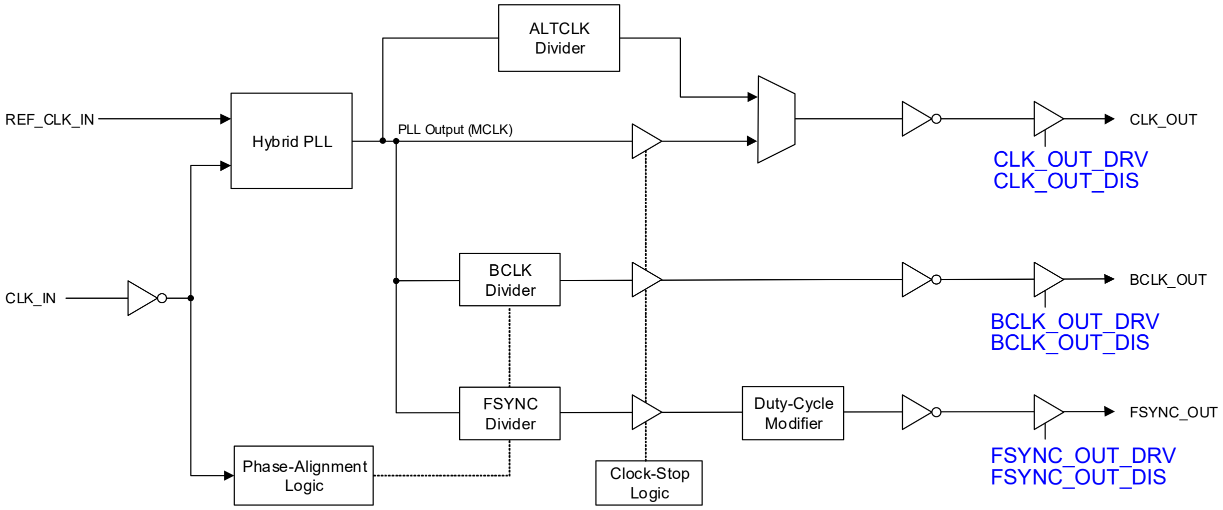


Figure 4-9. Clock Outputs

Each clock output can be enabled independently using the respective control field CLK_OUT_DIS, BCLK_OUT_DIS, or FSYNC_OUT_DIS. If an output is disabled, the respective driver is configured in a high-impedance (Hi-Z) state.

The drive strength for the clock outputs is configurable using the respective control field CLK_OUT_DRV, BCLK_OUT_DRV, or FSYNC_OUT_DRV.

4.5.1 CLK_OUT Configuration

The ALTCLK generator is an automatic divider that can be used to generate a fixed CLK_OUT frequency from a range of related PLL frequencies.

The CLK_OUT signal can be derived either directly from the PLL or else from the ALTCLK generator. The clock source is selected using CLK_OUT_SEL.

The polarity of the CLK_OUT signal can be inverted using CLK_OUT_INV. The inversion applies regardless of the CLK_OUT source, as shown in Fig. 4-10.

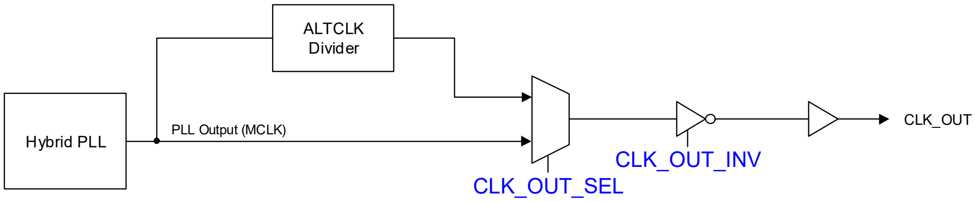


Figure 4-10. CLK_OUT Selection

If ALTCLK is selected as the clock source, the CLK_OUT frequency is generated as described in Table 4-2. Note that the PLL must be configured for one of the supported frequencies, using the applicable ratio in Multiplier or Synthesizer mode.

Table 4-2. CLK_OUT Frequency Select

PLL Frequency	CLK_OUT_SEL	CLK_OUT Frequency
Any	00	= PLL output
5.6448 MHz, 11.2896 MHz, 22.5792 MHz, or 45.1584 MHz	01	352.8 kHz
	10	1.882 MHz
	11	2.053 MHz
6.144 MHz, 12.288 MHz, 24.576 MHz, or 49.152 MHz	01	384 kHz
	10	2.048 MHz
	11	2.234 MHz

Notes:
- If CLK_OUT_SEL = 11, the PLL frequencies 5.6448 / 6.144 MHz are not supported
- If CLK_OUT_SEL = 11, the PLL frequencies 11.2896 / 12.288 MHz result in 45% output duty cycle

The ALTCLK generator is supported in Synthesizer Mode and Multiplier Mode. If the Holdover function is enabled (see Section 4.4.2) the PLL output is maintained under conditions where the reference is missing or unstable. Note that the clock-stop logic (see Section 4.5.4) does not affect the ALTCLK output.

4.5.2 BCLK and FSYNC Configuration

The CS2600 supports BCLK and FSYNC outputs, intended for use in digital-audio applications. These clock outputs are derived from the main PLL output (MCLK) using configurable dividers.

Note: The BCLK and FSYNC outputs are derived from the PLL output, regardless of whether ALTCLK is selected as the CLK_OUT source (see Section 4.5.1).

The BCLK and FSYNC outputs are shown in Fig. 4-11.

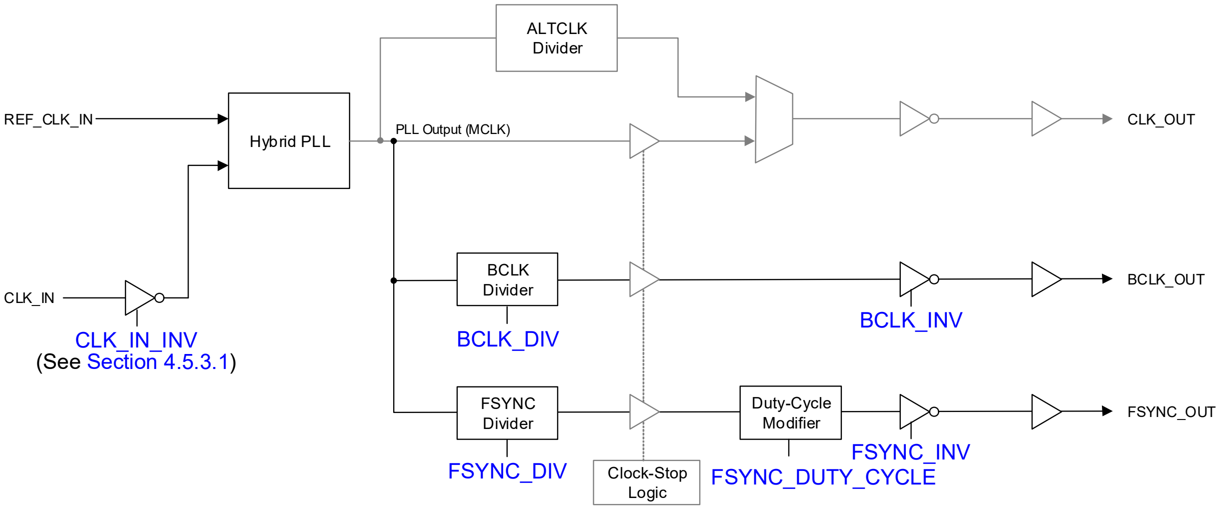


Figure 4-11. BCLK and FSYNC Outputs

The FSYNC frequency is configured using FSYNC_DIV. The frequency is defined as a ratio of the PLL output (MCLK). The duty cycle is configured using FSYNC_DUTY_CYCLE.

The BCLK frequency is configured using BCLK_DIV. Note that, for digital-audio applications, the BCLK frequency must be a valid integer multiple of the FSYNC frequency.

Note: If automatic rate control (ARC) is enabled, the BCLK frequency is configured using ARC_BCLK_DIV, and the FSYNC frequency is automatically aligned to the CLK_IN frequency reference. The BCLK_DIV and FSYNC_DIV fields are not used if ARC is enabled. See Section 4.4.4 for details of the ARC function.

The polarity of the BCLK and FSYNC outputs can be inverted using BCLK_INV and FSYNC_INV respectively. The polarity inversion can be used to support different digital-audio interface formats.

The recommended configuration for different digital-audio formats is defined in Table 4-3.

Table 4-3. Clock Configuration for Digital Audio Formats

Digital Audio Format	BCLK_INV	FSYNC_INV	FSYNC_DUTY_CYCLE
I2S	1 (inverted)	1 (inverted)	000 (50% duty cycle)
Left-Justified/Right-Justified	1 (inverted)	0 (not inverted)	000 (50% duty cycle)
TDM	1 (inverted)	0 (not inverted)	As required [1]

[1] Note the FSYNC duty cycle must be configured less than or equal to 50%.

Typical clock signals for different digital-audio formats are illustrated in Fig. 4-12 through Fig. 4-14.

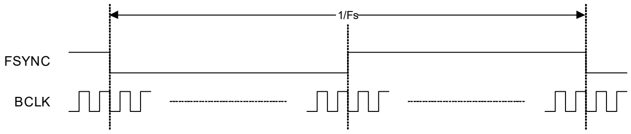


Figure 4-12. I2S Format

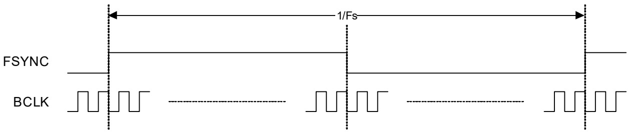


Figure 4-13. Left/Right Justified Format

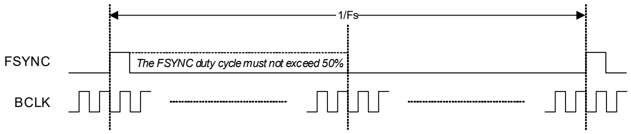


Figure 4-14. TDM Format

4.5.3 Phase Alignment

The phase-alignment function can be used to ensure the BCLK and FSYNC outputs are phase-aligned to the CLK_IN frequency reference. The function can be triggered manually using a control-register write, or automatically based on a configurable phase-offset threshold.

Phase alignment is enabled using PHASE_ALIGNMENT_EN. If this bit is set, the CS2600 monitors the phase offset between the FSYNC output and CLK_IN reference. For correct operation, the CLK_IN frequency must be less than 1 MHz, and the FSYNC frequency must be equal to, or an integer multiple of, CLK_IN frequency.

Phase alignment supports automatic or manual triggering; the applicable behavior is selected using PHASE_ALIGNMENT_MODE.

- If manual trigger is selected, the phase-alignment process is triggered by writing 1 to PHASE_ALIGNMENT_TRIG.
- If automatic trigger is selected, the phase-alignment process is triggered whenever the detected phase offset between CLK_IN and FSYNC exceeds the threshold configured using PHASE_ALIGNMENT_THR.

  An optional phase-stability monitor can also be used to gate the automatic phase-alignment process. If PHASE_ALIGNMENT_STB_EN is set, the phase stability is analyzed, and the phase alignment is only implemented if the phase offset is stable. Enabling the phase-stability monitor allows a lower phase-alignment threshold to be configured without erroneous trigger conditions.

Note that phase alignment is only supported if the PLL is frequency locked. If the trigger condition (manual or automatic) is detected and the PLL is not locked, the trigger is queued until frequency lock is achieved—phase alignment is applied after the PLL frequency-unlock indicator (F_UNLOCK) is cleared.

If a valid trigger condition is detected, the phase of the FSYNC and BCLK outputs is adjusted in order to restore the phase alignment. The phase is adjusted by extending the FSYNC clock period by a fixed amount, and maintaining this extended period until the phase offset is corrected. The maximum permitted extension of the FSYNC clock period is selected using PHASE_ALIGNMENT_SPEED; this controls how quickly the phase adjustment is implemented.

Note that, once the phase-alignment process has started, it runs to completion based on the initial phase-offset measurement, regardless of any subsequent changes in the CLK_IN phase. If the phase offset on completion exceeds the automatic-trigger threshold, or a new manual trigger is applied, the process starts again.

Additional guidance on configuring the phase-alignment function is provided in Section 5.2.

The phase-alignment process is illustrated in Fig. 4-15.

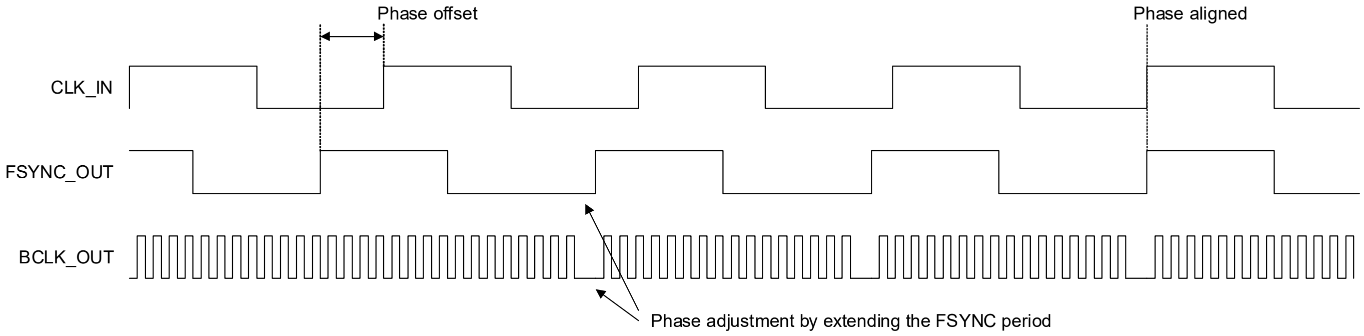


Figure 4-15. Phase Alignment

4.5.3.1 CLK_IN Phase Selection

Phase alignment ensures the start of an FSYNC period aligns with a transition of the CLK_IN signal. (Note that not every FSYNC period aligns with a CLK_IN transition—this depends upon the ratio of the two frequencies.)

The FSYNC period starts on a rising edge (FSYNC_INV = 0) or falling edge (FSYNC_INV = 1). The FSYNC period is aligned to a rising or falling CLK_IN transition as follows:

- If CLK_IN_INV = 0, the FSYNC period aligns with a rising CLK_IN edge.
- If CLK_IN_INV = 1, the FSYNC period aligns with a falling CLK_IN edge.

Note that, for each of the typical digital-audio formats described in Table 4-3, the CLK_IN_INV bit should be set to the same value as FSYNC_INV.

4.5.3.2 Phase Alignment Indication

The phase-alignment status is indicated using P_UNLOCK. This bit is set if the phase offset between FSYNC and CLK_IN exceeds the automatic-trigger threshold (including if the PLL is disabled or is not frequency locked). The bit is also set if the phase alignment is in progress (i.e., triggered but not yet complete). The phase-alignment status can be indicated on an auxiliary output pin as described in Section 4.6. The status can be used to automatically disable the clock outputs—see Section 4.5.4 for further details.

The phase-alignment status is also indicated using P_UNLOCK_STICKY. This is a latching bit—it is set when P_UNLOCK is set, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if P_UNLOCK is set.

4.5.4 Clock-Stop Logic

The clock output signals are valid if the PLL is enabled and locked. The clock signals are not valid if the PLL is not locked. If phase alignment is important for the target application, the clock signals may be considered invalid if the phase offset exceeds the required tolerance.

To avoid spurious clock generation, the OUT_GATE bit can be used to stop the outputs whenever the PLL is not locked. If OUT_GATE = 0, the clock outputs are stopped automatically if they are not valid. The OUT_GATE_TYPE field selects the logic condition used to determine whether the outputs are valid.

- If OUT_GATE_TYPE = 10, the clock outputs are gated by the analog-PLL lock status. The outputs are enabled if the analog PLL is locked to the timing reference.
- If OUT_GATE_TYPE = 00, the clock outputs are gated by the PLL frequency-lock status (F_UNLOCK). The outputs are enabled if the hybrid PLL (analog PLL and digital FLL) is frequency locked.

  Note that, if the FLL is not used (e.g., in Synthesizer Mode), the outputs are gated by the analog-PLL lock status.
- If OUT_GATE_TYPE = 01, the clock outputs are gated by the PLL phase-alignment status (P_UNLOCK). The outputs are enabled if the hybrid PLL is frequency locked and phase aligned with the frequency reference.

  Note that, if phase alignment is disabled, the outputs are gated by the frequency-lock status.

If the clock outputs are stopped as a result of the PLL lock or phase-alignment status, the CS2600 controls the signals to ensure there are no partial clock periods—the outputs are stopped at the end of a complete FSYNC period.

Notes: By default, the FSYNC period starts on a rising edge of the FSYNC signal. If FSYNC is inverted (FSYNC_INV = 1), the FSYNC period starts on a falling edge of FSYNC.

If the BCLK rate is a non-integer division of the FSYNC rate, the outputs are stopped at the end of a complete FSYNC frame that coincides with a BCLK edge.

The stopped clocks are Logic 0 if non-inverted, or Logic 1 if inverted. See Section 4.5.1 and Section 4.5.2 to invert the respective clock outputs.

The CS2600 maintains the timing of the FSYNC periods while the clocks are stopped. The timing is referenced to the CLK_IN signal prior to the clock-stop condition occurring. When the applicable conditions (see OUT_GATE_TYPE) allow the clocks to be enabled, the clocks resume at the start of the next FSYNC period.

The clock-stop timing is illustrated in Fig. 4-16. In the example shown FSYNC is noninverted, BCLK is inverted.

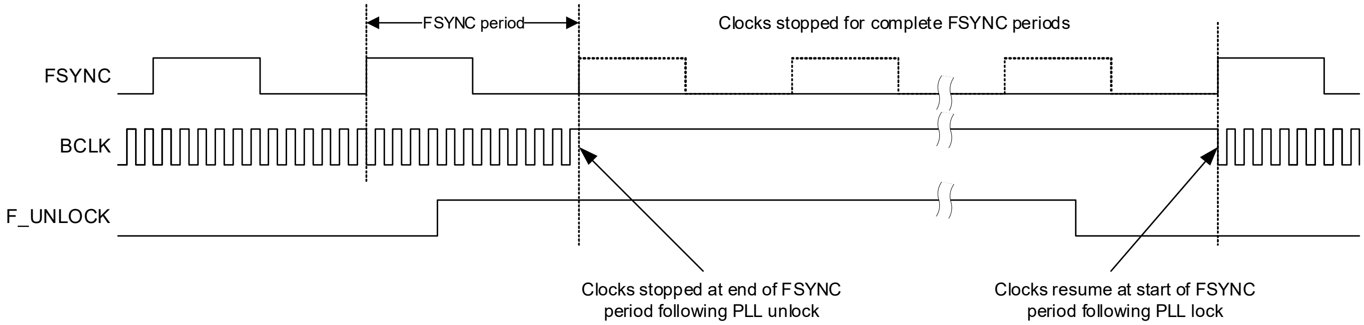

FSYNC period
Clocks stopped for complete FSYNC periods
FSYNC
BCLK
F_UNLOCK
Clocks stopped at end of FSYNC period following PLL unlock
Clocks resume at start of FSYNC period following PLL lock

Figure 4-16. Clock-Stop Timing

If the PLL is disabled, the clock outputs are stopped immediately; the stopped CLK_OUT, FSYNC_OUT, and BCLK_OUT signals can be either Logic 0 or Logic 1. Note that the clock outputs are initialized during PLL enable (Logic 0 if non-inverted, or Logic 1 if inverted), prior to starting the clock output; the timing is controlled to ensure there are no partial clock periods.

The clock-output logic is described in Table 4-4. The CLK_OUT, FSYNC_OUT, and BCLK_OUT clocks are configured using the respective control fields.

Table 4-4. Clock Output Logic—CLK_OUT, FSYNC_OUT, BCLK_OUT

x_OUT_DIS	PLL Enable	OUT_GATE	OUT_GATE_TYPE	F_UNLOCK	P_UNLOCK	APLL unlock Status	x_OUT_INV	x_OUT pin
1	—	—	—	—	—	—	—	Hi-Z
0	Disabled	—	—	—	—	—	—	0 or 1
	Enabled	0	00	0	—	—	—	Clock output
				1	—	—	0	0
							1	1
			01	—	0	—	—	Clock output
				—	1	—	0	0
							1	1
			10	—	—	Locked	—	Clock output
				—	—	Unlocked	0	0
							1	1
		1	—	—	—	—	—	Clock output

Notes:
- If the clocks are stopped due to PLL frequency/phase unlock, the clocks are stopped at the end of the FSYNC period.
- The CLK_OUT signal is not affected by the clock-stop logic if ALTCLK is selected as the clock source.

4.6 Auxiliary Output

The CS2600 supports two auxiliary outputs with selectable functionality. The AUX1_OUT pin can be configured as a clock or status output using AUX1_OUT_SEL. The supported functions for the AUX1 output are:

- Timing reference clock (REF_CLK_IN or internal oscillator)
- Frequency reference clock (CLK_IN)
- Output clock (CLK_OUT)
- PLL frequency-lock status (asserted if PLL is not frequency locked)
- Phase-alignment status (asserted if phase alignment is not locked)
- BCLK
- FSYNC
- Frequency reference (CLK_IN) status (asserted if CLK_IN is not present)

The second auxiliary output is supported on the SPI_SDO/AUX2_OUT/CONFIG5 pin. The AUX2_OUT function is enabled and configured using AUX2_OUT_SEL. The supported functions for the AUX2 output are:

- PLL frequency-lock status (asserted if PLL is not frequency locked)
- Phase-alignment status (asserted if phase alignment is not locked)
- Frequency reference (CLK_IN) status (asserted if CLK_IN is not present)

Note: If the AUX2_OUT function is enabled, the SPI_SDO function is not supported. In this configuration, the SPI interface supports write operations only.

A glitchless transition is provided if the auxiliary output is switched between the timing reference and CLK_OUT, ensuring there are no partial clock periods in the output signal. The glitchless transition is illustrated in Fig. 4-17.

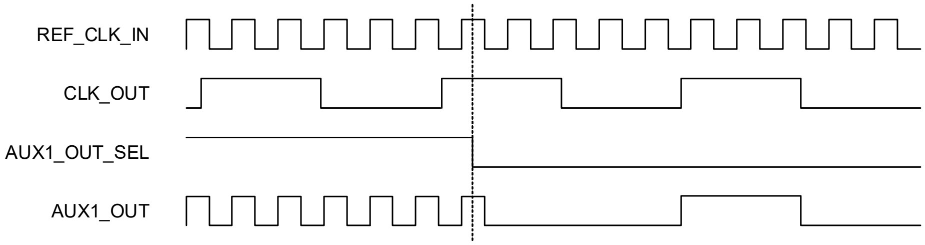


Figure 4-17. Glitchless Transition between Clock Signals

If an auxiliary output is configured as an unlock or clock-missing status, the respective output driver can be configured as either CMOS (active high) or open drain (active low). The output drivers are configured using AUX_OUT_CFG.

Note: If the auxiliary output is configured as a clock output, the output driver is CMOS in all cases.

The AUX1 output driver can be enabled using AUX1_OUT_DIS. If the AUX1 output is disabled, the driver is configured in a high-impedance (Hi-Z) state. The AUX1 drive strength is configurable using AUX1_OUT_DRV.

Note: The AUX1_OUT_DIS field must not be updated at the same time as AUX1_OUT_SEL (at the same register address). To update both fields, a separate control-interface transaction must be scheduled for each bit.

The auxiliary outputs are illustrated in Fig. 4-18.

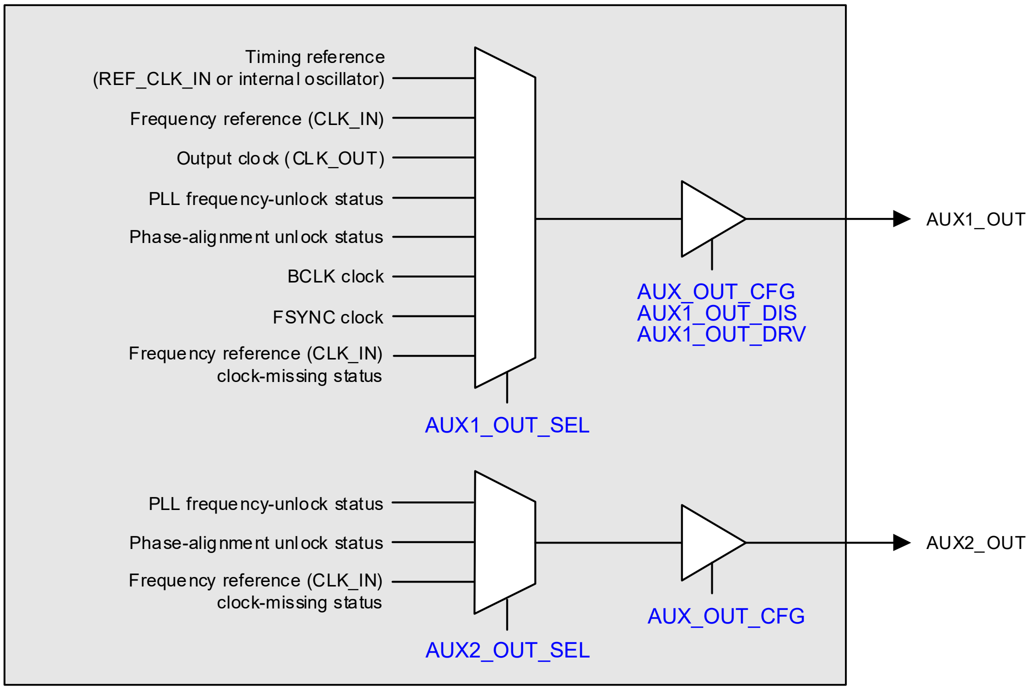

Timing reference
(REF_CLK_IN or internal oscillator)
Frequency reference (CLK_IN)
Output clock (CLK_OUT)
PLL frequency-unlock status
Phase-alignment unlock status
BCLK clock
FSYNC clock
Frequency reference (CLK_IN)
clock-missing status
AUX1_OUT_SEL
AUX_OUT_CFG
AUX1_OUT_DIS
AUX1_OUT_DRV
AUX1_OUT
PLL frequency-unlock status
Phase-alignment unlock status
Frequency reference (CLK_IN)
clock-missing status
AUX2_OUT_SEL
AUX_OUT_CFG
AUX2_OUT

Figure 4-18. Auxiliary Output Configuration

4.7 I2C/SPI Control Port

The CS2600 incorporates a control port, supporting I2C or SPI modes of operation. In Software Control Mode, the CS2600 is configured by writing to control registers using the control port.

The control port is configured in I2C mode or SPI mode using the I2C_ADDR/ $\overline{\text{SPI\_CS}}$ pin.

- I2C mode is selected by connecting the I2C_ADDR/ $\overline{\text{SPI\_CS}}$ pin to VDD or GND using a pull-up or pull-down resistor. The pin connection is used to select the target address on the I2C bus.
- SPI mode is selected by a high-to-low transition on the I2C_ADDR/$\overline{\text{SPI\_CS}}$ pin after power-on.

4.7.1 I2C Interface

The I2C control port is supported using the I2C_SCL and I2C_SDA pins.

The CS2600 is a target device on the I2C bus—SCL is a clock input, SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS2600 transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit target address (this is not the same as the address of each register in the register map). Note that the LSB of the target address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I2C target address is configured using the I2C_ADDR/$\overline{\text{SPI\_CS}}$ pin as described in Table 4-5.

Table 4-5. I2C Target Address Selection

I2C_ADDR Pin Connection		I2C Address
Pull-up to VDD	0 Ω	0x5E (write), 0x5F (read)
	4.7 kΩ	0x5C (write), 0x5D (read)
	22 kΩ	0x5A (write), 0x5B (read)
	100 kΩ	0x58 (write), 0x59 (read)
Pull-down to GND	100 kΩ	0x56 (write), 0x57 (read)
	22 kΩ	0x54 (write), 0x55 (read)
	4.7 kΩ	0x52 (write), 0x53 (read)
	0 Ω	0x50 (write), 0x51 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS2600 responds to the start condition and shifts in the next eight bits on SDA (8-bit target address, including read/write bit, MSB first). If the target address received matches the target address of The CS2600, it responds by pulling SDA low on the next clock pulse (ACK). If the target address is not recognized, the CS2600 returns to the idle condition and waits for a new start condition.

If the target address matches the target address of the CS2600, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence, the CS2600 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

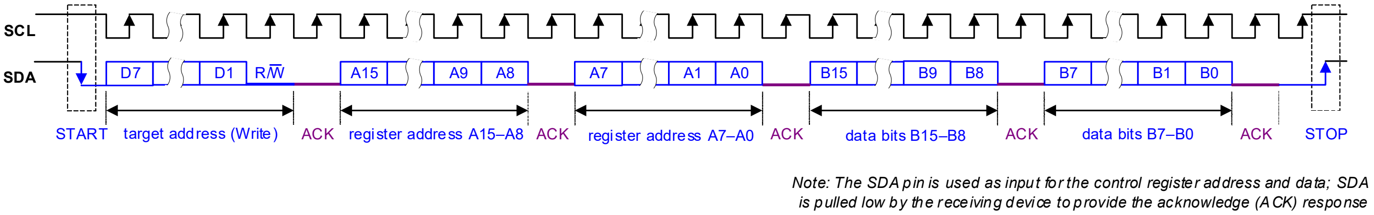
The I2C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). Note that the full I2C message protocol also includes a target address, a read/write bit, and other signaling bits (see Fig. 4-19 and Fig. 4-20).

The CS2600 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS2600 automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

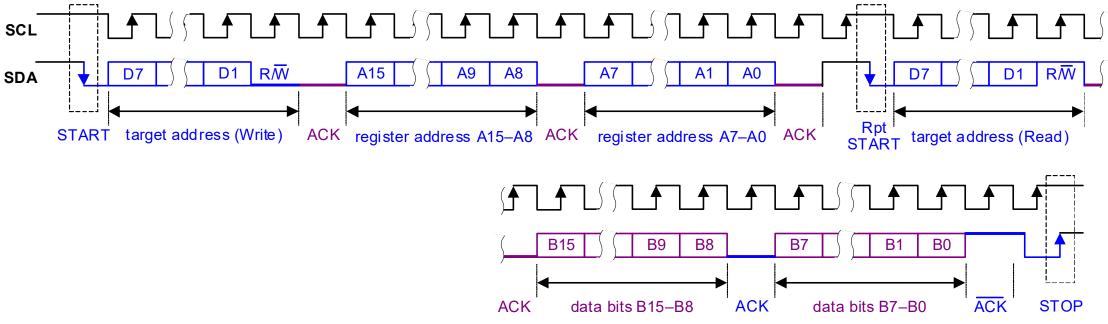
The I2C protocol for a single, 16-bit register write operation is shown in Fig. 4-19.



Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response

Figure 4-19. Control Interface I2C Register Write

The I2C protocol for a single, 16-bit register read operation is shown in Fig. 4-20.



Note: The SDA pin is driven by both the controller and target devices in turn to transfer target address, register address, data and ACK responses

Figure 4-20. Control Interface I2C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-21 through Fig. 4-24. The terminology used in the following figures is detailed in Table 4-6.

Table 4-6. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS2600
[Gray field]	Data from CS2600 to bus controller

Fig. 4-21 shows a single register write to a specified address.

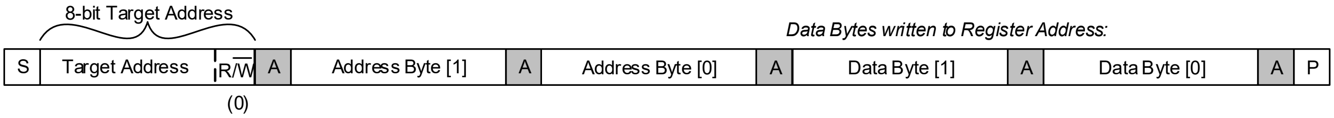


Figure 4-21. Single-Register Write to Specified Address

Fig. 4-22 shows a single register read from a specified address.

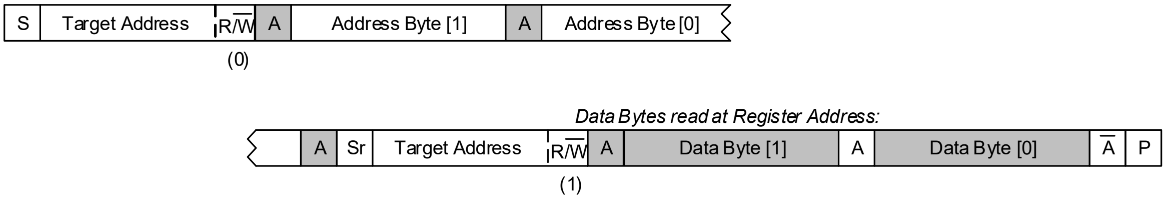


Figure 4-22. Single-Register Read from Specified Address

Fig. 4-23 shows a multiple register write to a specified address.

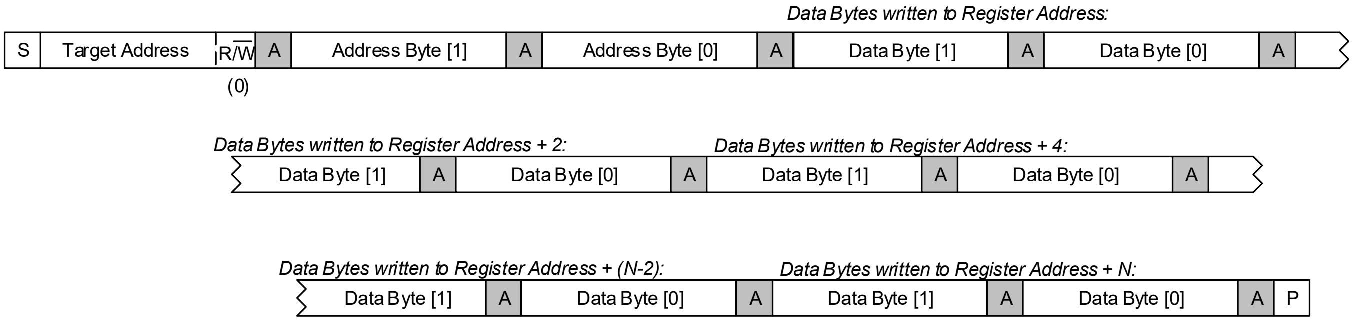

Data Bytes written to Register Address:
S
Target Address
R/$\overline{W}$
(0)
A
Address Byte [1]
Address Byte [0]
Data Byte [1]
Data Byte [0]
Data Bytes written to Register Address + 2:
Data Bytes written to Register Address + 4:
Data Bytes written to Register Address + (N-2):
Data Bytes written to Register Address + N:
P

Figure 4-23. Multiple-Register Write to Specified Address

Fig. 4-24 shows a multiple register read from a specified address.

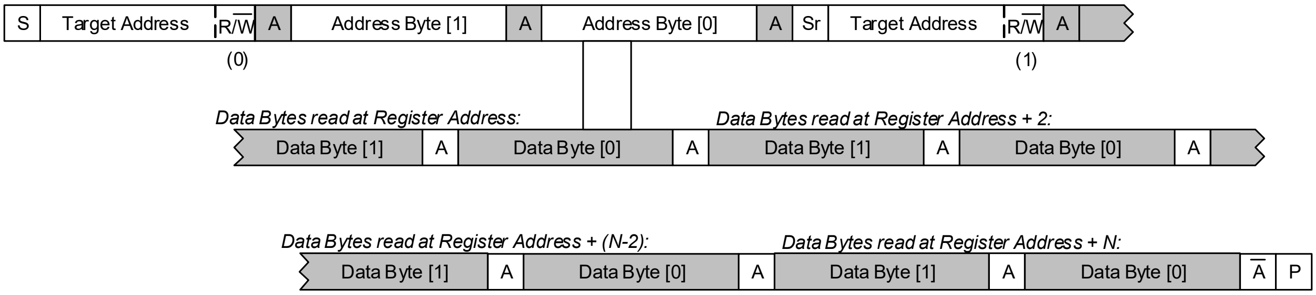

S
Target Address
R/$\overline{W}$
(0)
A
Address Byte [1]
Address Byte [0]
Sr
(1)
Data Bytes read at Register Address:
Data Bytes read at Register Address + 2:
Data Byte [1]
Data Byte [0]
Data Bytes read at Register Address + (N-2):
Data Bytes read at Register Address + N:
$\overline{A}$
P

Figure 4-24. Multiple-Register Read from Specified Address

4.7.2 SPI Interface

The SPI interface is supported using the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins.

The $\overline{\text{SPI\_CS}}$ pin provides the chip-select input (active low). Data is clocked in/out on the rising edge of SPI_SCK.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-6 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. Note that the full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-25 and Fig. 4-26).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS2600 automatically increments the register address at the end of each data word, for as long as $\overline{\text{CS}}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

Fig. 4-25 shows a single register write to a specified address.

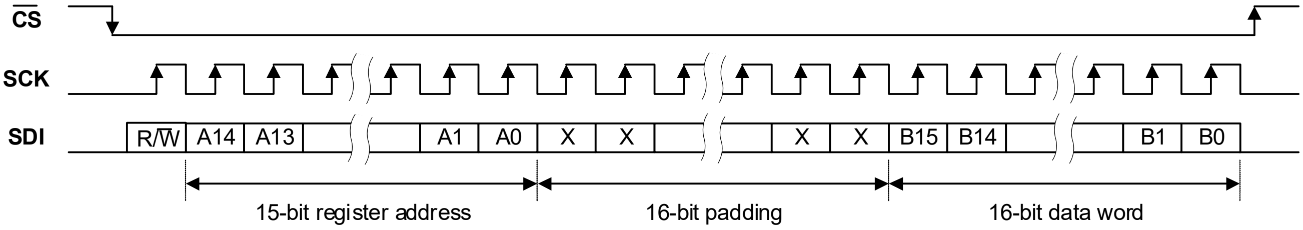


Figure 4-25. Control Interface SPI Register Write

Fig. 4-26 shows a single register read from a specified address.

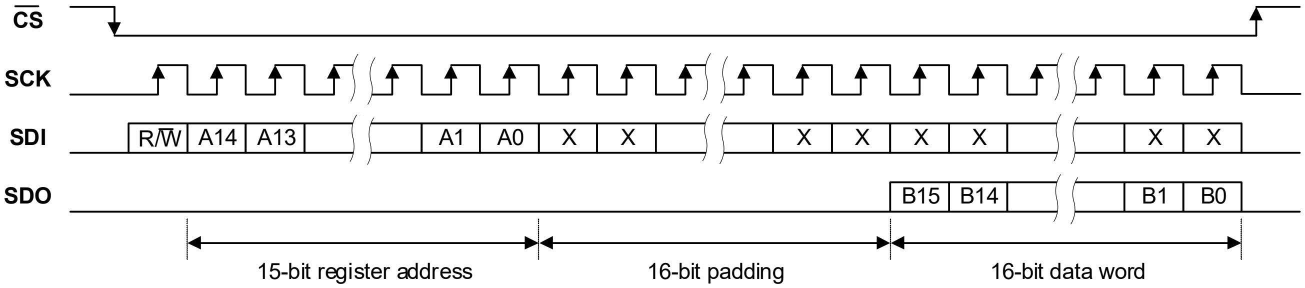


Figure 4-26. Control Interface SPI Register Read

4.7.3 Device Configuration

The device should be fully configured before enabling the PLL. When changing any register settings, it is recommended to disable the PLL, update the registers, then enable the PLL; this ensures there is no unintended behavior.

See Section 4.3.1 to enable and disable the PLL. Specific restrictions and exceptions on updating register fields are described in Section 4.7.3.2.

4.7.3.1 Freezable Fields

The register map supports a number of freezable fields, as listed in Table 4-7. If FREEZE_EN is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until FREEZE_EN is cleared. When FREEZE_EN is cleared, all of the frozen fields become active simultaneously.

Note: The FREEZE_EN bit should not be updated in the same write transaction as the freezable fields PLL_MODE_SEL or M_RATIO_SEL at the same register address. Separate write transactions should be used to ensure the correct sequencing of the freeze function.

Table 4-7. Freezable Fields

Address	Fields
0x0002	CLK_OUT_DIS, AUX1_OUT_DIS, S_RATIO_SEL, RATIO_MOD
0x0004	PLL_MODE_SEL, M_RATIO_SEL
0x0100	FSYNC_OUT_DIS, BCLK_OUT_DIS
0x0102	AUX1_OUT_SEL

4.7.3.2 Field Update Restrictions

The fields listed in Table 4-8 can be configured at any time, and do not result in any partial clock period in the outputs.

Table 4-8. Register Fields with No Write Restrictions

Address	Fields
0x0002	CLK_OUT_DIS, AUX1_OUT_DIS [1], PLL_EN1
0x0004	PLL_EN2, FREEZE_EN
0x0100	FSYNC_OUT_DIS, BCLK_OUT_DIS
0x0102	AUX1_OUT_SEL
0x0114	F_UNLOCK_STICKY, P_UNLOCK_STICKY
0x0116	ERR_STS1–ERR_STS8
0x0120	OTP_LDO_EN, OTP_LDO_DISCH_EN, OTP_VDD_EN
0x1104	USER_KEY
0x2340–0x236E	OTP_IMG_WR_BYTE1–OTP_IMG_WR_BYTE48
0x2400	OTP_PROG_EN

[1] Note the AUX1_OUT_DIS field must not be updated at the same time as AUX1_OUT_SEL. See Section 4.6.

The fields listed in Table 4-9 can be configured at any time, but may cause the PLL to lose lock temporarily.

Table 4-9. Register Fields with Restrictions

Address	Fields
0x0002	S_RATIO_SEL [1], RATIO_MOD
0x0004	PLL_MODE_SEL, M_RATIO_SEL [1]
0x0006–0x0008	RATIO1_1, RATIO1_2
0x000A–0x000C	RATIO2_1, RATIO2_2
0x000E–0x0010	RATIO3_1, RATIO3_2
0x0012–0x0014	RATIO4_1, RATIO4_2
0x0016	REF_CLK_IN_DIV, RATIO_CFG

[1] The S_RATIO_SEL and M_RATIO_SEL fields can be configured at any time, provided the respective field values differ from each other before the update and after the update. In all other cases, the PLL should be disabled before writing to either of these fields.

Note that, for all other control fields (not listed in Table 4-8 or Table 4-9), the PLL should be disabled before reconfiguring; failure to do so may result in unintended behavior, and may require a software reset to restart the device.

4.7.4 Software Reset

A software reset is triggered by writing 0x5A to the SW_RST field. A software reset causes all of the CS2600 control registers to be reset to their default states.

4.7.5 Power-On Reset

The power-on reset (POR) sequence is scheduled on initial power-up, and following any interruption to the VDD supply. The POR causes all of the CS2600 control registers to be reset to their default states.

4.8 One-Time Programmable (OTP) Memory

The CS2600 incorporates a customer-programmable OTP memory which can be used to automatically configure the device after power-up. The OTP memory enables the device to be factory programmed for a specific target application, removing the need for a host system to configure the device.

The OTP memory is programmed using the I^{2}C or SPI interface. The CS2600 supports two different OTP programming methods, for production and prototyping respectively. A device may be programmed using either method, but not both.

- Production programming ensures data integrity using an error correction code (ECC) algorithm.
- Prototype programming provides greater flexibility to reprogram the device during product development.

Note that the OTP memory contents have no effect if the CS2600 is used in Hardware Control Mode.

4.8.1 OTP Programming Supply

An OTP programming supply (VDD_OTP) is required when writing to the OTP memory. The programming supply may be provided internally or externally, depending on the system supply (VDD).

- If the VDD supply is 3.3 V, the programming supply can be provided using an internal LDO regulator; in this case, the output of the regulator, VLDO_OTP, should be connected to VDD_OTP.
- If the VDD supply is 1.8 V, the programming supply must be provided externally.

The external connections for the OTP programming supply are shown in Fig. 2-1.

Note: VDD must be present before enabling the VDD_OTP pin. The external VDD_OTP supply must be removed before powering down VDD.

4.8.2 Production Programming

Production programming is implemented using an image that defines the required settings of all the configurable registers. The image is generated using SoundClear Studio (SCS).

The image includes an ID field (1–7) and an error correction code (ECC) field. The ECC supports 3-bit error detection and 2-bit error correction.

The programmed contents of the OTP memory are loaded during startup. If the OTP memory contains an uncorrectable error, the clock outputs are disabled and the device startup is aborted. An OTP error is indicated using ERR_STS7.

The OTP memory can be programmed up to seven times. Each time the OTP memory is programmed, the previous images are automatically superseded.

4.8.3 Prototype Programming

Prototype programming is used to fine-tune the device settings for a specific application. The prototype programming configures selected fields only, with all other fields initializing to their respective default values.

Prototype programming is configured using SoundClear Studio (SCS). The programmed contents of the OTP memory are loaded during startup. Note there is no error checking when using the prototype programming option.

Iterative programming is supported, with modified values defined for specific fields. If a field is programmed multiple times in the OTP memory, the most recent programmed value is applied during startup.

The OTP memory can be programmed multiple times. The programming limit depends on which parameters are being configured. As an example, however, it is possible to program and modify the PLL ratio more than 25 times.

4.9 Hardware Control Mode

The CS2600 supports hardware and software control modes. In Hardware Control Mode, the device configuration is determined by external resistors connected to the hardware-control pins, CONFIG1–CONFIG6. The external resistors are connected to GND or VDD; different resistor values allow the CS2600 to detect eight configuration options per pin. Note that the external resistance must be within 5% of the specified value.

Hardware Control Mode is selected using an external resistor connected to CONFIG1. In Hardware Control Mode, the PLL is enabled in Synthesizer Mode or Multiplier Mode as specified in Table 4-11. Software Control Mode (I^{2}C/SPI) is selected by connecting CONFIG1 to GND.

In Hardware Control Mode, the device configuration is latched during the power-up sequence and cannot be changed while the device is operational. To update the device configuration, the device must be power cycled in order to read new settings on the CONFIGx pins.

If an invalid hardware configuration is selected, the clock outputs are disabled. Normal operation resumes when a valid configuration is detected. Note that a valid configuration may depend on the external clocks (e.g., CLK_IN frequency).

The CONFIG pins provide control over a subset of the overall device functionality. For the remaining functions, the respective default settings are applied. A summary of the CONFIG pin functions is shown in Table 4-10.

Table 4-10. CONFIG Pin Summary

CONFIG Pin	Description
CONFIG1	PLL Operating Mode and Timing Clock Reference
CONFIG2	Holdover Mode, PLL bandwidth, and AUX1 output
CONFIG3	Clock output
CONFIG4	BCLK frequency
CONFIG5	Automatic Rate Control and FSYNC frequency
CONFIG6	CLK_OUT frequency

The CONFIG1 pin selects the PLL operating mode and the timing-reference clock frequency as shown in Table 4-11.

Table 4-11. CONFIG1 Hardware Configuration

Pin Configuration		Operating Mode	Timing Reference Frequency [1]
Pull-up to VDD	0 Ω	Synthesizer	10 MHz
	4.7 kΩ		25 MHz
	22 kΩ		24.576 MHz
	100 kΩ		49.152 MHz
Pull-down to GND	100 kΩ	Multiplier	8–18 MHz
	22 kΩ		16–37.5 MHz
	4.7 kΩ		32–75 MHz
	0 Ω	Software Control Mode (I^{2}C/SPI)	

[1] The timing reference can be REF_CLK_IN, external crystal oscillator (XTAL_IN), or the internal oscillator (LCO). In Hardware Mode, the internal oscillator is supported for Multiplier Mode only.

In Multiplier Mode, the remaining CONFIGx pin functions are described in Section 4.9.1.

In Synthesizer Mode, the remaining CONFIGx pin functions are described in Section 4.9.2.

4.9.1 Multiplier Mode

The CONFIG2 pin selects Holdover Mode, PLL bandwidth, and the AUX1_OUT function as shown in Table 4-12.

Table 4-12. CONFIG2 Hardware Configuration—Multiplier Mode

Pin Configuration		Holdover Mode	PLL Bandwidth	AUX1 Output
Pull-up to VDD	0 Ω	Enabled	1 Hz	Frequency Unlock Indicator
	4.7 kΩ			Phase Unlock Indicator
	22 kΩ		128 Hz	Frequency Unlock Indicator
	100 kΩ			Phase Unlock Indicator
Pull-down to GND	100 kΩ	Disabled	1 Hz	Phase Unlock Indicator
	22 kΩ			Frequency Unlock Indicator
	4.7 kΩ		128 Hz	Phase Unlock Indicator
	0 Ω			Frequency Unlock Indicator

The CONFIG3 pin selects the clock output configuration as shown in Table 4-13. The supported configurations are designed for target applications using I^{2}S, LJ/RJ, or TDM serial data interfaces.

Table 4-13. CONFIG3 Hardware Configuration—Multiplier Mode

Pin Configuration		Phase Alignment	Target Application	Input/Output Configuration		
				CLK_IN	BCLK_OUT	FSYNC_OUT [1]
Pull-up to VDD	0 Ω	Enabled	I^{2}S	Inverted	Inverted	
	4.7 kΩ		LJ/RJ	Not Inverted	Inverted	Not Inverted
	22 kΩ		TDM–A [2]			
	100 kΩ		TDM–B [2]			
Pull-down to GND	100 kΩ	Disabled	I^{2}S		Inverted	
	22 kΩ		LJ/RJ		Inverted	Not Inverted
	4.7 kΩ		TDM–A [2]			
	0 Ω		TDM–B [2]			

[1] In TDM applications, the FSYNC duty cycle corresponds to 1 BCLK period. In other formats, the FSYNC duty cycle is 50%.

[2] The TDM–A and TDM–B selections provide the same inverted/non-inverted behavior. The two options differ from each other in how the BCLK frequency is determined, as described in Table 4-14.

The CONFIG4 pin selects the BCLK output frequency as shown in Table 4-14. Note the pin function is dependent on the target application (see CONFIG3 pin configuration in Table 4-13).

Table 4-14. CONFIG4 Hardware Configuration—Multiplier Mode

Pin Configuration		BCLK Frequency			
		I^{2}S	Left-Justified/ Right-Justified	TDM–A	TDM–B
Pull-up to VDD	0 Ω	Invalid			
	4.7 kΩ				
	22 kΩ				
	100 kΩ	64 × FSYNC	64 × FSYNC	1024 × FSYNC	CLK_OUT
Pull-down to GND	100 kΩ			512 × FSYNC	CLK_OUT / 2
	22 kΩ			256 × FSYNC	CLK_OUT / 4
	4.7 kΩ			128 × FSYNC	CLK_OUT / 8
	0 Ω			64 × FSYNC	CLK_OUT / 16

Note: Selecting a BCLK frequency referenced to FSYNC can result in an invalid BCLK divider value (depending on the FSYNC and MCLK_OUT frequencies). Refer to the BCLK_DIV field for the supported BCLK divider ratios. If an invalid selection is made, the clock outputs are disabled; normal operation resumes when a valid configuration is detected.

The CONFIG5 pin selects the ARC function and the FSYNC output frequency as shown in Table 4-15.

Table 4-15. CONFIG5 Hardware Configuration—Multiplier Mode

Pin Configuration		Automatic Rate Control (ARC)	FSYNC Frequency
Pull-up to VDD	0 Ω	Enabled	CLK_IN
	4.7 kΩ	Disabled	CLK_OUT / 1024
	22 kΩ		CLK_OUT / 512
	100 kΩ		CLK_OUT / 256
Pull-down to GND	100 kΩ		CLK_OUT / 128
	22 kΩ		CLK_OUT / 64
	4.7 kΩ		CLK_OUT / 32
	0 Ω		CLK_OUT / 16

The CONFIG6 pin selects the CLK_OUT frequency as shown in Table 4-16. Note the pin function is dependent on the ARC status (see CONFIG5 pin configuration in Table 4-15).

Table 4-16. CONFIG6 Hardware Configuration—Multiplier Mode

Pin Configuration		CLK_OUT Frequency	
		ARC Disabled	ARC Enabled
Pull-up to VDD	0 Ω	128 × CLK_IN	12.288 or 11.2896 MHz [1]
	4.7 kΩ	256 × CLK_IN	24.576 or 22.5792 MHz [1]
	22 kΩ	512 × CLK_IN	49.152 or 45.1584 MHz [1]
	100 kΩ	768 × CLK_IN	Invalid
Pull-down to GND	100 kΩ	1024 × CLK_IN	
	22 kΩ	1536 × CLK_IN	
	4.7 kΩ	3072 × CLK_IN	
	0 Ω	6144 × CLK_IN	

[1] The applicable frequency is the same base as CLK_IN

4.9.2 Synthesizer Mode

The CONFIG2 pin selects the AUX1_OUT function as shown in Table 4-17.

Table 4-17. CONFIG2 Hardware Configuration—Synthesizer Mode

Pin Configuration		AUX1 Output
Pull-up to VDD	0 Ω	Frequency Unlock Indicator
	4.7 kΩ	Disabled
	22 kΩ	
	100 kΩ	
Pull-down to GND	100 kΩ	
	22 kΩ	
	4.7 kΩ	
	0 Ω	CLK_OUT

The CONFIG3 pin has no function in Synthesizer Mode; the pin should be connected to VDD or GND.

The CONFIG4 pin selects the BCLK output frequency as shown in Table 4-18.

Table 4-18. CONFIG4 Hardware Configuration—Synthesizer Mode

Pin Configuration		BCLK Frequency
Pull-up to VDD	0 Ω	CLK_OUT / 16
	4.7 kΩ	CLK_OUT / 8
	22 kΩ	CLK_OUT / 4
	100 kΩ	CLK_OUT / 2
Pull-down to GND	100 kΩ	CLK_OUT
	22 kΩ	Invalid
	4.7 kΩ	
	0 Ω	

The CONFIG5 pin selects the FSYNC output frequency as shown in Table 4-19.

Table 4-19. CONFIG5 Hardware Configuration—Synthesizer Mode

Pin Configuration		FSYNC Frequency
Pull-up to VDD	0 Ω	Invalid
	4.7 kΩ	CLK_OUT / 1024
	22 kΩ	CLK_OUT / 512
	100 kΩ	CLK_OUT / 256
Pull-down to GND	100 kΩ	CLK_OUT / 128
	22 kΩ	CLK_OUT / 64
	4.7 kΩ	CLK_OUT / 32
	0 Ω	CLK_OUT / 16

The CONFIG6 pin selects the CLK_OUT frequency as shown in Table 4-20.

Table 4-20. CONFIG6 Hardware Configuration—Synthesizer Mode

Pin Configuration		CLK_OUT Frequency
Pull-up to VDD	0 Ω	Invalid
	4.7 kΩ	
	22 kΩ	11.2896 MHz
	100 kΩ	12.288 MHz
Pull-down to GND	100 kΩ	22.5792 MHz
	22 kΩ	24.576 MHz
	4.7 kΩ	45.1584 MHz
	0 Ω	49.152 MHz

4.10 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-21.

Table 4-21. Device ID

Label	Description
DEVID	Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Applications

5.1 Crystal Component Selection

The crystal oscillator (see Section 4.2.2) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

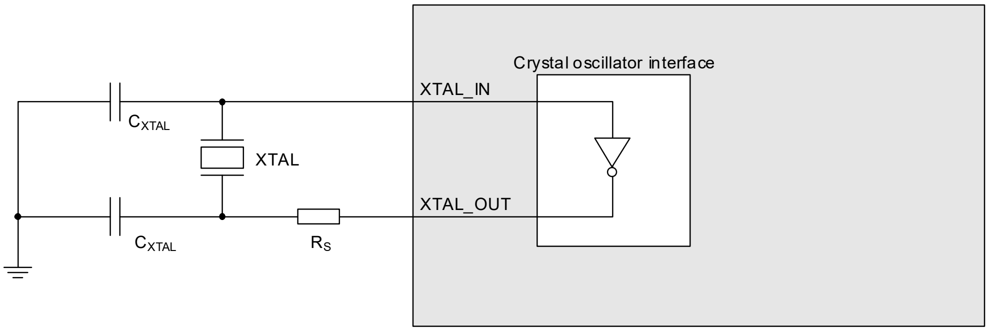


Figure 5-1. Crystal Oscillator Connection

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD operating voltage as described in Table 3-4.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS2600 is compatible with a wide variety of crystal components, including the NX3225SA, NX2016A, ECX-33Q, and ECX-2236Q families.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is 2 × C_L.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S, together with the crystal characteristics. If the gain margin is less than 5, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   R_S = series resistance (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

   If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

   The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

   where:

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   V = Peak voltage across the crystal (V)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in Fig. 5-2.

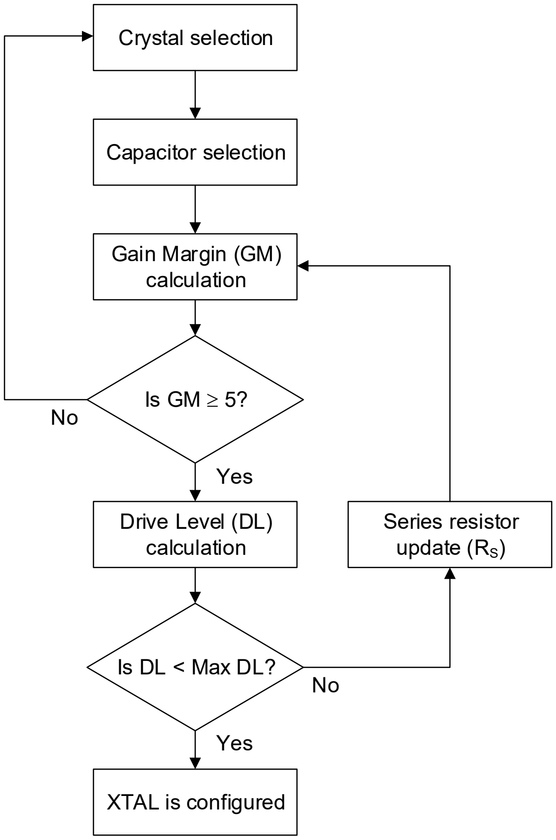


Figure 5-2. Crystal Oscillator Component Selection

5.2 Phase Alignment Configuration

The phase-alignment function (see Section 4.5.3) can be used to ensure the BCLK and FSYNC outputs are phase-aligned to the CLK_IN frequency reference. The function can be triggered manually using a control-register write, or automatically based on a configurable phase-offset threshold.

If automatic trigger is selected, the phase-alignment process is triggered whenever the detected phase offset between CLK_IN and FSYNC exceeds the threshold configured using PHASE_ALIGNMENT_THR.

- To avoid erroneous trigger conditions, the threshold must be set higher than the expected CLK_IN jitter. It is recommended to configure the threshold lower than the maximum acceptable phase-offset error, and at least 10 times larger then the expected peak CLK_IN jitter.

If automatic trigger is selected, a phase-stability monitor can be used to gate the automatic phase-alignment process. If PHASE_ALIGNMENT_STB_EN is set, the phase stability is analyzed, and the phase alignment is only implemented if the phase offset is stable.

- The phase-stability monitor should only be enabled if the phase offset is expected to drift for some time before settling (e.g., when the CLK_IN frequency changes).
- If the phase is unstable and PHASE_ALIGNMENT_STB_EN is not set, the phase alignment may be triggered multiple times; the final offset error may be larger than the specified level (see Table 3-4) and below the threshold to retrigger the phase-alignment process.

If a valid trigger condition is detected, the phase of the FSYNC and BCLK outputs is adjusted in order to restore the phase alignment. The PHASE_ALIGNMENT_SPEED field controls how quickly the phase adjustment is implemented.

- If PHASE_ALIGNMENT_SPEED = 00, the FSYNC period is extended by 1 MCLK period until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 124 FSYNC periods to complete.

  In this configuration, the phase alignment is slowest, but jitter and frequency deviation is minimized.
- If PHASE_ALIGNMENT_SPEED = 01, the FSYNC period is extended by a maximum of 10 MCLK periods until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 13 FSYNC periods to complete.
- If PHASE_ALIGNMENT_SPEED = 10, the FSYNC period is extended by a maximum of 50 MCLK periods until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 3 FSYNC periods to complete.
- If PHASE_ALIGNMENT_SPEED = 11, the FSYNC period is extended as much as is required to complete the phase alignment in a single FSYNC period.

  In this configuration, the phase alignment is fastest, but the transient FSYNC/BCLK period error may be large (depending on the size of the phase offset).

The phase-alignment speed should be configured according to the application requirements. If the output clocks are being used while the alignment is in progress, the slow rate may be chosen for optimal jitter/frequency stability. If the output clocks are not used during the alignment, the fastest rate may be preferred.

The phase-alignment process is illustrated in Fig. 5-3.

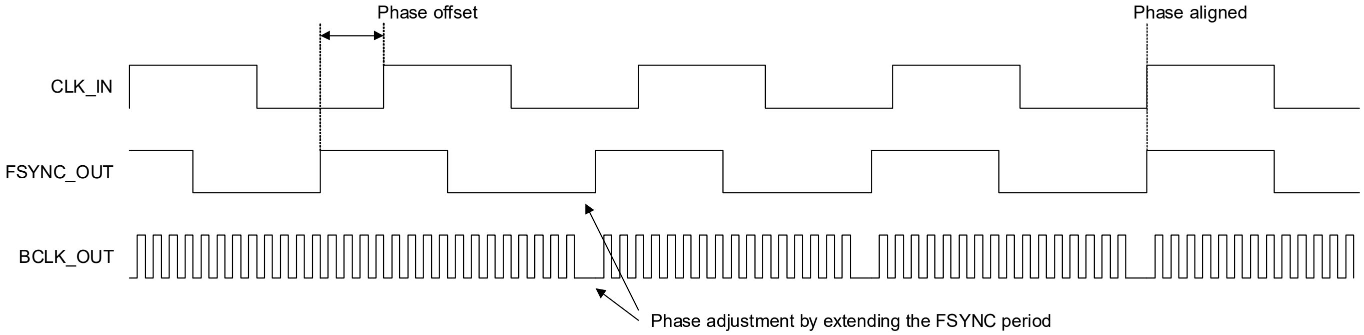


Figure 5-3. Phase Alignment

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS2600.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

□ Read/write access ░ Read-only access ▓ Write-only access ▢ User key password access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**CONFIG**	Section 6.1	Section 7.1
0x0000 1100	**KEYS**	Section 6.2	Section 7.2
0x0000 2000	**OTP_IF**	Section 6.3	Section 7.3
0x0000 2400	**OTP_CTRL**	Section 6.4	Section 7.4
0x0000 2480	**OTP_STS**	Section 6.5	Section 7.5

6.1 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0002	PLL_CFG1	RATIO_MOD			S_RATIO_SEL		—		PLL_EN1	—						AUX1_ OUT_DIS	CLK_ OUT_DIS
p. 44		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0x0000 0004	PLL_CFG2	—				FREEZE_ EN	—		PLL_EN2	—					M_RATIO_SEL		PLL_ MODE_ SEL
p. 44		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0x0000 0006	RATIO1_1	RATIO1_1															
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0008	RATIO1_2	RATIO1_2															
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 000A	RATIO2_1	RATIO2_1															
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 000C	RATIO2_2	RATIO2_2															
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 000E	RATIO3_1	RATIO3_1															
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0010	RATIO3_2	RATIO3_2															
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0012	RATIO4_1	RATIO4_1															
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0014	RATIO4_2	RATIO4_2															
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0016	PLL_CFG3	—	OUT_GATE_TYPE		OUT_ GATE	RATIO_ CFG	—				AUX_ OUT_ CFG	—	REF_CLK_IN_DIV		SYSCLK_SRC		—
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 001E	PLL_CFG4	—								FLL_BW_ MOD	FLL_BW			—			
p. 47		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0058	SW_RESET	—								SW_RST							
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0064	DRIVE_STRENGTH1	—	FSYNC_OUT_DRV			—	BCLK_OUT_DRV			—	AUX1_OUT_DRV			—	CLK_OUT_DRV		
p. 47		0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0x0000 0100	OUTPUT_CFG1	BCLK_DIV				FSYNC_DIV				BCLK_INV	BCLK_OUT_DIS	—	FSYNC_DUTY_CYCLE			FSYNC_INV	FSYNC_OUT_DIS
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0102	OUTPUT_CFG2	CLK_IN_INV	—		AUX1_OUT_SEL			AUX2_OUT_SEL		—				CLK_OUT_SEL		CLK_OUT_INV	—
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0104	AUTOMATIC_RATE_CONTROL_CFG1	—									ARC_EN	ARC_BCLK_DIV				ARC_MCLK	
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0108	PHASE_ALIGNMENT_CFG1	PHASE_ALIGNMENT_EN	—							PHASE_ALIGNMENT_STB_EN	PHASE_ALIGNMENT_MODE	PHASE_ALIGNMENT_TRIG	PHASE_ALIGNMENT_SPEED		PHASE_ALIGNMENT_THR		
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0110	DEVICE_ID1	DEVID															
p. 50		0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0
0x0000 0112	DEVICE_ID2	—								AREVID				MTLREVID			
p. 50		0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
0x0000 0114	UNLOCK_INDICATORS	—												P_UNLOCK_STICKY	P_UNLOCK	F_UNLOCK_STICKY	F_UNLOCK
p. 50		0	0	0	0	0	0	0	0	0	0	0	0	0	X	0	X
0x0000 0116	ERROR_STS	—								ERR_STS8	ERR_STS7	ERR_STS6	ERR_STS5	ERR_STS4	ERR_STS3	ERR_STS2	ERR_STS1
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0120	OTP_VDD_CTRL	—												OTP_VDD_EN	—	OTP_LDO_DISCH_EN	OTP_LDO_EN
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 KEYS

Address	Register	15 … 8	7	6	5	4	3	2	1	0
0x0000 1104	USER_KEY_REG	—	USER_KEY							
p. 52		0x00	0	0	0	0	0	0	0	0

6.3 OTP_IF

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2300	OTP_IMG_RD1	OTP_IMG_RD_BYTE2								OTP_IMG_RD_BYTE1							
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2302	OTP_IMG_RD2	OTP_IMG_RD_BYTE4								OTP_IMG_RD_BYTE3							
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2304	OTP_IMG_RD3	OTP_IMG_RD_BYTE6								OTP_IMG_RD_BYTE5							
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2306	OTP_IMG_RD4	OTP_IMG_RD_BYTE8								OTP_IMG_RD_BYTE7							
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2308	OTP_IMG_RD5	OTP_IMG_RD_BYTE10								OTP_IMG_RD_BYTE9							
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 230A	OTP_IMG_RD6	OTP_IMG_RD_BYTE12								OTP_IMG_RD_BYTE11							
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 230C	OTP_IMG_RD7	OTP_IMG_RD_BYTE14								OTP_IMG_RD_BYTE13							
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 230E	OTP_IMG_RD8	OTP_IMG_RD_BYTE16								OTP_IMG_RD_BYTE15							
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2310	OTP_IMG_RD9	OTP_IMG_RD_BYTE18								OTP_IMG_RD_BYTE17							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2312	OTP_IMG_RD10	OTP_IMG_RD_BYTE20								OTP_IMG_RD_BYTE19							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2314	OTP_IMG_RD11	OTP_IMG_RD_BYTE22								OTP_IMG_RD_BYTE21							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2316	OTP_IMG_RD12	OTP_IMG_RD_BYTE24								OTP_IMG_RD_BYTE23							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2318	OTP_IMG_RD13	OTP_IMG_RD_BYTE26								OTP_IMG_RD_BYTE25							
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 231A	OTP_IMG_RD14	OTP_IMG_RD_BYTE28								OTP_IMG_RD_BYTE27							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 231C	OTP_IMG_RD15	OTP_IMG_RD_BYTE30								OTP_IMG_RD_BYTE29							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 231E	OTP_IMG_RD16	OTP_IMG_RD_BYTE32								OTP_IMG_RD_BYTE31							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2320	OTP_IMG_RD17	OTP_IMG_RD_BYTE34								OTP_IMG_RD_BYTE33							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2322	OTP_IMG_RD18	OTP_IMG_RD_BYTE36								OTP_IMG_RD_BYTE35							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2324	OTP_IMG_RD19	OTP_IMG_RD_BYTE38								OTP_IMG_RD_BYTE37							
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2326	OTP_IMG_RD20	OTP_IMG_RD_BYTE40								OTP_IMG_RD_BYTE39							
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2328	OTP_IMG_RD21	OTP_IMG_RD_BYTE42								OTP_IMG_RD_BYTE41							
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 232A	OTP_IMG_RD22	OTP_IMG_RD_BYTE44								OTP_IMG_RD_BYTE43							
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 232C	OTP_IMG_RD23	OTP_IMG_RD_BYTE46								OTP_IMG_RD_BYTE45							
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 232E	OTP_IMG_RD24	OTP_IMG_RD_BYTE48								OTP_IMG_RD_BYTE47							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2340	OTP_IMG_WR1	OTP_IMG_WR_BYTE2								OTP_IMG_WR_BYTE1							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2342	OTP_IMG_WR2	OTP_IMG_WR_BYTE4								OTP_IMG_WR_BYTE3							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2344	OTP_IMG_WR3	OTP_IMG_WR_BYTE6								OTP_IMG_WR_BYTE5							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2346	OTP_IMG_WR4	OTP_IMG_WR_BYTE8								OTP_IMG_WR_BYTE7							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2348	OTP_IMG_WR5	OTP_IMG_WR_BYTE10								OTP_IMG_WR_BYTE9							
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 234A	OTP_IMG_WR6	OTP_IMG_WR_BYTE12								OTP_IMG_WR_BYTE11							
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 234C	OTP_IMG_WR7	OTP_IMG_WR_BYTE14								OTP_IMG_WR_BYTE13							
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 234E	OTP_IMG_WR8	OTP_IMG_WR_BYTE16								OTP_IMG_WR_BYTE15							
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2350	OTP_IMG_WR9	OTP_IMG_WR_BYTE18								OTP_IMG_WR_BYTE17							
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2352 p. 59	OTP_IMG_WR10	OTP_IMG_WR_BYTE20								OTP_IMG_WR_BYTE19							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2354 p. 59	OTP_IMG_WR11	OTP_IMG_WR_BYTE22								OTP_IMG_WR_BYTE21							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2356 p. 59	OTP_IMG_WR12	OTP_IMG_WR_BYTE24								OTP_IMG_WR_BYTE23							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2358 p. 59	OTP_IMG_WR13	OTP_IMG_WR_BYTE26								OTP_IMG_WR_BYTE25							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 235A p. 59	OTP_IMG_WR14	OTP_IMG_WR_BYTE28								OTP_IMG_WR_BYTE27							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 235C p. 60	OTP_IMG_WR15	OTP_IMG_WR_BYTE30								OTP_IMG_WR_BYTE29							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 235E p. 60	OTP_IMG_WR16	OTP_IMG_WR_BYTE32								OTP_IMG_WR_BYTE31							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2360 p. 60	OTP_IMG_WR17	OTP_IMG_WR_BYTE34								OTP_IMG_WR_BYTE33							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2362 p. 60	OTP_IMG_WR18	OTP_IMG_WR_BYTE36								OTP_IMG_WR_BYTE35							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2364 p. 60	OTP_IMG_WR19	OTP_IMG_WR_BYTE38								OTP_IMG_WR_BYTE37							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2366 p. 61	OTP_IMG_WR20	OTP_IMG_WR_BYTE40								OTP_IMG_WR_BYTE39							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2368 p. 61	OTP_IMG_WR21	OTP_IMG_WR_BYTE42								OTP_IMG_WR_BYTE41							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 236A p. 61	OTP_IMG_WR22	OTP_IMG_WR_BYTE44								OTP_IMG_WR_BYTE43							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 236C p. 61	OTP_IMG_WR23	OTP_IMG_WR_BYTE46								OTP_IMG_WR_BYTE45							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 236E p. 61	OTP_IMG_WR24	OTP_IMG_WR_BYTE48								OTP_IMG_WR_BYTE47							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4 OTP_CTRL

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2400 p. 62	OTP_CONTROL1	—														OTP_PROG_EN	—
		0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0

6.5 OTP_STS

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 24A8 p. 62	OTP_STS2	—				OTP_IMG_ID				—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 24AC p. 62	OTP_STS3	—						OTP_IMG_ECC_STS		—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 24BC p. 62	OTP_STS6	—									OTP_IMG_NUM			—			OTP_MODE
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS2600.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

□ Read/write access ░ Read-only access ▒ Write-only access ▣ User key password access

7.1 CONFIG

7.1.1 PLL_CFG1

Address: 0x0000 0002

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO_MOD			S_RATIO_SEL		—		PLL_EN1	—						AUX1_OUT_DIS	CLK_OUT_DIS
Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description
15:13	RATIO_MOD	Ratio modifier control. Adjusts the PLL ratio by the selected multiplier/division factor. 000 = (Default) Multiply x1 001 = Multiply x2 010 = Multiply x4 011 = Multiply x8 100 = Divide /2 101 = Divide /4 110 = Divide /8 111 = Divide /16
12:11	S_RATIO_SEL	Ratio selection in Synthesizer Mode. 00 = (Default) Ratio 1 01 = Ratio 2 10 = Ratio 3 11 = Ratio 4
10:9	—	Reserved
8	PLL_EN1	PLL enable. Note that PLL_EN2 must also be set to enable the PLL. 0 = (Default) Disabled 1 = Enabled
7:2	—	Reserved
1	AUX1_OUT_DIS	AUX1_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)
0	CLK_OUT_DIS	CLK_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)

7.1.2 PLL_CFG2

Address: 0x0000 0004

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				FREEZE_EN	—		PLL_EN2	—					M_RATIO_SEL		PLL_MODE_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description
15:12	—	Reserved
11	FREEZE_EN	Freeze register control. If enabled, the freezable fields hold their current values. Any updates to these fields are buffered until FREEZE_EN is cleared. 0 = (Default) Disabled 1 = Enabled
10:9	—	Reserved

Bits	Name	Description
8	PLL_EN2	PLL enable. Note that PLL_EN1 must also be set to enable the PLL. 0 = (Default) Disabled 1 = Enabled
7:3	—	Reserved
2:1	M_RATIO_SEL	Ratio selection in Multiplier Mode. 00 = (Default) Ratio 1 01 = Ratio 2 10 = Ratio 3 11 = Ratio 4
0	PLL_MODE_SEL	PLL mode control. Selects Multiplier Mode or Synthesizer Mode. Only valid if S_RATIO_SEL and M_RATIO_SEL are set to the same value. 0 = (Default) Synthesizer Mode 1 = Multiplier Mode

7.1.3 RATIO1_1

Address: 0x0000 0006

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO1_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO1_1	Ratio 1, bits [31:16].

7.1.4 RATIO1_2

Address: 0x0000 0008

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO1_2															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO1_2	Ratio 1, bits [15:0].

7.1.5 RATIO2_1

Address: 0x0000 000A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO2_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO2_1	Ratio 2, bits [31:16].

7.1.6 RATIO2_2

Address: 0x0000 000C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO2_2															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO2_2	Ratio 2, bits [15:0].

7.1.7 RATIO3_1

Address: 0x0000 000E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO3_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO3_1	Ratio 3, bits [31:16].

7.1.8 RATIO3_2

Address: 0x0000 0010

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO3_2															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO3_2	Ratio 3, bits [15:0].

7.1.9 RATIO4_1

Address: 0x0000 0012

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO4_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO4_1	Ratio 4, bits [31:16].

7.1.10 RATIO4_2

Address: 0x0000 0014

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RATIO4_2															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	RATIO4_2	Ratio 4, bits [15:0].

7.1.11 PLL_CFG3

Address: 0x0000 0016

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	OUT_GATE_TYPE		OUT_GATE	RATIO_CFG	—				AUX_OUT_CFG	—	REF_CLK_IN_DIV		SYSCLK_SRC		—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	—	Reserved
14:13	OUT_GATE_TYPE	Output gate type. Selects the logic condition used to determine if the outputs are valid. 00 = (Default) Frequency unlock (F_UNLOCK) 01 = Phase unlock (P_UNLOCK) 10 = Analog PLL unlock 11 = Reserved
12	OUT_GATE	Output gate control. Selects whether the clock outputs are stopped automatically if they are not valid. 0 = (Default) Enabled 1 = Disabled
11	RATIO_CFG	Ratio format control. Selects format for the ratio selected by M_RATIO_SEL. Note this field has no effect in Synthesizer Mode. 0 = (Default) High multiplication (20.12) 1 = High resolution (12.20)
10:7	—	Reserved
6	AUX_OUT_CFG	AUX1 and AUX2 driver configuration. Only valid for lock/status output signals; clock outputs are CMOS in all cases. 0 = (Default) CMOS. Active high (Logic 1 indicates unlock or clock-missing status). 1 = Open Drain. Active low (Logic 0 indicates unlock or clock-missing status).
5	—	Reserved
4:3	REF_CLK_IN_DIV	REF_CLK_IN input divider. 00 = (Default) Divide by 4 01 = Divide by 2 10 = Divide by 1 11 = Reserved
2:1	SYSCLK_SRC	Source selection for the PLL timing reference SYSCLK between REF_CLK_IN and the internal oscillator 00 = (Default) Automatic selection 01 = REF_CLK_IN 10 = Internal oscillator 11 = Reserved
0	—	Reserved

7.1.12 PLL_CFG4

Address: 0x0000 001E

RW	15…8	7	6	5	4	3	2	1	0
	—	FLL_BW_MOD	FLL_BW			—			
Default	0x00	1	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7	FLL_BW_MOD	FLL bandwidth multiplication factor. Modifies the bandwidth selected by FLL_BW. 0 = FLL_BW is multiplied by 1 1 = (Default) FLL_BW is multiplied by 16
6:4	FLL_BW	FLL bandwidth select. Note the FLL bandwidth is also determined by the multiplication factor, FLL_BW_MOD. 000 = (Default) 1 Hz 001 = 2 Hz 010 = 4 Hz … 111 = 128 Hz
3:0	—	Reserved

7.1.13 SW_RESET

Address: 0x0000 0058

WO	15…8	7	6	5	4	3	2	1	0
	—	SW_RST							
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:0	SW_RST	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.1.14 DRIVE_STRENGTH1

Address: 0x0000 0064

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	FSYNC_OUT_DRV			—	BCLK_OUT_DRV			—	AUX1_OUT_DRV			—	CLK_OUT_DRV		
Default	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bits	Name	Description
15	—	Reserved
14:12	FSYNC_OUT_DRV	FSYNC_OUT drive strength. 000 = 2 mA 001 = 4 mA … 100 = (Default) 10 mA … 111 = 16 mA
11	—	Reserved
10:8	BCLK_OUT_DRV	BCLK_OUT drive strength. 000 = 2 mA 001 = 4 mA … 100 = (Default) 10 mA … 111 = 16 mA
7	—	Reserved
6:4	AUX1_OUT_DRV	AUX1_OUT drive strength. 000 = 2 mA 001 = 4 mA … 100 = (Default) 10 mA … 111 = 16 mA
3	—	Reserved
2:0	CLK_OUT_DRV	CLK_OUT drive strength. 000 = 2 mA 001 = 4 mA … 100 = (Default) 10 mA … 111 = 16 mA

7.1.15 OUTPUT_CFG1

Address: 0x0000 0100

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BCLK_DIV				FSYNC_DIV				BCLK_INV	BCLK_ OUT_DIS	—	FSYNC_DUTY_CYCLE			FSYNC_ INV	FSYNC_ OUT_DIS
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	BCLK_DIV	BCLK output divider. Note this field has no effect if automatic rate control (ARC) is enabled. 0x0 = (Default) Divide by 1 0x1 = Divide by 2 0x2 = Divide by 3 0x3 = Divide by 4 0x4 = Divide by 6 0x5 = Divide by 8 0x6 = Divide by 12 0x7 = Divide by 16 0x8 = Divide by 24 0x9 = Divide by 32 0xA = Divide by 48 0xB–0xF = Reserved
11:8	FSYNC_DIV	FSYNC output divider. Note this field has no effect if automatic rate control (ARC) is enabled. 0x0 = (Default) Divide by 16 0x1 = Divide by 32 0x2 = Divide by 64 0x3 = Divide by 128 0x4 = Divide by 256 0x5 = Divide by 512 0x6 = Divide by 1024 0x7 = Divide by 192 0x8 = Divide by 384 0x9 = Divide by 768 0xA = Divide by 1536 0xB = Divide by 576 0xC = Divide by 1152 0xD–0xF = Reserved
7	BCLK_INV	BCLK polarity select. 0 = (Default) Normal 1 = Inverted
6	BCLK_OUT_DIS	BCLK_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)
5	—	Reserved
4:2	FSYNC_DUTY_ CYCLE	FSYNC output duty-cycle control. Note the FSYNC duty cycle must be configured less than or equal to 50%. 000 = (Default) 50% duty cycle 001 = 1 BCLK period 010 = 2 BCLK periods 011 = 4 BCLK periods 100 = 8 BCLK periods 101 = 16 BCLK periods 110 = 32 BCLK periods 111 = Reserved
1	FSYNC_INV	FSYNC polarity select. 0 = (Default) Normal 1 = Inverted
0	FSYNC_OUT_DIS	FSYNC_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)

7.1.16 OUTPUT_CFG2

Address: 0x0000 0102

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK_IN_ INV	—		AUX1_OUT_SEL			AUX2_OUT_SEL		—				CLK_OUT_SEL		CLK_OUT_ INV	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	CLK_IN_INV	CLK_IN polarity select. 0 = (Default) Normal 1 = Inverted
14:13	—	Reserved
12:10	AUX1_OUT_SEL	AUX1_OUT function select. 000 = (Default) REF_CLK_IN 001 = CLK_IN 010 = CLK_OUT 011 = Frequency unlock (F_UNLOCK) 100 = Phase unlock (P_UNLOCK) 101 = BCLK 110 = FSYNC 111 = CLK_IN (clock missing)
9:8	AUX2_OUT_SEL	AUX2_OUT function select. 00 = (Default) Disabled 01 = Frequency unlock (F_UNLOCK) 10 = Phase unlock (P_UNLOCK) 11 = CLK_IN (clock missing)
7:4	—	Reserved

Bits	Name	Description
3:2	CLK_OUT_SEL	CLK_OUT function. Selects clock source for CLK_OUT. 00 = (Default) MCLK 01 = ALTCLK 352.8/384.0 kHz 10 = ALTCLK 1.882/2.048 MHz 11 = ALTCLK 2.053/2.234 MHz
1	CLK_OUT_INV	CLK_OUT polarity select. 0 = (Default) Normal 1 = Inverted
0	—	Reserved

7.1.17 AUTOMATIC_RATE_CONTROL_CFG1

Address: 0x0000 0104

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ARC_EN	ARC_BCLK_DIV				ARC_MCLK	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ARC_EN	Automatic rate control (ARC) enable. 0 = (Default) Disabled 1 = Enabled
5:2	ARC_BCLK_DIV	BCLK output control in ARC mode. 0x0 = (Default) FSYNC x64 0x1 = FSYNC x128 0x2 = FSYNC x256 0x3 = FSYNC x512 0x4 = FSYNC x1024 0x5 = MCLK /1 0x6 = MCLK /2 0x7 = MCLK /4 0x8 = MCLK /8 0x9 = MCLK /16 0xA–0xF = Reserved
1:0	ARC_MCLK	MCLK output control in ARC mode. Note the output frequency depends on whether the clock reference is a multiple of 48 kHz or 44.1 kHz. 00 = (Default) 12.288/11.2896 MHz 01 = 24.576/22.5792 MHz 10 = 49.152/45.1584 MHz 11 = Reserved

7.1.18 PHASE_ALIGNMENT_CFG1

Address: 0x0000 0108

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PHASE_ALIGNMENT_EN	—							PHASE_ALIGNMENT_STB_EN	PHASE_ALIGNMENT_MODE	PHASE_ALIGNMENT_TRIG	PHASE_ALIGNMENT_SPEED		PHASE_ALIGNMENT_THR		
Access	RW	—							RW	RW	WO	RW		RW		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	PHASE_ALIGNMENT_EN	Phase-alignment enable. 0 = (Default) Disabled 1 = Enabled
14:8	—	Reserved
7	PHASE_ALIGNMENT_STB_EN	Phase-alignment stability control. If this bit is set, the phase-alignment process is only executed if the phase offset is stable. 0 = (Default) Disabled 1 = Enabled
6	PHASE_ALIGNMENT_MODE	Phase-alignment trigger mode. 0 = (Default) Automatic 1 = Manual
5	PHASE_ALIGNMENT_TRIG	Phase-alignment manual trigger. Write 1 to trigger the phase-alignment process in manual mode. 0 = (Default) No action 1 = Trigger

Bits	Name	Description
4:3	PHASE_ ALIGNMENT_ SPEED	Phase-alignment speed. Selects the phase-alignment rate by configuring the maximum permitted stretching of the FSYNC cycle. 00 = (Default) 1 MCLK per FSYNC cycle 01 = 10 MCLK per FSYNC cycle 10 = 50 MCLK per FSYNC cycle 11 = Maximum
2:0	PHASE_ ALIGNMENT_THR	Phase-alignment threshold. Selects the phase-offset threshold to trigger the phase-alignment process in automatic mode. 000 = (Default) 2 MCLK periods 001 = 4 MCLK periods 010 = 8 MCLK periods 011 = 16 MCLK periods 100 = 32 MCLK periods 101 = 64 MCLK periods 110 = 128 MCLK periods 111 = 256 MCLK periods

7.1.19 DEVICE_ID1

Address: 0x0000 0110

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID															
Default	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	DEVID	Device ID. A value of 0x2600 indicates the device is a CS2600.

7.1.20 DEVICE_ID2

Address: 0x0000 0112

RO	15…8	7	6	5	4	3	2	1	0
	—	AREVID				MTLREVID			
Default	0x00	X	X	X	X	X	X	X	X

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	All-layer device revision. This field is incremented for every all-layer revision of the device.
3:0	MTLREVID	Metal-layer device revision. This field is incremented for every metal-layer revision of the device.

7.1.21 UNLOCK_INDICATORS

Address: 0x0000 0114

	15…8	7	6	5	4	3	2	1	0
	—	—				P_UNLOCK_STICKY	P_UNLOCK	F_UNLOCK_STICKY	F_UNLOCK
Access	—	—				W1C	RO	W1C	RO
Default	0x00	0	0	0	0	0	X	0	X

Bits	Name	Description
15:4	—	Reserved
3	P_UNLOCK_STICKY	Phase-unlock status. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Locked 1 = Unlocked
2	P_UNLOCK	Phase-unlock status. 0 = Locked 1 = Unlocked
1	F_UNLOCK_STICKY	Frequency-unlock status. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Locked 1 = Unlocked
0	F_UNLOCK	Frequency-unlock status. 0 = Locked 1 = Unlocked

7.1.22 ERROR_STS

Address: 0x0000 0116

W1C	15…8	7	6	5	4	3	2	1	0
	—	ERR_STS8	ERR_STS7	ERR_STS6	ERR_STS5	ERR_STS4	ERR_STS3	ERR_STS2	ERR_STS1
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7	ERR_STS8	Error status bit indicates the device is defective. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
6	ERR_STS7	Error status bit indicates the OTP memory is corrupt. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
5	ERR_STS6	Error status bit indicates invalid register configuration. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
4	ERR_STS5	Error status bit indicates the PLL is disabled. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
3	ERR_STS4	Error status bit indicates invalid hardware configuration. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
2	ERR_STS3	Error status bit indicates REF_CLK_IN is not present. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
1	ERR_STS2	Error status bit indicates CLK_IN is not stable. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error
0	ERR_STS1	Error status bit indicates CLK_IN is not present. This bit is latching when set, it remains set until cleared by writing 1. 0 = (Default) Normal 1 = Error

7.1.23 OTP_VDD_CTRL

Address: 0x0000 0120

RW	15…8	7	6	5	4	3	2	1	0
	—	—				OTP_VDD_EN	—	OTP_LDO_DISCH_EN	OTP_LDO_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:4	—	Reserved
3	OTP_VDD_EN	Enables the OTP programming supply 0 = (Default) Disabled 1 = Enabled
2	—	Reserved
1	OTP_LDO_DISCH_EN	LDO output discharge 0 = (Default) Disabled 1 = Enabled
0	OTP_LDO_EN	LDO enable (for OTP programming) 0 = (Default) Disabled 1 = Enabled

7.2 KEYS

7.2.1 USER_KEY_REG

Address: 0x0000 1104

WO	15…8	7	6	5	4	3	2	1	0
	—	USER_KEY							
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:0	USER_KEY	User Key control – requires two writes to set (unlock): 0xAA followed by 0x55 sets the key A write of any other byte value unsets (locks) the key

7.3 OTP_IF

7.3.1 OTP_IMG_RD1

Address: 0x0000 2300

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE2								OTP_IMG_RD_BYTE1							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE2	OTP image byte 2 read field
7:0	OTP_IMG_RD_ BYTE1	OTP image byte 1 read field

7.3.2 OTP_IMG_RD2

Address: 0x0000 2302

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE4								OTP_IMG_RD_BYTE3							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE4	OTP image byte 4 read field
7:0	OTP_IMG_RD_ BYTE3	OTP image byte 3 read field

7.3.3 OTP_IMG_RD3

Address: 0x0000 2304

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE6								OTP_IMG_RD_BYTE5							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE6	OTP image byte 6 read field
7:0	OTP_IMG_RD_ BYTE5	OTP image byte 5 read field

7.3.4 OTP_IMG_RD4

Address: 0x0000 2306

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE8								OTP_IMG_RD_BYTE7							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE8	OTP image byte 8 read field
7:0	OTP_IMG_RD_ BYTE7	OTP image byte 7 read field

7.3.5 OTP_IMG_RD5

Address: 0x0000 2308

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE10								OTP_IMG_RD_BYTE9							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE10	OTP image byte 10 read field
7:0	OTP_IMG_RD_ BYTE9	OTP image byte 9 read field

7.3.6 OTP_IMG_RD6

Address: 0x0000 230A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE12								OTP_IMG_RD_BYTE11							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE12	OTP image byte 12 read field
7:0	OTP_IMG_RD_ BYTE11	OTP image byte 11 read field

7.3.7 OTP_IMG_RD7

Address: 0x0000 230C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE14								OTP_IMG_RD_BYTE13							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE14	OTP image byte 14 read field
7:0	OTP_IMG_RD_ BYTE13	OTP image byte 14 read field

7.3.8 OTP_IMG_RD8

Address: 0x0000 230E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE16								OTP_IMG_RD_BYTE15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE16	OTP image byte 16 read field
7:0	OTP_IMG_RD_ BYTE15	OTP image byte 15 read field

7.3.9 OTP_IMG_RD9

Address: 0x0000 2310

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE18								OTP_IMG_RD_BYTE17							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE18	OTP image byte 18 read field
7:0	OTP_IMG_RD_ BYTE17	OTP image byte 17 read field

7.3.10 OTP_IMG_RD10

Address: 0x0000 2312

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE20								OTP_IMG_RD_BYTE19							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE20	OTP image byte 20 read field
7:0	OTP_IMG_RD_ BYTE19	OTP image byte 19 read field

7.3.11 OTP_IMG_RD11

Address: 0x0000 2314

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE22								OTP_IMG_RD_BYTE21							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE22	OTP image byte 22 read field
7:0	OTP_IMG_RD_ BYTE21	OTP image byte 21 read field

7.3.12 OTP_IMG_RD12

Address: 0x0000 2316

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE24								OTP_IMG_RD_BYTE23							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE24	OTP image byte 24 read field
7:0	OTP_IMG_RD_ BYTE23	OTP image byte 23 read field

7.3.13 OTP_IMG_RD13

Address: 0x0000 2318

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE26								OTP_IMG_RD_BYTE25							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_ BYTE26	OTP image byte 26 read field
7:0	OTP_IMG_RD_ BYTE25	OTP image byte 25 read field

7.3.14 OTP_IMG_RD14

Address: 0x0000 231A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE28								OTP_IMG_RD_BYTE27							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE28	OTP image byte 28 read field
7:0	OTP_IMG_RD_BYTE27	OTP image byte 27 read field

7.3.15 OTP_IMG_RD15

Address: 0x0000 231C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE30								OTP_IMG_RD_BYTE29							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE30	OTP image byte 30 read field
7:0	OTP_IMG_RD_BYTE29	OTP image byte 29 read field

7.3.16 OTP_IMG_RD16

Address: 0x0000 231E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE32								OTP_IMG_RD_BYTE31							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE32	OTP image byte 32 read field
7:0	OTP_IMG_RD_BYTE31	OTP image byte 31 read field

7.3.17 OTP_IMG_RD17

Address: 0x0000 2320

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE34								OTP_IMG_RD_BYTE33							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE34	OTP image byte 34 read field
7:0	OTP_IMG_RD_BYTE33	OTP image byte 33 read field

7.3.18 OTP_IMG_RD18

Address: 0x0000 2322

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE36								OTP_IMG_RD_BYTE35							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE36	OTP image byte 36 read field
7:0	OTP_IMG_RD_BYTE35	OTP image byte 35 read field

7.3.19 OTP_IMG_RD19

Address: 0x0000 2324

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE38								OTP_IMG_RD_BYTE37							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE38	OTP image byte 38 read field
7:0	OTP_IMG_RD_BYTE37	OTP image byte 37 read field

7.3.20 OTP_IMG_RD20

Address: 0x0000 2326

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE40								OTP_IMG_RD_BYTE39							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE40	OTP image byte 40 read field
7:0	OTP_IMG_RD_BYTE39	OTP image byte 39 read field

7.3.21 OTP_IMG_RD21

Address: 0x0000 2328

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE42								OTP_IMG_RD_BYTE41							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE42	OTP image byte 42 read field
7:0	OTP_IMG_RD_BYTE41	OTP image byte 41 read field

7.3.22 OTP_IMG_RD22

Address: 0x0000 232A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE44								OTP_IMG_RD_BYTE43							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE44	OTP image byte 44 read field
7:0	OTP_IMG_RD_BYTE43	OTP image byte 43 read field

7.3.23 OTP_IMG_RD23

Address: 0x0000 232C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE46								OTP_IMG_RD_BYTE45							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE46	OTP image byte 46 read field
7:0	OTP_IMG_RD_BYTE45	OTP image byte 45 read field

7.3.24 OTP_IMG_RD24

Address: 0x0000 232E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_RD_BYTE48								OTP_IMG_RD_BYTE47							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_RD_BYTE48	OTP image byte 48 read field
7:0	OTP_IMG_RD_BYTE47	OTP image byte 47 read field

7.3.25 OTP_IMG_WR1

Address: 0x0000 2340

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE2								OTP_IMG_WR_BYTE1							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE2	OTP image byte 2 write field
7:0	OTP_IMG_WR_BYTE1	OTP image byte 1 write field

7.3.26 OTP_IMG_WR2

Address: 0x0000 2342

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE4								OTP_IMG_WR_BYTE3							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE4	OTP image byte 4 write field
7:0	OTP_IMG_WR_BYTE3	OTP image byte 3 write field

7.3.27 OTP_IMG_WR3

Address: 0x0000 2344

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE6								OTP_IMG_WR_BYTE5							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE6	OTP image byte 6 write field
7:0	OTP_IMG_WR_BYTE5	OTP image byte 5 write field

7.3.28 OTP_IMG_WR4

Address: 0x0000 2346

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE8								OTP_IMG_WR_BYTE7							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE8	OTP image byte 8 write field
7:0	OTP_IMG_WR_BYTE7	OTP image byte 7 write field

7.3.29 OTP_IMG_WR5

Address: 0x0000 2348

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE10								OTP_IMG_WR_BYTE9							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE10	OTP image byte 10 write field
7:0	OTP_IMG_WR_BYTE9	OTP image byte 9 write field

7.3.30 OTP_IMG_WR6

Address: 0x0000 234A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE12								OTP_IMG_WR_BYTE11							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE12	OTP image byte 12 write field
7:0	OTP_IMG_WR_BYTE11	OTP image byte 11 write field

7.3.31 OTP_IMG_WR7

Address: 0x0000 234C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE14								OTP_IMG_WR_BYTE13							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE14	OTP image byte 14 write field
7:0	OTP_IMG_WR_BYTE13	OTP image byte 14 write field

7.3.32 OTP_IMG_WR8

Address: 0x0000 234E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE16								OTP_IMG_WR_BYTE15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE16	OTP image byte 16 write field
7:0	OTP_IMG_WR_BYTE15	OTP image byte 15 write field

7.3.33 OTP_IMG_WR9

Address: 0x0000 2350

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE18								OTP_IMG_WR_BYTE17							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE18	OTP image byte 18 write field
7:0	OTP_IMG_WR_BYTE17	OTP image byte 17 write field

7.3.34 OTP_IMG_WR10

Address: 0x0000 2352

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE20								OTP_IMG_WR_BYTE19							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE20	OTP image byte 20 write field
7:0	OTP_IMG_WR_ BYTE19	OTP image byte 19 write field

7.3.35 OTP_IMG_WR11

Address: 0x0000 2354

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE22								OTP_IMG_WR_BYTE21							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE22	OTP image byte 22 write field
7:0	OTP_IMG_WR_ BYTE21	OTP image byte 21 write field

7.3.36 OTP_IMG_WR12

Address: 0x0000 2356

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE24								OTP_IMG_WR_BYTE23							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE24	OTP image byte 24 write field
7:0	OTP_IMG_WR_ BYTE23	OTP image byte 23 write field

7.3.37 OTP_IMG_WR13

Address: 0x0000 2358

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE26								OTP_IMG_WR_BYTE25							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE26	OTP image byte 26 write field
7:0	OTP_IMG_WR_ BYTE25	OTP image byte 25 write field

7.3.38 OTP_IMG_WR14

Address: 0x0000 235A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE28								OTP_IMG_WR_BYTE27							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE28	OTP image byte 28 write field
7:0	OTP_IMG_WR_ BYTE27	OTP image byte 27 write field

7.3.39 OTP_IMG_WR15

Address: 0x0000 235C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE30								OTP_IMG_WR_BYTE29							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE30	OTP image byte 30 write field
7:0	OTP_IMG_WR_BYTE29	OTP image byte 29 write field

7.3.40 OTP_IMG_WR16

Address: 0x0000 235E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE32								OTP_IMG_WR_BYTE31							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE32	OTP image byte 32 write field
7:0	OTP_IMG_WR_BYTE31	OTP image byte 31 write field

7.3.41 OTP_IMG_WR17

Address: 0x0000 2360

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE34								OTP_IMG_WR_BYTE33							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE34	OTP image byte 34 write field
7:0	OTP_IMG_WR_BYTE33	OTP image byte 33 write field

7.3.42 OTP_IMG_WR18

Address: 0x0000 2362

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE36								OTP_IMG_WR_BYTE35							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE36	OTP image byte 36 write field
7:0	OTP_IMG_WR_BYTE35	OTP image byte 35 write field

7.3.43 OTP_IMG_WR19

Address: 0x0000 2364

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE38								OTP_IMG_WR_BYTE37							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_BYTE38	OTP image byte 38 write field
7:0	OTP_IMG_WR_BYTE37	OTP image byte 37 write field

7.3.44 OTP_IMG_WR20

Address: 0x0000 2366

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE40								OTP_IMG_WR_BYTE39							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE40	OTP image byte 40 write field
7:0	OTP_IMG_WR_ BYTE39	OTP image byte 39 write field

7.3.45 OTP_IMG_WR21

Address: 0x0000 2368

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE42								OTP_IMG_WR_BYTE41							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE42	OTP image byte 42 write field
7:0	OTP_IMG_WR_ BYTE41	OTP image byte 41 write field

7.3.46 OTP_IMG_WR22

Address: 0x0000 236A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE44								OTP_IMG_WR_BYTE43							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE44	OTP image byte 44 write field
7:0	OTP_IMG_WR_ BYTE43	OTP image byte 43 write field

7.3.47 OTP_IMG_WR23

Address: 0x0000 236C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE46								OTP_IMG_WR_BYTE45							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE46	OTP image byte 46 write field
7:0	OTP_IMG_WR_ BYTE45	OTP image byte 45 write field

7.3.48 OTP_IMG_WR24

Address: 0x0000 236E

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTP_IMG_WR_BYTE48								OTP_IMG_WR_BYTE47							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	OTP_IMG_WR_ BYTE48	OTP image byte 48 write field
7:0	OTP_IMG_WR_ BYTE47	OTP image byte 47 write field

7.4 OTP_CTRL

7.4.1 OTP_CONTROL1

Address: 0x0000 2400

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OTP_PROG_EN	—
Default	0x04	0	0	0	1	1	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OTP_PROG_EN	OTP programming enable 0 = (Default) Disabled (OTP writes ignored) 1 = Enabled (OTP writes permitted)
0	—	Reserved

7.5 OTP_STS

7.5.1 OTP_STS2

Address: 0x0000 24A8

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				OTP_IMG_ID				—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	OTP_IMG_ID	Bits [3:1] indicate the ID of the current OTP image. Valid for Production Mode programming only. Note that Bit[0] is not valid. Zero indicates the device has not been programmed in Production Mode. 0x0–0x1 = (Default) Blank 0x2–0x3 = ID = 1 0x4–0x5 = ID = 2 0x6–0x7 = ID = 3 0x8–0x9 = ID = 4 0xA–0xB = ID = 5 0xC–0xD = ID = 6 0xE–0xF = ID = 7
7:0	—	Reserved

7.5.2 OTP_STS3

Address: 0x0000 24AC

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						OTP_IMG_ECC_STS		—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9:8	OTP_IMG_ECC_STS	Indicates the number of errors detected in the OTP payload and parity bits. 00 = (Default) No Error, or ECC not run 01 = Single Error 10 = Double Error 11 = Three or more errors
7:0	—	Reserved

7.5.3 OTP_STS6

Address: 0x0000 24BC

RO	15…8	7	6	5	4	3	2	1	0
	—	—	OTP_IMG_NUM			—			OTP_MODE
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6:4	OTP_IMG_NUM	Indicates the number of Production Mode OTP images programmed. A maximum of 7 images can be programmed. 000 = (Default) 0 images 001 = 1 images … 111 = 7 images

Bits	Name	Description
3:1	—	Reserved
0	OTP_MODE	Indicates which mode of OTP programming is supported. Note that a blank device supports production or prototype programming. If OTP_MODE=0, check OTP_IMG_NUM to determine if the OTP has already been programmed in Production Mode. If OTP_MODE=0 and OTP_IMG_NUM=0x0, the OTP is blank and supports both programming modes. 0 = (Default) Production mode 1 = Prototyping mode

8 Performance Plots

Performance data is provided for a variety of test cases. Performance is measured at the main clock output (CLK_OUT).

Test conditions (unless otherwise specified): T_A = 25°C, output load = 15 pF, output drive strength = 10 mA, REF_CLK is jitter-free (phase noise at least 20 dB lower than the device phase noise), VDD is noise free (noise present does not impact on jitter specifications).

8.1 Jitter Performance

Sinusoidal phase-deviation tolerance is illustrated in Fig. 8-1. Phase deviation is applied to the CLK_IN frequency reference; the performance plots show the phase deviation that can be tolerated without losing PLL lock.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (Performance is measured with external 12 MHz reference clock, 12 MHz crystal, and internal oscillator; the plot shows worst-case performance.)

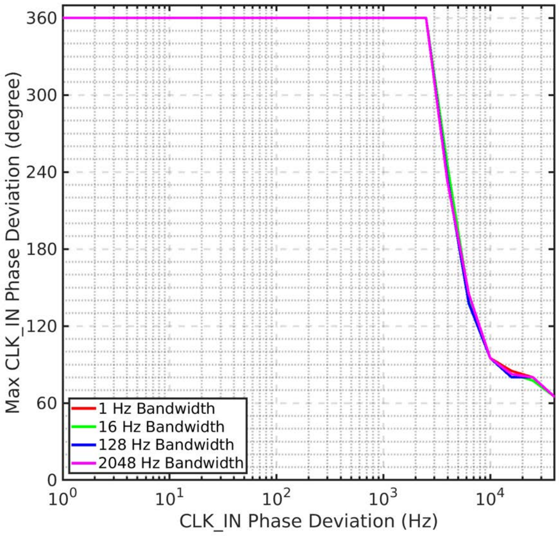


Figure 8-1. Sinusoidal Phase-Deviation Tolerance—External Clock or Internal Oscillator

Random TIE jitter rejection and tolerance is illustrated in Fig. 8-2 and Fig. 8-3. Jitter is applied to the CLK_IN frequency reference.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (External clock is provided using 12 MHz reference or 12 MHz crystal; the plot shows worst-case performance.)

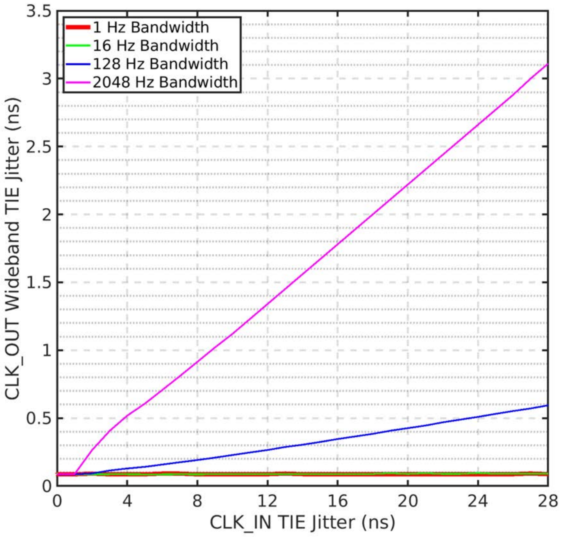


Figure 8-2. Random Jitter Rejection—External Clock

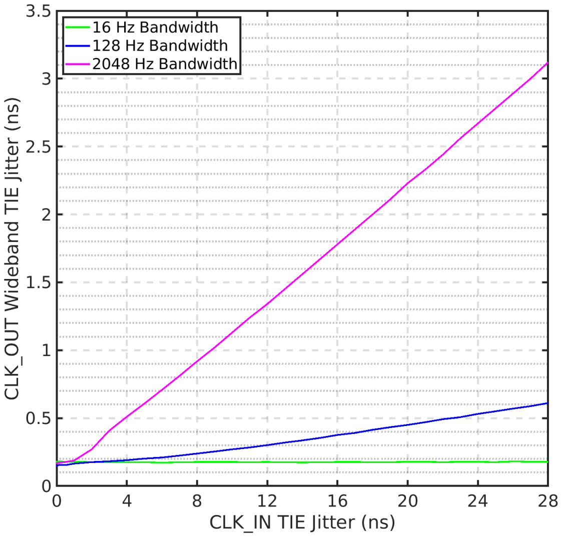


Figure 8-3. Random Jitter Rejection—Internal Oscillator

Sinusoidal TIE jitter transfer is illustrated in Fig. 8-4. Jitter is applied to the CLK_IN frequency reference; the performance plots show the output jitter level relative to the input jitter level.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (Performance is measured with external 12 MHz reference clock, 12 MHz crystal, and internal oscillator; the plot shows worst-case performance.)

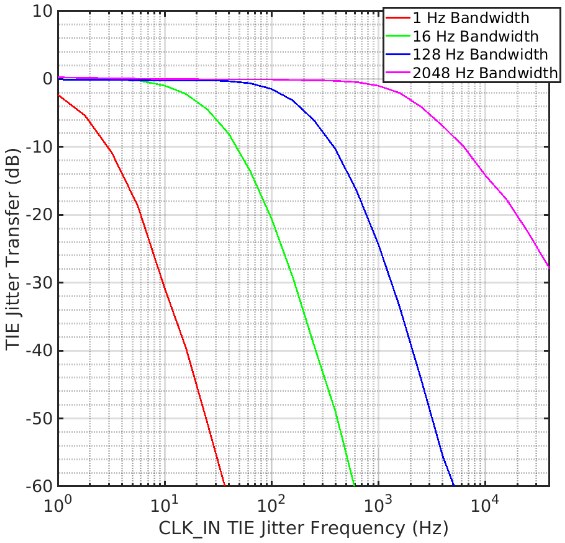
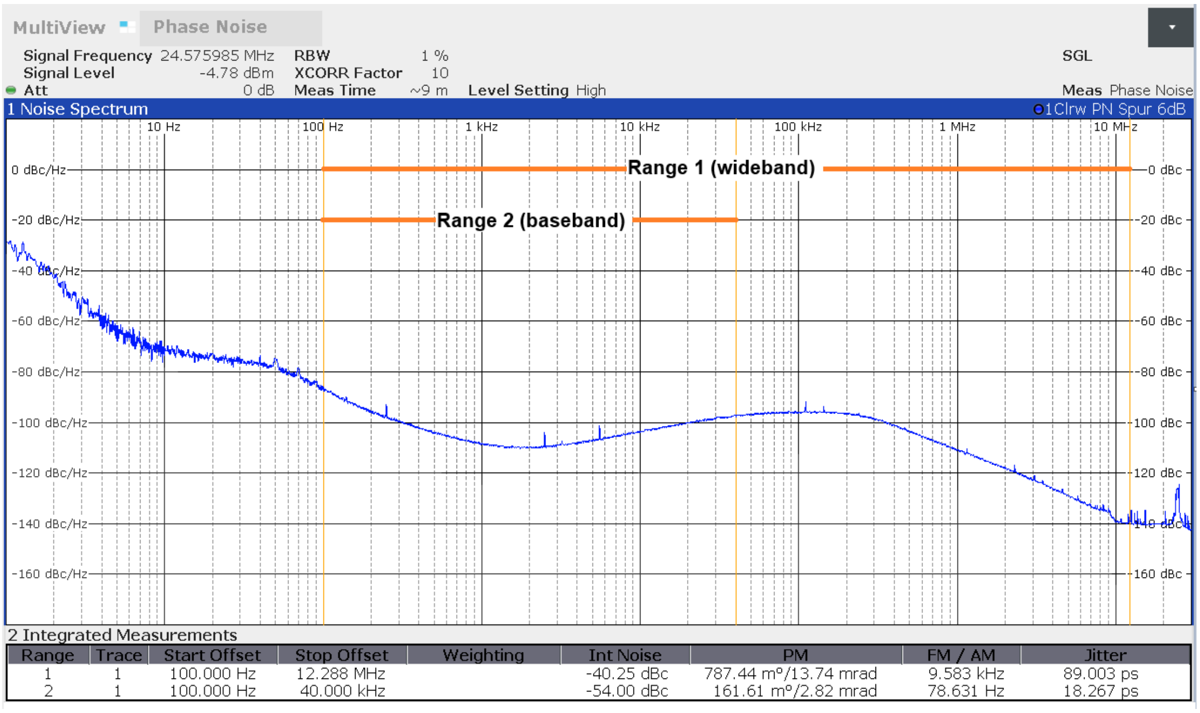


Figure 8-4. Sinusoidal Jitter Transfer—External Clock or Internal Oscillator

8.2 Phase Noise

The intrinsic phase-noise performance is illustrated in Fig. 8-5 and Fig. 8-6. The performance plots show the output phase noise under typical operating conditions. Note that the CLK_IN frequency reference is jitter-free for these tests.

Test conditions: CLK_IN = 48 kHz, CLK_OUT = 24.576 MHz, REF_CLK = External 12 MHz or internal oscillator. (External clock is provided using 12 MHz reference or 12 MHz crystal; the plot shows worst-case performance.)



MultiView Phase Noise

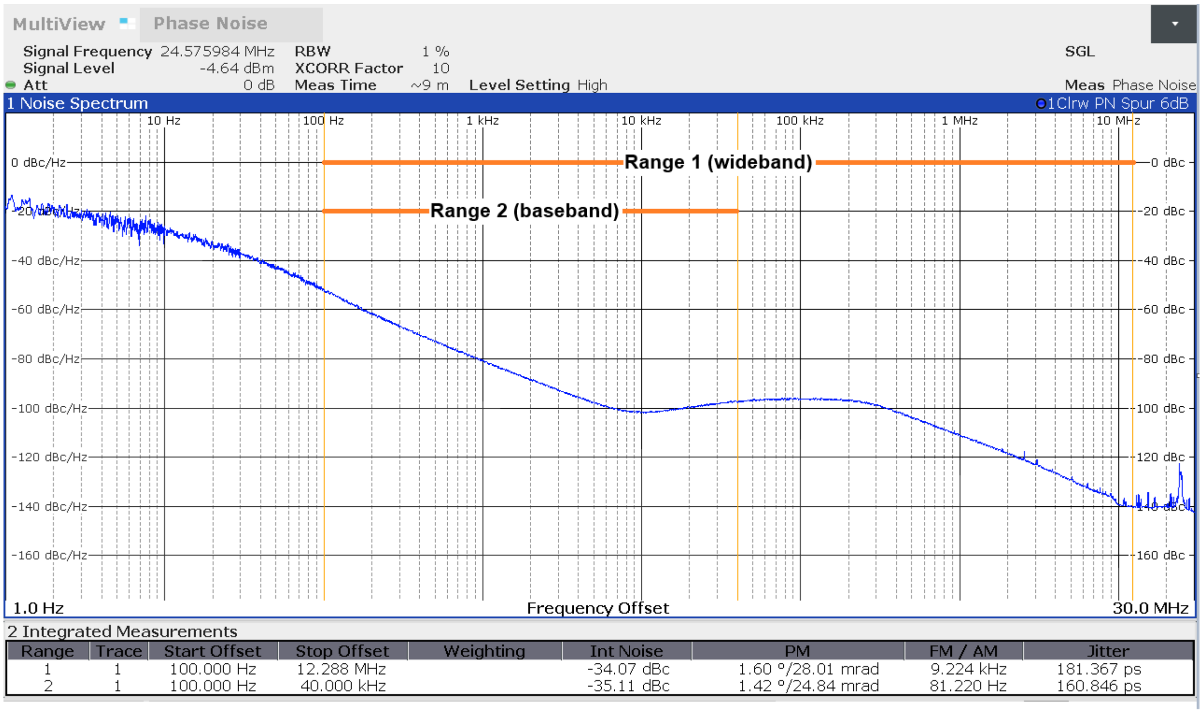
Signal Frequency 24.575985 MHz RBW 1 % SGL
Signal Level -4.78 dBm XCORR Factor 10
Att 0 dB Meas Time ~9 m Level Setting High Meas Phase Noise

1 Noise Spectrum 1Clrw PN Spur 6dB

2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	100.000 Hz	12.288 MHz		-40.25 dBc	787.44 m°/13.74 mrad	9.583 kHz	89.003 ps
2	1	100.000 Hz	40.000 kHz		-54.00 dBc	161.61 m°/2.82 mrad	78.631 Hz	18.267 ps

Figure 8-5. Phase Noise—External Clock



MultiView Phase Noise

Signal Frequency 24.575984 MHz RBW 1 % SGL
Signal Level -4.64 dBm XCORR Factor 10
Att 0 dB Meas Time ~9 m Level Setting High Meas Phase Noise

1 Noise Spectrum 1Clrw PN Spur 6dB

2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	100.000 Hz	12.288 MHz		-34.07 dBc	1.60 °/28.01 mrad	9.224 kHz	181.367 ps
2	1	100.000 Hz	40.000 kHz		-35.11 dBc	1.42 °/24.84 mrad	81.220 Hz	160.846 ps

Figure 8-6. Phase Noise—Internal Oscillator

9 Thermal Characteristics

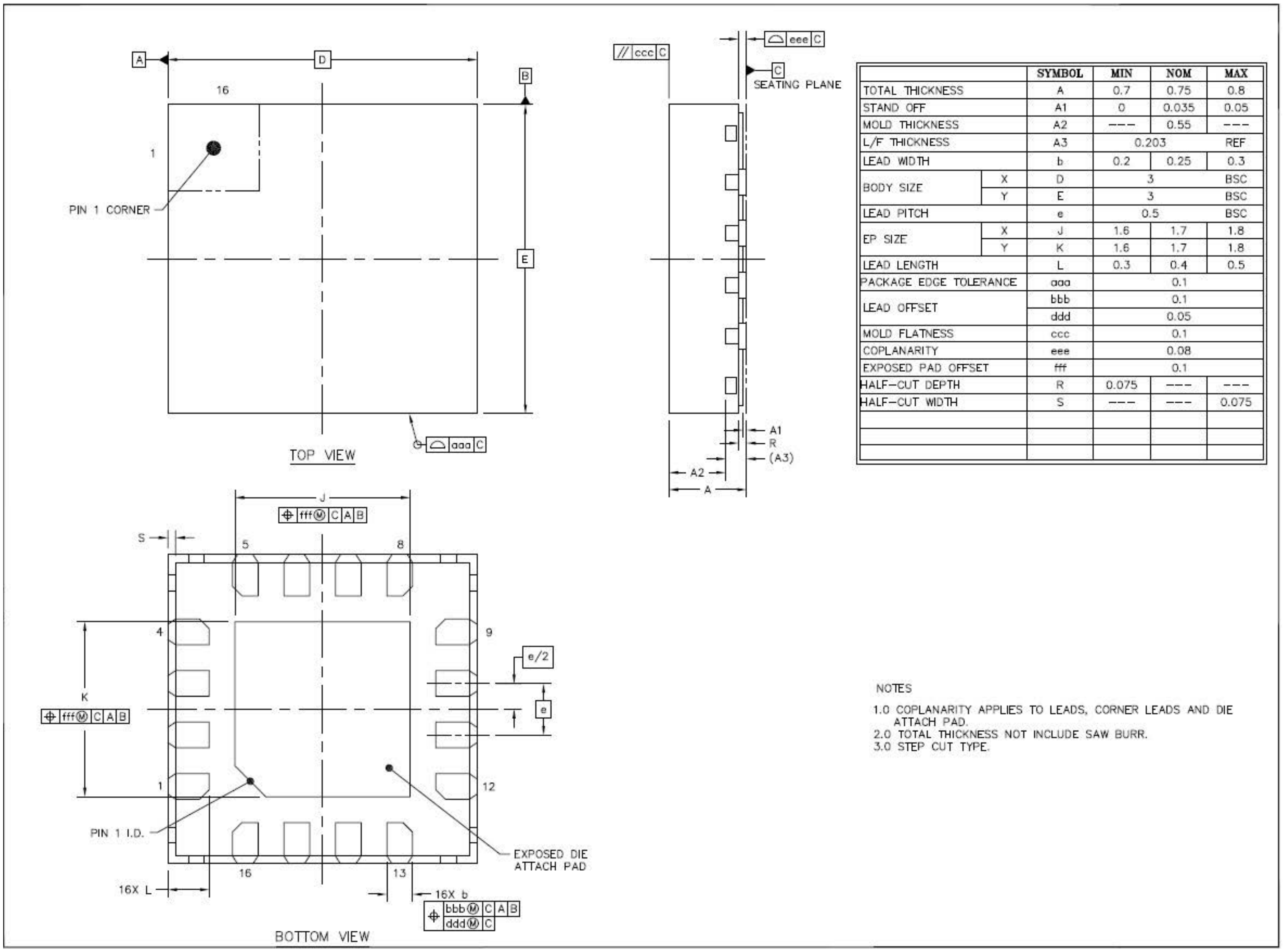
Table 9-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	72.85	°C/W
Junction-to-board thermal resistance	θ_{JB}	60.99	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	240.45	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	52.18	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	23.16	°C/W

Notes:

- Natural convection at the maximum recommended operating temperature T_A (see Table 3-1)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

10 Package Dimensions



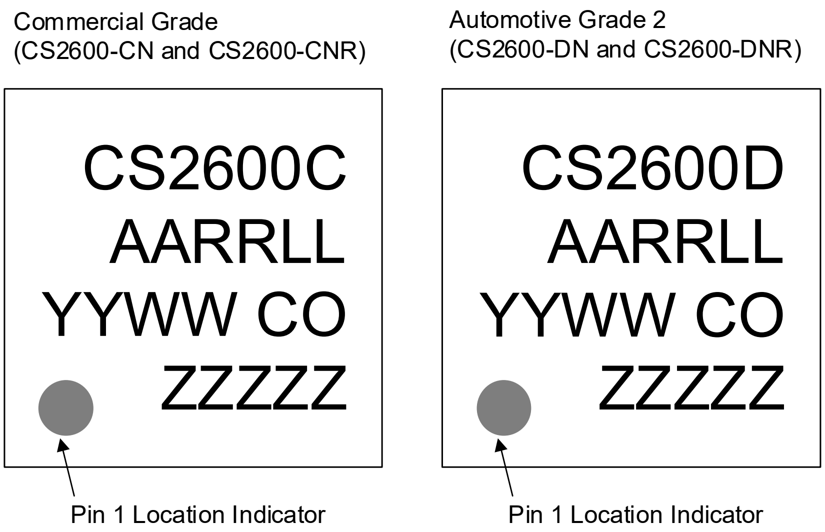
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203		REF
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	3		BSC
	Y	E	3		BSC
LEAD PITCH		e	0.5		BSC
EP SIZE	X	J	1.6	1.7	1.8
	Y	K	1.6	1.7	1.8
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
EXPOSED PAD OFFSET		fff	0.1		
HALF-CUT DEPTH		R	0.075	---	---
HALF-CUT WIDTH		S	---	---	0.075

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.
3.0 STEP CUT TYPE.

Figure 10-1. QFN Package Dimensions

11 Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Package mark date/Country of origin
Line 4: Encoded wafer/device ID

Package Mark Fields
AA = Assembly site code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture
CO = Country of origin

Figure 11-1. Package Marking

12 Ordering Information

Table 12-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS2600	Clock Synthesizer and Multiplier	16-pin QFN	Yes	Commercial	–40 to +85°C	Tray	CS2600–CN
						Tape and Reel	CS2600–CNR
				Automotive Grade 2	–40 to +105°C	Tray	CS2600–DN
						Tape and Reel	CS2600–DNR

13 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

14 Revision History

Table 14-1. Revision History

Revision	Change
F1 APR 2025	• Initial production release

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

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