Agilex™ 3 FPGA and SoC C-Series Development Kits User Guide

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1. Overview

Agilex™ 3 FPGA and SoC C-Series Development Kits provide hardware development platforms for evaluating the performance and features of the Agilex 3 FPGA and SoC C-Series FPGAs with transceivers capable of running up to 12.5 Gbps NRZ.

Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 3 FPGA C-Series Development Kit	DK-A3Y135BM16AEA	A3CY135BM16AE6S	A3CYDKP02252001001
Agilex 3 FPGA and SoC C-Series Development Kit	DK-A3W135BM16AEA	A3CW135BM16AE6S	A3CWDKP02252701001

Figure 1. Agilex 3 FPGA C-Series Development Kit (Top View)

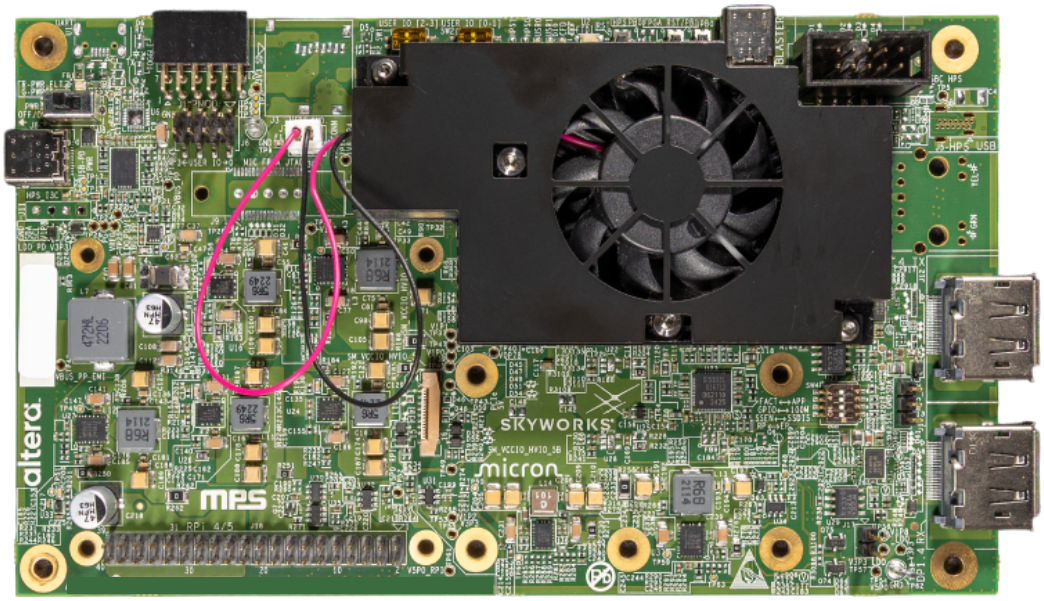


Figure 2. Agilex 3 FPGA C-Series Development Kit (Bottom View)

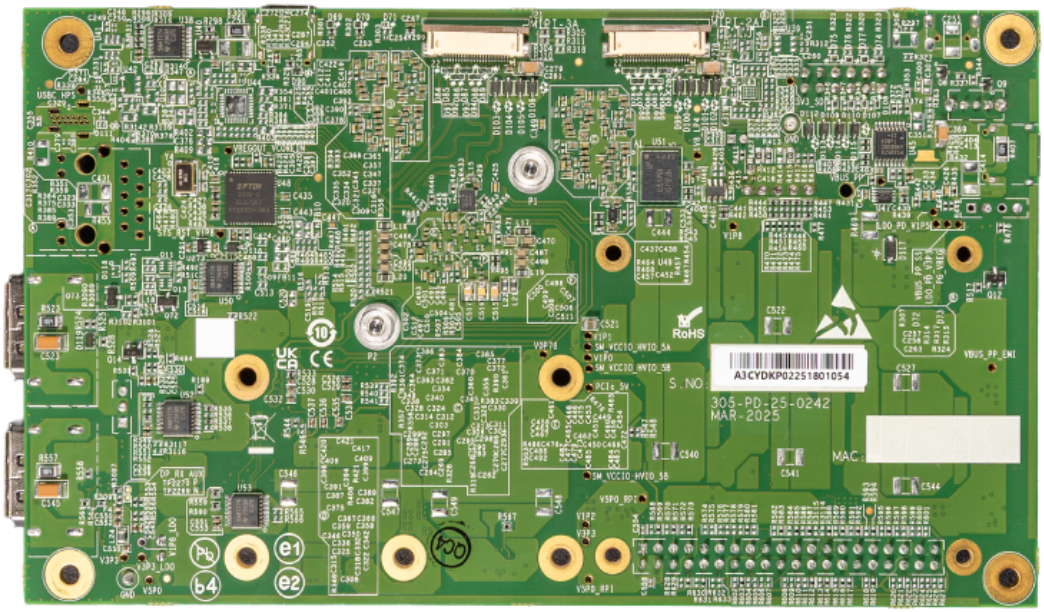


Figure 3. Agilex 3 FPGA and SoC C-Series Development Kit (Top View)

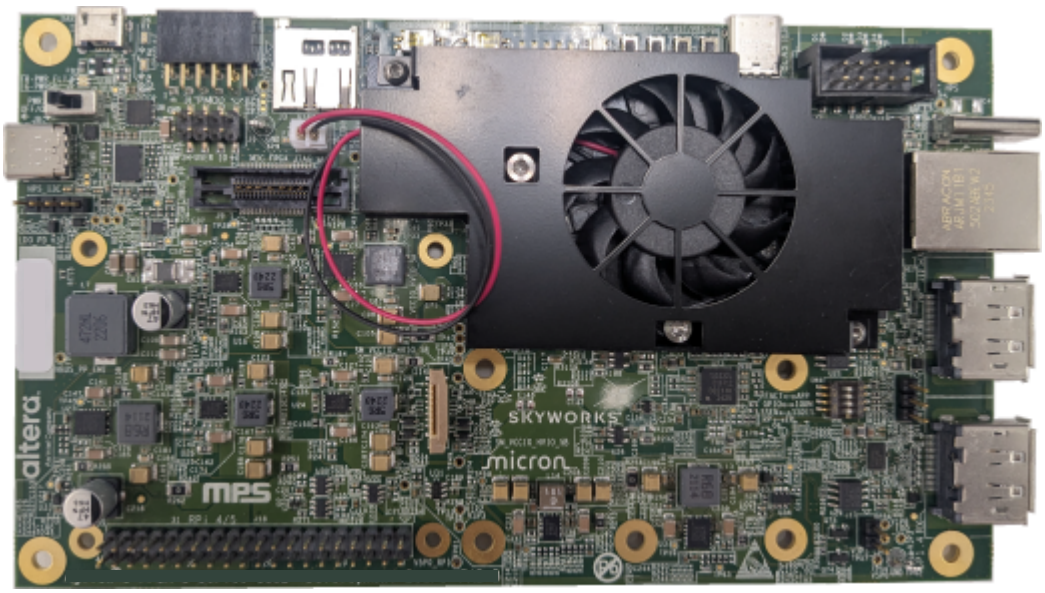
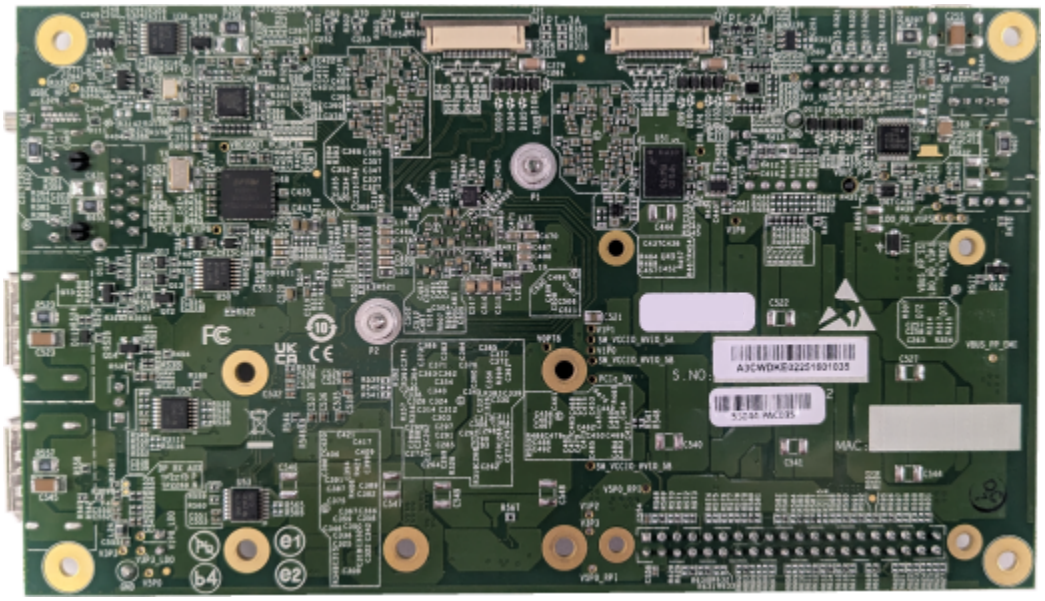


Figure 4. Agilex 3 FPGA and SoC C-Series Development Kit (Bottom View)



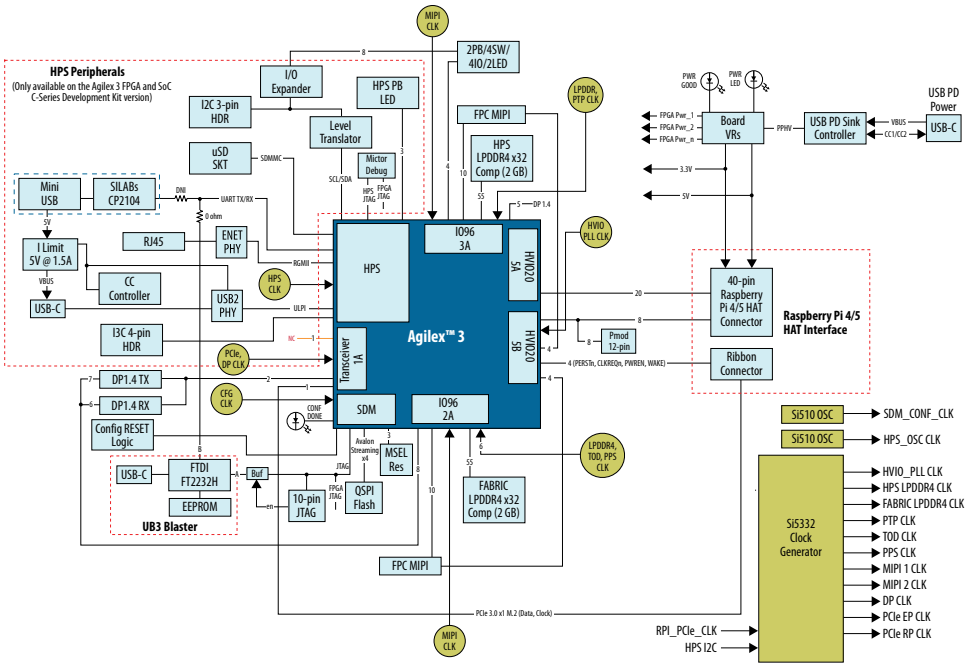
Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 3 FPGA and SoC C-Series Development Kits.

Related Information

Development Kit Components on page 42

1.1. Block Diagram

Figure 5. Agilex 3 FPGA/FPGA and SoC C-Series Development Kit Block Diagram



1.2. Feature Summary

- Agilex 3 FPGA/FPGA and SoC C-Series device in 16 mm × 16 mm 896-ball Ball Grid Array (BGA) package
  - Dual-core 64-bit Arm* Cortex*-A55 hard processor (HPS) @ 800 MHz (Agilex 3 FPGA and SoC C-Series device only)
  - Four transceiver TX and RX lanes supporting up to 12.5 Gbps NRZ data rates per lane
  - 135K logic elements (LE)
  - 46.8K adaptive logic modules (ALM)
  - 188 variable precision digital signal processing (DSP) blocks
- FPGA configuration
  - JTAG header for device programming
  - Built-in USB-Blaster III for device programming
  - Active serial (AS) x4 configuration mode support
  - 512 Mb flash for AS x4
- Clocking
  - Onboard clock generator

- Transceiver interfaces
  - PCI Express* (PCIe*) x1 interface supporting PCIe 3.0 root-port and end-point applications with an optional Altera PCIe gold finger daughter board or Raspberry Pi* 5 M.2 HAT board, respectively.
  - DisplayPort v1.4 transmit and receive interfaces at 8.1 Gbps/lane
- Memory interfaces
  - Two independent 2 GB LPDDR4 x32 at 2,133 Mbps
- HPS communication ports (only available on the Agilex 3 FPGA and SoC C-Series Development Kit version)
  - 10/100/1000 RJ45 Ethernet
  - 2-wire universal asynchronous receiver–transmitter (UART)
  - USB 2.0 Dual Role Port (DRP) supporting both host and devices mode
  - Micro-SD card slot for HPS Boot
- Video Interfaces
  - Two independent Mobile Industry Processor Interface (MIPI)
  - DisplayPort v1.4 transmitter
  - DisplayPort v1.4 receiver
- Expansion Interface
  - 40-pin header for interfacing standard Raspberry Pi 4/5 daughter cards
  - 22-pin flex cable connector for installing Raspberry Pi 5 M.2 daughter card or optional Altera PCIe 3.0 x1 gold finger daughter card
- HPS/user buttons, switches, I/Os, and status LEDs
  - HPS dedicated general-purpose push button
  - HPS dedicated Cold Reset push button
  - Two user general-purpose push buttons, one can be dedicated for FPGA reset
  - Four general-purpose user DIP switches
  - Four general-purpose user I/Os connected to 0.1 mm headers
  - Two HPS dedicated green LEDs
  - Two dedicated USER green LEDs
  - One tri-color (red/green/blue) for USB-Blaster III cable status LED
  - FPGA configuration done green LED
  - Ethernet Link (green) and Activity (yellow) status LEDs
- Heatsink and fan
  - Active 5 V fan-cooled heatsink assembly

- Power
  - USB-PD board power status LED (Green/Red)
  - On/off slide power switch
- Mechanical
  - 3.8" × 6.6" board size
  - Optional PCIe gold finger daughter card expansion for conversion into PCIe full height, half-length add-in card
- Operating environment
  - 0°C–35°C

1.3. Box Contents

- Agilex 3 FPGA C-Series Development Kit or Agilex 3 FPGA and SoC C-Series Development Kit
- 3 ft USB Type-A to USB Type-C cable
- Dear Customer Letter
- FCC Safety Flyer
- China RoHS declaration

Related Information

Agilex 3 FPGA C-Series Development Kit Website

1.4. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0°C–35°C
Recommended board operating power	27 W to 54 W depending on FPGA workload
FPGA maximum power supported by active heat sink/fan	16 W

Related Information

Handling the Board on page 10

2. Getting Started

2.1. Before You Begin

You must check the kit contents and inspect the board to verify that you received all of the items in the box before using the kit and installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix C.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

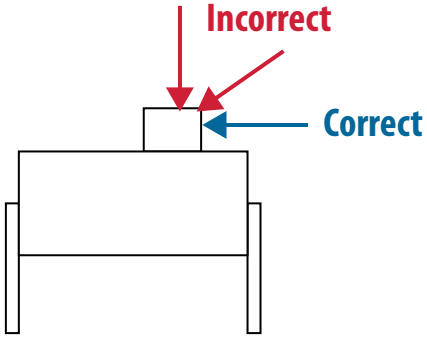
Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.

2.2.1. Handling the DIP Switches

Operating the DIP Switch Safely

- Do not apply excessive force when operating the slide-type switch, as this might cause damage or deformation, leading to malfunction.
- Apply the operating load from the side of the striker.
- Avoid applying force at an angle or from above the striker, as this might deform the switch contact.



Setting the DIP Switch

- To set the slide-type switch, use a small, rounded object like the end of a ballpoint pen or a tiny screwdriver.
- Do not use sharp tools, such as tweezers, to set the switch as they might damage it.
- Do not use a mechanical pencil, as its point could leave lead particles behind. These particles might interfere with the switch and the internal circuit board, potentially causing malfunction. Lead buildup can also reduce the dielectric strength of the circuit board.

2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Pro Edition software
- Agilex 3 FPGA and SoC C-Series Development Kits software
- Ashling* RiscFree* Integrated Development Environment (IDE)
- USB-Blaster III driver

2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the FPGA Software Download Center webpage of the Altera website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Altera® FPGA Software Installation and Licensing*.

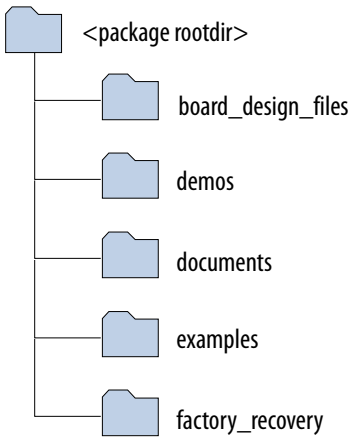
Related Information

- Quartus Prime Pro Edition User Guide: Getting Started
- Altera FPGA Software Installation and Licensing

2.3.2. Installing the Development Kit

1. Download the Agilex 3 FPGA/FPGA and SoC C-Series Development Kit installer package from the Agilex 3 FPGA C-Series Development Kit webpage on the Altera website.
2. Unzip the Agilex 3 FPGA/FPGA and SoC C-Series Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 6. Agilex 3 FPGA/FPGA and SoC C-Series Development Kit Directory Structure



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

Table 3. Installed Development Kit Directory Description

Lists the file directory names and a description of their contents.

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
`demos`	Contains demonstration applications when available.
`documents`	Contains the development kit documentation.
`examples`	Contains the sample design files for the Agilex 3 FPGA and SoC C-Series Development Kits: • Board Test System (BTS): BTS GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO, and PCIe 3.0
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3.3. Installing the Ashling* RiscFree Integrated Development Environment (IDE)

RiscFree is Ashling's Eclipse* C/C++ Development Toolkit (CDT) based integrated development environment (IDE) for Altera FPGAs Arm*-based HPS and RISC-V based Nios® V processors. The RiscFree IDE provides a complete, seamless environment for C and C++ software development.

RiscFree IDE has two types of installation options:

- Bundled installation option when installing the Quartus Prime software
- Standalone installation which requires you to install one of the following to use the debugger:
  - The Quartus Prime Programmer and Tools
  - The Quartus Prime software

For the installation instructions of the RiscFree IDE, refer to the *Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide*.

Related Information

Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide

2.3.4. Installing the USB-Blaster III Driver

The Agilex 3 FPGA and SoC C-Series Development Kits includes onboard USB-Blaster III circuits for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster III driver on the host computer.

The USB-Blaster III driver is available after you install the Quartus Prime software (version 25.1.1 or higher) in the `<Quartus Prime installation directory>\quartus\drivers` directory.

3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 3 FPGA and SoC C-Series Development Kits for specific use cases.

3.1. Default Settings

The Agilex 3 FPGA/FPGA and SoC C-Series development kit ships with its board switches and jumpers preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch and jumper settings table to return to its factory settings before proceeding ahead.

Table 4. Factory Default Switch and Jumper Settings

Note: Do not set the switches when the power is on. Only set the switches after the power is off.

Switch	Default Position	Function
SW3	OFF	Board slide power switch • Slide SW3 to the ON position to power on the board • Slide SW3 to the OFF position to power off the board
SW4[1:4]	OFF/OFF/OFF/OFF	Board configuration DIP switch SW4.1 • OFF—Sets the board to function as a PCIe End Point • ON—Sets the board to function as a PCIe Root Port
		Board configuration DIP switch SW4.2 • OFF—Enables the -0.5% spread spectrum modulation for the PCIe clock • ON—Disables the -0.5% spread spectrum modulation for the PCIe clock
		Board configuration DIP switch SW4.3 • OFF—Connects a 100 MHz clock to the HVIO bank 5B, pin AJ27 • ON—Connects the Raspberry Pi GPIO26 to HVIO bank 5B, pin AJ27
		SW4.4 • OFF—Sets the FPGA to load the user application image from the QSPI flash • ON—Sets the FPGA to load the factory recover image from the QSPI flash *Note:* Current Altera designs do not use SW4.4. You can include this switch in your design, depending on your application needs.
S1	OFF	HPS COLD RESET tactile push button • Pushing and releasing S1 generates a 20 ms active low pulse to the HPS_COLD_RESETn input of the FPGA

continued...

Switch	Default Position	Function
S2	OFF	Dedicated general-purpose tactile push button for the HPS interface • Pushing this button drives the HPS push button input logic low • Releasing this button drives the HPS push button input logic high
S3	OFF	USER dedicated general-purpose tactile push button (PB1/ FPGA_RSTN) connected to HSIO bank 3A, pin M1. This button can be used as a general-purpose push button or as a FPGA RESET push button for user designs. • Pushing this button drives the USER push button PB1/ FPGA_RSTN input logic low • Releasing this button drives the USER push button PB1/ FPGA_RSTN input logic high
S4	OFF	USER dedicated general-purpose tactile push button (PB0) connected to HSIO bank 3A, pin L1 • Pushing this button drives the USER push button PB0 input logic low • Releasing this button drives the USER push button PB0 input logic high
J17	OPEN	Voltage selection jumper for HVIO bank 5A • Shunting J17 sets the HVIO bank 5A voltage to 1.8 V • Leaving J17 open sets the HVIO bank 5A voltage to 3.3 V You must use this jumper to set the HVIO 5A bank voltage (either 1.8 V or 3.3 V) to match the voltage of the expansion daughter card that is plugged into Raspberry Pi connector (J14) or Pmod expansion connector (J1). Failure to set the proper bank voltage can cause damage to the development kit and any attached Raspberry Pi/Pmod expansion boards. The default HVIO 5A bank voltage is set to 3.3 V (no shunt on J17).

3.2. Powering Up the Development Board

The Agilex 3 FPGA/FPGA and SoC C-Series development board is designed to be powered by a standard USB-PD Type-C compliant power adapter capable of providing a minimum of 27 W.

Depending on the FPGA workload, you need a USB-PD adapter that can supply higher power. As a recommendation, a typical 65 W USB-PD power adapter used for powering laptops is more than sufficient to fully power the Agilex 3 FPGA/FPGA and SoC C-Series development board for all use cases. Lower USB-PD power adapters can be used for lower power designs.

Note: You must provide a USB-PD Type-C power adapter as it is not supplied with the development kits.

Recommended power adapter:

- Lenovo 65W AC adapter
- Model No: ADLX65YSCC3A

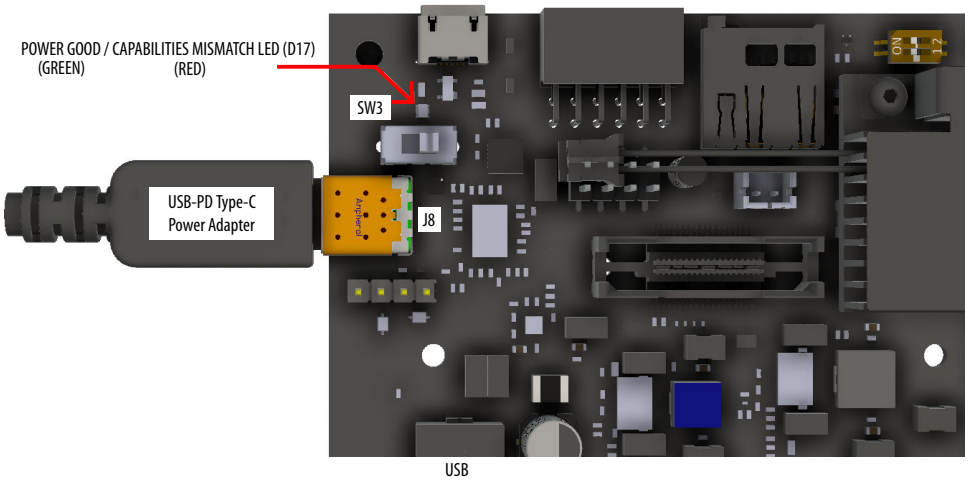
To power up the development board:

1. Connect the USB Type-C end of the USB-PD power adapter to the left edge of the board's USB Type-C mating connector (J8), and connect the other end of the USB-PD adapter to an appropriate wall power outlet.
2. For the Agilex 3 FPGA and SoC C-Series Development Kit, connect the Type-C cable from the USB Type-C connector J2 to the host PC.
3. For the Agilex 3 FPGA and SoC C-Series Development Kit, launch the UART terminal application on the host PC, and follow the setting list:
   - Speed: 115200
   - Data: 8 bit
   - Parity: none
   - Stop bits: 1 bit
   - Flow control: none
4. Set the power switch SW3 (located next to the J8 power connector) to the ON position to turn on the board.
5. When powered on, observe that the board's POWER GOOD green LED (D17) is turned on. If this LED blinks RED, it indicates that the USB-PD power adapter is incompatible with the board. In this event, replace the USB-PD power adapter with a compatible one and try again.

When powered on, the board negotiates an appropriate power contract with the USB-PD adapter. Depending on the capabilities of the USB-PD adapter, an input voltage of 9 V to 20 V is applied to the board.

A successfully negotiated power contract turns on the green POWER GOOD LED. For USB power adapters that are not PD compliant or have insufficient power, the board does not power on and instead the red CAPABILITIES MISMATCH LED blinks or does not turn on. The POWER GOOD and CAPABILITIES MISMATCH LED (D17) are located next to the power switch (SW3).

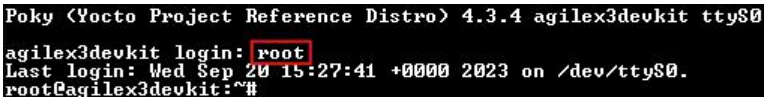
Figure 7. Powering the Agilex 3 FPGA/FPGA and SoC C-Series Development Board



After the POWER GOOD green LED turns on, you can observe the functionality of the development kits:

- On the Agilex 3 FPGA C-Series Development Kit, the QSPI flash is pre-programmed with GPIO image. When powered on, observe that LED D9 is blinking. For more GPIO functions, refer to the *The GPIO Tab* section.
- On the Agilex 3 FPGA and SoC C-Series Development Kit, the QSPI flash is pre-programmed with GHRD image. When powered on, observe the HPS boot-up on the UART terminal.

Figure 8. Linux Log with Username



After Linux boots up, log in using root as username, no password is required.

Related Information

- Development Kit Components on page 42
- System Power on page 64
- The GPIO Tab on page 25

3.3. Modes of Operations

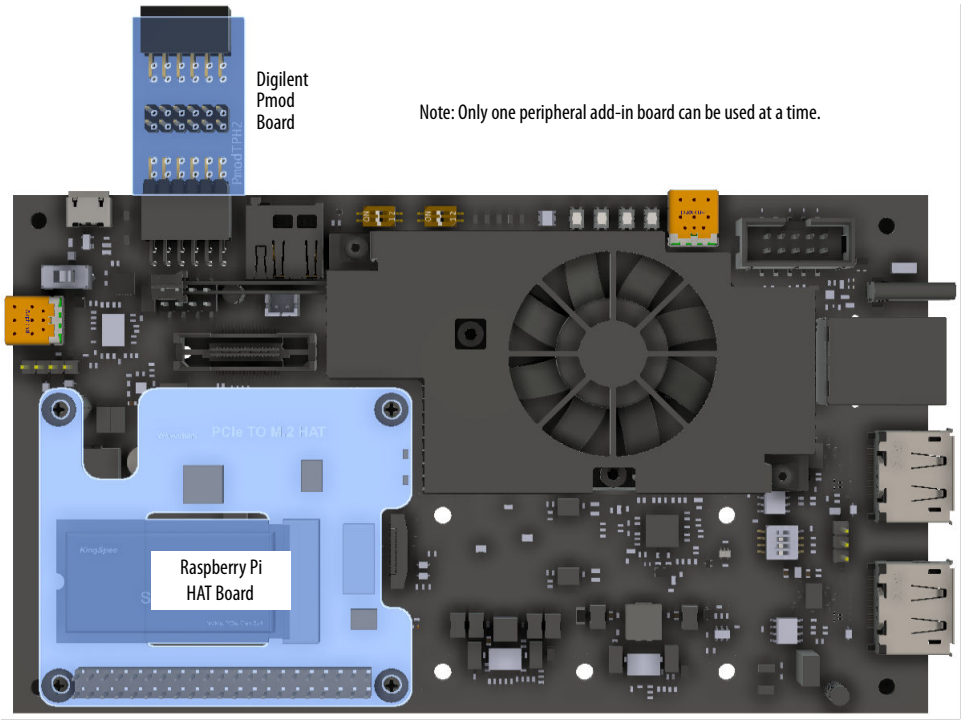
The Agilex 3 FPGA/FPGA and SoC C-Series development board is designed to operate in two main modes—in bench-top mode and as a PCIe add-in card.

In Bench-Top Mode (Default Mode)

You only need to connect a USB-PD compliant power adapter to J8 to power on the board and run the example designs included in the development kit. The example designs allow you to evaluate the functionality of various provided features of this development kit. In this mode, you can also use the Agilex 3 FPGA/FPGA and SoC C-Series development board to interface with and create custom FPGA designs for various Raspberry Pi 4/5 HAT boards and Digilent Pmod* (peripheral module) boards for those respective ecosystems.

Note: The Raspberry Pi HAT board and Digilent Pmod peripherals share the same HVIO banks so only one add-in board can be used at a time.

Figure 9. Optional Raspberry Pi HAT and Digilent Pmod Boards Attached



As a PCIe Add-in Card

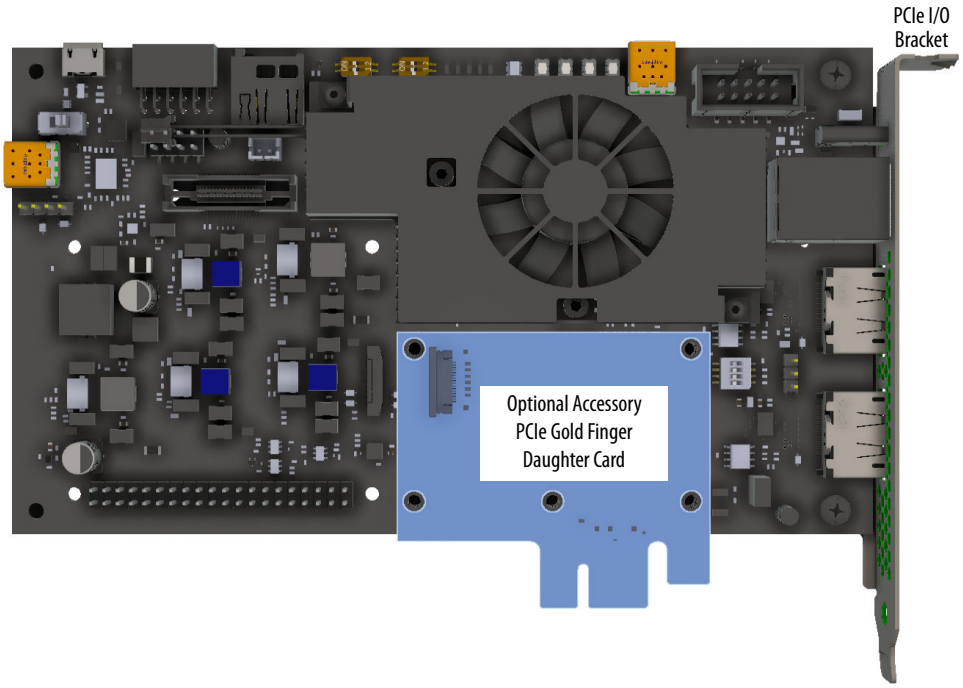
To convert the Agilex 3 FPGA/FPGA and SoC C-Series development board into a PCIe add-in card, you must purchase the optional Altera PCIe 3.0 x1 gold finger daughter card and mount it to this board. The PCIe gold finger daughter card kit includes the PCIe I/O bracket and all necessary hardware to convert the Agilex 3 FPGA/FPGA and SoC C-Series development board into a PCIe add-in card.

Note: Power for the development kit must still be provided by the USB-PD power adapter because the Altera PCIe 3.0 x1 gold finger daughter card does not pass power from the PCIe slot to power the Agilex 3 FPGA/FPGA and SoC C-Series development board.

Table 5. Available PCIe Daughter Cards

Model	Compatible Development Kit
DC-A3PCIE	• DK-A3Y135BM16AEA
DC-A3SOCPCIE	• DK-A3W135BM16AEA • DK-A3Y135BM16AEA

Figure 10. Optional Altera PCIe 3.0 x1 Gold Finger Daughter Board and PCIe I/O Bracket Attached



When operating the card in a PCIe system, insert the card into an available PCIe slot and connect a USB-PD compliant power to connector J8 as described previously. All power for the Agilex 3 FPGA and SoC C-Series Development Kits are derived from the external USB-PD power supply.

Note:

1. When operating as a PCIe add-in card, the board does not power on unless power is supplied to J8 and switch SW3 is ON as described previously.
2. When operating as a PCIe add-in card, Altera does not recommend that you attach a Raspberry Pi HAT because the added height of the HAT board can interfere with the adjacent PCIe cards in the PCIe system.
3. When used as a PCIe add-in card inserted into a PCIe server, Altera does not recommend that you attach additional PCIe cards in adjacent slots of the same server. This is because overcrowding between two adjacent PCIe daughter cards may affect signal performance.

3.4. Performing Board Restore

The Agilex 3 FPGA C-Series Development Kit ships with GPIO design examples stored in the QSPI flash device U51 for the Active Serial (AS) x4 configuration.

The Agilex 3 FPGA and SoC C-Series Development Kit ships with GHRD design examples stored in the QSPI flash device U51 for the Active Serial (AS) x4 configuration.

You must perform board restore using the following instructions through the Quartus Prime Programmer GUI.

3.4.1. Restoring Board QSPI Flash U51 with Default Factory Image on Agilex 3 FPGA C-Series Development Kit

Note: The QSPI flash is pre-programmed with GPIO image. Completing the steps overwrites this image.

1. Open the Quartus Prime Programmer GUI, and click **Auto Detect**.
2. Right click on the FPGA device, and choose **change file** to the `bts_config.jic` under `~factory_recovery` folder.
3. Start the Programmer until it is 100% successful.
4. Power cycle the board and observe that LED `D9` is blinking.

3.4.2. Restoring Board QSPI Flash U51 with Default Factory Image on Agilex 3 FPGA and SoC C-Series Development Kit

Note: The QSPI flash is pre-programmed with GHRD image. Completing the steps overwrites the AS x4 image. Refer to Altera FPGA Developer Site to recover and update GHRD image on QSPI flash.

1. Open the Quartus Prime Programmer GUI, and click **Auto Detect**.
2. Right click on the FPGA device, and choose **change file** to use the GHRD image.
3. Start the Programmer until it is 100% successful.
4. Power cycle the board.

3.4.3. Restoring SD Card with Default Factory Image on Agilex 3 FPGA and SoC C-Series Development Kit

Note: The SD card is pre-programmed with sdimage. Completing the steps overwrites this image. Refer to Altera FPGA Developer Site to recover and update sdimage on SD card.

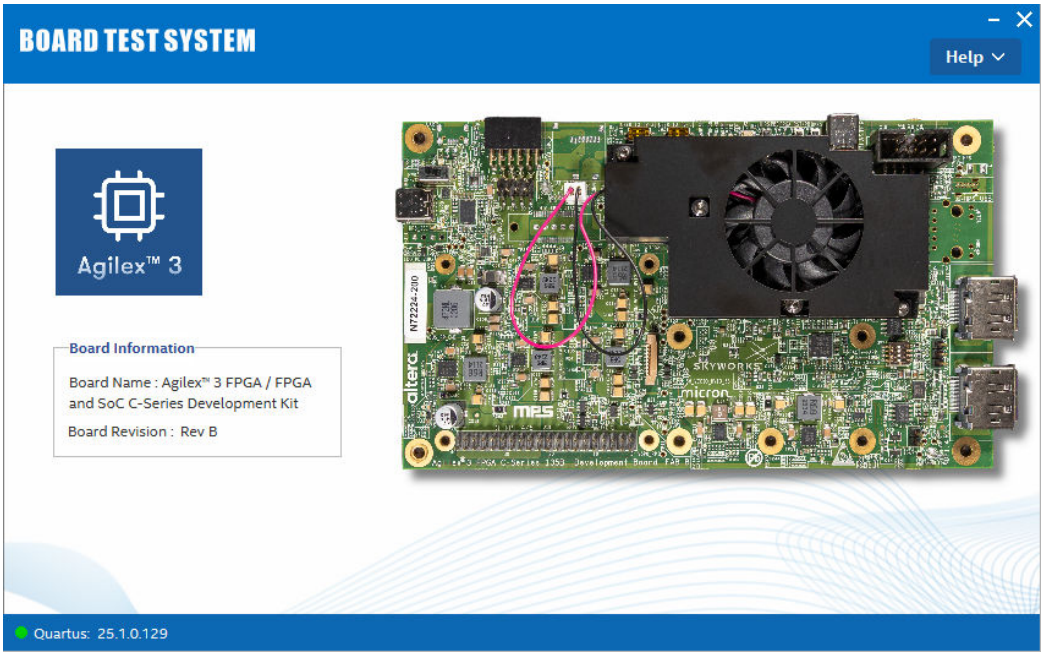
1. Download the SD card image from Altera FPGA Developer Site and extract the archive, obtaining the `.wic` file.
2. Write the SD card image to the micro SD card using Win32DiskImager on Windows*.

4. Board Test System

The Agilex 3 FPGA and SoC C-Series Development Kits include design examples and the Board Test System (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, and observe performance.

The following figure shows the GUI of a board that is in factory configuration.

Figure 11. BTS GUI



4.1. Set Up the BTS GUI Running Environment

4.1.1. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `readme.txt` file in the `examples\board_test_system` directory.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Programmer, the System Console, and the Signal Tap Logic Analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in the **System Properties** in Windows*. The BTS uses this environment variable to locate the Quartus Prime library.

4.1.2. Running the BTS GUI

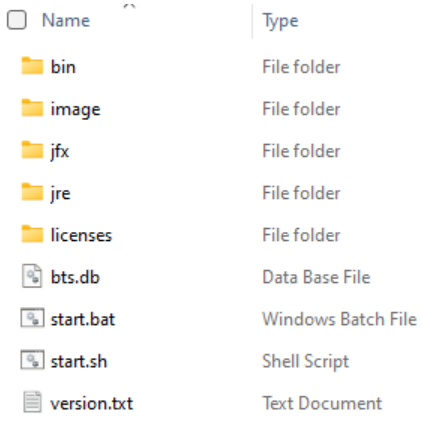
With the power to the board off, follow these steps:

1. Connect the Type-C USB cable to your PC and the board (`J2`).
2. Check the development board switches and jumpers are set according to your preferences. Refer to the Development Kit Setup section.
3. Turn on the board power switch (`SW3`).

Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application.

Navigate to the *<packagedir>*`\examples\board_test_system` directory to run BTS. The BTS release folder always includes the following files.

Figure 12. BTS Package Folder



You can run BTS GUI easily with the following scripts:

1. On **Windows** system, double click the `.bat` files to run BTS GUI.
2. On **Linux** system, set permissions correctly and run the shell script using the following command:

```
# cd $TOP_LEVEL/examples/board_test_system
# chmod +x ./start.sh
# chmod +x -R ./jre/
# sh start.sh
```

After running the start script, the BTS GUI appears, and the running log is saved in the `board_test_system\log` folder.

4.2. BTS Functionalities

This section describes each control in the BTS.

4.2.1. The Agilex 3 FPGA Functionality

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 3 device.

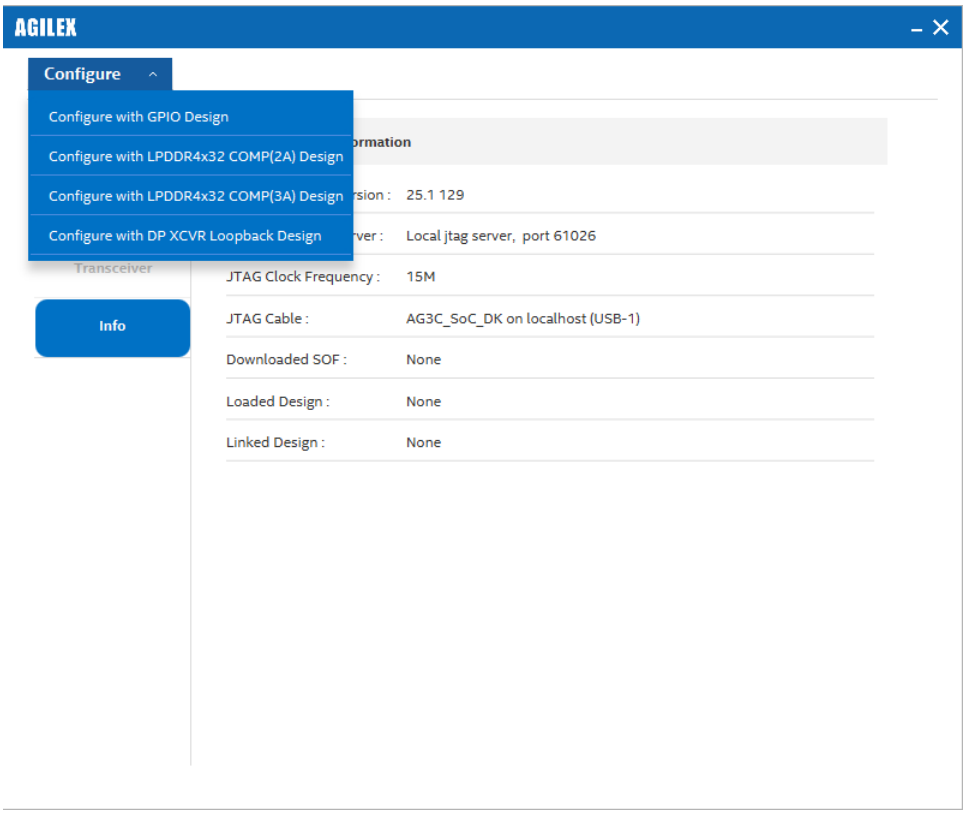
The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

Select the **Agilex** icon on BTS GUI to launch the Agilex 3 FPGA feature.

4.2.1.1. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 13. The Configure Menu



To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (`.sof`) to the FPGA. The download process usually takes less than a minute.

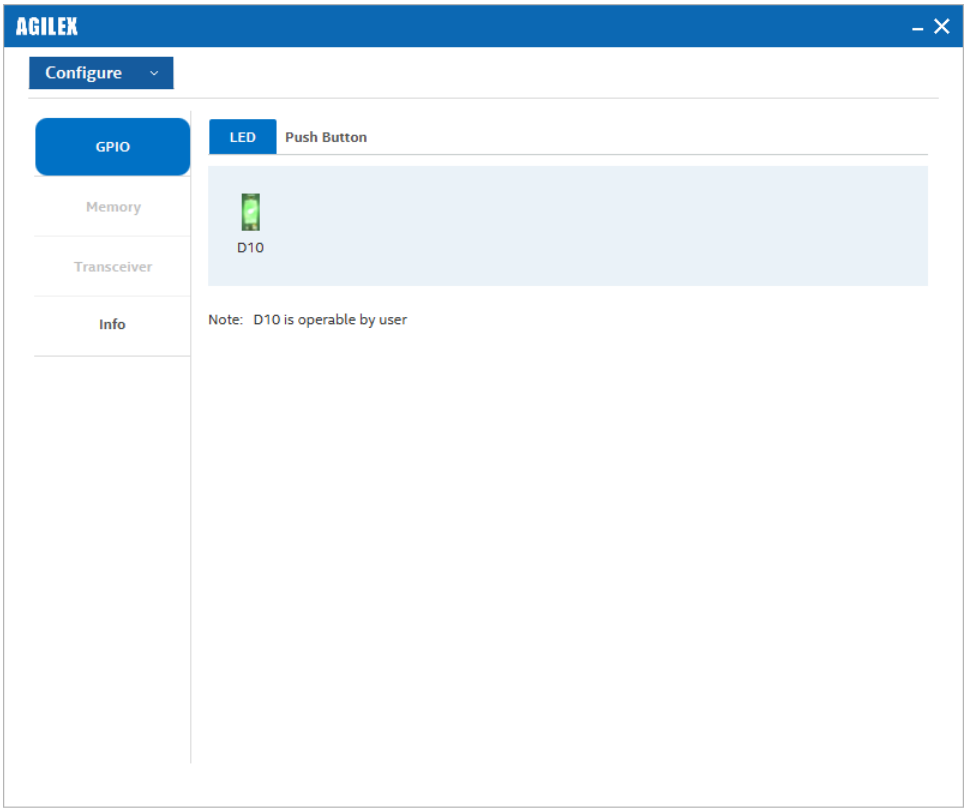
When configuration is completed, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design is now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.2.1.2. The GPIO Tab

The **GPIO** tab allows you to interact with the general-purpose user I/O components on your board. You can turn LED on and off, see the status of push buttons, and detected I^2C slaves on the I^2C bus. Download the design through the BTS **Configure** menu.

4.2.1.2.1. The LED Tab

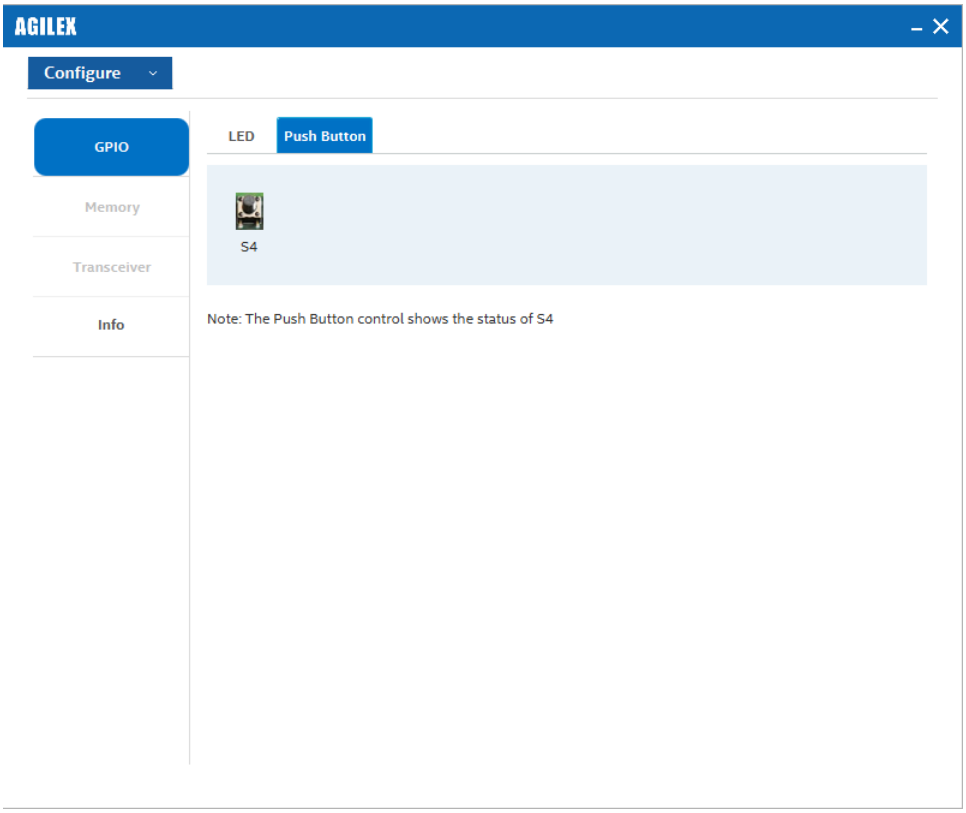
Figure 14. The LED Tab



The **LED** control displays the current state of the user LED. Toggle the LED button to turn the board LED on and off.

4.2.1.2.2. The Push Button Tab

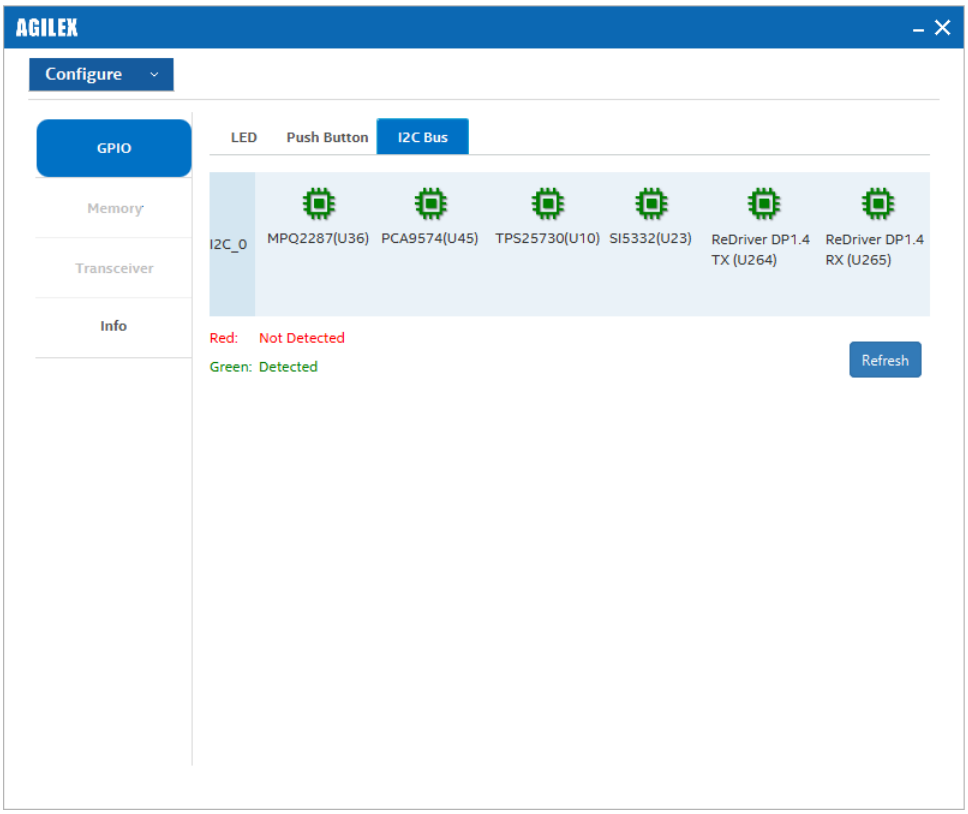
Figure 15. The Push Button Tab



The **Push Button** control shows the status of `S4`.

4.2.1.2.3. The I2C Bus Tab

Figure 16. The I2C Bus Tab



For Agilex 3 FPGA C-Series Development Kit, the BTS GUI can detect the I^2C slaves on the I^2C bus from the Agilex 3 FPGA.

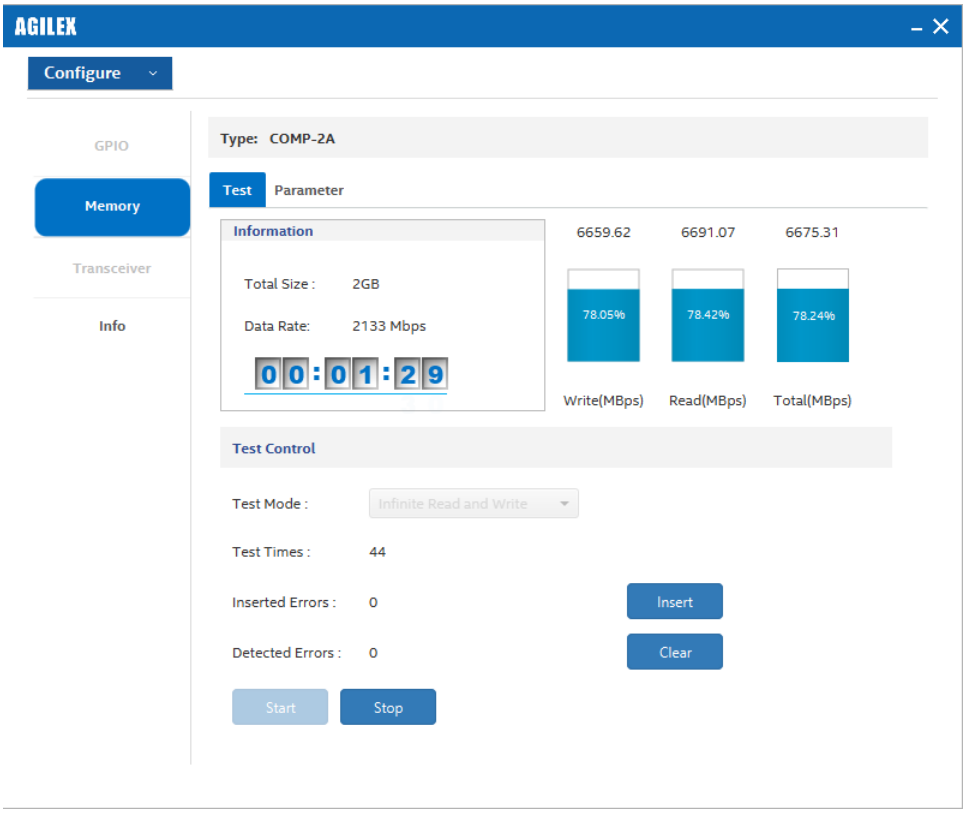
The **I2C Bus** tab shows the detection status.

4.2.1.3. The Memory Tab

This tab allows you to read and write LPDDR4-COMP memory on your board. Download the design through BTS **Configure** menu.

4.2.1.3.1. The Fabric COMP Tab

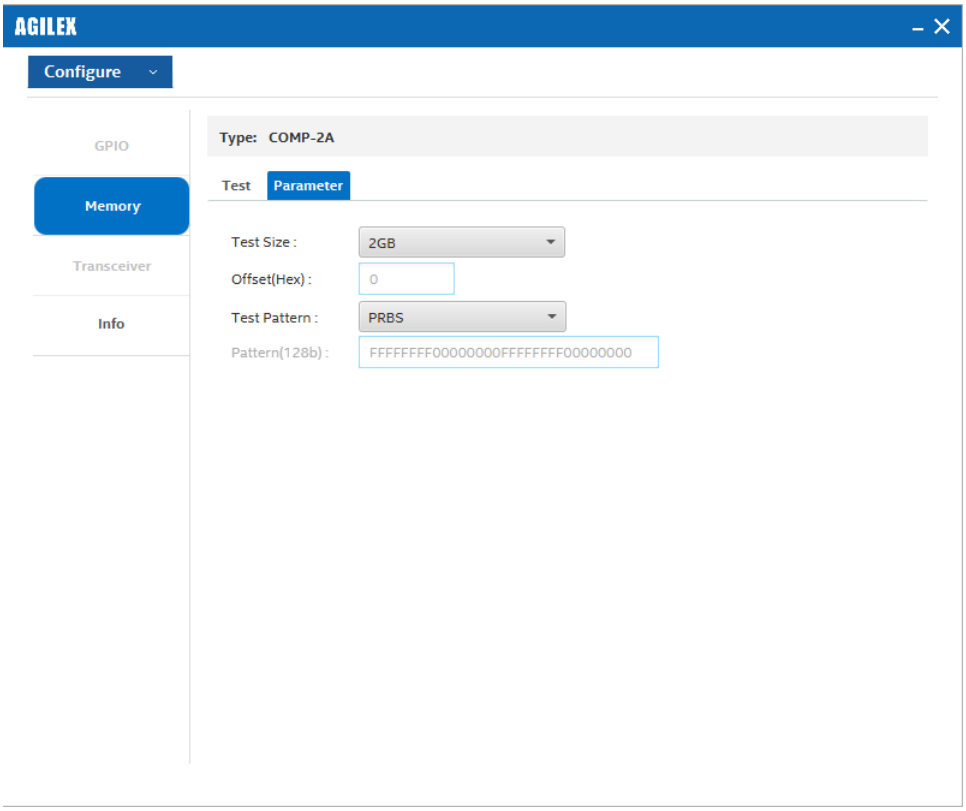
Figure 17. The Fabric COMP Test Tab



The following sections describe controls on this tab.

- **Start**: Initiates LPDDR4 memory transaction performance analysis.
- **Stop**: Terminates transaction performance analysis.
- **Test Control**
  - **Test Mode**: Infinite Read and Write (default), Single Read and Write.
  - **Test times**: Number of times that write and read DDR occurs.
  - **Detected Errors**: Displays the number of data errors detected in the hardware.
  - **Inserted Errors**: Displays the number of errors inserted into the transaction stream.
  - **Insert**: Inserts a one-word error into the transaction stream each time you click the button. **Insert** is only enabled during transaction performance analysis.
  - **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.
- **Performance Indicators**: These controls display current transaction performance analysis information collected since you last clicked **Start**:
  - **Write**, **Read**, and **Total Performance** bars: Show the percentage (%) of maximum theoretical data rate that the requested transactions are able to achieve.
  - **Write (MBps)**, **Read (MBps)**, **Total (MBps)**: Show the number of bytes analyzed per second.

Figure 18. The Fabric COMP Parameter Tab



- **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, 1 GB, and 2 GB (default).
- **Offset (Hex)**: You can define the memory start address to test.
- **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

4.2.1.3.2. The HPS/Fabric COMP Tab

The **HPS/Fabric COMP** tab shares the same settings with the **Fabric LPDDR4 COMP** tab.

Figure 19. The HPS/Fabric COMP Test Tab

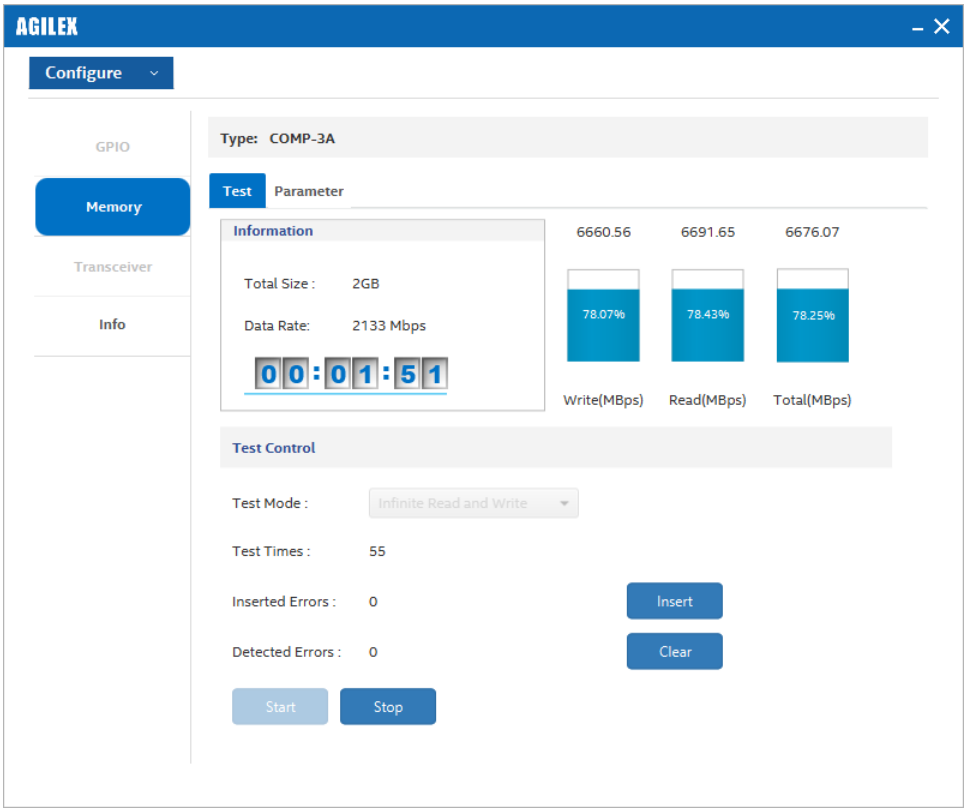
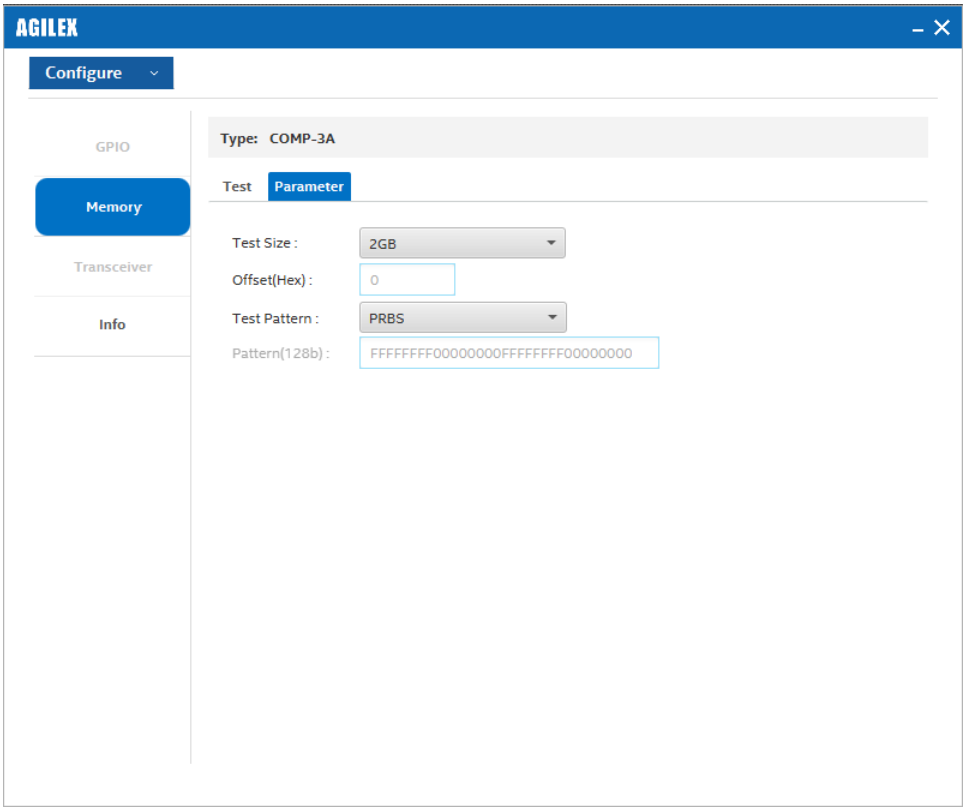


Figure 20. The HPS/Fabric COMP Parameter Tab



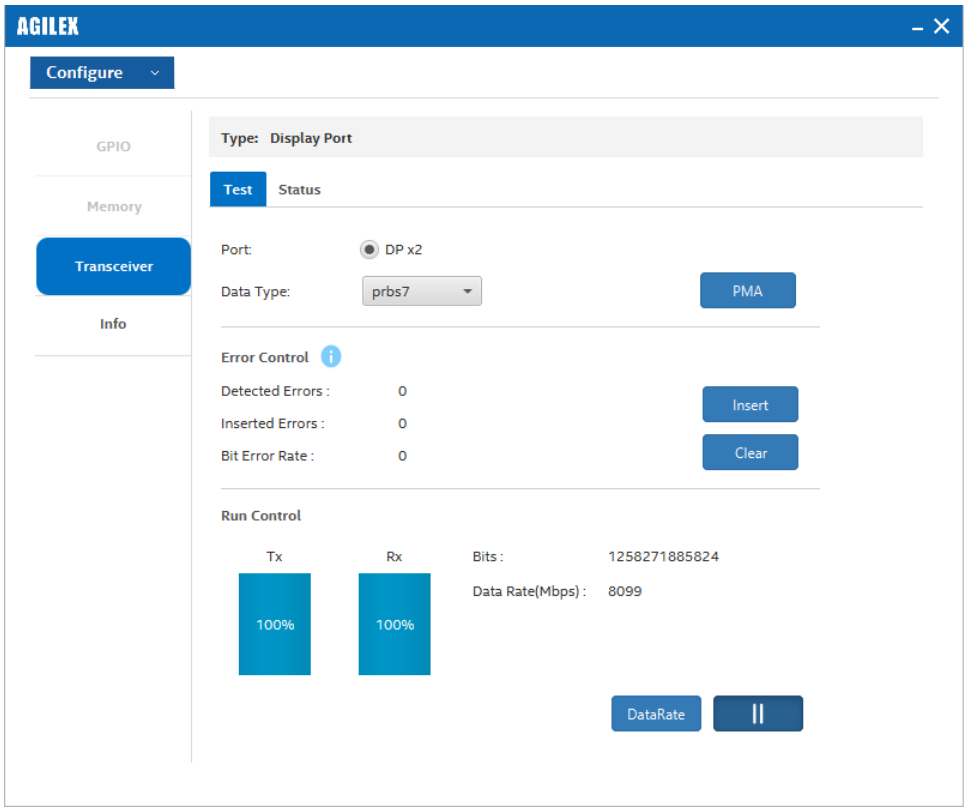
4.2.1.4. The Transceiver Tab

The Transceiver tab allows you to run transceiver tests on your board.

The following port test is available—**DP x2**.

4.2.1.4.1. The DP Tab

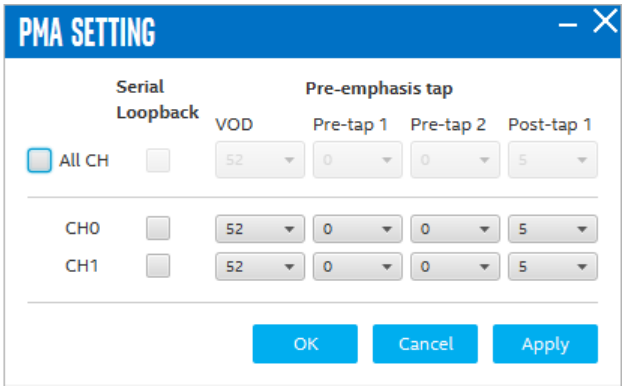
Figure 21. The DP Test Tab



Use the following controls to select an interface to apply PMA settings, data type, and error control.

- **Port**: Allows you to specify which interface to test. The following port test is available:
  - **DP x2**
- **PMA Setting**: This setting allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:
  - **Serial Loopback**: Displays the signal status between the transmitter and the receiver.
  - **VOD**: Specifies the voltage output differential of the transmitter buffer.
  - **Pre-emphasis tap**:
    - **Pre-tap 1**: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
    - **Pre-tap 2**: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
    - **Post-tap 1**: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 22. DP Test—PMA Setting



- **Data Type**: The **Data Type** control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:
  - **PRBS7**: Pseudo-random 7-bit binary sequences
  - **PRBS15**: Pseudo-random 15-bit binary sequences
  - **PRBS23**: Pseudo-random 23-bit binary sequences
  - **PRBS31**: Pseudo-random 31-bit binary sequences

- **Error Control**: This control displays data errors detected during analysis and allows you to insert errors:
  - **Detected Errors**: Displays the number of data errors detected in the received bit stream.
  - **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
  - **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
  - **Insert**: Inserts a one-word error into the transmit data stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
  - **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.
- **Run Control**
  - **TX and RX performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions can achieve.
  - **Start**: This control initiates the loopback tests.
  - **Data Rate**: Displays the XCVR type and data rate of each channel.

Figure 23. DP Test—Data Rate

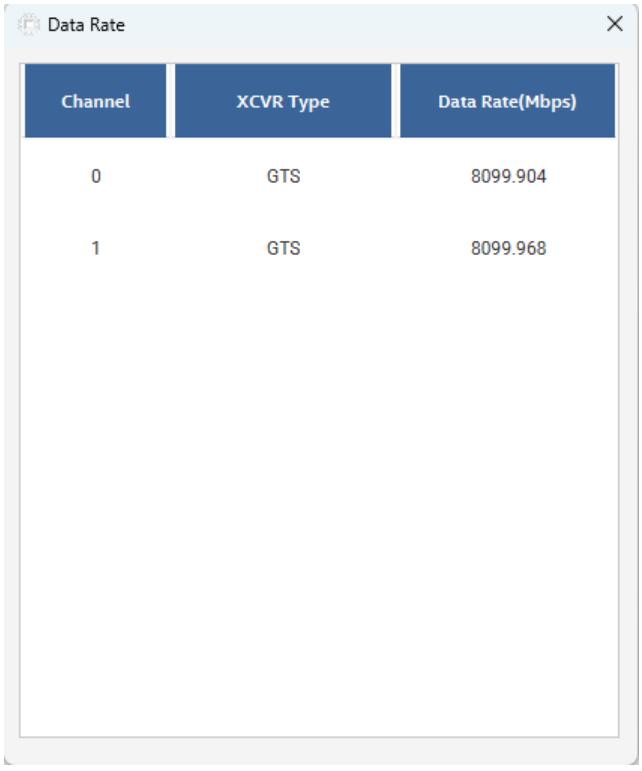
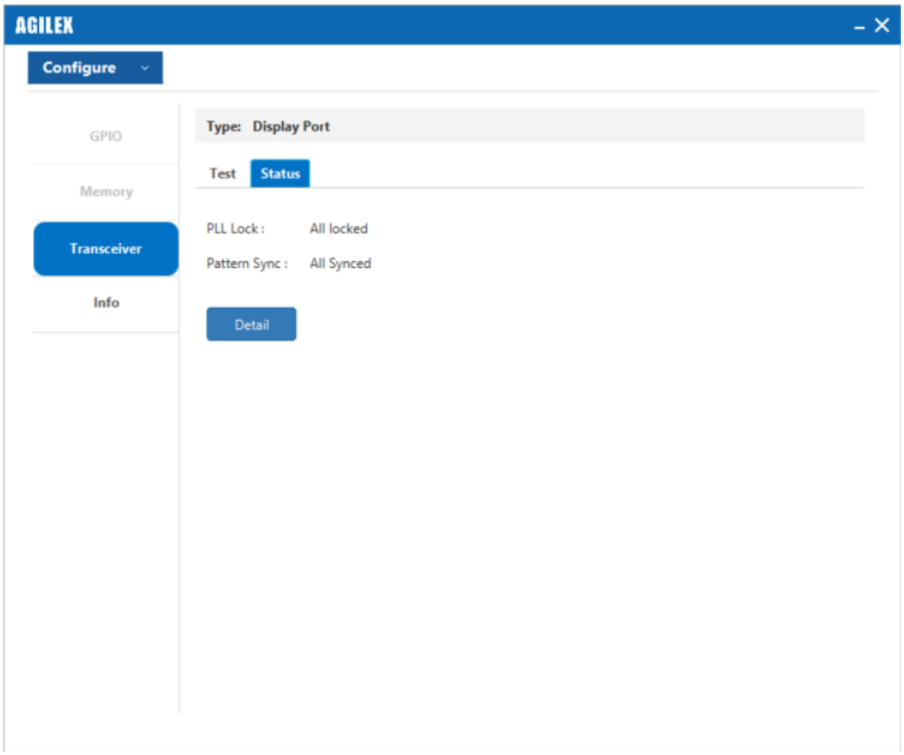


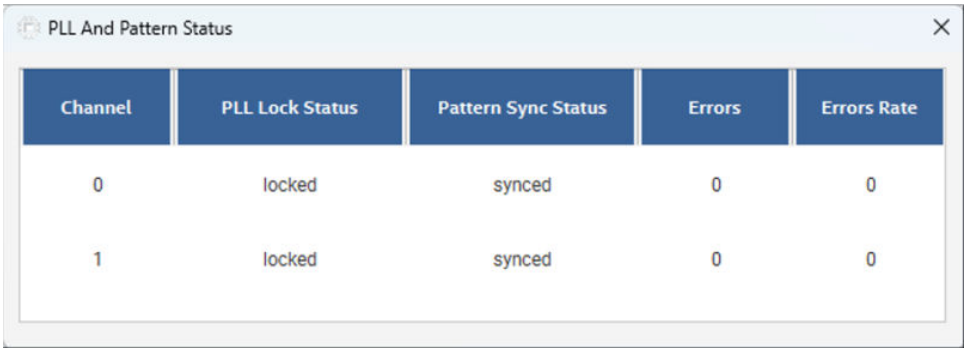
Figure 24. The DP Status Tab



The **Status** tab displays the following status information during the loopback test:

- **PLL Lock**: Shows the PLL locked or unlocked state.
- **Pattern Sync**: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail**: Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

Figure 25. DP Status—PLLand Pattern Status



4.2.2. Other Functionalities

4.2.2.1. The Bottom Information Bar

The bottom information bar shows the recognized Quartus Prime software version.

- **Quartus Prime Version**: Displays the current installed and active Quartus Prime software version on your system. The text turns red if your version is older than the required version. Change the `QUARTUS_ROOTDIR` environment variable to the required version.

5. Development Kit Hardware and Configuration

The Agilex 3 FPGA and SoC C-Series Development Kits can support multiple configuration modes as listed in the following table. You need to change either the hardware setting or re-program system images, or both, for these cases.

The configuration modes are set by resistor strappings on the board. The default configuration is AS x4 (Fast) using a 512 Mb QSPI flash device, and under normal use cases, you should not need to change the default configuration settings. However, to change configuration modes, you must modify the resistor strappings on the board. Refer to the board schematics for detailed information.

Table 6. Supported Configuration Modes

MSEL2	MSEL1	MSEL0	Configuration Mode
1	1	1	JTAG
0	0	1	AS x4 (Fast) (Default)
0	1	1	AS x4 (Normal)

5.1. Configuring the FPGA and Accessing HPS Debug Access Port by JTAG

Note: The configuration mode defaults to AS x4 fast mode.

1. Plug the USB Type-C cable to J2 or USB-Blaster dongle to J4.

   Note: If both J2 and J4 are connected, the on-board USB-Blaster III (J2) is disabled and the Blaster dongle connected to J4 takes precedent.
2. Open the Quartus Prime Programmer to configure the FPGA.
3. For the Agilex 3 FPGA and SoC C-Series Development Kit, open the Ashling* RiscFree* Integrated Development Environment (IDE) to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

5.2. Configuring the FPGA Device by Active Serial (AS) Modes (Default Mode)

Note: The AS x4 fast mode is the default configuration mode for the board shipped from factory.

Power on the board. The FPGA configures itself with the programming file stored within the QSPI flash (U51) connected directly to the FPGA SDM interface.

6. Custom Projects for the Development Kit

6.1. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, define I/O standard, direction and general termination.

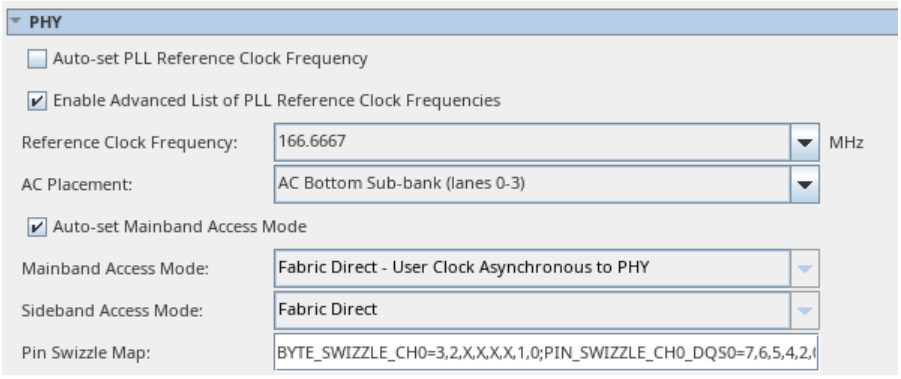
1. Define a macro to enable or disable the corresponding interface in the top-level design entity, and the interfaces that require IP connection are disabled by default.
2. Open the macro according to the requirements. If the pins are not connected to the IP, a fitter error occurs.

6.2. EMIF Pin Swizzling Setting

DQ pins within a DQS group or/and DQS group are swapped to simplify board design.

To achieve the swizzling, you must enter the swizzling setting in the **Pin Swizzle Map** field in the **PHY** section of the **High-level Configuration IP Parameters** tab in the External Memory Interfaces (EMIF) IP parameter editor.

Figure 26. Entering a PIN_SWIZZLE Specification



1. For LPDDR4 bank 2A, use the following settings:

```
BYTE_SWIZZLE_CH0=1,0,X,X,X,X,2,3;
PIN_SWIZZLE_CH0_DQS0=0,1,3,2,6,7,4,5;
PIN_SWIZZLE_CH0_DQS1=15,14,13,12,9,11,8,10;
PIN_SWIZZLE_CH0_DQS2=19,20,21,18,17,16,23,22;
PIN_SWIZZLE_CH0_DQS3=25,30,24,31,27,26,28,29;
```

2. For LPDDR4 bank 3A, use the following settings:

```
BYTE_SWIZZLE_CH0=3,2,X,X,X,X,1,0;
PIN_SWIZZLE_CH0_DQS0=1,0,3,2,4,7,6,5;
PIN_SWIZZLE_CH0_DQS1=9,15,14,13,8,11,10,12;
PIN_SWIZZLE_CH0_DQS2=19,18,20,21,16,23,22,17;
PIN_SWIZZLE_CH0_DQS3=26,27,24,25,30,31,28,29;
```

Related Information

External Memory Interfaces (EMIF) IP User Guide: Agilex 3 FPGAs and SoCs

7. Document Revision History for the Agilex 3 FPGA and SoC C-Series Development Kits User Guide

Document Version	Changes
2025.09.02	• Added new topic—*Ashling* RiscFree* Integrated Development Environment (IDE)*. • Updated *Installing the USB-Blaster III Driver*. • Updated step 2 in *Powering Up the Development Board*. • Updated *Modes of Operations*: — Added new Table: *Available PCIe Daughter Cards*. — Updated information about the PCIe add-in card. • Updated the steps in *Configuring the FPGA and Accessing HPS Debug Access Port by JTAG*. • Updated appendix topic *Board Overview*: — Updated Figure: *Components in Agilex 3 FPGA/FPGA and SoC C-Series Development Kit (Top View)*. — Updated the note about HPS UART in Agilex 3 FPGA and SoC C-Series version of the development kit. • Updated the appendix topic *Board Components:* — Updated the description for the onboard USB-Blaster III cable (J2) in Table: *Configuration, Setup, and Status Elements*. — Removed HPS UART interface information in Table: *Configuration, Setup, and Status Elements*. — Updated board reference for UART in Table: *HPS Components and Ports* from U1 to J2. • Added new appendix topic—*Expansion Boards*. • Updated document for the latest branding standards.
2025.05.15	Initial release.

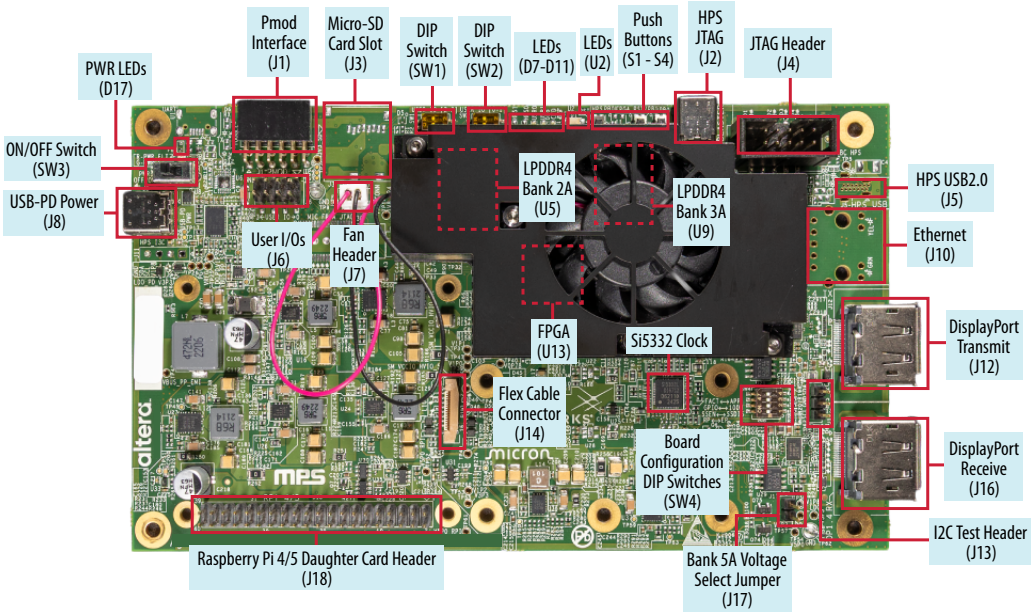
A. Development Kit Components

A.1. Board Overview and Components

This section describes the key components on the development board. A complete set of schematics, a physical layout database, and Gerber files for the development board reside in the development kit documents directory.

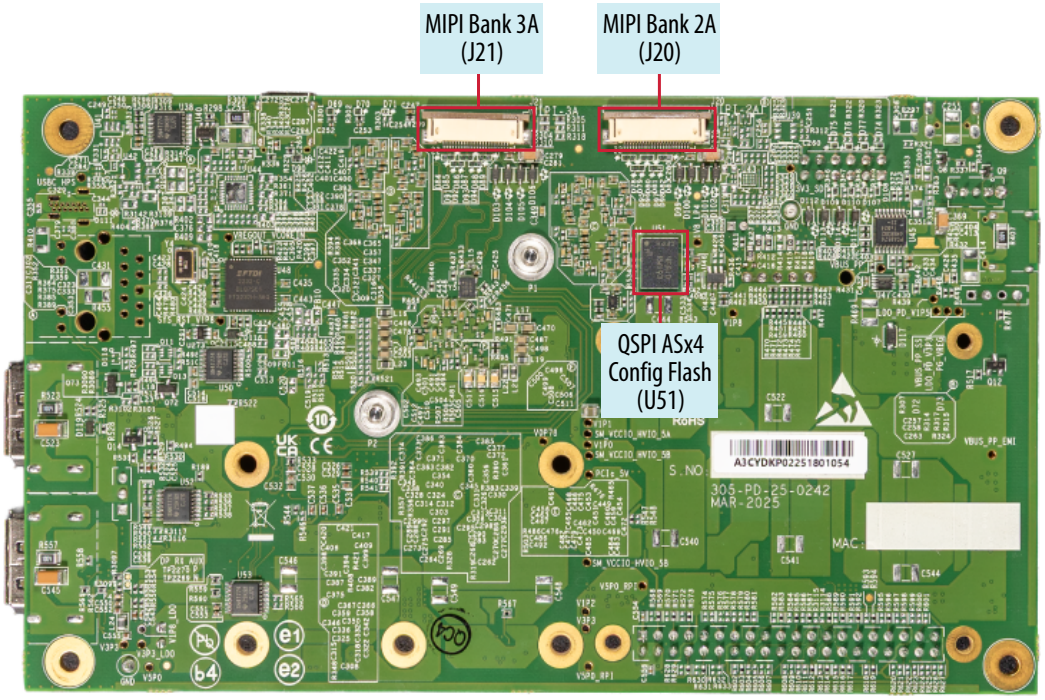
A.1.1. Board Overview

Figure 27. Components in Agilex 3 FPGA/FPGA and SoC C-Series Development Kit (Top View)



Note: The HPS UART (J2), Micro-SD card slot (J3), HPS USB2.0 (J5), and Ethernet (J10) are only available on the Agilex 3 FPGA and SoC C-Series version of the development kit.

Figure 28. Components in Agilex 3 FPGA/FPGA and SoC C-Series Development Kit (Bottom View)



A.1.2. Board Components

Table 7. Featured Devices

Board Reference	Type	Description
U13	FPGA	Agilex 3 FPGA C-Series, A3CY135BM16AE6S or Agilex 3 FPGA and SoC C-Series, A3CW135BM16AE6S • 135K logic elements (LE) • 46.8K adaptive logic elements (ALM) • 13,272 M20K blocks • 45,640 MLABs • 188 DSP blocks • 212 GPIOs

Table 8. Configuration, Setup, and Status Elements

Board Reference	Type	Description
J8	USB-PD compliant power input	USB Type-C input for connecting a USB-PD compliant power adapter capable of providing 27 W (min) for powering the Agilex 3 FPGA/FPGA and SoC C-Series Development Kit. For full-load operation, Altera recommends you use a 65 W USB-PD compliant power adapter to cover all workload use cases.
SW3	Power on slide switch	This switch turns on and off the board.
D17	Power status LED	This bicolor (Red/Green) LED indicates the status of the board power. This LED blinks green when the board is powered up successfully. This LED is off, or blinks red when insufficient

continued...

Board Reference	Type	Description
		power is applied to the board. When the LED blinks red, the USB-PD power contract negotiation was unsuccessful due to an incompatible USB power adapter.
J2	Onboard USB-Blaster III cable	1. USB Type-C connector to FTDI FT2232H JTAG converter for programming and debugging the FPGA. 2. USB Type-C connector to FTDI FT2232H UART converter for the HPS 2-wire UART interface.
J4	10-pin JTAG programming header	Programming header for connecting an USB-Blaster II/USB-Blaster III programming dongle. When the external dongle is used, the onboard programming feature (FTDI FT2232H) is automatically disabled.
SW1[1:0]	USER DIP switches 0 and 1	General-purpose USER DIP switches 0 and 1
SW2[1:0]	USER DIP switches 2 and 3	General-purpose USER DIP switches 2 and 3
D7	Dedicated HPS LED 1	One of two green LEDs connected to the FPGA's HPS I/O. The HPS LED1 is connected to HPS_GPIO0_IO11 (U13, pin A26).
D8	Dedicated HPS LED 0	One of two green LEDs connected to the FPGA's HPS I/O. The HPS LED0 is connected to HPS_GPIO0_IO0 (U13, pin B29).
D9	Dedicated USER LED 0	One of two green USER LEDs connected to the FPGA's I/O bank 3A. USER LED 0 is connected to U13 pin K1.
D10	Dedicated USER LED 1	One of two green USER LEDs connected to the FPGA's I/O bank 3A. USER LED 1 is resistor muxed with the transmit DisplayPort's CONFIG_SENSE control signal. USER LED 1 is configured by default and connected to U13 pin L2.
D11	Configuration Done LED	Green LED to indicate successful FPGA configuration. This LED is turned on when the FPGA is successfully configured. This LED is turned off when the FPGA is unconfigured.
U2	Tricolor Status LED for onboard USB-Blaster III cable	This tricolor LED (red, green, blue) provides status information for the onboard USB-Blaster III.
S1	HPS COLD RESETn push button	Dedicated active low HPS COLD RESETn push button. Pushing and releasing this button generates a 20 ms active low pulse to the HPS_COLD_RESETn input of the FPGA.
S2	General-purpose HPS push button	Dedicated general-purpose tactile push button for the HPS interface. • Pushing this button drives the HPS push button input logic low. • Releasing this button drives the HPS push button input logic high.
S3	General-purpose USER push button	USER dedicated general-purpose tactile push button (PB1/FPGA_RSTN) connected to HSIO bank 3A, pin M1. This pin can be used as a general-purpose push button or as a FPGA RESET push button for user designs. • Pushing this button drives the USER push button PB1/FPGA_RSTN input logic low. • Releasing this button drives the USER push button PB1/FPGA_RSTN input logic high.
S4	General-purpose USER push button	USER dedicated general-purpose tactile push button (PB0) connected to HSIO bank 3A, pin L1. • Pushing this button drives the USER push button PB0 input logic low. • Releasing this button drives the USER push button PB0 input logic high.

continued...

Board Reference	Type	Description
J6	General-purpose USER IO[3:0]	Four dedicated general-purpose USER IO[3:0] with pull-up resistors on even numbered pins 2, 4, 6, and 8. Odd numbered pins 1, 3, 5, and 7 are connected to the board ground.
J1	Pmod interface	12-pin Digilent Pmod* interface for connecting standard Digilent Pmod I/O Interface boards.
J3	Micron-SD card slot	Micro-SD card slot for the HPS interface
J5	USB-C 2.0 interface	USB 2.0 DRP (Dual Role Port) Type-C connector for the HPS interface
J10	RJ45 Ethernet interface	10/100/1000 Ethernet for the HPS interface
J12	DisplayPort transmit interface	DisplayPort v1.4 transmitter interface connected to the FPGA's transceiver bank 1A, lanes[1:0]. Each lane of this interface is capable of 8.1 Gbps data rates.
J16	DisplayPort receive interface	DisplayPort v1.4 receiver interface connected to the FPGA's transceiver bank 1A, lanes[1:0]. Each lane of this interface is capable of 8.1 Gbps data rates.
SW4[1:4]	DIP Switches	Board configuration DIP switch SW4.1 This feature is used in conjunction with the optional PCIe 3.0 x1 gold finger daughter card (End-point), or a Raspberry Pi5 M.2 HAT board (Root-port). • OFF—Sets the board to function as a PCIe end-point • ON—Sets the board to function as a PCIe root port
		Board configuration DIP switch SW4.2 This feature is used in conjunction with the optional PCIe 3.0 x1 gold finger daughter card (End-point), or a Raspberry Pi5 M.2 HAT board (Root-port). • OFF—Enables the -0.5% spread spectrum modulation for the PCIe clock • ON—Disables the -0.5% spread spectrum modulation for the PCIe clock
		Board configuration DIP switch SW4.3 • OFF—Connects a 100 MHz clock to the HVIO bank 5B, pin AJ27 • ON—Connects the Raspberry Pi GPIO26 to HVIO bank 5B, pin AJ27
		SW4.4 • OFF—Sets the FPGA to load the USER Application Image from QSPI flash • ON—Sets the FPGA to load the Factory Recover Image from QSPI flash
J17	Voltage selection jumper	Voltage selection jumper for HVIO bank 5A • Shunting J17 sets the HVIO bank 5A voltage to 1.8 V • Leaving J17 open sets the HVIO bank 5A voltage to 3.3 V

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Board Reference	Type	Description
J14	Flex cable connector	Flex cable connector for the FPGA transceiver bank 1A, lane 0. Options: • Connect the flex cable provided with the optional PCIe 3.0 x1 gold finger expansion daughter card to J14 to convert the Agilex 3 FPGA/FPGA and SoC C-Series Development Kit into a PCIe adapter card. • Connect the flex cable provided with a Raspberry Pi 5 M.2 HAT daughter board to J14 to interface Raspberry Pi 5 daughter cards to the Agilex 3 FPGA/FPGA and SoC C-Series Development Kit.
J18	Raspberry Pi 4/5 HAT interface	40-pin header for mounting a Raspberry Pi 4/5 HAT daughter board. For Raspberry Pi 5, you should also connect the flex cable to J14.
J20	MIPI bank 2A connector	22-pin FPC MIPI interface connected to bank 2A
J21	MIPI bank 3A connector	22-pin FPC MIPI interface connected to bank 3A

Table 9. Featured Devices

Board Reference	Type	Description
U23	Si5332 I^2C programmable clock generator	Default frequencies: • Out 0—100 MHz CMOS-3.3V for HVIO bank 5B reference clock • Out 1—166.67 MHz LVDS-1.8V for LPDDR4 bank 2A reference clock • Out 2—166.25 MHz LVDS-1.8V for LPDDR4 bank 3A reference clock • Out 3—250 MHz LVDS-1.8V converted to LVCMOS-1.1V for bank 3A PTP reference clock • Out 4—125 MHz CMOS-1.8V converted to LVCMOS-1.1V for bank 2A TOD reference clock • Out 5—10 MHz CMOS-1.8V converted to LVCOMS-1.1V for bank 2A PPS reference clock • Out 6—150 MHz LVDS-1.8V for MIPI bank 2A reference clock • Out 7—150 MHz LVDS-1.8V for MIPI bank 3A reference clock • Out 8—150 MHz LVDS-1.8V for DisplayPort bank 1A reference clock • Out 9—100 MHz PCIe end-point reference clock connected to FPGA bank 1A • Out 10—Not Used • Out 11—100 MHz PCIe root-port reference clock connected to J14 for the Raspberry Pi 5 M.2 HAT daughter board
Y5	Si510 clock oscillator	100 MHz CMOS-1.8V configuration clock connected to the SDM
Y1	Si510 clock oscillator	25 MHz CMOS-1.8V HPS clock

Table 10. Transceiver Interfaces

Board Reference	Type	Description
J14	PCIe x1 connected to flex cable connector	PCIe TX/RX x1 interface from FPGA bank 1A, lane 0 connected to a flex cable connector (J14). This PCIe 3.0 x1 interface can be used for the optional PCIe x1 gold finger daughter card or Raspberry Pi 5 daughter card.
J12	DisplayPort transmit connector	Two TX channels from FPGA bank 1A, lanes 2 and 3 used for DisplayPort transmit interface
J16	DisplayPort receive connector	Two RX channels from FPGA bank 1A, lanes 2 and 3 used for DisplayPort receive interface

Table 11. Memory Devices

Board Reference	Type	Description
U5	LPDDR4 DRAM	LPDDR4 x32 component on bank 2A for FPGA fabric
U9	LPDDR4 DRAM	LPDDR4 x32 component on bank 3A for HPS/FPGA fabric
U51	512 Mbit QSPI flash	FPGA AS x4 configuration flash

Table 12. Communication Ports

Board Reference	Type	Description
J4	10-pin JTAG header	For connecting to an external USB-Blaster II/USB-Blaster III dongle
J2	USB Type-C to JTAG connector	For connecting to the onboard USB-Blaster III to a host PC for JTAG programming of the FPGA

Table 13. Miscellaneous Ports

Board Reference	Type	Description
J7	FAN header	2-pin 5 V FAN header for the FPGA heatsink/fan
J11	Test header	For Altera internal testing only
J13	I^2C test header	3.3 V I^2C test header connected to the HPS IO48 interface

Table 14. HPS Components and Ports

Board Reference	Type	Description
J5	USB-C 2.0 Dual Role Port (DRP)	USB Type-C connector for USB2.0 interface connected to the HPS IO48 interface
J10	10/100/1000 Ethernet	Triple-Speed Ethernet connected to the HPS IO48 interface. This interface supports USB Dual Role Port (DRP).
J2	UART	2-wire UART connected to the HPS IO48 interface
J13	I^2C test header	3.3 V I^2C test header connected to the HPS IO48 interface
J3	Micro-SD card slot	Micro-SD card slot connected to the HPS IO48 interface
J9	Mictor test connector	For Altera testing only. This feature is depopulated by default on the board.
J11	I^3C test header	For Altera testing only. This feature is depopulated by default on the board.

continued...

Board Reference	Type	Description
D8	HPS LED0	HPS dedicated LED connected to the HPS IO48 interface
D7	HPS LED1	HPS dedicated LED connected to the HPS IO48 interface
Y1	HPS clock	25 MHz oscillator for the HPS interface
S2	HPS push button	HPS dedicated push button connected to the HPS IO48 Interface

Table 15. Expansion Ports

Board Reference	Type	Description
J1	Pmod	Expansion interface for optional Digilent Pmod* boards connected to HVIO bank 5A.
J18	Raspberry Pi	Expansion interface for optional Raspberry Pi 4/5 HAT boards connected to HVIO banks 5A and 5B. Raspberry Pi 4 HAT boards only use the J18 expansion port. Raspberry Pi 5 HAT boards use J18 and J14 expansion ports.
J14	Flex cable	Expansion interface for optional PCIe 3.0 x1 gold finger daughter board and Raspberry Pi 5 HAT boards. Raspberry Pi 4 HAT boards only use the J18 expansion port. Raspberry Pi 5 HAT boards use J18 and J14 expansion ports.

Table 16. Power Supplies

Board Reference	Type	Description
J8	USB-PD Type-C power input	Input power range: 9 V @ 3 A to 20 V @ 3.25 A
U10	Texas Instruments TPS25730	USB-PD sink controller
U12	Texas Instruments LM73100	Inrush, reverse polarity, and overvoltage protection controller
U37	Monolithic Power Systems MPQ4731	5 V DC-DC buck regulator
U27	Monolithic Power Systems MPQ4731	3.3 V DC-DC buck regulator
U36	Monolithic Power Systems MPQ2287	0.78 V DC-DC buck regulator for FPGA power
U24	Monolithic Power Systems MPQ4324	1.0 V DC-DC buck regulator for FPGA power
U16	Monolithic Power Systems MPQ4324	1.8 V DC-DC buck regulator for FPGA power
U26	Monolithic Power Systems MPQ4324	1.2 V DC-DC buck regulator for FPGA power
U215	Monolithic Power Systems MPQ4371	1.1 V DC-DC buck regulator for FPGA power
U46	Texas Instruments TPS22917	1.8 V load switch for LPDDR4 memory
U32	Texas Instruments TPS22917	3.3 V load switch for FPGA HVIO bank 5B
U30	Texas Instruments TPS22917	3.3 V load switch for FPGA HVIO bank 5A
U35	Texas Instruments TPS22917	1.8 V load switch for FPGA HVIO bank 5A
U31	Monolithic Power Systems MP5036	5.0 V load switch for Raspberry Pi header
U39	Texas Instruments TPS22917	3.3 V load switch for Micro-SD card slot
U22	Texas Instruments TLV75518	1.8 V LDO for clock power (optional, DNI by default)
U28	Texas Instruments TLV75533	3.3 V LDO for clock power (optional, DNI by default)

A.2. Input and Output Components

A.2.1. Push Buttons

The Agilex 3 FPGA/FPGA and SoC C-Series development board includes dedicated user push buttons. When you press and hold down the button, the device pin is set to logic 0. When you release the button, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 17. Push Buttons

Board Reference	Description	Schematic Signal Name	I/O Standard
S1	HPS COLD RESET tactile push button. Pushing and releasing S1 generates a 20 ms active low pulse to the HPS_COLD_RESETn input of the FPGA.	BTN_RST_N	1.8 V
S2	Dedicated general-purpose tactile push button for the HPS interface. • Pushing this button drives the HPS push button input logic low • Releasing this button drives the HPS push button input logic high	HPS_PUSHBUTTON0	1.8 V
S3	User dedicated general-purpose tactile push button (PB1/FPGA_RSTN) connected to HSIO bank 3A, pin M1. This pin can be used as a general-purpose push button or as an FPGA RESET push button for user designs. • Pushing this button drives the user push button PB1/FPGA_RSTN input logic low • Releasing this button drives the user push button PB1/FPGA_RSTN input logic high	IO96_3A_PB1_FPGA_RST_N	1.1 V
S4	User dedicated general-purpose tactile push button (PB0) connected to HSIO bank 3A, pin L1. • Pushing this button drives the user push button PB0 input logic low • Releasing this button drives the user push button PB0 input logic high	IO96_3A_PB0	1.1 V

A.2.2. Switches

The Agilex 3 FPGA/FPGA and SoC C-Series development board includes user-controlled DIP switches for selecting various features on the board. When the switch is in the ON position, logic 0 is selected. Note that the USER_IO_SWITCH[3:0] switches are accessible with an I^2C I/O expander (U45) connected to the HPS and FPGA HVIO bank.

Table 18. Switches

Board Reference	Description	Schematic Signal Name	I/O Standard
SW1.1	General-purpose user DIP switches 2	USER_IO_SW2	3.3 V
SW1.2	General-purpose user DIP switches 3	USER_IO_SW3	3.3 V
SW2.1	General-purpose user DIP switches 0	USER_IO_SW0	3.3 V

continued...

Board Reference	Description	Schematic Signal Name	I/O Standard
SW2.2	General-purpose user DIP switches 1	USER_IO_SW1	3.3 V
SW3	Board power-on slide switch	N/A	9 V–20 V USB power
SW4.1	Board configuration DIP switch SW4.1 This feature is used in conjunction with the optional PCIe 3.0 x1 gold finger daughter card (End-point), or a Raspberry Pi 5 M.2 HAT board (Root-port). • OFF—Sets the board to function as a PCIe end-point • ON—Sets the board to function as a PCIe root port	OUT11_OE_L	3.3 V
SW4.2	Board configuration DIP switch SW4.2 This feature is used in conjunction with the optional PCIe 3.0 x1 gold finger daughter card (End-point), or a Raspberry Pi 5 M.2 HAT board (Root-port). • OFF—Enables the -0.5% spread spectrum modulation for the PCIe clock • ON—Disables the -0.5% spread spectrum modulation for the PCIe clock	SS_EN	3.3 V
SW4.3	Board configuration DIP switch SW4.3 • OFF—Connects a 100 MHz clock to the HVIO bank 5B, pin AJ27 • ON—Connects the Raspberry Pi GPIO26 to HVIO bank 5B, pin AJ27	TMUX_SEL	3.3 V
SW4.4	SW4.4 • OFF—Sets the FPGA to load the user application image from the QSPI flash • ON—Sets the FPGA to load the factory recover image from the QSPI flash *Note:* Current Altera designs do not use SW4.4. You can include this switch in your design, depending on your application needs.	LOAD_FACTORY_IMAGE	1.8 V

A.2.3. LEDs

The Agilex 3 FPGA/FPGA and SoC C-Series development board provides various LEDs for indicating board status information. The LEDs illuminate when a logic 1 is driven and turn OFF when a logic 0 is driven. There are no board-specific functions for these LEDs.

Table 19. Switches

Board Reference	Description	Schematic Signal Name	I/O Standard
D7	Dedicated green HPS LED 1	HPS_LED1	1.8 V
D8	Dedicated green HPS LED 0	HPS_LED0	1.8 V
D9	Dedicated green USER LED 0	IO_96_3A_LED0	1.1 V
D10	Dedicated green USER LED 1	IO_96_3A_LED1	1.1 V
D11	FPGA Configuration Done blue status LED	SDM_CONF_DONE	1.8 V

continued...

Board Reference	Description	Schematic Signal Name	I/O Standard
D17.GREEN D17.RED	Bicolor power status LED • ON Green indicates power good • Blinking RED indicates incompatible USB power adapter or insufficient USB input power	PG_VREG CAP_MIS	1.8 V 1.8 V
U2 RED LED U2 GREEN LED U2 BLUE LED	Tri-color status LED indicating the state of the USB-Blaster III cable. • Off indicates no power, not connected, or suspend mode. • Blue LED indicates connected, not in use • Green LED indicates connected, an application is using JTAG, no traffic • Blinking PURPLE indicates that an identify function has been triggered on this cable	FTDI_LED_RED FTDI_LED_GREEN FTDI_LED_BLUE	3.3 V 3.3 V 3.3 V
J10 GREEN LED J10 YELLOW LED	Ethernet port LEDs • Green LED indicates link status • Yellow LED indicates Ethernet port activity	LINK_LED ACTIVITY_LED	3.3 V 3.3 V

A.3. Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Agilex 3 FPGA/FPGA and SoC C-Series FPGA device.

A.3.1. PCI Express (PCIe) Interface

For PCIe applications, the power for the Agilex 3 FPGA/FPGA and SoC C-Series development board must be sourced by an external USB-PD Type-C power adapter as the board is not designed to receive power from the PCIe host system.

The board is designed to fit entirely into a PCIe host system with a x1 PCI Express slot that can accommodate a full height, 1/2 length form factor add-in card when the optional Altera PCIe 3.0 x1 gold finger daughter board is installed. The supported data rate for this application is 8 Gbps (PCIe 3.0) using the Agilex 3 FPGA's PCI Express hard IP block, saving logic resources for the user logic application.

Table 20. PCI Express (PCIe) Pin Assignments with Gold Finger Daughter Board

Gold Finger Pin Number	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
A1	PRSNT1_N	—	—	Card present
A11	RPI_PCIE_X1_RST_B	AG26	3.3 V LVCMOS	PCIe reset
A13	RPI_PCIE_REFCLK_P	To Si5332 clock generator (U23)	HCSL	Host PCIe clock
A14	RPI_PCIE_REFCLK_N	To Si5332 clock generator (U23)	HCSL	Host PCIe clock
A16	RPI_PCIE_X1_PETP	P30	True Differential	PCIe receive lane 0
A17	RPI_PCIE_X1_PETN	P29	True Differential	PCIe receive lane 0

continued...

Gold Finger Pin Number	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
B5	FRU_ID_EEPROM_SCL	FRUID EEPROM (U1 on Altera PCIe 3.0 x1 gold finger board)	3.3 V	SMB clock
B6	FRU_ID_EEPROM_SDA	FRUID EEPROM (U1 on Altera PCIe 3.0 x1 gold finger board)	3.3 V	SMB data
B11	EDGE_PCIE_X1_WAKE	AH27	3.3 V	PCIe wake
B12	RPI_PCIE_X1_CLKREQ_N	AK19	3.3 V	PCIe Clock request
B14	RPI_PCIE_X1_PERP	K30	True Differential	PCIe transmit lane 0
B15	RPI_PCIE_X1_PERP	K29	True Differential	PCIe transmit lane 0
B17	PRSNT1_N	—	—	Card present

A.3.2. DisplayPort Interface

The Agilex 3 FPGA/FPGA and SoC C-Series development board provides two DisplayPort v1.4 interfaces capable of operating at 8.1 Gbps per lane.

The transmit DisplayPort interface (J12) connects TX lanes 2 and 3 from the transceiver bank 1A. The receive DisplayPort interface (J16) connects RX lanes 2 and 3 from the transceiver bank 1A. In addition, the DisplayPort control signals and Auxiliary (AUX) channels connect to the HSIO banks 2A and 3A. The AUX channels are converted from differential to single ended signals for connection to the HSIO banks.

Table 21. DisplayPort Pin Assignment

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
DP_TX_0_DRV_DP	K27	True Differential	DisplayPort transmit data 0 (True)
DP_TX_0_DRV_DN	J27	True Differential	DisplayPort transmit data 0 (Compliment)
DP_TX_1_DRV_DP	G27	True Differential	DisplayPort transmit data 1 (True)
DP_TX_1_DRV_DN	F27	True Differential	DisplayPort transmit data 1 (Compliment)
DP_TX_CON_HPD_1V1	Y6	1.1 V	DisplayPort transmit hot plug detect
DP_TX_CON_CONFIG1_1V1	W7	1.1 V	DisplayPort transmit configuration 1
DP_TX_CON_CONFIG2_DRIVE_N_1V1	V7	1.1 V	DisplayPort transmit configuration 2
DP_TX_AUX_DEV_OE_1V1	AB5	1.1 V	DisplayPort TX AUX channel output enable
DP_TX_AUX_DEV_OUT_1V1	H2	1.1 V	DisplayPort TX AUX channel write data
DP_TX_AUX_DEV_IN_1V1	J1	1.1 V	DisplayPort TX AUX channel read data
DP_RX_0_DRV_DP	F30	True Differential	DisplayPort receive data 0 (True)
DP_RX_0_DRV_DN	F29	True Differential	DisplayPort receive data 0 (Compliment)

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
DP_RX_1_DRV_DP	D30	True Differential	DisplayPort receive data 1 (True)
DP_RX_1_DRV_DN	D29	True Differential	DisplayPort receive data 1 (Compliment)
DP_RX_CON_HPD_1V1	AB6	1.1 V	DisplayPort receive hot plug detect
DP_RX_AUX_DEV_OE_1V1	Y7	1.1 V	DisplayPort RX AUX channel output enable
DP_RX_AUX_DEV_OUT_1V1	K2	1.1 V	DisplayPort RX AUX channel write data
DP_RX_AUX_DEV_IN_1V1	H1	1.1 V	DisplayPort RX AUX channel read data
DP_RX_AUX_DP_SENSE_1V1	AA7	1.1 V	DisplayPort RX AUX channel sense (true)
DP_RX_AUX_DN_SENSE_1V1	AA6	1.1 V	DisplayPort RX AUX channel sense (compliment)

A.3.3. MIPI Interface

The Agilex 3 FPGA/FPGA and SoC C-Series development board provides two FPC MIPI interface connected to HSIO banks 2A and 3A.

Table 22. MIPI Bank 2A

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
MIPI_CONN_2A_CAM_D3_P	R1	1.1 V	MIPI bank 2A data 3 (true)
MIPI_CONN_2A_CAM_D3_N	P2	1.1 V	MIPI bank 2A data 3 (compliment)
MIPI_CONN_2A_CAM_D2_P	R2	1.1 V	MIPI bank 2A data 2 (true)
MIPI_CONN_2A_CAM_D2_N	T1	1.1 V	MIPI bank 2A data 2 (compliment)
MIPI_CONN_2A_CAM_D1_P	V2	1.1 V	MIPI bank 2A data 1 (true)
MIPI_CONN_2A_CAM_D1_N	V2	1.1 V	MIPI bank 2A data 1 (compliment)
MIPI_CONN_2A_CAM_D0_P	Y1	1.1 V	MIPI bank 2A data 0 (true)
MIPI_CONN_2A_CAM_D0_N	W2	1.1 V	MIPI bank 2A data 0 (compliment)
MIPI_CONN_2A_CAM_CK_P	T2	1.1 V	MIPI bank 2A clock (true)
MIPI_CONN_2A_CAM_CK_N	U1	1.1 V	MIPI bank 2A clock (compliment)

Table 23. MIPI Bank 3A

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
MIPI_CONN_3A_CAM_D3_P	G3	1.1 V	MIPI bank 3A data 3 (true)
MIPI_CONN_3A_CAM_D3_N	F3	1.1 V	MIPI bank 3A data 3 (compliment)
MIPI_CONN_3A_CAM_D2_P	F4	1.1 V	MIPI bank 3A data 2 (true)
MIPI_CONN_3A_CAM_D2_N	E4	1.1 V	MIPI bank 3A data 2 (compliment)
MIPI_CONN_3A_CAM_D1_P	F6	1.1 V	MIPI bank 3A data 1 (true)
MIPI_CONN_3A_CAM_D1_N	E6	1.1 V	MIPI bank 3A data 1 (compliment)

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
MIPI_CONN_3A_CAM_D0_P	C5	1.1 V	MIPI bank 3A data 0 (true)
MIPI_CONN_3A_CAM_D0_N	D4	1.1 V	MIPI bank 3A data 0 (compliment)
MIPI_CONN_3A_CAM_CK_P	D5	1.1 V	MIPI bank 3A clock (true)
MIPI_CONN_3A_CAM_CK_N	E5	1.1 V	MIPI bank 3A clock (compliment)

A.3.4. LPDDR4 Interfaces

The Agilex 3 FPGA/FPGA and SoC C-Series development board provides two LPDDR4 x32 interfaces connected to the FPGA at banks 2A and 3A.

Table 24. LPDDR4 Bank 2A Pin Assignments

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
LP4_2A_CA0	AF7	1.1 V	LPDDR4 memory command/address 0
LP4_2A_CA1	AE7	1.1 V	LPDDR4 memory command/address 1
LP4_2A_CA2	AF6	1.1 V	LPDDR4 memory command/address 2
LP4_2A_CA3	AE6	1.1 V	LPDDR4 memory command/address 3
LP4_2A_CA4	AH5	1.1 V	LPDDR4 memory command/address 4
LP4_2A_CA5	AG5	1.1 V	LPDDR4 memory command/address 5
LP4_2A_CKE_R0	AH6	1.1 V	LPDDR4 memory clock enable
LP4_2A_CS_N0	AF4	1.1 V	LPDDR4 memory chip select
LP4_2A_REFCLK_P	AF3	1.1 V	LPDDR4 memory FPGA reference clock (true)
LP4_2A_REFCLK_N	AE4	1.1 V	LPDDR4 memory FPGA reference clock (compliment)
LP4_2A_RESET_N	AD4	1.1 V	LPDDR4 memory reset
LP4_2A_CK_P	AB3	1.1 V	LPDDR4 memory clock (true)
LP4_2A_CK_N	AA4	1.1 V	LPDDR4 memory clock (compliment)
RZQ_B_2A_R	AD3	N/A	LPDDR4 RZQ
LP4_2A_DQ0	AB1	1.1 V	LPDDR4 memory data 0
LP4_2A_DQ1	AA2	1.1 V	LPDDR4 memory data 1
LP4_2A_DQ2	AA1	1.1 V	LPDDR4 memory data 2
LP4_2A_DQ3	Y2	1.1 V	LPDDR4 memory data 3
LP4_2A_DQ4	AG1	1.1 V	LPDDR4 memory data 4
LP4_2A_DQ5	AF2	1.1 V	LPDDR4 memory data 5
LP4_2A_DQ6	AF1	1.1 V	LPDDR4 memory data 6
LP4_2A_DQ7	AE2	1.1 V	LPDDR4 memory data 7

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
LP4_2A_DM0	AD2	1.1 V	LPDDR4 memory data mask 0
LP4_2A_DQS_P0	AC1	1.1 V	LPDDR4 memory data strobe 0 (True)
LP4_2A_DQS_N0	AD2	1.1 V	LPDDR4 memory data strobe 0 (Compliment)
LP4_2A_DQ8	AK6	1.1 V	LPDDR4 memory data 8
LP4_2A_DQ9	AK7	1.1 V	LPDDR4 memory data 9
LP4_2A_DQ10	AJ7	1.1 V	LPDDR4 memory data 10
LP4_2A_DQ11	AJ8	1.1 V	LPDDR4 memory data 11
LP4_2A_DQ12	AG3	1.1 V	LPDDR4 memory data 12
LP4_2A_DQ13	AH2	1.1 V	LPDDR4 memory data 13
LP4_2A_DQ14	AH3	1.1 V	LPDDR4 memory data 14
LP4_2A_DQ15	AJ3	1.1 V	LPDDR4 memory data 15
LP4_2A_DM1	AJ5	1.1 V	LPDDR4 memory data mask 1
LP4_2A_DQS_P1	AK4	1.1 V	LPDDR4 memory data strobe 1 (True)
LP4_2A_DQS_N1	AJ4	1.1 V	LPDDR4 memory data strobe 1 (Compliment)
LP4_2A_DQ16	P4	1.1 V	LPDDR4 memory data 16
LP4_2A_DQ17	P5	1.1 V	LPDDR4 memory data 17
LP4_2A_DQ18	U3	1.1 V	LPDDR4 memory data 18
LP4_2A_DQ19	V3	1.1 V	LPDDR4 memory data 19
LP4_2A_DQ20	W3	1.1 V	LPDDR4 memory data 20
LP4_2A_DQ21	U4	1.1 V	LPDDR4 memory data 21
LP4_2A_DQ22	P3	1.1 V	LPDDR4 memory data 22
LP4_2A_DQ23	N3	1.1 V	LPDDR4 memory data 23
LP4_2A_DM2	T3	1.1 V	LPDDR4 memory data mask 2
LP4_2A_DQS_P2	U5	1.1 V	LPDDR4 memory data strobe 2 (True)
LP4_2A_DQS_N2	T4	1.1 V	LPDDR4 memory data strobe 2 (Compliment)
LP4_2A_DQ24	V5	1.1 V	LPDDR4 memory data 24
LP4_2A_DQ25	V6	1.1 V	LPDDR4 memory data 25
LP4_2A_DQ26	N7	1.1 V	LPDDR4 memory data 26
LP4_2A_DQ27	N6	1.1 V	LPDDR4 memory data 27
LP4_2A_DQ28	R7	1.1 V	LPDDR4 memory data 28
LP4_2A_DQ29	P7	1.1 V	LPDDR4 memory data 29
LP4_2A_DQ30	W5	1.1 V	LPDDR4 memory data 30

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
LP4_2A_DQ31	U6	1.1 V	LPDDR4 memory data 31
LP4_2A_DM3	T6	1.1 V	LPDDR4 memory data mask 3
LP4_2A_DQS_P3	R5	1.1 V	LPDDR4 memory data strobe 3 (True)
LP4_2A_DQS_N3	R6	1.1 V	LPDDR4 memory data strobe 3 (Compliment)

Table 25. LPDDR4 Bank 3A Pin Assignments

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
LP4_3A_CA0	C2	1.1 V	LPDDR4 memory command/address 0
LP4_3A_CA1	D3	1.1 V	LPDDR4 memory strobe/address 1
LP4_3A_CA2	C3	1.1 V	LPDDR4 memory strobe/address 2
LP4_3A_CA3	B3	1.1 V	LPDDR4 memory strobe/address 3
LP4_3A_CA4	A6	1.1 V	LPDDR4 memory strobe/address 4
LP4_3A_CA5	B5	1.1 V	LPDDR4 memory strobe/address 5
LP4_3A_CKE_R0	A4	1.1 V	LPDDR4 memory data enable
LP4_3A_CS_N0	C7	1.1 V	LPDDR4 memory chip select
LP4_3A_REFCLK_P	A7	1.1 V	LPDDR4 memory FPGA reference data (true)
LP4_3A_REFCLK_N	B6	1.1 V	LPDDR4 memory FPGA reference data (compliment)
LP4_3A_RESET_N	E15	1.1 V	LPDDR4 memory reset
LP4_3A_CK_P	E9	1.1 V	LPDDR4 memory data (true)
LP4_3A_CK_N	E10	1.1 V	LPDDR4 memory data (compliment)
RZQ_B_3A_R	E14	N/A	LPDDR4 RZQ
LP4_3A_DQ0	H6	1.1 V	LPDDR4 memory data 0
LP4_3A_DQ1	H7	1.1 V	LPDDR4 memory data 1
LP4_3A_DQ2	G5	1.1 V	LPDDR4 memory data 2
LP4_3A_DQ3	G6	1.1 V	LPDDR4 memory data 3
LP4_3A_DQ4	M6	1.1 V	LPDDR4 memory data 4
LP4_3A_DQ5	N5	1.1 V	LPDDR4 memory data 5
LP4_3A_DQ6	M6	1.1 V	LPDDR4 memory data 6
LP4_3A_DQ7	L6	1.1 V	LPDDR4 memory data 7
LP4_3A_DM0	L7	1.1 V	LPDDR4 memory data mask 0
LP4_3A_DQS_P0	K7	1.1 V	LPDDR4 memory data strobe 0 (True)
LP4_3A_DQS_N0	J7	1.1 V	LPDDR4 memory data strobe 0 (Compliment)

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
LP4_3A_DQ8	L3	1.1 V	LPDDR4 memory data 8
LP4_3A_DQ9	J5	1.1 V	LPDDR4 memory data 9
LP4_3A_DQ10	M3	1.1 V	LPDDR4 memory data 10
LP4_3A_DQ11	L4	1.1 V	LPDDR4 memory data 11
LP4_3A_DQ12	M4	1.1 V	LPDDR4 memory data 12
LP4_3A_DQ13	G4	1.1 V	LPDDR4 memory data 13
LP4_3A_DQ14	H3	1.1 V	LPDDR4 memory data 14
LP4_3A_DQ15	H5	1.1 V	LPDDR4 memory data 15
LP4_3A_DM1	K5	1.1 V	LPDDR4 memory data mask 1
LP4_3A_DQS_P1	J4	1.1 V	LPDDR4 memory data strobe 1 (True)
LP4_3A_DQS_N1	J3	1.1 V	LPDDR4 memory data strobe 1 (Compliment)
LP4_3A_DQ16	D15	1.1 V	LPDDR4 memory data 16
LP4_3A_DQ17	C13	1.1 V	LPDDR4 memory data 17
LP4_3A_DQ18	C10	1.1 V	LPDDR4 memory data 18
LP4_3A_DQ19	D10	1.1 V	LPDDR4 memory data 19
LP4_3A_DQ20	C8	1.1 V	LPDDR4 memory data 20
LP4_3A_DQ21	D9	1.1 V	LPDDR4 memory data 21
LP4_3A_DQ22	D14	1.1 V	LPDDR4 memory data 22
LP4_3A_DQ23	C15	1.1 V	LPDDR4 memory data 23
LP4_3A_DM2	D13	1.1 V	LPDDR4 memory data mask 2
LP4_3A_DQS_P2	D12	1.1 V	LPDDR4 memory data strobe 2 (True)
LP4_3A_DQS_N2	C11	1.1 V	LPDDR4 memory data strobe 2 (Compliment)
LP4_3A_DQ24	A8	1.1 V	LPDDR4 memory data 24
LP4_3A_DQ25	B8	1.1 V	LPDDR4 memory data 25
LP4_3A_DQ26	A9	1.1 V	LPDDR4 memory data 26
LP4_3A_DQ27	B9	1.1 V	LPDDR4 memory data 27
LP4_3A_DQ28	B13	1.1 V	LPDDR4 memory data 28
LP4_3A_DQ29	A13	1.1 V	LPDDR4 memory data 29
LP4_3A_DQ30	B14	1.1 V	LPDDR4 memory data 30
LP4_3A_DQ31	A14	1.1 V	LPDDR4 memory data 31
LP4_3A_DM3	B11	1.1 V	LPDDR4 memory data mask 3
LP4_3A_DQS_P3	B10	1.1 V	LPDDR4 memory data strobe 3 (True)
LP4_3A_DQS_N3	A11	1.1 V	LPDDR4 memory data strobe 3 (Compliment)

A.3.5. Raspberry Pi, Pmod, and PCIe x1 Interfaces

The Agilex 3 FPGA/FPGA and SoC C-Series development board provides connections to Raspberry Pi 4/5, Digilent Pmod*, and Altera PCIe 3.0 x1 gold finger expansion boards via HVIO banks 5A and 5B.

Table 26. Bank 5A Pin Assignments

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
RPI_GPIO2	AJ24	3.3 V	Raspberry Pi GPIO2
RPI_GPIO3	AJ23	3.3 V	Raspberry Pi GPIO3
RPI_GPIO4	AH21	3.3 V	Raspberry Pi GPIO4
RPI_GPIO5	AJ19	3.3 V	Raspberry Pi GPIO5
RPI_GPIO6	AH23	3.3 V	Raspberry Pi GPIO6
RPI_GPIO7	AH22	3.3 V	Raspberry Pi GPIO7
RPI_GPIO8	AG23	3.3 V	Raspberry Pi GPIO8
RPI_GPIO9	AH20	3.3 V	Raspberry Pi GPIO9
RPI_GPIO10	AJ22	3.3 V	Raspberry Pi GPIO10
RPI_GPIO11	AJ20	3.3 V	Raspberry Pi GPIO11
RPI_GPIO12	AH18	3.3 V	Raspberry Pi GPIO12
RPI_GPIO13	AG21	3.3 V	Raspberry Pi GPIO13
RPI_GPIO14	AF24	3.3 V	Raspberry Pi GPIO14
RPI_GPIO15	AG24	3.3 V	Raspberry Pi GPIO15
RPI_GPIO16	AF23	3.3 V	Raspberry Pi GPIO16
RPI_GPIO17	AG20	3.3 V	Raspberry Pi GPIO17
RPI_GPIO18	AG19	3.3 V	Raspberry Pi GPIO18
RPI_GPIO19	AF22	3.3 V	Raspberry Pi GPIO19
RPI_ID_SD	AF19	3.3 V	Raspberry Pi ID_SD
RPI_ID_SC	AF21	3.3 V	Raspberry Pi ID_SC

Table 27. Bank 5B Pin Assignments

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
RPI_GPIO20	AK24	3.3 V / 1.8 V selectable	Raspberry Pi GPIO20 / Pmod GPIO0
RPI_GPIO21	AH26	3.3 V / 1.8 V selectable	Raspberry Pi GPIO21 / Pmod GPIO1
RPI_GPIO22	AJ25	3.3 V / 1.8 V selectable	Raspberry Pi GPIO22 / Pmod GPIO2
RPI_GPIO23	AH25	3.3 V / 1.8 V selectable	Raspberry Pi GPIO23 / Pmod GPIO3
RPI_PCIE_X1_RST_B	AG26	3.3 V / 1.8 V selectable	PCIe reset
RPI_GPIO24	AE25	3.3 V / 1.8 V selectable	Raspberry Pi GPIO24 / Pmod GPIO4

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
RPI_GPIO25	AK25	3.3 V / 1.8 V selectable	Raspberry Pi GPIO25 / Pmod GPIO5
RPI_PCIE_X1_PWR_EN	AF26	3.3 V / 1.8 V selectable	Raspberry Pi power enable
HVIO_PLL_REFCLK / RPI_GPIO26	AJ27	3.3 V / 1.8 V selectable	HVIO reference clock / Raspberry Pi GPIO26 / Pmod GPIO6
RPI_PCIE_X1_WAKE	AH27	3.3 V / 1.8 V selectable	PCIe wake
RPI_PCIE_X1_CLKREQ_N	AK19	3.3 V / 1.8 V selectable	PCIe clock request
RPI_GPIO27	AK22	3.3 V / 1.8 V selectable	Raspberry Pi GPIO27 / Pmod GPIO7
POWER_EN_MIPI_CONN_1	AJ29	3.3 V / 1.8 V selectable	MIPI bank 2A power enable
LED_EN_MIPI_CONN_1	AK26	3.3 V / 1.8 V selectable	MIPI bank 2A LED enable
MIPI_CONN_1_SCL	AH28	3.3 V / 1.8 V selectable	MIPI bank 2A I^2C clock
MIPI_CONN_1_SDA	AK20	3.3 V / 1.8 V selectable	MIPI bank 2A I^2C data
POWER_EN_MIPI_CONN_2	AF27	3.3 V / 1.8 V selectable	MIPI bank 3A power enable
LED_EN_MIPI_CONN_2	AJ28	3.3 V / 1.8 V selectable	MIPI bank 3A LED enable
MIPI_CONN_2_SCL	AK21	3.3 V / 1.8 V selectable	MIPI bank 3A I^2C clock
MIPI_CONN_2_SDA	AK27	3.3 V / 1.8 V selectable	MIPI bank 2A I^2C data

A.3.6. HPS I/O48 Interface

The Agilex 3 FPGA and SoC C-Series development board connects the 48 HPS I/Os (HPS_GPIO[47:0]) directly to various HPS components on the board. For the Agilex 3 FPGA C-Series development board versions, the HPS components are depopulated from the board. The HPS components include: USB2.0 DRP (Dual Role Port), 2-wire UART, 10/100/1000 Ethernet, Micro-SD card, I^2C, and JTAG accessibility.

Table 28. HPS Pin Assignments

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
HPS_GPIO0	B29	1.8 V	HPS LED0
HPS_GPIO1	A27	1.8 V	Ethernet interrupt
HPS_GPIO2	C27	1.8 V	UART transmit
HPS_GPIO3	F24	1.8 V	UART receive
HPS_GPIO4	B28	1.8 V	I^2C data
HPS_GPIO5	F23	1.8 V	I^2C clock
HPS_GPIO6	D27	1.8 V	Ethernet MDIO
HPS_GPIO7	E22	1.8 V	Ethernet MDC
HPS_GPIO8	C26	1.8 V	I^3C data
HPS_GPIO9	D22	1.8 V	I^3C clock
HPS_GPIO10	A23	1.8 V	HPS 25 MHz clock

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
HPS_GPIO11	A26	1.8 V	HPS LED1
HPS_GPIO12	D25	1.8 V	USB2.0 clock
HPS_GPIO13	B26	1.8 V	USB2.0 STP
HPS_GPIO14	B25	1.8 V	USB2.0 DIR
HPS_GPIO15	E17	1.8 V	USB2.0 DATA 0
HPS_GPIO16	A16	1.8 V	USB2.0 DATA 1
HPS_GPIO17	E16	1.8 V	USB2.0 NXT
HPS_GPIO18	D24	1.8 V	USB2.0 DATA 2
HPS_GPIO19	E21	1.8 V	USB2.0 DATA 3
HPS_GPIO20	B23	1.8 V	USB2.0 DATA 4
HPS_GPIO21	D20	1.8 V	USB2.0 DATA 5
HPS_GPIO22	B24	1.8 V	USB2.0 DATA 6
HPS_GPIO23	A24	1.8 V	USB2.0 DATA 7
HPS_GPIO24	D23	1.8 V	SD card data 0
HPS_GPIO25	C25	1.8 V	SD card data 1
HPS_GPIO26	A18	1.8 V	SD card clock
HPS_GPIO27	C20	1.8 V	SD card I/O voltage select
HPS_GPIO28	A17	1.8 V	HPS push button 0
HPS_GPIO29	C21	1.8 V	SD card data 2
HPS_GPIO30	C23	1.8 V	SD card data 3
HPS_GPIO31	E20	1.8 V	SD card command
HPS_GPIO32	C22	1.8 V	HPS JTAG TCK
HPS_GPIO33	D19	1.8 V	HPS JTAG TMS
HPS_GPIO34	B21	1.8 V	HPS JTAG TDO
HPS_GPIO35	A22	1.8 V	HPS JTAG TDI
HPS_GPIO36	B16	1.8 V	Ethernet TX clock
HPS_GPIO37	B18	1.8 V	Ethernet TX enable
HPS_GPIO38	E19	1.8 V	Ethernet RX clock
HPS_GPIO39	B20	1.8 V	Ethernet RX data valid
HPS_GPIO40	C18	1.8 V	Ethernet TX data 0
HPS_GPIO41	A21	1.8 V	Ethernet TX data 1
HPS_GPIO42	D17	1.8 V	Ethernet RX data 0
HPS_GPIO43	A19	1.8 V	Ethernet RX data 1
HPS_GPIO44	D18	1.8 V	Ethernet TX data 2

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
HPS_GPIO45	B19	1.8 V	Ethernet TX data 3
HPS_GPIO46	C17	1.8 V	Ethernet RX data 2
HPS_GPIO47	C16	1.8 V	Ethernet Rx data 3

A.3.7. I²C

An I²C bus is used to connect various devices and interfaces to the Agilex 3 FPGA.

For the Agilex 3 FPGA and SoC C-Series Development Kit version, the I²C chain is connected to the HPS IO48 interface so that the HPS is the I²C master. For the Agilex 3 FPGA C-Series Development Kit version, the I²C chain connects to HVIO bank 5A. In this case, you can implement an I²C master in the FPGA fabric to communicate with the connected I²C devices on the chain.

Figure 29. I²C Block Diagram

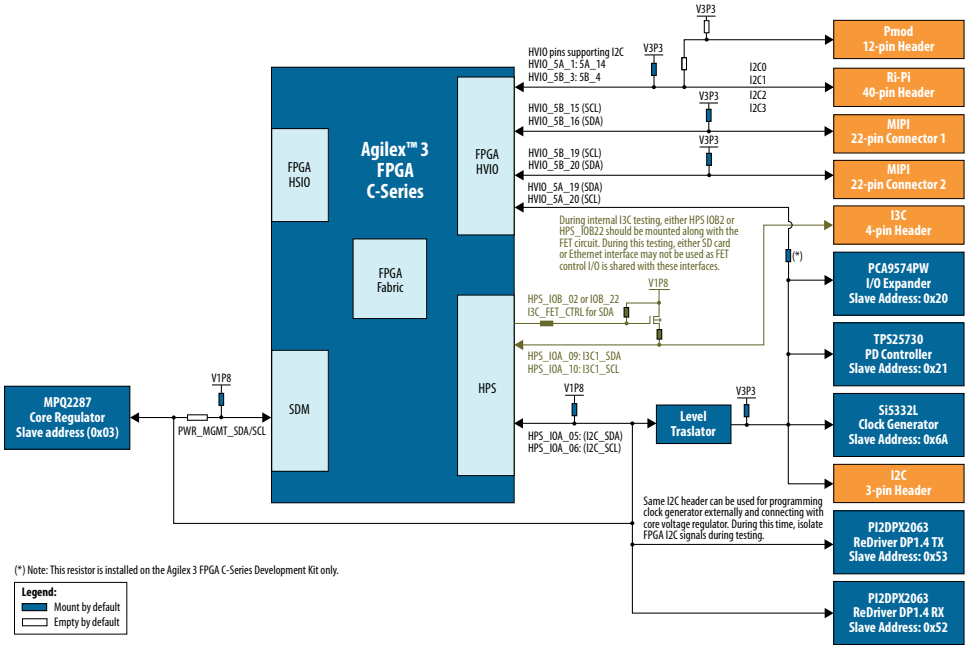


Table 29. FPGA I²C Signals

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
HPS_I2C_SCL	F23	1.8 V open drain	HPS I²C clock connected to Si5332 programmable clock generator, DisplayPort TX redriver, DisplayPort RX redriver, USB-PD input power sink controller, FPGA V_{CC} core regulator, 8-bit I/O expander, and I²C 3-pin test header.

continued...

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
			This signal is only applicable for the Agilex 3 FPGA and SoC C-Series Development Kit.
HPS_I2C_SDA	B28	1.8 V open drain	HPS I^2C data connected to Si5332 programmable clock generator, DisplayPort TX redriver, DisplayPort RX redriver, USB-PD input power sink controller, FPGA V_{CC} core regulator, 8-bit I/O expander, and I^2C 3-pin test header. This signal is only applicable for the Agilex 3 FPGA and SoC C-Series Development Kit.
MIPI_CONN_1_SCL	AH28	3.3 V open drain	HVIO bank 5B I^2C clock connected to FPC MIPI 2A connector
MIPI_CONN_1_SDA	AK20	3.3 V open drain	HVIO bank 5B I^2C data connected to FPC MIPI 2A connector
MIPI_CONN_2_SCL	AK21	3.3 V open drain	HVIO bank 5B I^2C clock connected to FPC MIPI 3A connector
MIPI_CONN_2_SDA	AK27	3.3 V open drain	HVIO bank 5B I^2C data connected to FPC MIPI 3A connector
RPI_ID_SC	AF21	3.3 V open drain	HVIO bank 5A I^2C clock connected to Raspberry Pi 40-pin header/Pmod connector This signal is only applicable for the Agilex 3 FPGA C-Series Development Kit.
RPI_ID_SD	AF19	3.3V open drain	HVIO bank 5A I^2C clock connected to Raspberry Pi 40-pin header/Pmod connector This signal is only applicable for the Agilex 3 FPGA C-Series Development Kit.

Table 30. I^2C Address

Device	Reference	I^2C Address	Description
TPS25730DREFR	U10	0x21	Texas Instruments USB-PD input power sink controller
MPQ2287GLE	U36	0x03	MPS voltage regulator for FPGA core power
SI5332LD16712-GM3	U23	0x6A	Skyworks I^2C programmable clock generator
PCA9574PW	U45	0x20	NXP I^2C to 8-bit I/O expander
PI2DPX2063FLAEX	U264	0x53	Diodes Inc DisplayPort ReDriver* used for TX
PI2DPX2063FLAEX	U265	0x52	Diodes Inc DisplayPort ReDriver* used for RX

A.4. Clock Circuits

Figure 30. Agilex 3 FPGA/FPGA and SoC C-Series Development Kit Clocks and Default Frequencies

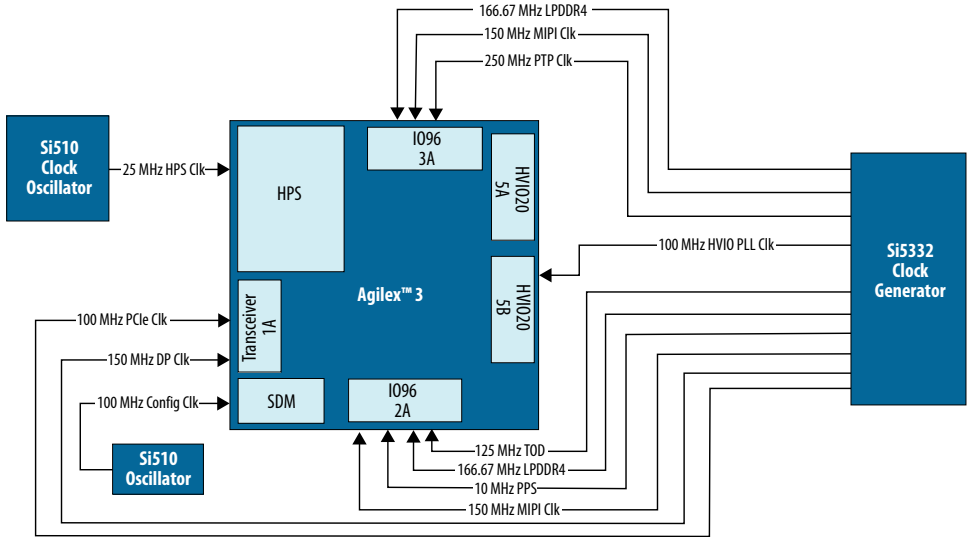


Table 31. Onboard Oscillators Sources for the FPGA

Source	Schematic Signal Name	Frequency (MHz)	I/O Standard	Agilex 3 Pin Number (P/N)	Application
U23	HVIO_PLLREFCLK	100	3.3V LVCMOS	AJ27	HVIO PLL reference clock
	LP4_2A_REFCLK_P/N	166.67	LVDS	AF3/AE4	LPDDR4 bank 2A reference clock
	LP4_3A_REFCLK_P/N	166.67	LVDS	A7/B6	LPDDR4 bank 3A reference clock
	PTP_3A_REFCLK	250	1.1V LVCMOS	E2	PTP bank 3A reference clock
	FPGA_FABRIC_TOD_CLK	125	1.1V LVCMOS	N1	TOD bank 2A reference clock
	PPS_2A_REFCLK	10	1.1V LVCMOS	N2	PPS bank 2A reference clock
	MIPI_2A_REFCLK_P/N	150	LVDS	AC6/AC5	MIPI bank 2A reference clock
	MIPI_3A_REFCLK_P/N	150	LVDS	F2/E1	MIPI bank 3A reference clock
	DP_BANK1A_REFCLK_P/N	150	LVDS	P25/P24	DisplayPort bank 1A reference clock
	RPI_PCIE_REFCLK_P/N	100	HCSL	J14.4/J14.5	PCIe root port reference clock

continued...

Source	Schematic Signal Name	Frequency (MHz)	I/O Standard	Agilex 3 Pin Number (P/N)	Application
	PCIE_EP_REFCLK_P/N	100	HCSL	M24/M25	PCIe bank 1A endpoint clock
Y5	SDM_CONFIG_CLK	100	1.8V LVCMOS	AG11	FPGA configuration clock
Y1	HPS_OSC_CLK	25	1.8V LVCMOS	A23	HPS system clock

A.5. System Power

This section describes the Agilex 3 FPGA/FPGA and SoC C-Series development board's power supply requirements. As a power supply is not provided with the development kit, you must supply a USB-PD Type-C power adapter capable of supplying between 27 W to 65 W output to power the board. Refer to the *Powering Up the Development Board* section.

Related Information

Powering Up the Development Board on page 15

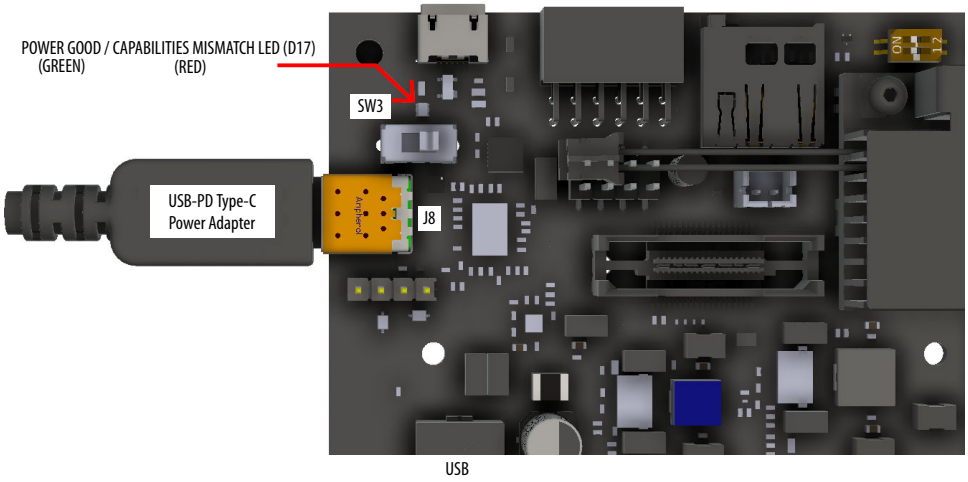
A.6. Power Guidelines

The Agilex 3 FPGA/FPGA and SoC C-Series Development Kit has two modes of operation. The primary mode of the development kit is to allow you to operate the board as a bench top evaluation platform. An optional mode allows the board to function as a PCIe add-in card. This second mode requires the optional Altera PCIe 3.0 x1 gold finger daughter card accessory to convert the board into a PCIe add-in card.

A.6.1. Primary Mode—As a Standalone Evaluation Board

In this mode, plug the user-supplied USB-PD Type-C compliant power adapter into the USB Type-C input power connector (J8) and the AC power cord of the power supply into a power outlet. Slide the power switch SW3 to the ON position to power on the board. The POWERGOOD LED lights green when the board is successfully powered on. The POWERGOOD LED remains off or blinks red when a power capability mismatch is detected due to a non USB-PD power adapter is being used. In this event, slide the power switch SW3 to the OFF position and replace the power adapter with a USB-PD compliant one.

Figure 31. Powering the Agilex 3 FPGA C-Series Development Board

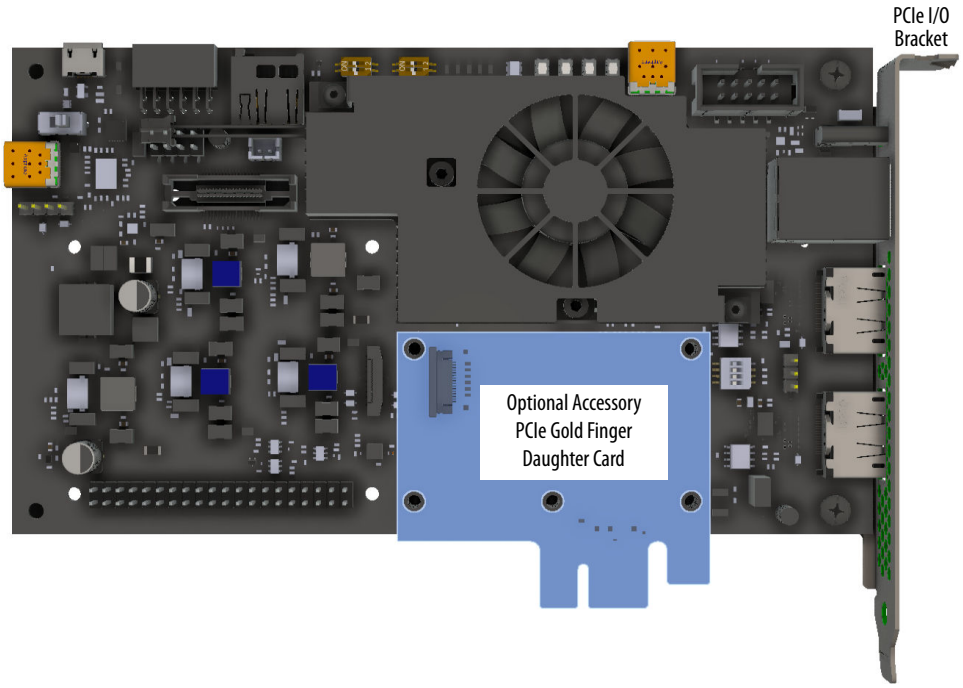


A.6.2. Optional Mode—As a PCIe Add-in Card in PCIe Host System

This mode is optional and requires the user to install the optional Altera PCIe 3.0 x1 gold finger daughter card to convert the development board into a PCIe add-in card. Once the PCIe gold finger daughter card is installed, plug the PCIe add-in card into an available PCIe card slot in your host system and secure the card to the chassis by screwing the card's I/O bracket to the host system with the supplied hardware included in your Altera PCIe 3.0 x1 daughter card.

When operating as a PCIe add-in card, you must still provide power to J8 with a USB-PD compliant power adapter plugged into J8. Slide the switch SW3 to the ON position to power on the board. The board cannot be powered on without a USB-PD power adapter plugged into J8 as the board does not receive any power from the host's PCIe card slot through the PCIe gold finger daughter card.

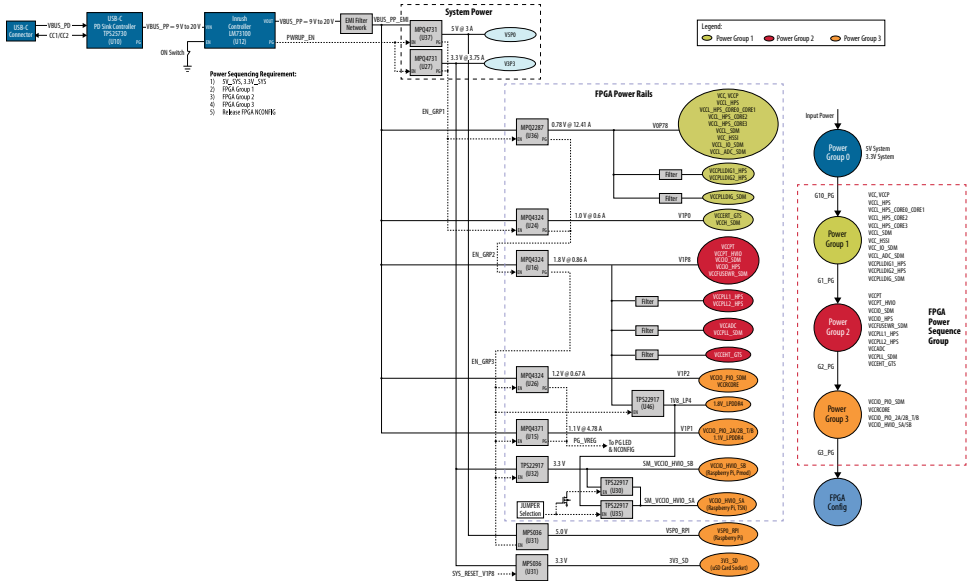
Figure 32. Optional PCIe Gold Finger Daughter Board Attached



A.7. Power Distribution System

The following figure shows the power distribution and power sequencing on the Agilex 3 FPGA/FPGA and SoC C-Series development board. This figure shows the complete power rail connections for the Agilex 3 FPGA and SoC C-Series development board. For the Agilex 3 FPGA C-Series development board, you can omit any "*_HPS" or "*_HPS_*" named power rails.

Figure 33. Power Tree



The Agilex 3 FPGA/FPGA and SoC C-Series Development Kit is designed to operate in a typical laboratory environment with an ambient temperature of approximately 25°C. The cooling solution provided with the development kit allows sufficient cooling for the board to operate up to a maximum power consumption of 54 W with a maximum FPGA workload of 16 W.

A.8. Expansion Boards

Altera PCIe gold finger daughter board supports PCIe 3.0 x1 (8 Gbps) that is connected to the connector (`J14`) on development kit board.

Table 32. PCIe FPGA Pinout for PCIe Gold Finger Daughter Board

FPGA Pin Number	Signal Name	Description	I/O Direction[1]
To Si5332 clock generator (`U23`)	`RPI_PCIE_REFCLK_P`	Host PCIe clock	b
To Si5332 clock generator (`U23`)	`RPI_PCIE_REFCLK_N`	Host PCIe clock	b
K30	`RPI_PCIE_X1_PERP`	PCIe data lane 0	i
K29	`RPI_PCIE_X1_PERN`	PCIe data lane 0	i
P30	`RPI_PCIE_X1_PETP`	PCIe data lane 0	o
P29	`RPI_PCIE_X1_PETN`	PCIe data lane 0	o
AF26	`RPI_PCIE_X1_PWR_EN`	PCIe power enable	i

continued...

(1) The signal direction is viewed at the sides of the Agilex 3 FPGA and SoC C-Series Development Kits.

FPGA Pin Number	Signal Name	Description	I/O Direction[1]
AH27	RPI_PCIE_X1_WAKE	PCIe wake	i
AK19	RPI_PCIE_X1_CLKREQ_N	PCIe clock request	i
AHG26	RPI_PCIE_X1_RST_B	PCIe reset	b

(1) The signal direction is viewed at the sides of the Agilex 3 FPGA and SoC C-Series Development Kits.

B. Developer Resources

Use the following links to check the Altera website for other related information.

Table 33. Agilex 3 FPGA and SoC C-Series Development Kits References

Reference	Description
Agilex 3 FPGA C-Series Development Kit page	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
Altera FPGA Developer Site	Provides key information about Altera FPGAs including: • Documentation for how to use example designs and tutorials found on altera-fpga GitHub site. • Comprehensive software development resources including information on Linux, Zephyr, Baremetal drivers, and software utilities.
Device Design Guidelines: Agilex 3 FPGAs and SoCs	Guidelines, recommendations, and a list of factors to consider for designs that use the Agilex 3 FPGAs and SoCs.
AN 958: Board Design Guidelines	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
Power Management User Guide: Agilex 3 FPGAs and SoCs	Describes the power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems, and power optimization techniques for the Agilex 3 FPGAs and SoCs.
Device Configuration User Guide: Agilex 3 FPGAs and SoCs	Agilex 3 FPGA and SoC C-Series FPGAs and SoCs support configuration using the following interfaces: Avalon® streaming, JTAG, CvP, and Active Serial (AS) normal and fast modes. This user guide explains the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
Documentation: Agilex 3	Agilex 3 device documentation.
Cadence* Capture CIS Schematic Symbols	Agilex 3 OrCAD symbols.

C. Safety and Regulatory Compliance Information

C.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

C.1.1. Safety Warnings

Power Supply Hazardous Voltage

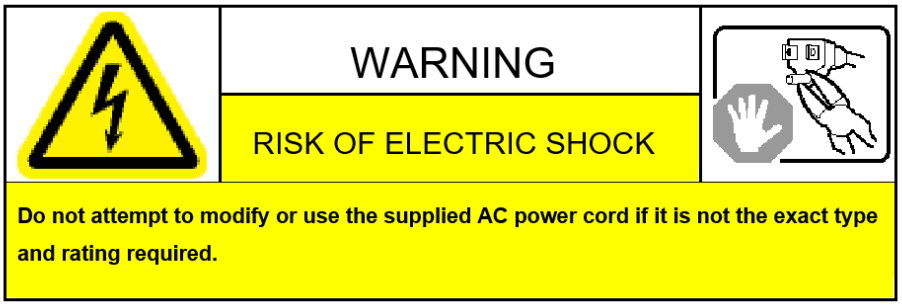
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

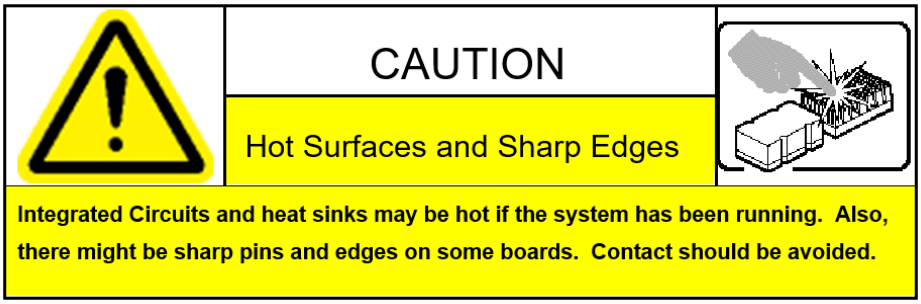
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

C.1.2. Safety Cautions



Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Altera for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Altera service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

(Translation - please recycle batteries)

Please return this product to Altera for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

C.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.