

**IMBG32L4KBB**  
**32Gbit LPDDR4/LPDDR4x SDRAM**  
**8Bank x 128Mbit x 16 x 2 Channel x 1 Rank**

	<b>046</b>
	LPDDR4-4266
Clock Cycle Time (tCK)	0.468ns
System Frequency (f <sub>CK(MAX)</sub> )	2133MHz

**Specification**

**Option**

**Marking**

- Density: 32Gbits
- Organization: 8Bank x 128Mbit x 16 x 2 Channel x 1 Rank
- Package: 200-ball FBGA
- Data Rate: 4266Mbps
- Power Supply
  - V<sub>DD1</sub> = 1.8V (1.70V ~ 1.95V) LPDDR4/LPDDR4x
  - V<sub>DD2</sub> = 1.1V (1.06V ~ 1.17V) LPDDR4/LPDDR4x
  - V<sub>DDQ</sub> = 1.1V (1.06V ~ 1.17V) LPDDR4  
0.6V (0.57V ~ 0.65V) LPDDR4x
- Double-Data-Rate Architecture
- Differential Clock Input (CK<sub>t</sub>, CK<sub>c</sub>)
- Bi-directional Differential Data Strobe (DQS<sub>t</sub>, DQS<sub>c</sub>)
- Command and address entered on both rising and falling CK<sub>t</sub> edge. Data and Data Mask referenced to both edges of DQS<sub>t</sub>
- DMI Pin
  - DBI (Data Bus Inversion) during normal Read and Write
  - DM (Data Mask) for masked write when DBI off; Counting # of DQ's 1 for masked write when DBI on
- 8 Internal Bank for each Channel
- Burst Length: 16, 32 and on-the-fly (OTF)  
On the fly mode is enabled by MRS
- Burst Type: Sequential
- Auto Precharge option for each Burst Access
- Configurable Drive Strength
- Refresh and Self Refresh mode
- Partial Array Self Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self Refresh
  - ATCSR by built-in temperature sensor
- All bank auto refresh and directed per bank auto refresh supported
- Write Leveling
- CA Calibration
- Internal V<sub>REF</sub> and V<sub>REF</sub> Training
- FIFO based Write/Read Training
- MPC (Multi-Purpose Command)
- LVSTLE (Low Voltage Swing Terminated Logic Extension) I/O
- V<sub>SSQ</sub> Termination
- Edge align Data Output; Write Training for Data Input Center align
- Refresh Rate: 3.9µs

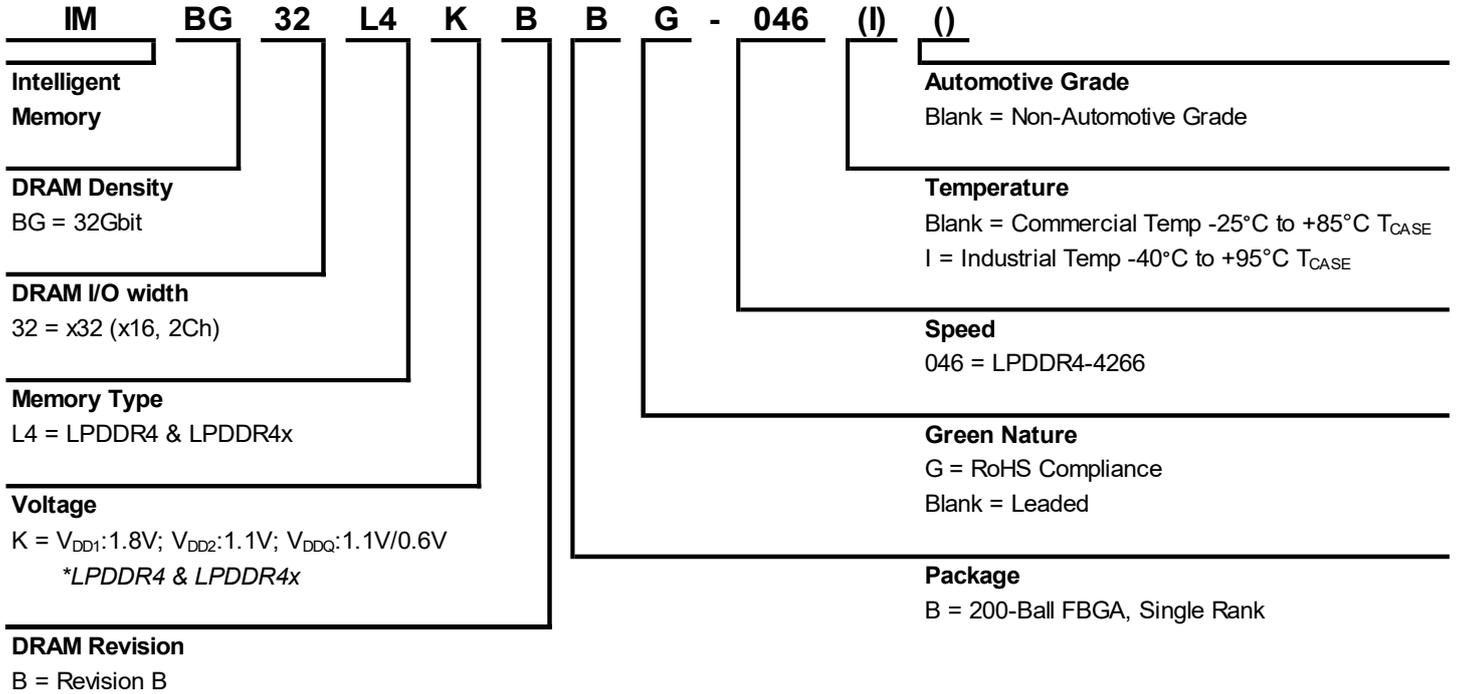
- Capacity
  - 32Gbit BG
- DRAM I/O Width
  - x32 (x16, 2Ch) 32
- Package
  - 200-Ball FBGA, Single Rank B
- Green Nature
  - RoHS Compliance G
  - Leaded [Blank]
- Speed
  - LPDDR4-4266 (0.468ns) 046
- Temperature (T<sub>CASE</sub>)
  - Commercial Temperature (-25°C to 85°C) [Blank]
  - Industrial Temperature (-40°C to 95°C) I
- Automotive Grade
  - Non-Automotive Grade [Blank]

Available Part Number: IMBG32L4KBGG-046I

## Version History

Version	History	Date	Remarks
0.1	Preliminary Release	Jun, 2024	
0.2	Add AC Timing table	Sep, 2024	
1.0	Formal Release	Sep, 2024	

## Part Number Information



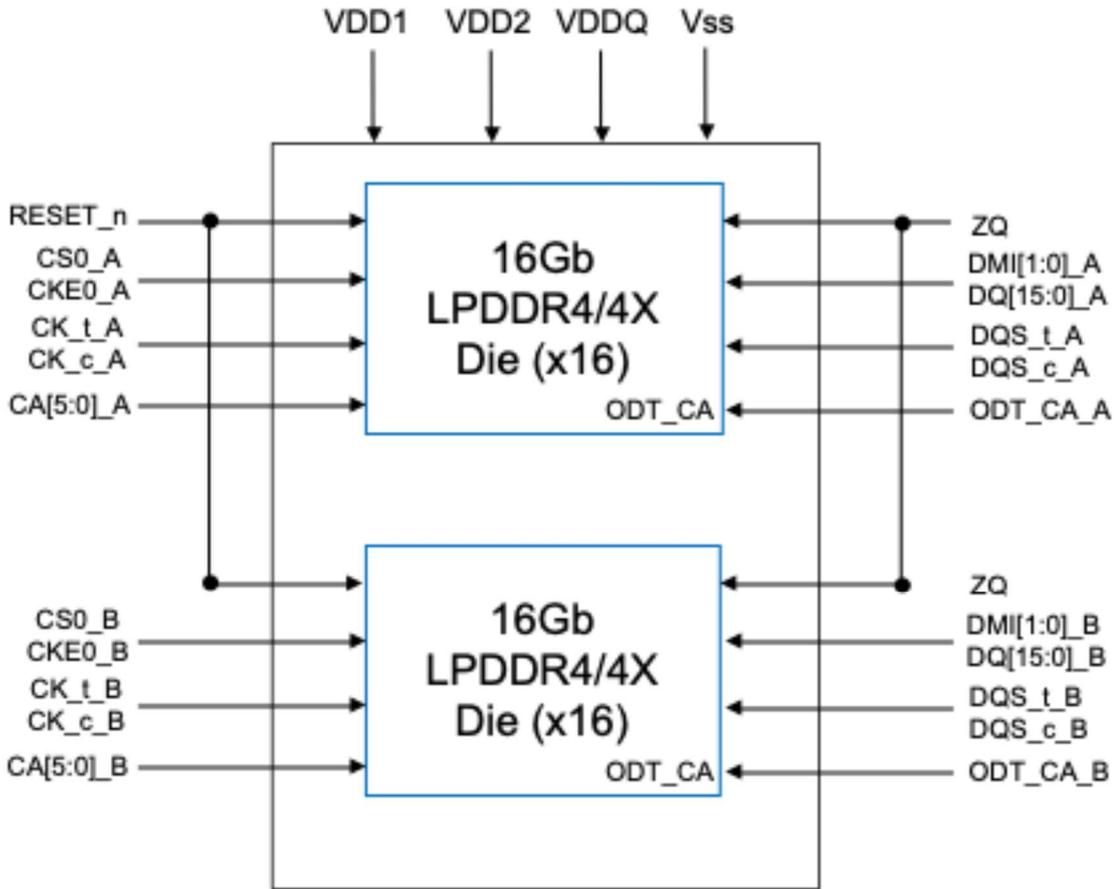
## LPDDR4 SDRAM Addressing

Configuration		LPDDR4
Memory Density		32Gbit
Configuration		8Bank x 128Mb x 16 x 2 Channel x 1 Rank
Number of Channel		2
Number of Rank		1
Total Density (per Channel)		16Gbit
Number of Bank (per Channel)		8
Number of Row (per Channel)		131,072
Number of Column (Fetch Boundaries)		64
Array Pre-Fetch (bit, per Channel)		256
Burst Starting Address Boundary		64bit
Bank Address		BA0 ~ BA2
x16	Row Address	R0 ~ R16
	Column Address	C0 ~ C9

**Note:**

- The lower two column addresses (C0-C1) are assumed to be “zero” and are not transmitted on the CA bus.
- Row and Column address values on the CA bus that are not used for a particular density are required to be at valid logic level.

### Functional Block Diagram



# Pin Configuration

## 200-Ball FBGA (x16,2Ch configuration)

0.80mm Pitch

		1	2	3	4	5	6	7	8	9	10	11	12	
0.65mm Pitch	A	DNU	DNU	V <sub>SS</sub>	V <sub>DD2</sub>	ZQ0			NC	V <sub>DD2</sub>	V <sub>SS</sub>	DNU	DNU	
	B	DNU	DQ0_A	V <sub>DDQ</sub>	DQ7_A	V <sub>DDQ</sub>			V <sub>DDQ</sub>	DQ15_A	V <sub>DDQ</sub>	DQ8_A	DNU	
	C	V <sub>SS</sub>	DQ1_A	DMI0_A	DQ6_A	V <sub>SS</sub>			V <sub>SS</sub>	DQ14_A	DM1_A	DQ9_A	V <sub>SS</sub>	
	D	V <sub>DDQ</sub>	V <sub>SS</sub>	DQS0_t_A	V <sub>SS</sub>	V <sub>DDQ</sub>			V <sub>DDQ</sub>	V <sub>SS</sub>	DQS1_t_A	V <sub>SS</sub>	V <sub>DDQ</sub>	
	E	V <sub>SS</sub>	DQ2_A	DQS0_c_A	DQ5_A	V <sub>SS</sub>			V <sub>SS</sub>	DQ13_A	DQS1_c_A	DQ10_A	V <sub>SS</sub>	
	F	V <sub>DD1</sub>	DQ3_A	V <sub>DDQ</sub>	DQ4_A	V <sub>DD2</sub>			V <sub>DD2</sub>	DQ12_A	V <sub>DDQ</sub>	DQ11_A	V <sub>DD1</sub>	
	G	V <sub>SS</sub>	ODT_CA_A <sup>1</sup>	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>SS</sub>			V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	
	H	V <sub>DD2</sub>	CA0_A	NC	CS0_A	V <sub>DD2</sub>			V <sub>DD2</sub>	CA2_A	CA3_A	CA4_A	V <sub>DD2</sub>	
	J	V <sub>SS</sub>	CA1_A	V <sub>SS</sub>	CKE0_A	NC			CK_t_A	CK_c_A	V <sub>SS</sub>	CA5_A	V <sub>SS</sub>	
	K	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	NC			NC	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>DD2</sub>	
	L													
	M													
	N	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	NC			NC	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>DD2</sub>	
	P	V <sub>SS</sub>	CA1_B	V <sub>SS</sub>	CKE0_B	NC			CK_t_B	CK_c_B	V <sub>SS</sub>	CA5_B	V <sub>SS</sub>	
	R	V <sub>DD2</sub>	CA0_B	NC	CS0_B	V <sub>DD2</sub>			V <sub>DD2</sub>	CA2_B	CA3_B	CA4_B	V <sub>DD2</sub>	
	T	V <sub>SS</sub>	ODT_CA_B <sup>1</sup>	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>SS</sub>			V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>SS</sub>	RESET_n	V <sub>SS</sub>	
U	V <sub>DD1</sub>	DQ3_B	V <sub>DDQ</sub>	DQ4_B	V <sub>DD2</sub>			V <sub>DD2</sub>	DQ12_B	V <sub>DDQ</sub>	DQ11_B	V <sub>DD1</sub>		
V	V <sub>SS</sub>	DQ2_B	DQS0_c_B	DQ5_B	V <sub>SS</sub>			V <sub>SS</sub>	DQ13_B	DQS1_c_B	DQ10_B	V <sub>SS</sub>		
W	V <sub>DDQ</sub>	V <sub>SS</sub>	DQS0_t_B	V <sub>SS</sub>	V <sub>DDQ</sub>			V <sub>DDQ</sub>	V <sub>SS</sub>	DQS1_t_B	V <sub>SS</sub>	V <sub>DDQ</sub>		
Y	V <sub>SS</sub>	DQ1_B	DMI0_B	DQ6_B	V <sub>SS</sub>			V <sub>SS</sub>	DQ14_B	DMI1_B	DQ9_B	V <sub>SS</sub>		
AA	DNU	DQ0_B	V <sub>DDQ</sub>	DQ7_B	V <sub>DDQ</sub>			V <sub>DDQ</sub>	DQ15_B	V <sub>DDQ</sub>	DQ8_B	DNU		
AB	DNU	DNU	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>			V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	DNU	DNU		

- Note:**
1. ODT\_CA[x] balls are wired to ODT\_CA[x] pads of Rank 0 DRAM die. ODT\_CA[x] pads for other ranks (if present) are disabled in the package
  2. Die pad V<sub>SS</sub> and V<sub>SS0</sub> signals are combined to V<sub>SS</sub> package balls.

## Signal Pin Description

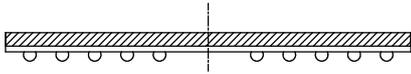
Pin	Type	Function
CK_t_[A,B], CK_c_[A,B]	Input	<b>Clock:</b> CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE0_[A,B]	Input	<b>Clock Enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS0_[A,B]	Input	<b>Chip Select:</b> CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_[A,B]	Input	<b>Command/Address Input:</b> CA signals provide the command and address inputs according to the Command Truth Table. Each channel (A & B) has its own CA signals.
ODT_CA_[A,B]	Input	<b>CA ODT Control:</b> The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_[A,B]	I/O	<b>Data Input/Output:</b> Bi-direction data bus
DQS[1:0]_t_[A,B], DQS[1:0]_c_[A,B]	I/O	<b>Data Strobe:</b> DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_[A,B]	I/O	<b>Data Mask Inversion:</b> DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ0	Reference	<b>Calibration Reference:</b> Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V <sub>DDQ</sub> through a 240ohm ± 1% resistor.
RESET_n	Input	<b>RESET:</b> When asserted Low, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.
V <sub>DD1</sub> , V <sub>DD2</sub> , V <sub>DDQ</sub>	Supply	<b>Power Supplies:</b> Isolated on the die for improved noise immunity.
V <sub>SS</sub> , V <sub>SSQ</sub>	GND	<b>Ground Reference:</b> Power supply ground reference.
NC	-	<b>No Connect</b>

### Note:

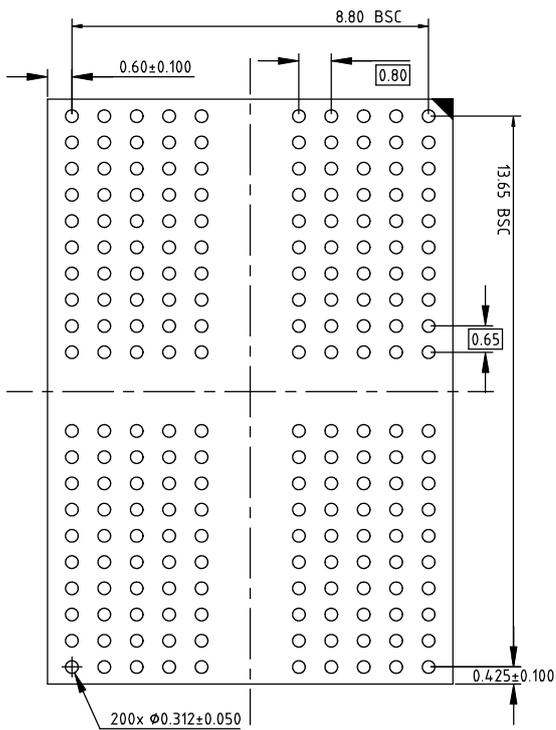
1. “\_A” and “\_B” indicate DRAM channel “\_A” pads are present in all devices. “\_B” pads are present in dual channel SDRAM devices only.

# Package Diagram

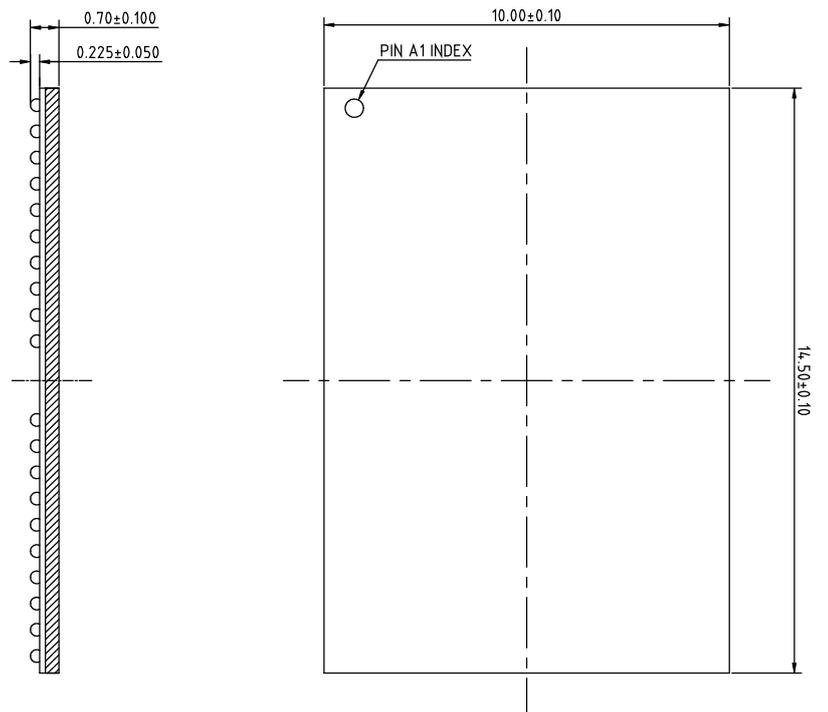
## 200-Ball Fine Pitch Ball Grid Array Outline



BOTTOM VIEW



TOP VIEW



**Note:** All dimensions are in millimeters.

## IDD Specification

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire elevated temperature range.

Parameter / Condition	Symbol	Power Supply	Note
<b>Operating one bank Active-Precharge Current:</b> tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching Data bus inputs are stable; ODT is disabled	IDD0 <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD0 <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD0 <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Idle Power-Down Standby Current:</b> tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD2P <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD2P <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Idle Power-Down Standby Current with Clock stop:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2PS <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD2PS <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD2PS <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Idle non Power-Down Standby Current:</b> tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2N <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD2N <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD2N <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Idle non Power-Down Standby Current with Clock stopped:</b> CK <sub>t</sub> =LOW; CK <sub>c</sub> =HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2NS <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD2NS <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD2NS <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Active Power-Down Standby Current:</b> tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3P <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD3P <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD3P <sub>Q</sub>	V <sub>DDQ</sub>	1,3,10
<b>Active Power-Down Standby Current with Clock stop:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3PS <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD3PS <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD3PS <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10

Parameter / Condition	Symbol	Power Supply	Note
<b>Active non Power-Down Standby Current:</b> tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3N <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD3N <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD3N <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>Active non Power-Down Standby Current with Clock stopped:</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3NS <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD3NS <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD3NS <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>Operating Burst READ Current:</b> tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	IDD4R <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD4R <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD4R <sub>Q</sub>	V <sub>DDQ</sub>	1,5,10
<b>Operating Burst WRITE Current:</b> tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	IDD4W <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD4W <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD4W <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>All-bank REFRESH Burst Current:</b> tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5 <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD5 <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD5 <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>All-bank REFRESH Average Current:</b> tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5AB <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD5AB <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD5AB <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>Per-bank REFRESH Average Current:</b> tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PB <sub>1</sub>	V <sub>DD1</sub>	1,10
	IDD5PB <sub>2</sub>	V <sub>DD2</sub>	1,10
	IDD5PB <sub>Q</sub>	V <sub>DDQ</sub>	1,4,10
<b>Power Down Self refresh current (-40°C to +95°C):</b> CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH; CKE is LOW; CA bus inputs are stable Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT is disabled	IDD6 <sub>1</sub>	V <sub>DD1</sub>	6,7,9,10
	IDD6 <sub>2</sub>	V <sub>DD2</sub>	6,7,9,10
	IDD6 <sub>Q</sub>	V <sub>DDQ</sub>	4,6,7,9,10

**Note:**

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000<sub>B</sub>.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of V<sub>DDQ</sub> and V<sub>DD2</sub>.
5. Guaranteed by design with output load = 5pF and RON = 40ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR4x device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. For all IDD measurements, V<sub>IHCKE</sub> = 0.8 x V<sub>DD2</sub>, V<sub>ILCKE</sub> = 0.2 x V<sub>DD2</sub>.
9. IDD6 25°C is guaranteed, IDD6 95°C is typical of the distribution of the arithmetic mean.
10. These specification values are the summation of all the channel current and both channels are under the same condition at the same time.
11. Dual Channel devices are specified in dual channel operation (both channels operating together).

Symbol		Power Supply	32Gb 1CS x32 (2Ch, x16/Ch)	Unit	
			4266		
IDD0	IDD0 <sub>1</sub>	V <sub>DD1</sub>	10	mA	
	IDD0 <sub>2</sub>	V <sub>DD2</sub>	52	mA	
	IDD0 <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD2P	IDD2P <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD2P <sub>2</sub>	V <sub>DD2</sub>	6.8	mA	
	IDD2P <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD2PS	IDD2PS <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD2PS <sub>2</sub>	V <sub>DD2</sub>	6.8	mA	
	IDD2PS <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD2N	IDD2N <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD2N <sub>2</sub>	V <sub>DD2</sub>	28	mA	
	IDD2N <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD2NS	IDD2NS <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD2NS <sub>2</sub>	V <sub>DD2</sub>	24	mA	
	IDD2NS <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD3P	IDD3P <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD3P <sub>2</sub>	V <sub>DD2</sub>	12.4	mA	
	IDD3P <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD3PS	IDD3PS <sub>1</sub>	V <sub>DD1</sub>	4.8	mA	
	IDD3PS <sub>2</sub>	V <sub>DD2</sub>	12.4	mA	
	IDD3PS <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD3N	IDD3N <sub>1</sub>	V <sub>DD1</sub>	6.8	mA	
	IDD3N <sub>2</sub>	V <sub>DD2</sub>	32	mA	
	IDD3N <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD3NS	IDD3NS <sub>1</sub>	V <sub>DD1</sub>	6.8	mA	
	IDD3NS <sub>2</sub>	V <sub>DD2</sub>	28	mA	
	IDD3NS <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD4R	IDD4R <sub>1</sub>	V <sub>DD1</sub>	22	mA	
	IDD4R <sub>2</sub>	V <sub>DD2</sub>	410	mA	
	IDD4R <sub>Q</sub>	V <sub>DDQ</sub>	188	mA	
IDD4W	IDD4W <sub>1</sub>	V <sub>DD1</sub>	22	mA	
	IDD4W <sub>2</sub>	V <sub>DD2</sub>	320	mA	
	IDD4W <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD5	IDD5 <sub>1</sub>	V <sub>DD1</sub>	46	mA	
	IDD5 <sub>2</sub>	V <sub>DD2</sub>	290	mA	
	IDD5 <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD5AB	IDD5AB <sub>1</sub>	V <sub>DD1</sub>	13.2	mA	
	IDD5AB <sub>2</sub>	V <sub>DD2</sub>	48	mA	
	IDD5AB <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD5PB	IDD5PB <sub>1</sub>	V <sub>DD1</sub>	9.6	mA	
	IDD5PB <sub>2</sub>	V <sub>DD2</sub>	48	mA	
	IDD5PB <sub>Q</sub>	V <sub>DDQ</sub>	1.5	mA	
IDD6	IDD6 <sub>1</sub>	25°C	V <sub>DD1</sub>	1	mA
		95°C		8	mA
	IDD6 <sub>2</sub>	25°C	V <sub>DD2</sub>	2.4	mA
		95°C		20	mA
	IDD6 <sub>Q</sub>	25°C	V <sub>DDQ</sub>	0.04	mA
		95°C		1.5	mA

# 1 Function Description

## 1.1 Power-up Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as below Table 1 and Table 2.

### LPDDR4 (1.1V $V_{DDQ}$ ) - MRS Defaults Settings

Table 1 - MRS Default Settings (LPDDR4)

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00 <sub>B</sub>	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0 <sub>B</sub>	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000 <sub>B</sub>	WL = 4
RL	MR2 OP[2:0]	000 <sub>B</sub>	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000 <sub>B</sub>	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00 <sub>B</sub>	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000 <sub>B</sub>	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000 <sub>B</sub>	DQ ODT is disabled
$V_{REFCA}$ Setting	MR12 OP[6]	1 <sub>B</sub>	$V_{REFCA}$ Range[1] enabled
$V_{REFCA}$ Value	MR12 OP[5:0]	001101 <sub>B</sub>	Range1: 27.2% of $V_{DD2}$
$V_{REFDQ}$ Setting	MR14 OP[6]	1 <sub>B</sub>	$V_{REFDQ}$ Range[1] enabled
$V_{REFDQ}$ Value	MR14 OP[5:0]	001101 <sub>B</sub>	Range1: 27.2% of $V_{DDQ}$

### LPDDR4X (0.6V $V_{DDQ}$ ) - MRS defaults settings

Table 2 - MRS Default Settings (LPDDR4X)

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00 <sub>B</sub>	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0 <sub>B</sub>	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000 <sub>B</sub>	WL = 4
RL	MR2 OP[2:0]	000 <sub>B</sub>	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000 <sub>B</sub>	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00 <sub>B</sub>	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000 <sub>B</sub>	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000 <sub>B</sub>	DQ ODT is disabled
$V_{REFCA}$ Setting	MR12 OP[6]	1 <sub>B</sub>	$V_{REFCA}$ Range[1] enabled
$V_{REFCA}$ Value	MR12 OP[5:0]	011101 <sub>B</sub>	Range1: 50.3% of $V_{DDQ}$
$V_{REFDQ}$ Setting	MR14 OP[6]	1 <sub>B</sub>	$V_{REFDQ}$ Range[1] enabled
$V_{REFDQ}$ Value	MR14 OP[5:0]	011101 <sub>B</sub>	Range1: 50.3% of $V_{DDQ}$

### 1.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after  $T_a$ ), RESET\_n is recommended to be LOW ( $\leq 0.2 \times V_{DD2}$ ) and all other inputs must be between  $V_{IL(min)}$  and  $V_{IH(max)}$ . The device outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table 8.  $V_{DD1}$  must ramp at the same time or earlier than  $V_{DD2}$ .  $V_{DD2}$  must ramp at the same time or earlier than  $V_{DDQ}$ .

Table 3 - Voltage Ramp Conditions

After	Applicable Condition
Ta is reached	$V_{DD1}$ must be greater than $V_{DD2}$
	$V_{DD2}$ must be greater than $V_{DDQ} - 200mV$

**Note:**

1.  $T_a$  is the point when any power supply first reaches 300mV.
  2. Voltage ramp conditions in above table apply between  $T_a$  and power-off (controlled or uncontrolled).
  3.  $T_b$  is the point at which all supply and reference voltages are within their defined ranges.
  4. Power ramp duration  $t_{INIT0}$  ( $T_b - T_a$ ) must not exceed 20ms.
  5. The voltage difference between any  $V_{SS}$  and  $V_{SSQ}$  pins must not exceed 100mV.
2. Following the completion of the voltage ramp ( $T_b$ ), RESET\_n must be maintained LOW. DQ, DMI, DQS\_t and DQS\_c voltage levels must be between  $V_{SSQ}$  and  $V_{DDQ}$  during voltage ramp to avoid latch-up. CKE, CK\_t, CK\_c, CS\_n and CA input levels must be between  $V_{SS}$  and  $V_{DD2}$  during voltage ramp to avoid latch-up.
  3. Beginning at  $T_b$ , RESET\_n must remain LOW for at least  $t_{INIT1}(T_c)$ , after which RESET\_n can be de-asserted to HIGH( $T_c$ ). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

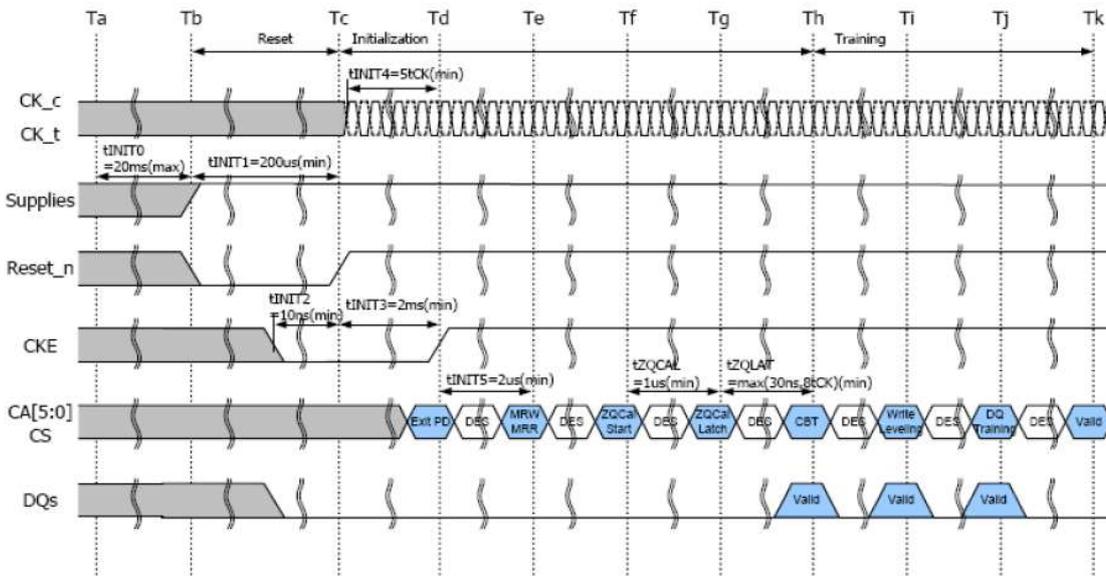


Figure 1 - Power Ramp and Initialization Sequence

**Note:**

1. Training is optional and may be done at the system architects' discretion. The training sequence after ZQ\_CAL Latch (The Sequence7-9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.
4. After RESET\_n is de-asserted ( $T_c$ ), wait at least  $t_{INIT3}$  before activating CKE. Clock (CK\_t,CK\_c) is required to be start- ed and stabilized for  $t_{INIT4}$  before CKE goes active( $T_d$ ). CS is required to be maintained LOW when controller activates CKE.
5. After setting CKE high, wait minimum of  $t_{INIT5}$  to issue any MRR or MRW commands ( $T_e$ ). For both MRR and MRW commands, the clock frequency must be within the range defined for  $tCKb$ . Some AC parameters (for example,  $tDQSCKb$ ) could have relaxed timings (such as  $tDQSCKb$ ) before the system is appropriately configured.
6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory ( $T_f$ ). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after  $tZQCAL$  ( $T_g$ ) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal V<sub>REFCA</sub>, CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V<sub>REF</sub> and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and V<sub>REFCA</sub> set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/ exit the training mode.
8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS\_t/\_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.
9. After write leveling, the DQ Bus (internal V<sub>REFDQ</sub>, DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust V<sub>REFDQ</sub> (Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and V<sub>REFDQ</sub> set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.
10. At Tk the LPDDR4 device is ready for normal operation and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

**Table 4 - Initialization Timing Parameters**

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0		20	ms	Maximum Voltage Ramp Time
tINIT1	200		us	Minimum RESET_N Low time after completion of voltage ramp
tINIT2	10		ns	Minimum CKE Low time before RESET_n goes High
tINIT3	2		ms	Minimum CKE Low time after RESET_n goes High
tINIT4	5		tCK	Minimum stable clock before first CKE High
tINIT5	2		us	Minimum idle time before first MRW/MRR command
tZQCAL	1		us	ZQ Calibration time
tZQLAT	Max(30ns, 80tCK)		ns	ZQCAL latch quite time
tCKb	Note 1,2	Note 1,2	ns	Clock cycle time during boot

**Note:**

1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

### 1.1.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET\_n below 0.2 x V<sub>DD2</sub> anytime when reset is needed. RESET\_n needs to be maintained for minimum tPW\_RESET. CKE must be pulled Low at least 10ns before de-asserting RESET\_n.
2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

**Table 5 - Reset Timing Parameter**

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low time for Reset Initialization with stable power

### 1.1.3 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ( $\leq 0.2 \times V_{DD2}$ ) and all other inputs must be between  $V_{IL(min)}$  and  $V_{IH(max)}$ . The device's output remains at High-Z while CKE is held LOW. DQ, DMI, DQS\_t and DQS\_c voltage levels must be between  $V_{SSQ}$  and  $V_{DDQ}$  during voltage ramp to avoid latch-up. RESET\_n, CK\_t, CK\_c, CS and CA input levels must be between  $V_{SS}$  and  $V_{DD2}$  during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

**Table 6 - Power Supply Condition**

Between	Applicable Conditions
Tx and Tz	$V_{DD1}$ must be greater than $V_{DD2}$
	$V_{DD2}$ must be greater than $V_{DDQ} - 200mV$

**Note:**

- The voltage difference between any of  $V_{SS}$ ,  $V_{SSQ}$  pins must not exceed 100mV

### 1.1.4 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled.  $V_{DD1}$  and  $V_{DD2}$  must decrease with a slope lower than  $0.5 V/\mu s$  between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Table 7 - Timing Parameter Power Off**

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-off ramp item

## 1.2 Mode Register Definition

### 1.2.1 Mode Register Assignment and Definition in LPDDR4 SDRAM

Below table shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

**Table 8 - Mode Register Assignment in LPDDR4 SDRAM**

MR#	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
0	R	RFU			RZQI		RFM Support	Latency Mode	Refresh mode	
1	W	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL		
2	W	WR Lev	WLS	WL			RL			
3	W	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL	
4	R/W	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate			
5	R	LPDDR4 Manufacturer ID								
6	R	Revision ID-1								
7	R	Revision ID-2								
8	R	I/O Width			Density				Type	
9	W	Vendor Specific Test Register								
10	W	RFU								ZQ-Reset
11	W	RFU	CA ODT			RFU	DQ ODT			
12	R/W	RFU	VR-CA	V <sub>REFCA</sub>						
13	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT	
14	R/W	RFU	VR-DQ	V <sub>REFDQ</sub>						
15	W	Lower-Byte Invert Register for DQ Calibration								
16	W	PASR Bank Mask								
17	W	PASR Segment Mask								
18	R	DQS Oscillator Count – LSB								
19	R	DQS Oscillator Count – MSB								
20	W	Upper-Byte Invert Register for DQ Calibration								
21	N/A	RFU								
22	W	ODTD for x8 2ch(Byte) mode	ODT-CA	ODT-CS	ODT-CK	SoC ODT				
23	W	DQS Interval Timer Run Time Setting								
24	R/W	TRR mode	TRR mode BAn			Unlimited MAC	MAC Value			
	R	RAAMMT			RAAIMT					RFM
25	R	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0	
26:29	N/A	RFU								
30	N/A	Reserved for Testing – SDRAM will ignore								
31	N/A	RFU								
32	W	DQ Calibration Pattern "A" (Default = 5A <sub>H</sub> )								
33:35	N/A	RFU								
36	R	RFU						RAADEC		
37:38	N/A	Do Not Use								
39	N/A	Reserved for Testing – SDRAM will ignore								
40	W	DQ Calibration Pattern "B" (Default = 3C <sub>H</sub> )								
41:47	N/A	Do Not Use								
48:63	N/A	RFU								

**Note:**

- RFU bits shall be set to '0' during write.
- RFU bits shall be read as '0' during read.
- All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS\_t, DQS\_c shall be toggled.
- All mode registers that are specified as RFU shall not be written.
- Write to read-only registers shall have no impact on the functionality of the device.

### 1.3 Simplified State Diagram

LPDDR4 SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see Section “Command Definition and Timing Diagram”.

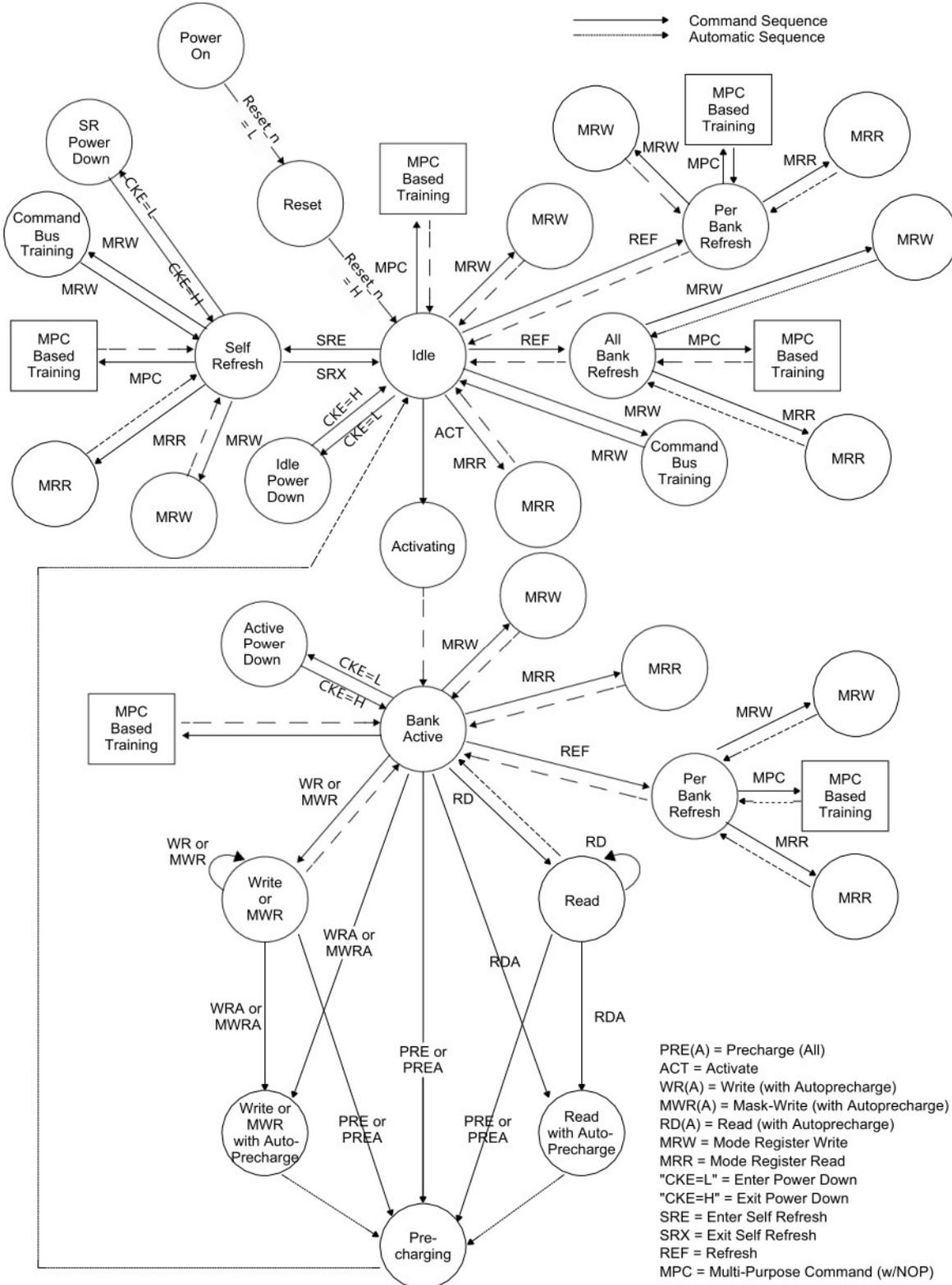


Figure 2 - LPDDR4 Simplified Bus Interface State Diagram - Sheet 1

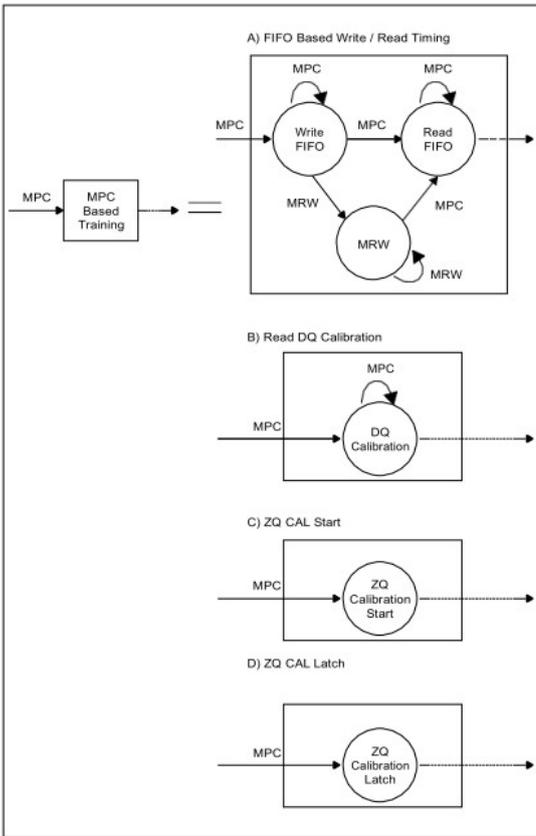


Figure 3 - LPDDR4 Simplified Bus Interface State Diagram - Sheet 2

**Note:**

1. From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2. In IDLE state, all banks are precharged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET\_n pin can be asserted from any state and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET\_n.

## 2 Command Definitions and Timing Diagrams

### 2.1 Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4x device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held High when the commands listed in the command truth table input.

#### 2.1.1 Command Truth Table

Table 9 - Command Truth Table

SDRAM Command	SDR Command Pin	SDR CA Pin							Note	
	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge		
Deselect (DES)	L	X							R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9	
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2		
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4	
	L	BA0	BA1	BA2	V	V	V	R2		
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4	
	L	BA0	BA1	BA2	V	V	V	R2		
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2	
	L	V								R2
Write-1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9	
	L	BA0	BA1	BA2	V	C9	AP	R2		
Self Refresh Exist (SRX)	H	L	L	H	L	H	V	R1	1,2	
	L	V								R2
Mask Write-1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9	
	L	BA0	BA1	BA2	V	C9	AP	R2		
RFU	H	L	L	H	H	H	V	R1	1,2	
	L	V								R2
Read (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9	
	L	BA0	BA1	BA2	V	C9	AP	R2		
CAS-2 (Write-2, Mask Write-2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9	
	L	C2	C3	C4	C5	C6	C7	R2		
RFU	H	L	H	L	H	L	V	R1	1,2	
	L	V								R2
RFU	H	L	H	L	H	H	V	R1	1,2	
	L	V								R2
Mode Register Write-1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11	
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2		
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11	
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2		
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12	
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2		
RFU	H	L	H	H	H	H	V	R1	1,2	
	L	V								R2
Activate-1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10	
	L	BA0	BA1	BA2	R16	R10	R11	R2		
Activate-2 (ACT-2)	H	R17	R18	R6	R7	R8	R9	R1	1,10,13	
	L	R0	R1	R2	R3	R4	R5	R2		

**Note:**

- All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
- "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
- Bank addresses BA[2:0] determine which bank is to be operated upon.
- AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
- Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
- AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.
- If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
- For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
- Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
- Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
- MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
- MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.
- For device densities not requiring R17 and R18, R17 and R18 must both be driven High for every ACT-2 command to maintain backward compatibility. For device densities not requiring R18, R18 must be driven High for every ACT-2 command to maintain backward compatibility.
- CA3 R2 edge is 'V' when RFM is not required, but becomes 'RFM' when read-only MR24 OP[0]=1B.
- Issuing the RFMpb or RFMab command allows the LPDDR4 to use the command period for additional Refresh Management.

## 2.2 Pull Up/Pul Down Driver Characteristics and Calibration

The characteristics and calibration are shown in Table 10 through Table 12.

**Table 10 - Pull down Driver Characteristic, with ZQ calibration**

RONPD,NOM	Resistor	Min	Nom	Max	Unit
40ohm	RON40PD	0.90	1.00	1.10	RZQ/6
48ohm	RON48PD	0.90	1.00	1.10	RZQ/5
60ohm	RON60PD	0.90	1.00	1.10	RZQ/4
80ohm	RON80PD	0.90	1.00	1.10	RZQ/3
120ohm	RON120PD	0.90	1.00	1.10	RZQ/2
240ohm	RON240PD	0.90	1.00	1.10	RZQ/1

**Note:**

- All values are after ZQ Calibration. Without ZQ Calibration RONPD values are ±30%.

**Table 11 - Pull-up Driver Characteristic, with ZQ Calibration**

VOH <sub>pu,nom</sub>	VOH,nom (mV)	Min	Nom	Max	Unit
<b>LPDDR4 (1.1V V<sub>DDQ</sub>)</b>					
V <sub>DDQ</sub> / 2.5	440	0.90	1.00	1.10	VOH,nom
V <sub>DDQ</sub> / 3	367	0.90	1.00	1.10	VOH,nom
<b>LPDDR4X (0.6V V<sub>DDQ</sub>)</b>					
V <sub>DDQ</sub> x 0.5	300	0.90	1.00	1.10	VOH,nom
V <sub>DDQ</sub> x 0.6	360	0.90	1.00	1.10	VOH,nom

**Note:**

- All values are after ZQ Calibration. Without ZQ Calibration VOH(nom)<sub>OH(nom)</sub> values are ±30%.
- VOH,nom for LPDDR4 values are based on a nominal V<sub>DDQ</sub> = 1.1V.
- VOH,nom for LPDDR4 values are based on a nominal V<sub>DDQ</sub> = 0.6V.

Table 12 - Valid Calibration Point

VOH <sub>PU,nom</sub>	ODT Value					
	240	120	80	60	48	40
<b>LPDDR4 (1.1V V<sub>DDQ</sub>)</b>						
V <sub>DDQ</sub> / 2.5	VALID	VALID	VALID	DNU	DNU	DNU
V <sub>DDQ</sub> / 3	VALID	VALID	VALID	VALID	VALID	VALID
<b>LPDDR4X (0.6V V<sub>DDQ</sub>)</b>						
V <sub>DDQ</sub> x 0.5	VALID	VALID	VALID	VALID	VALID	VALID
V <sub>DDQ</sub> x 0.6	DNU	VALID	DNU	VALID	DNU	DNU

**Note:**

- Once the output is calibrated for a given V<sub>OH(nom)</sub> calibration point, the ODT value may be changed without recalibration.
- If the V<sub>OH(nom)</sub> calibration point is changed, then re-calibration is required.
- DNU = Do Not Use.

### 3 Absolute Maximum DC Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13 - Absolute Maximum DC Rating

Parameter	Symbol	Min	Max	Unit	Note
V <sub>DD1</sub> supply voltage relative to V <sub>SS</sub>	V <sub>DD1</sub>	-0.4	2.1	V	1
V <sub>DD2</sub> supply voltage relative to V <sub>SS</sub>	V <sub>DD2</sub>	-0.4	1.4	V	1
V <sub>DDQ</sub> supply voltage relative to V <sub>SSQ</sub>	V <sub>DDQ</sub>	-0.4	1.4	V	1
Voltage on any ball except V <sub>DD1</sub> relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.4	1.4	V	
Storage Temperature	T <sub>STG</sub>	-55	125	°C	2

**Note:**

- See Power Ramp for relationship between power supplies.
- Storage Temperature is the case surface temperature on the center/top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2 standard

## 4 AC and DC Operating Conditions

### 4.1 Recommended DC Operating Condition

#### LPDDR4 (1.1V $V_{DDQ}$ ) – Recommended DC Operating Condition

Table 14 - Recommended DC Operating Conditions (LPDDR4)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{DD1}$	Core 1 Power	1.70	1.80	1.95	V	1,2
$V_{DD2}$	Core 2 Power / Input Buffer Power	1.06	1.10	1.17	V	1,2,3
$V_{DDQ}$	I/O Buffer Power	1.06	1.10	1.17	V	2,3

**Note:**

- $V_{DD1}$  uses significantly less current than  $V_{DD2}$ .
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
- $V_{dIVW}$  and  $T_{dIVW}$  limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20 MHz.

#### LPDDR4X (0.6V $V_{DDQ}$ ) - Recommended DC Operating Condition

Table 15 - Recommended DC Operating Conditions (LPDDR4X)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{DD1}$	Core 1 Power	1.70	1.80	1.95	V	1,2
$V_{DD2}$	Core 2 Power / Input Buffer Power	1.06	1.10	1.17	V	1,2,3
$V_{DDQ}$	I/O Buffer Power	0.57	0.6	0.65	V	2,3,4,5

**Note:**

- $V_{DD1}$  uses significantly less current than  $V_{DD2}$ .
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
- The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the  $T_{dIVW}$ .
- $V_{DDQ}(\max)$  may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.
- Pull up, pull down and ZQ calibration tolerance spec is valid only in normal  $V_{DDQ}$  tolerance range (0.57 V - 0.65 V).

### 4.2 Input Leakage Current

Table 16 - Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input Leakage Current	$I_L$	-4	4	uA	1,2

**Note:**

- For  $CK_t$ ,  $CK_c$ ,  $CKE$ ,  $CS$ ,  $CA$ ,  $ODT_{CA}$  and  $RESET_n$ . Any input  $0V \leq V_{IN} \leq V_{DD2}$  (All other pins not under test = 0V)
- $CA$  ODT is disabled for  $CK_t$ ,  $CK_c$ ,  $CS$  and  $CA$ .

### 4.3 Input/Output Leakage Current

Table 17 - Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/Output Leakage Current	$I_{OZ}$	-5	5	uA	1,2

**Note:**

- For  $DQ$ ,  $DQS_t$ ,  $DQS_c$  and  $DMI$ . Any I/O  $0V \leq V_{OUT} \leq V_{DDQ}$
- I/O status are disabled. High Impedance and ODT off.

## 4.4 Operating Temperature Range

Table 18 - Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit	Note
Commercial Temperature	$T_{\text{OPER}}$	-25	85	°C	1,2
Industrial Temperature		-40	95	°C	1,2

**Note:**

1. Operating Temperature is the case surface temperature on the center top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2.
2. Either the device case temperature rating or the temperature sensor (see Section 4.37 in JESD209-4) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the  $T_{\text{OPER}}$  rating that applies for the Commercial or Industrial Temperature Ranges. For example,  $T_{\text{CASE}}$  may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.

## 5 AC and DC Input/Output Measurement Levels

### 5.1 1.1V High Speed LVCMOS (HS\_LLVC MOS)

#### 5.1.1 Standard Specification

All Voltages are referenced to ground except where noted.

#### 5.1.2 DC Electrical Characteristics

##### 5.1.2.1 LPDDR4 Input Level for CKE

This definition applies to CKE\_A/B. Table 19 provides the input levels; Figure 4 shows the timing.

Table 19 - LPDDR4 Input Level for CKE

Parameter	Symbol	Min	Max	Unit	Note
Input High Level (AC)	$V_{IH(AC)}$	$0.75 \times V_{DD2}$	$V_{DD2} + 0.2$	V	1
Input Low Level (AC)	$V_{IL(AC)}$	-0.2	$0.25 \times V_{DD2}$	V	1
Input High Level (DC)	$V_{IH(DC)}$	$0.65 \times V_{DD2}$	$V_{DD2} + 0.2$	V	
Input Low Level (DC)	$V_{IL(DC)}$	-0.2	$0.35 \times V_{DD2}$	V	

**Note:**

1. Refer to LPDDR4 AC Over/Undershoot section.

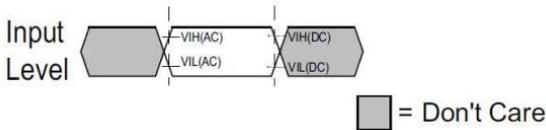


Figure 4 - LPDDR4 Input AC Timing Definition for CKE

**Note:**

1. AC level is guaranteed transition point.
2. DC level is hysteresis.

##### 5.1.2.2 LPDDR4 Input Level for Reset\_n and ODT\_CA

This definition applies to RESET\_n and ODT\_CA. Table 20 provides the input levels; Figure 5 shows the timing.

Table 20 - LPDDR4 Input Level for Reset\_n and ODT\_CA

Parameter	Symbol	Min	Max	Unit	Note
Input High Level	$V_{IH}$	$0.80 \times V_{DD2}$	$V_{DD2} + 0.2$	V	1
Input Low Level	$V_{IL}$	-0.2	$0.20 \times V_{DD2}$	V	1

**Note:**

1. Refer to LPDDR4 AC Over/Undershoot section.

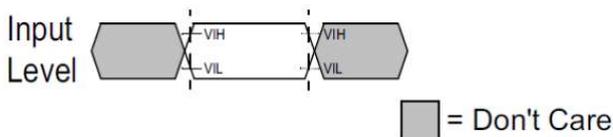


Figure 5 - LPDDR4 Input AC Timing Definition for Reset\_n and ODT\_CA

## 5.2 Differential Input Voltage

### 5.2.1 Differential Input Voltage for CK

The minimum input voltage needs to satisfy both  $V_{indiff\_CK}$  and  $V_{indiff\_CK}/2$  specification at input receiver and their measurement period is  $1t_{CK}$ .  $V_{indiff\_CK}$  is the peak-to-peak voltage centered on 0 volts differential and  $V_{indiff\_CK}/2$  is max and min peak voltage from 0V.

Figure 6 and Table 21 shows the input voltage.

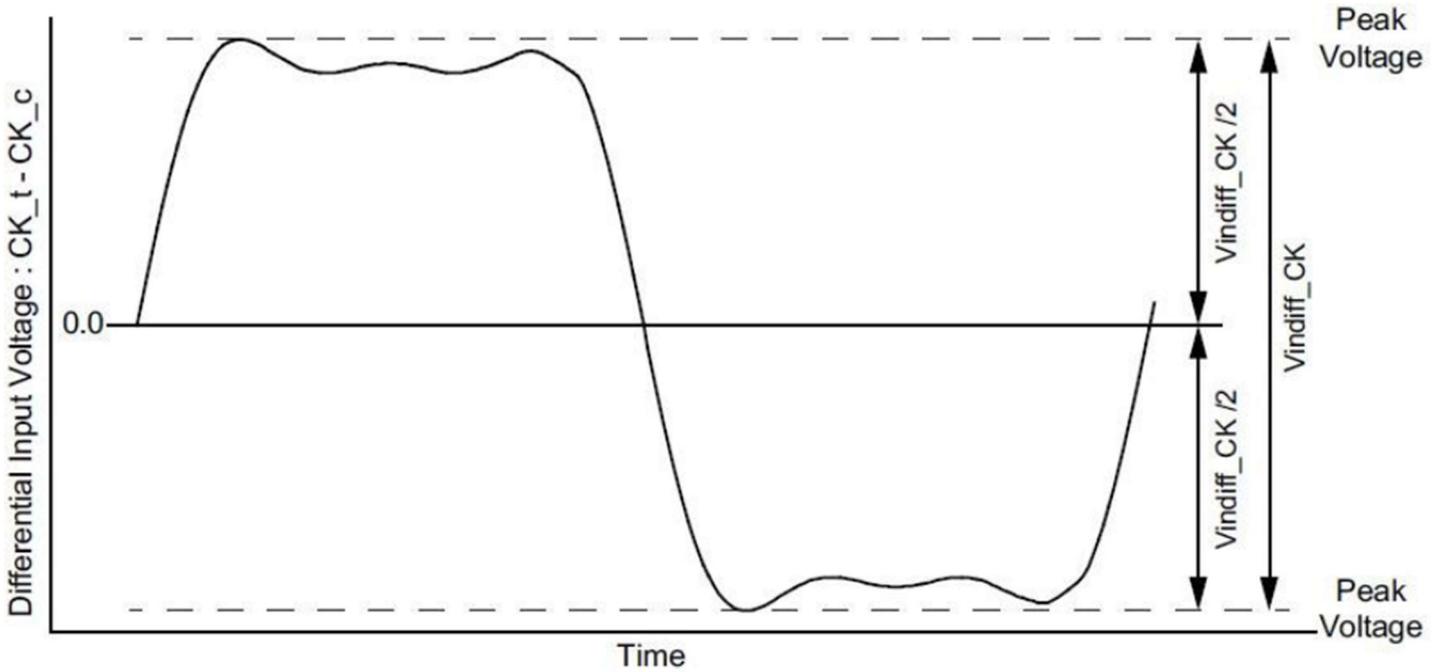


Figure 6 - CK Differential Input Voltage

Table 21 - CK Differential Input Voltage

Parameter	Symbol	Data Rate		Unit	Note
		3733 / 4266			
		Min	Max		
CK Differential Input Voltage	$V_{indiff\_CK}$	360	-	mV	1

**Note:**

1. The peak voltage of Differential CK signals is calculated in the following equation.

$$V_{indiff\_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

- Max Peak Voltage =  $\text{Max}(f(t))$
- Min Peak Voltage =  $\text{Min}(f(t))$
- $f(t) = V_{CK\_t} - V_{CK\_c}$

### 5.2.2 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals is calculated in the following equation.

$$VIH.DIFF.PEAK \text{ Voltage} = \text{Max}(f(t))$$

$$VIL.DIFF.PEAK \text{ Voltage} = \text{Min}(f(t))$$

$$f(t) = VCK\_t - VCK\_c$$

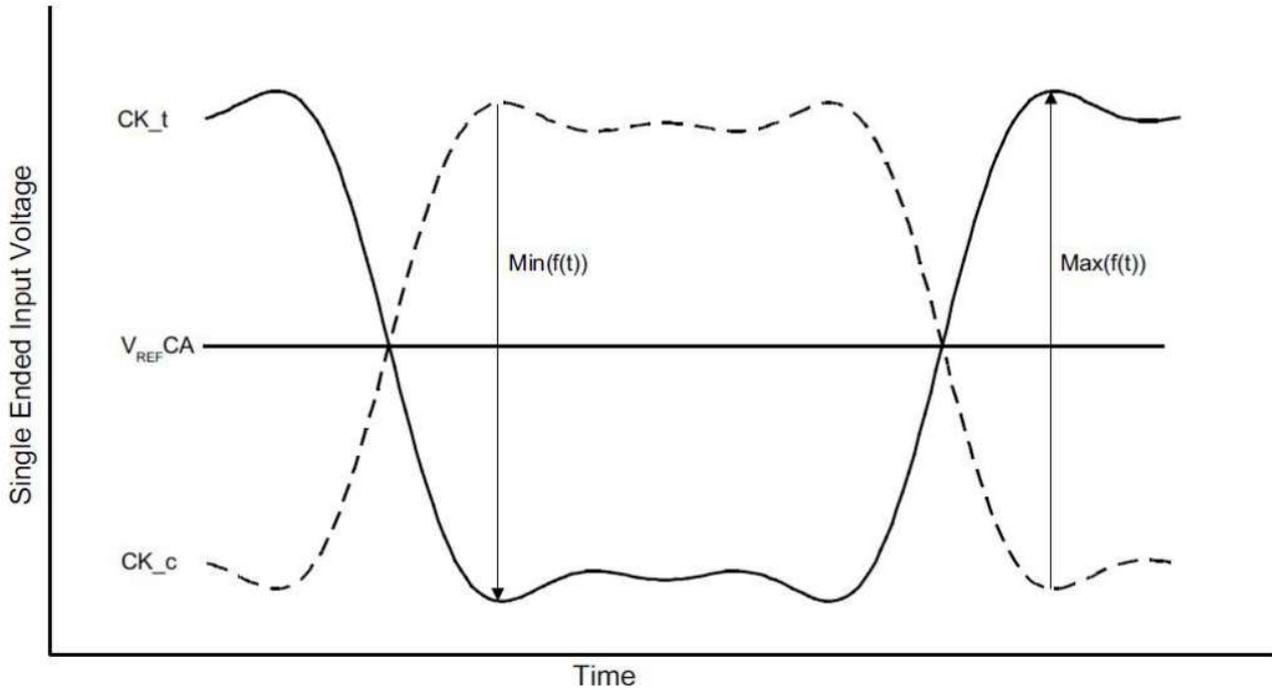


Figure 7 - Definition of Differential Clock Peak Voltage

Note:

1.  $V_{REF\_CA}$  is LPDDR4 internal setting value by  $V_{REF}$  Training.

### 5.2.3 Single-ended Input Voltage for Clock

The minimum input voltage needs to satisfy both both  $V_{inse\_CK}$ ,  $V_{inse\_CK\_High/Low}$  specification at input receiver. (See Figure 8 and Table 22)

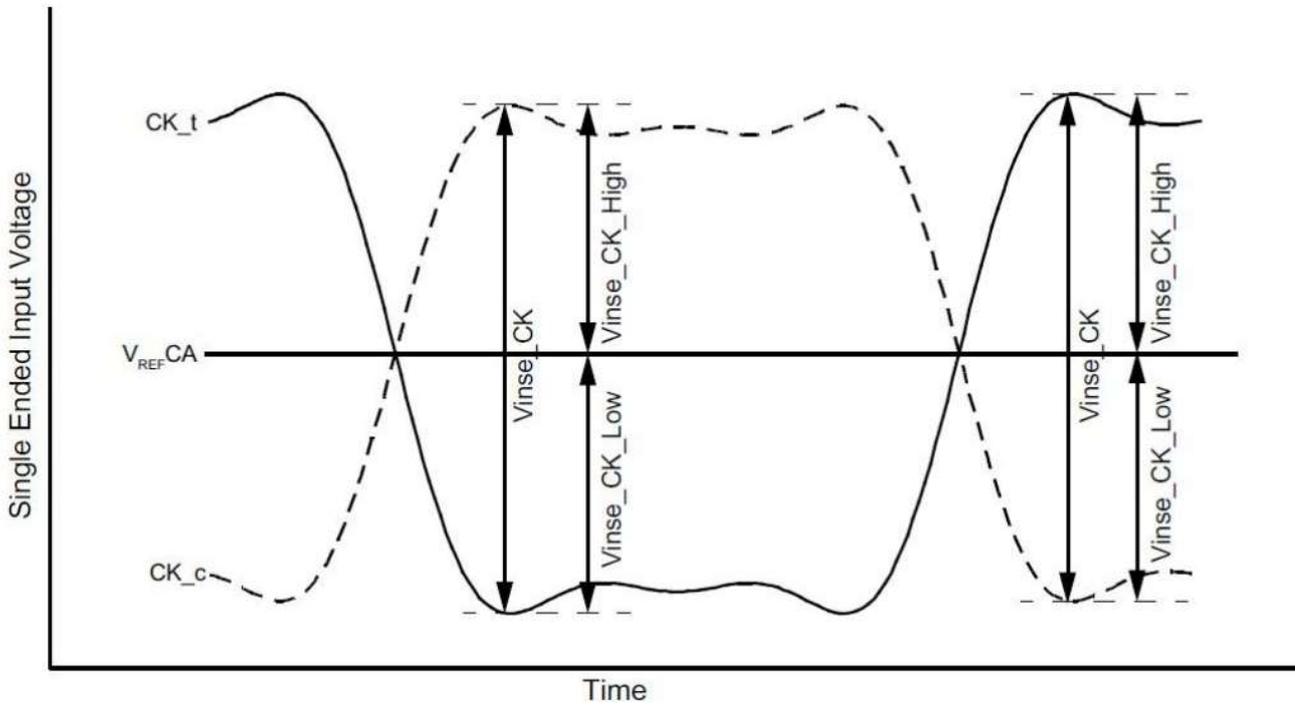


Figure 8 - Clock Single-Ended Input Voltage

Note:

- $V_{REFCA}$  is LPDDR4 internal setting value by  $V_{REF}$  Training.

Table 22 – Clock Single-Ended Input Voltage

Parameter	Symbol	Data Rate		Unit
		3733 / 4266		
		Min	Max	
Clock Single-Ended Input Voltage	$V_{inse\_CK}$	180	-	mV
Clock Single-Ended Input Voltage High for $V_{REFDQ}$	$V_{inse\_CK\_High}$	90	-	mV
Clock Single-Ended Input Voltage Low for $V_{REFDQ}$	$V_{inse\_CK\_Low}$	90	-	mV

### 5.2.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK<sub>t</sub>, CK<sub>c</sub>) are defined and measured as shown in Figure 9 and Table 23 through Table 25.

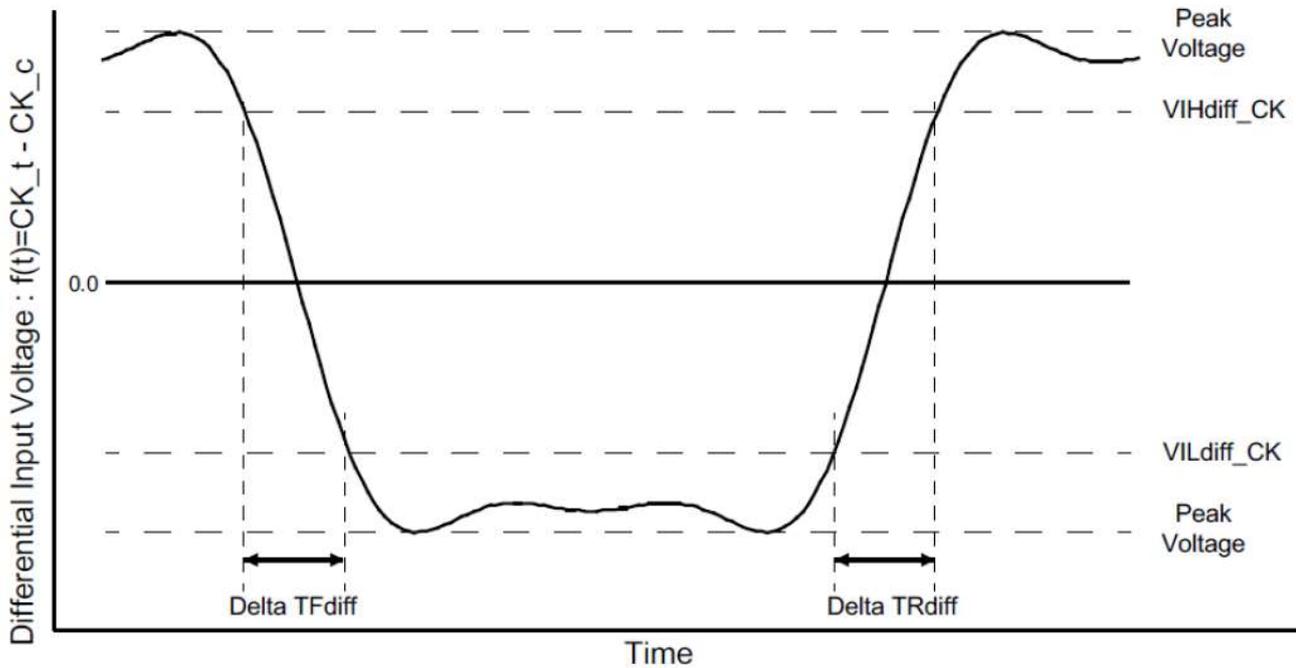


Figure 9 – Differential Input Slew Rate Definition for CK<sub>t</sub> and CK<sub>c</sub>

Note:

1. Differential signal rising edge from VILdiff\_CK to VIHdiff\_CK must be monotonic slope.
2. Differential signal falling edge from VIHdiff\_CK to VILdiff\_CK must be monotonic slope.

Table 23 – Differential Input Slew Rate Definition for CK<sub>t</sub> and CK<sub>c</sub>

Description	From	To	Defined by
Differential Input Slew Rate for Rising Edge (CK <sub>t</sub> – CK <sub>c</sub> )	VILdiff_CK	VIHdiff_CK	$ VILdiff\_CK - VIHdiff\_CK  / \Delta TRdiff$
Differential Input Slew Rate for Falling Edge (CK <sub>t</sub> – CK <sub>c</sub> )	VIHdiff_CK	VILdiff_CK	$ VILdiff\_CK - VIHdiff\_CK  / \Delta TFdiff$

Table 24 – Differential Input Level for CK<sub>t</sub> and CK<sub>c</sub>

Parameter	Symbol	Date Rate		Unit
		3733 / 4266		
		Min	Max	
Differential Input High	VILdiff_CK	145	-	mV
Differential Input Low	VIHdiff_CK	-	-145	mV

Table 25 - Differential Input Slew Rate for CK<sub>t</sub> and CK<sub>c</sub>

Parameter	Symbol	Date Rate		Unit
		3733 / 4266		
		Min	Max	
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	V/ns

### 5.2.5 Differential Input Cross Point Voltage for Clock

The cross-point voltage of differential input signals (CK<sub>t</sub>, CK<sub>c</sub>) are shown in Figure 10 and must meet the requirements in the Table 26. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level.

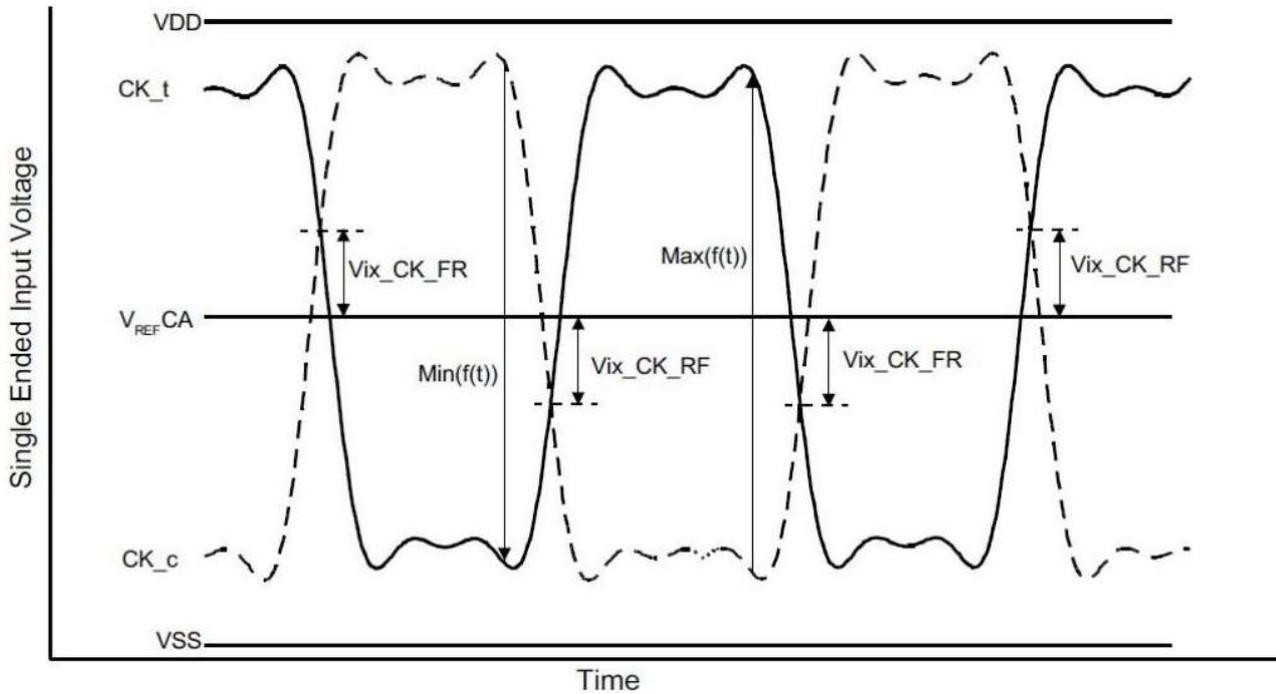


Figure 10 – VIX Definition (Clock)

**Note**

1. The base level of VIX\_CK\_FR/RF is V<sub>REFCA</sub> that is LPDDR4 SDRAM internal setting value by V<sub>REF</sub> Training

Table 26 – Cross Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	Data Rate		Unit	Note
		3733 / 4266			
		Min	Max		
Clock Differential Input Cross Point Voltage Ratio	VIX_CK_ratio	-	25	%	1,2,3,4

**Note:**

1. VIX\_CK\_ratio is defined by this equation:  $VIX\_CK\_ratio = VIX\_CK\_FR / |Min(f(t))|$
2. VIX\_CK\_ratio is defined by this equation:  $VIX\_CK\_ratio = VIX\_CK\_RF / Max(f(t))$
3. VIX\_CK\_FR is defined as delta between cross point (CK<sub>t</sub> fall, CK<sub>c</sub> rise) to Max(f(t))/2.  
VIX\_CK\_RF is defined as delta between cross point (CK<sub>t</sub> rise, CK<sub>c</sub> fall) to Max(f(t))/2.
4. In LPDDR4x un-terminated case, CK mid-level is calculated as:  
High level = V<sub>DDQ</sub>, Low level = V<sub>SS</sub>, Mid-level = V<sub>DDQ</sub>/2  
In LPDDR4 un-terminated case, Mid-level must be equal or lower than 369mV (33.6% of V<sub>DD2</sub>).

### 5.2.6 Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both  $V_{indiff\_DQS}$  and  $V_{indiff\_DQS}/2$  specification at input receiver and their measurement period is  $1UI(t_{CK}/2)$ .  $V_{indiff\_DQS}$  is the peak-to-peak voltage centered on 0 volts differential and  $V_{indiff\_DQS}/2$  is max and min peak voltage from 0V. (See Figure 11 and Table 27).

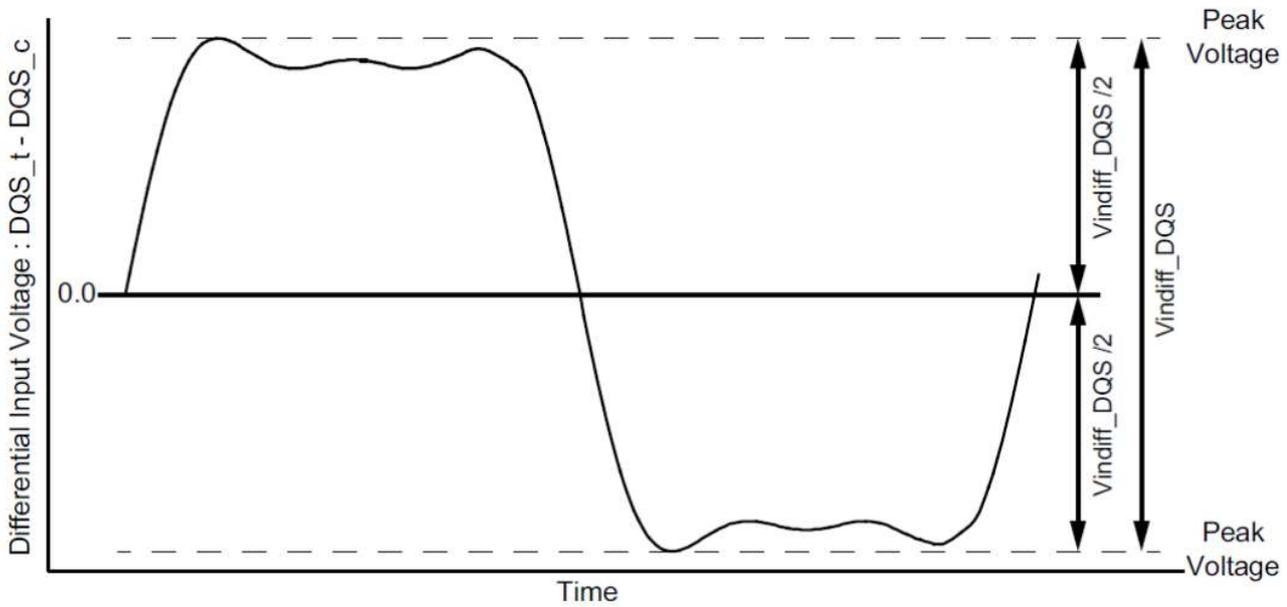


Figure 11 – DQS Differential Input Voltage

Table 27 – DQS Differential Input Voltage

Parameter	Symbol	Data Rate		Unit	Note
		3733 / 4266			
		Min	Max		
DQS Differential Input	$V_{indiff\_DQS}$	340	-	mV	1

**Note:**

- The peak voltage of Differential DQS signals is calculated in the following equation.
  - $V_{indiff\_DQS} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$
  - Max Peak Voltage =  $\text{Max}(f(t))$
  - Min Peak Voltage =  $\text{Min}(f(t))$
  - $f(t) = VDQS\_t - VDQS\_c$

### 5.2.7 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals is calculated in the following equation.

$$VIH.DIFF.Peak\ Voltage = \text{Max}(f(t))$$

$$VIL.DIFF.Peak\ Voltage = \text{Min}(f(t))$$

$$f(t) = VDQS\_t - VDQS\_c$$

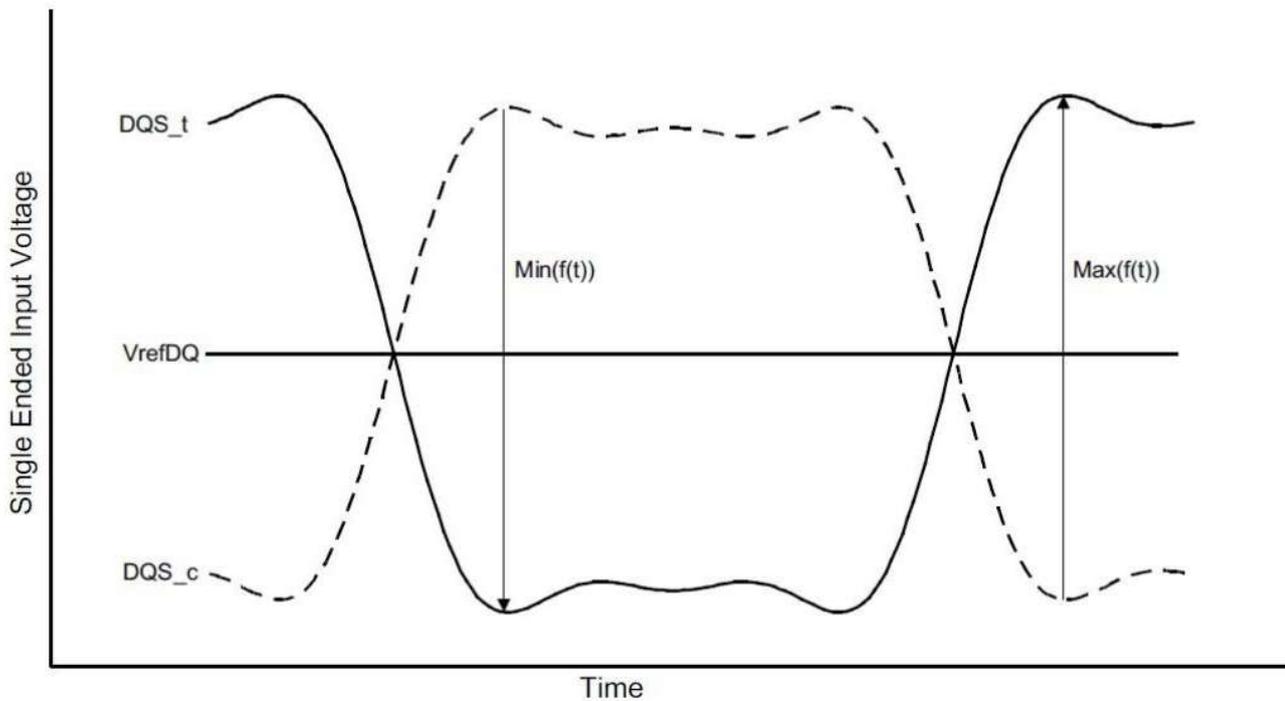


Figure 12 – Definition of Differential DQS Peak Voltage

Note:

1.  $V_{REFDQ}$  is LPDDR4 SDRAM Internal setting value by  $V_{REF}$  Training.

### 5.2.8 Single-ended Input Voltage for DQS

The minimum input voltage needs to satisfy both  $V_{inse\_DQS}$ ,  $V_{inse\_DQS\_High/Low}$  specification at input receiver as shown in Figure 13 and Table 28.

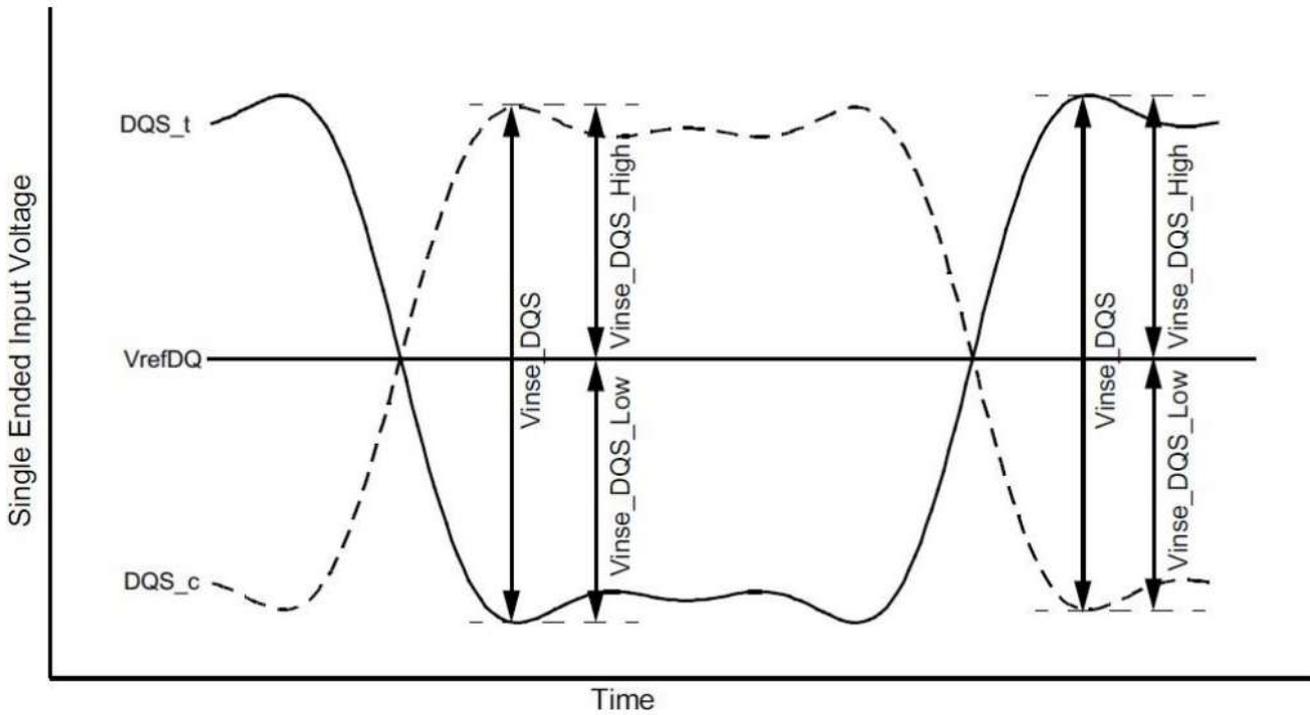


Figure 13 – DQS Single-ended Input Voltage

Note:

- $V_{REFDQ}$  is LPDDR4 SDRAM Internal setting value by  $V_{REF}$  Training.

Table 28 – DQS Single-ended Input Voltage

Parameter	Symbol	Data Rate		Unit	Note
		3733 / 4266			
		Min	Max		
DQS Single-ended Input Voltage	$V_{inse\_DQS}$	170	-	mV	
DQS Single-ended Input Voltage High from $V_{REFDQ}$	$V_{inse\_DQS\_High}$	85	-	mV	
DQS Single-ended Input Voltage Low from $V_{REFDQ}$	$V_{inse\_DQS\_Low}$	85	-	mV	

### 5.2.9 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS<sub>t</sub>, DQS<sub>c</sub>) are defined and measured as shown in Figure 14 and Table 29 through Table 31.

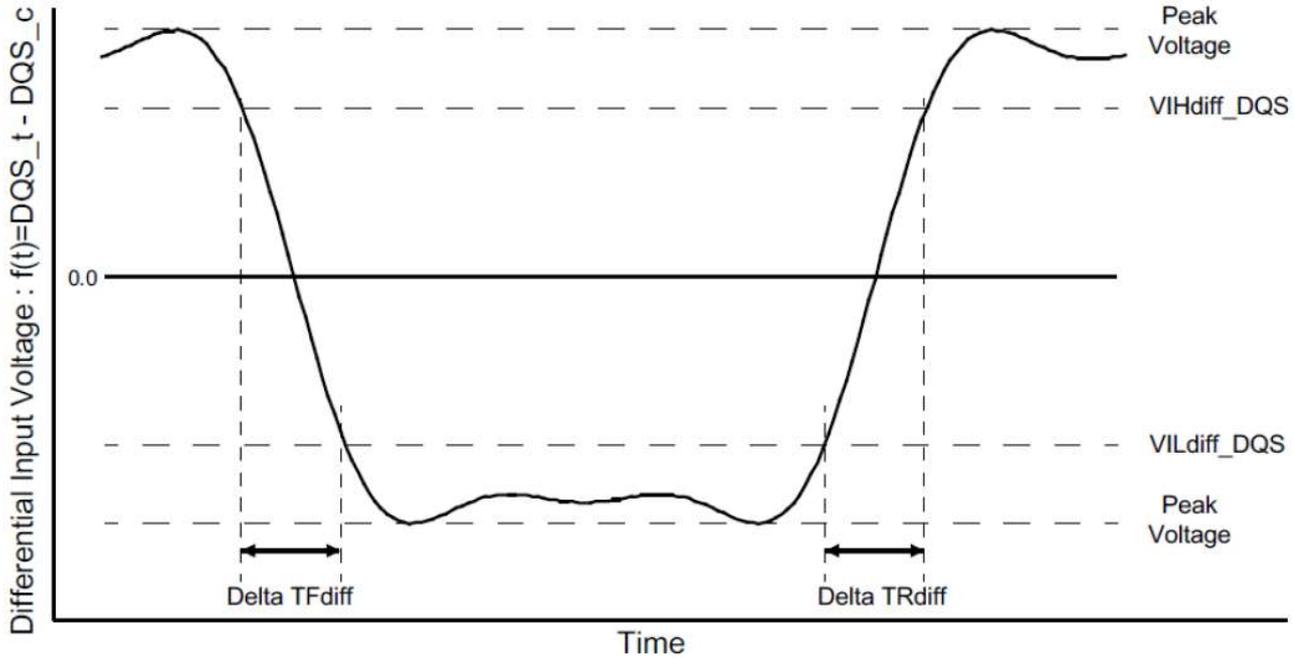


Figure 14 – Differential Input Slew Rate Definition for DQS<sub>t</sub>, DQS<sub>c</sub>

Note:

1. Differential signal rising edge from VILdiff\_DQS to VIHdiff\_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff\_DQS to VILdiff\_DQS must be monotonic slope.

Table 29 – Differential Input Slew Rate Definition for DQS<sub>t</sub>, DQS<sub>c</sub>

Description	From	To	Defined by
Differential Input Slew Rate for Rising Edge (DQS <sub>t</sub> - DQS <sub>c</sub> )	VILdiff_DQS	VIHdiff_DQS	$ VILdiff\_DQS - VIHdiff\_DQS  / \Delta TRdiff$
Differential Input Slew Rate for Falling Edge (DQS <sub>t</sub> - DQS <sub>c</sub> )	VIHdiff_DQS	VILdiff_DQS	$ VILdiff\_DQS - VIHdiff\_DQS  / \Delta TFdiff$

Table 30 – Differential Input Level for DQS<sub>t</sub>, DQS<sub>c</sub>

Parameter	Symbol	Date Rate		Unit
		3733 / 4266		
		Min	Max	
Differential Input High	VIHdiff_DQS	120	-	mV
Differential Input Low	VILdiff_DQS	-	-120	mV

Table 31 – Differential Input Slew Rate for DQS<sub>t</sub>, DQS<sub>c</sub>

Parameter	Symbol	Date Rate		Unit
		3733 / 4266		
		Min	Max	
Differential Input Slew Rate	SRIdiff	2	14	V/ns

### 5.2.10 Differential Input Cross Point Voltage for DQS

The cross-point voltage of differential input signals (DQS<sub>t</sub>, DQS<sub>c</sub>) must meet the requirements in Table 32. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is V<sub>REFDQ</sub>, as shown in Figure 15.

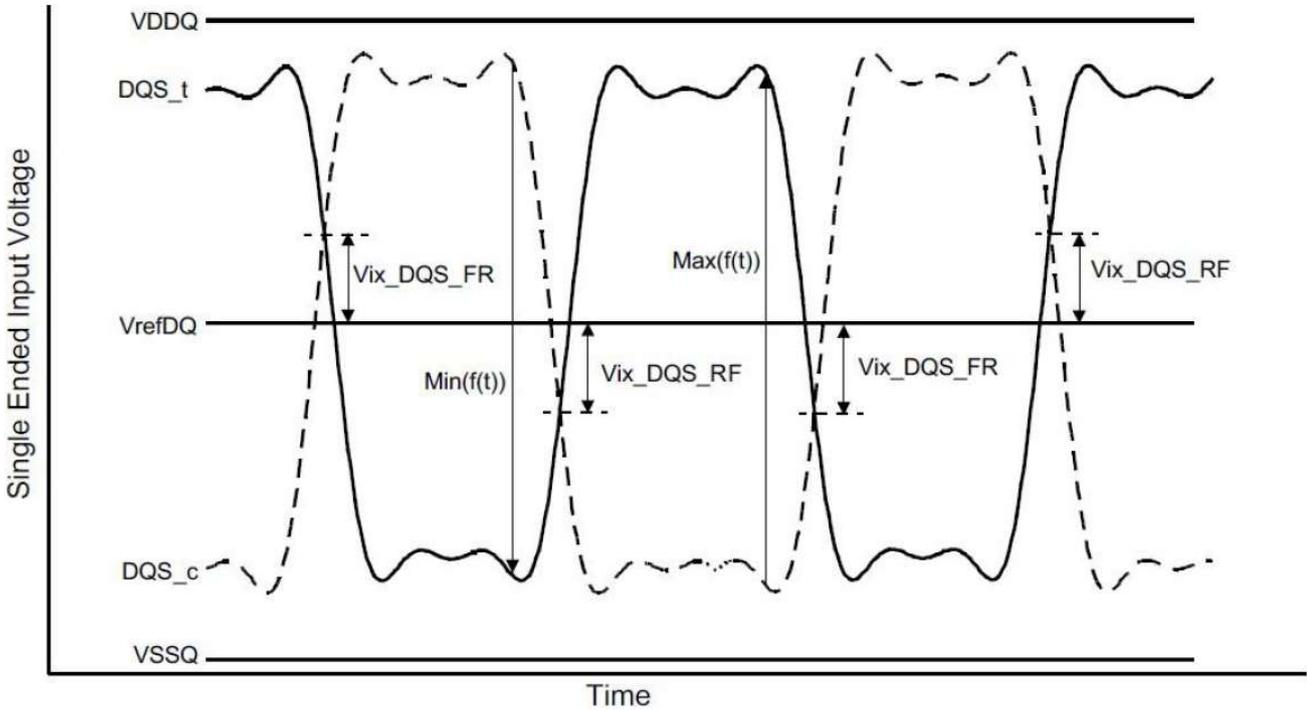


Figure 15 – VIX Definition

**Note:**

1. The base level of VIX\_DQS\_FR/RF is V<sub>REFDQ</sub> that is LPDDR4 SDRAM internal setting value by V<sub>REF</sub> training

Table 32 – Cross point voltage for Differential Input Signals (DQS)

Parameter	Symbol	Date Rate		Unit	Note
		3733 / 4266			
		Min	Max		
Clock Differential Input Cross Point Voltage Ratio	VIX_CK_ratio	-	20	%	1,2

**Note:**

1. VIX\_CK\_ratio is defined by this equation:  $VIX\_CK\_ratio = VIX\_CK\_FR / |\text{Min}(f(t))|$
2. VIX\_CK\_ratio is defined by this equation:  $VIX\_CK\_ratio = VIX\_CK\_RF / \text{Max}(f(t))$

### 5.3 Input Level for ODT(CA) Input

The levels are provided in Table 33.

Table 33 – LPDDR4 Input Level for ODT(CA)

Parameter	Symbol	Min	Max	Unit	Note
ODT Input High Level	VIHODT	$0.75 \times V_{DD2}$	$V_{DD2} + 0.2$	V	
ODT Input Low Level	VILODT	-0.2	$0.25 \times V_{DD2}$	V	

### 5.4 Single Ended Output Slew Rate

The slew rate is provided in Figure 16 and Table 34.

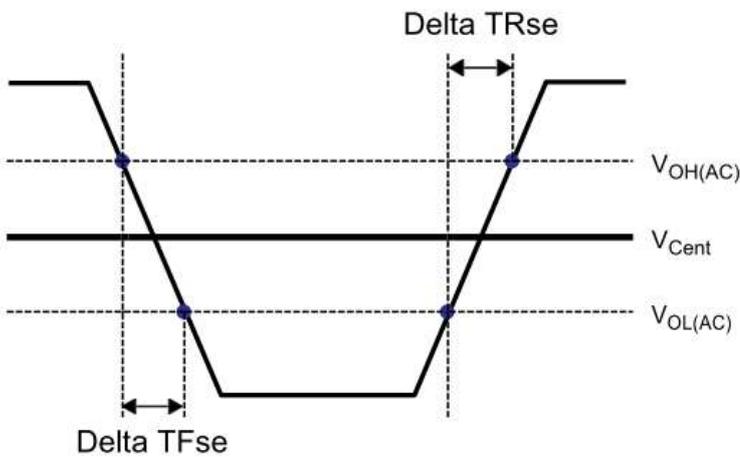


Figure 16 – Single Ended Output Slew Rate Definition

Table 34 – Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Unit
		Min	Max	
<b>LPDDR4 (1.1V V<sub>DDQ</sub>)</b>				
Single-ended Output Slew Rate ( $VOH = V_{DDQ} / 3$ )	SRQse	3.5	9.0	V/ns
Output Slew-Rate matching Ratio (Rise to Fall)		0.8	1.2	
<b>LPDDR4X (0.6V V<sub>DDQ</sub>)</b>				
Single-ended Output Slew Rate ( $VOH = V_{DDQ} \times 0.5$ )	SRQse	3.0	9.0	V/ns
Output Slew-Rate matching Ratio (Rise to Fall)		0.8	1.2	

**Note:**

- Description:  
SR: Slew Rate  
Q = Query Output (like in DQ, which stands for Data-in, Query-Output)  
se = Single-ended Signals
- Measured with output reference load.
- The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- The output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$  and  $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$ .
- Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

## 5.5 Differential Output Slew Rate

The slew rate is provided in Figure 17 and Table 35.

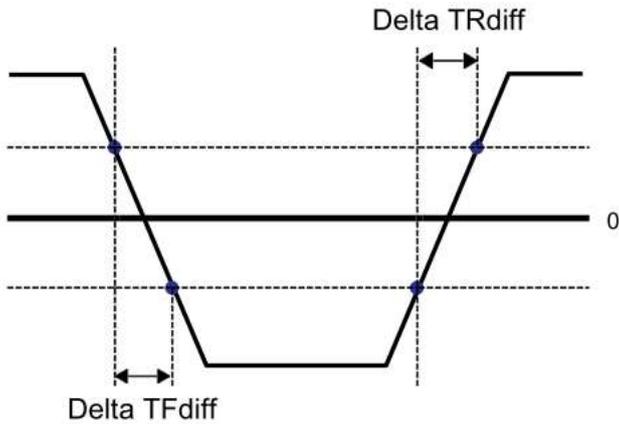


Figure 17 – Differential Output Slew Rate Definition

Table 35 – Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
<b>LPDDR4 (1.1V V<sub>DDQ</sub>)</b>				
Differential Output Slew Rate (VOH = V <sub>DDQ</sub> /3)	SRQdiff	7	18	V/ns
<b>LPDDR4X (0.6V V<sub>DDQ</sub>)</b>				
Differential Output Slew Rate (VOH = V <sub>DDQ</sub> x 0.5)	SRQdiff	6	18	V/ns

**Note:**

- Description:  
SR: Slew Rate  
Q = Query Output (like in DQ, which stands for Data-in, Query-Output)  
diff = Differential signal
- Measured with output reference load.
- The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.8×VOH(DC) and VOH(AC)=0.8×VOH(DC).
- Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

## 6. Input/Output Capacitance

The input/output capacitance is provided in Table 36

**Table 36 - Input/Output Capacitance**

Parameter	Symbol	3733 / 4266		Unit	Note
		Min	Max		
Input Capacitance, CK_t and CK_c	CCK	0.5	0.9	pF	1,2
Input Capacitance delta, CK_t and CK_c	CDCK	0	0.09	pF	1,2,3
Input Capacitance, all other input-only pins	CI	0.5	0.9	pF	1,2,4
Input Capacitance delta, all other input-only pins	CDI	-0.1	0.1	pF	1,2,5
Input/Output Capacitance, DQ, DMI, DQS_t and DQS_c	CIO	0.7	1.3	pF	1,2,6
Input/Output Capacitance delta, DQS_t and DQS_c	CDDQS	0	0.1	pF	1,2,7
Input/Output Capacitance delta, DQ and DMI	CDIO	-0.1	0.1	pF	1,2,8
Input/Output Capacitance, ZQ pin	CZQ	0	0.5	pF	1,2

**Note:**

1. This parameter applies to LPDDR4 die only (does not include package capacitance).
2. This parameter is not subject to production testing; It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, and VSS applied; All other pins are left floating.
3. Absolute value of CCK\_t – CCK\_c.
4. CI applies to CS, CKE, and CA[5:0].
5.  $CDI = CI - 0.5 \times (CCK_t + CCK_c)$ ; It does not apply to CKE.
6. DMI loading matches DQ and DQS.

Absolute value of CDQS\_t and CDQS\_c.

## 7 Electrical Characteristics and AC Timing

### 7.1 Clock Timing

Clock timing is presented in Table 37.

**Table 37 - Clock AC Timing**

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Absolute Clock Period	tCK(avg)	0.535	100	0.468	100	ns	
Average High Pulse Width	tCH(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low Pulse Width	tCL(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	-	tCK(avg)min + tJIT(per)min	-	ns	
Absolute High Clock Pulse Width	tCH(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low Clock Pulse Width	tCL(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period Jitter	tJIT(per)	-34	34	-30	30	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	68	-	60	ps	

### 7.2 Mode Register Timing Parameter

**Table 38 – Mode Register Timing Parameter**

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Mode Register Write (MRW) command period	tMRW	Max(10ns, 10tCK)		Max(10ns, 10tCK)		ns	
Mode Register Set command delay	tMRD	Max(14ns, 10tCK)		Max(14ns, 10tCK)		ns	
Mode Register Read (MRR) command period	tMRR	8		8		tCK(avg)	
Additional time after tXP has expired until the MRR command maybe issued	tMRR1	tRCD(Min) + 3tCK		tRCD(Min) + 3tCK		ns	
Delay from MRW command to DQS driven out	tSDO	Max(12tCK, 20ns)		Max(12tCK, 20ns)		ns	

### 7.3 Read Timing

Table 39 - Read Timing

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
DQS Output Access Time from CK_t/CK_c	tDQSK	1500	3500	1500	3500	ps	1
DQS Output Access Time from CK_t/CK_c – Voltage Variation	tDQSK_VOLT		7		7	ps/mV	2
DQS Output Access Time from CK_t/CK_c – Temperature Variation	tDQSK_TEMP		4		4	ps/°C	3
CK to DQS Rank to Rank Variation	tDQSK_Rank2Rank		1		1	ns	4,5
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI Disabled)	tDQSQ	-	0.18	-	0.18	UI	6
DQ Output Hold Time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min(tQSH, tQSL)	-	Min(tQSH, tQSL)	-	UI	6
DQ Output Window Time total per pin (DBI Disabled)	tQW_total	0.7	-	0.7	-	UI	6,11
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI Enabled)	tDQSQ_DBI	-	0.18	-	0.18	UI	6
DQ Output Hold Time total from DQS_t, DQS_c (DBI Enabled)	tQH_DBI	Min(tQSH_DBI, tQSL_DBI)	-	Min(tQSH_DBI, tQSL_DBI)	-	UI	6
DQ Output Window Time total per pin (DBI Enabled)	tQW_total_DBI	0.70	-	0.70	-	UI	6,11
DQS_t, DQS_c Differential Output Low time (DBI Disabled)	tQSL	tCK(abs) - 0.05	-	tCK(abs) - 0.05	-	tCK(avg)	9,11
DQS_t, DQS_c Differential Output High time (DBI Disabled)	tQSH	tCH(abs) - 0.05	-	tCH(abs) - 0.05	-	tCK(avg)	10,11
DQS_t, DQS_c Differential Output Low time (DBI Enabled)	tQSL_DBI	tCK(abs) - 0.045	-	tCK(abs) - 0.045	-	tCK(avg)	9,11
DQS_t, DQS_c Differential Output High time (DBI Enabled)	tQSH_DBI	tCH(abs) - 0.045	-	tCH(abs) - 0.045	-	tCK(avg)	10,11
Read Preamble	tRPRE	1.8		1.8		tCK(avg)	
Read Postamble (0.5 tCK)	tRPST	0.4		0.4		tCK(avg)	
Read Postamble (1.5 tCK)	tRPST	1.4		1.4		tCK(avg)	
DQS Low-Z from Clock	tLZ(DQS)	<b>[Min]</b> (RL x tCK) + tDQSK(Min) - (tRPRE(Max) x tCK) - 200ps				ps	
DQ Low-Z from Clock	tLZ(DQ)	<b>[Min]</b> (RL x tCK) + tDQSK(Min) - 200ps				ps	
DQS High-Z from Clock	tHZ(DQS)	<b>[Max]</b> (RL x tCK) + tDQSK(Max) + (BL/2 x tCK) + (tRPST(Max) x tCK) - 100ps				ps	
DQ High-Z from Clock	tHZ(DQ)	<b>[Max]</b> (RL x tCK) + tDQSK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps				ps	

**Note:**

1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
2. tDQSK\_volt max delay variation as a function of DC voltage variation for V<sub>DD0</sub> and V<sub>DD2</sub>. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the MAX[ABS(tDQSK(MIN)@V1 - tDQSK(MAX)@V2), ABS(tDQSK(MAX)@V1 - tDQSK(MIN)@V2)]/ABS(V1 - V2).
3. tDQSK\_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to tDQSK\_Rank-2-Rank.
5. tDQSK\_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from one falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the minimum value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) - 0.04.

## 7.4 Write Timing

Table 40 - Write Timing

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Rx Timing Window total at VdIVW voltage levels	TdIVW_total	-	0.25	-	0.25	UI	1,2,3
DQ and DMI Input Pulse Width (at V <sub>CENT_DQ</sub> )	TdIPW	0.45	-	0.45	-	UI	7
DQ-to-DQS Offset	tDQS2DQ	200	800	200	800	ps	6
DQ-to-DQ Offset	tDQDQ		30		30	ps	7
DQ-to-DQS Offset – Temperature Variation	tDQS2DQ_temp		0.6		0.6	ps/°C	8
DQ-to-DQS Offset – Voltage Variation	tDQS2DQ_volt		33		33	ps/50mV	9
DQ-to-DQS Offset – Rank-to-Rank Variation	tDQS2DQ_Rank2Rank		200		200	ps	10,11
Write Command to first DQ Transition	tDQSS	0.75	1.25	0.75	1.25	tCK(avg)	
DQS Input High Level Width	tDQSH	0.4		0.4		tCK(avg)	
DQS Input Low Level Width	tDQSL	0.4		0.4		tCK(avg)	
DQS Falling edge to CK Setup time	tDSS	0.2		0.2		tCK(avg)	
DQS Falling edge from CK Hold time	tDSH	0.2		0.2		tCK(avg)	
Write Postamble (0.5 tCK)	tWPST	0.4		0.4		tCK(avg)	
Write Postamble (1.5 tCK)	tWPST	1.4		1.4		tCK(avg)	
Write Preamble	tWPRE	1.8		1.8		tCK(avg)	

**Note:**

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the VdIVW voltage levels.
3. Defined over the DQ internal V<sub>REF</sub> range. The Rx mask at the pin must be within the internal V<sub>REF(DQ)</sub> range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the V<sub>CENT\_DQ</sub>(pin\_mid).
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. tDQS2DQ(MAX) delay variation as a function of temperature.
9. tDQS2DQ(MAX) delay variation as a function of the DC voltage variation for V<sub>DDQ</sub> and V<sub>DD2</sub>. It includes the V<sub>DDQ</sub> and V<sub>DD2</sub> AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
10. The same voltage and temperature are applied to tDQS2DQ\_rank2rank.
11. tDQS2DQ\_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
12. UI = tCK(avg)(Min)/2

## 7.5 CKE Input Timing

Table 41 - CKE Input Timing

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
CKE Minimum Pulse Width (High and Low Pulse Width)	tCKE	Max(7.5ns, 4tCK)		Max(7.5ns, 4tCK)		ns	1
Delay from Valid command to CKE Input Low	tCMDCKE	Max(1.75ns, 3tCK)		Max(1.75ns, 3tCK)		ns	1
Valid Clock Requirement after CKE Input Low	tCKELCK	Max(5ns, 5tCK)		Max(5ns, 5tCK)		ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	1.75		1.75		ns	
Valid CS Requirement after CKE Input Low	tCKELCS	Max(5ns, 5tCK)		Max(5ns, 5tCK)		ns	1
Valid Clock Requirement before CKE Input High	tCKCKEH	Max(1.75ns, 3tCK)		Max(1.75ns, 3tCK)		ns	1
Exit Power-down to next Valid Command delay	tXP	Max(7.5ns, 5tCK)		Max(7.5ns, 5tCK)		ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	1.75		1.75		ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Max(7.5ns, 5tCK)		Max(7.5ns, 5tCK)		ns	1
Valid Clock and CS Requirement after CKE Input Low after MRW Command	tMRWCKEL	Max(14ns, 10tCK)		Max(14ns, 10tCK)		ns	1
Valid Clock and CS Requirement after CKE Input Low after ZQCAL Start Command	tZQCKE	Max(1.75ns, 3tCK)		Max(1.75ns, 3tCK)		ns	1

**Note:**

- Delay time has to satisfy both analog time(ns) and clock count (nCK). For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3nCK is applied to is shown below.

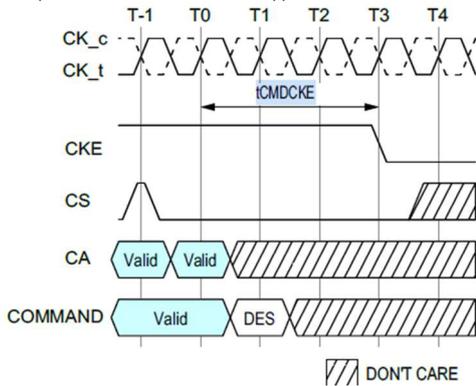


Figure 18 - tCMDCKE Timing

## 7.6 Temperature Derating for AC timing

Temperature derating is shown in Table 42.

Table 42 - Temperature Derating AC Timing

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
DQS Output Access time from CK_t/CK_c (derated)	tDQSCKd	3600	-	3600	-	ps	
RAS-to-CAS delay (derated)	tRCDD	-	tRCD + 1.875	-	tRCD + 1.875	ns	
Activate-to-Activate Command period (derated)	tRCd	-	tRC + 3.75	-	tRC + 3.75	ns	
Row Active Time (derated)	tRASd	-	tRAS + 1.875	-	tRAS + 1.875	ns	
Row Precharge time (derated)	tRPd	-	tRP + 1.875	-	tRP + 1.875	ns	
Active bank A to Active bank B (derated)	tRRDd	-	tRRD + 1.875	-	tRRD + 1.875	ns	

**Note:**

- Timing derating applies for operating at 85°C to 95°C.

## 7.7 Core Timing Parameter

Refresh Rate is determined by the value in MR4 OP[2:0].

Table 43 - Core Timing Parameter

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Activate-to-Activate command period (same bank)	tRC	with all-bank precharge: tRAS + tRPab with per-bank precharge: tRAS + tRPpb				ns	
Minimum Self Refresh time (Entry to Exit)	tSR	Max(15ns, 3tCK)		Max(15ns, 3tCK)		ns	
Self Refresh Exit to next valid command delay	tXSR	[Min] Max(tRFCab + 7.5ns, 2tCK)				ns	
CAS-to-CAS delay	tCCD	8		8		tCK(avg)	
CAS-to-CAS delay masked write	tCCDMW	32		32		tCK(avg)	
Internal READ-to-PRE-CHARGE command delay	tRTP	Max(7.5ns, 8tCK)		Max(7.5ns, 8tCK)		ns	
RAS-to-CAS delay	tRCD	Max(18ns, 4tCK)		Max(18ns, 4tCK)		ns	
Row Precharge Time (single bank)	tRPpb	Max(18ns, 3tCK)		Max(18ns, 3tCK)		ns	
Row Precharge Time (all banks)	tRPab	Max(21ns, 3tCK)		Max(21ns, 3tCK)		ns	
Row Active Time	tRAS	[Min] Max(42ns, 3tCK)				ns	
		[Max] Min(9 x tREFI x Refresh Rate, 70.2)				Us	
Write Recovery Time	tWR	Max(18ns, 4tCK)		Max(18ns, 4tCK)		ns	
Write-to-Read delay	tWTR	Max(10ns, 8tCK)		Max(10ns, 8tCK)		ns	
Active Bank A to Active Bank B	tRRD	Max(10ns, 4tCK)		Max(7.5ns, 4tCK)		ns	1
Precharge-to-Precharge delay	tPPD	4		4		tCK(avg)	2
Four-bank Activate Window	tFAW	40		30		ns	1
Delay from SRE command to CKE Input Low	tESCKE	Max(1.75ns, 3tCK)		Max(1.75ns, 3tCK)			3

**Note:**

- 4267 Mb/s timing value is supported at lower data rates if the device is supporting 4266Mb/s speed grade.
- Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
- Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

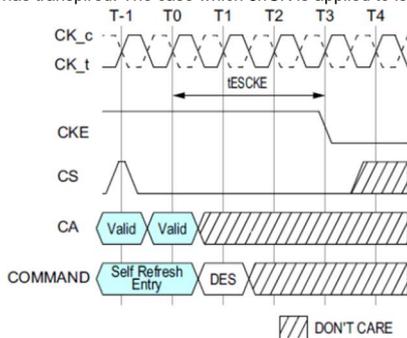


Figure 19 - tESCKE Timing

## 7.8 CA Bus Training Parameter

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Valid Clock Requirement after CKE Input Low	tCKELCK	Max(5ns, 5tCK)		Max(5ns, 5tCK)		tCK	
Data Setup for V <sub>REF</sub> Training mode	tDStrain	2		2		ns	
Data Hold for V <sub>REF</sub> Training mode	tDHtrain	2		2		ns	
Asynchronous Data Read	tADR	20		20		ns	
CA Bus Training Command-to-Command delay	tCACD	RU(tADR / tCK)		RU(tADR / tCK)		tCK	1
Valid Strobe Requirement before CKE Low	tDQSCKE	10		10		ns	
First CA Bus Training Command follow CKE Low	tCAENT	250		250		ns	
V <sub>REF</sub> Step Time – Multiple steps	tV <sub>REFCA_LONG</sub>	250		250		ns	
V <sub>REF</sub> Step Time – One step	tV <sub>REFCA_SHORT</sub>	80		80		ns	
Valid Clock Requirement before CS High	tCKPRECS	2tCK + tXP		2tCK + tXP			
Valid Clock Requirement after CS High	tCKPSTCS	Max(7.5ns, 5tCK)		Max(7.5ns, 5tCK)			
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	2		2		tCK	
Minimum delay from CKE High to Strobe High-Z	tCKEHDQS	10		10		ns	
CA Bus Training CKE High to DQ tri-state	tMRZ	1.5		1.5		ns	
ODT turn-on latency from CKE	tCKELODTon	20		20		ns	
ODT turn-off latency from CKE	tCKEHODToff	20		20		ns	
Exit command bus training mode to next valid command delay	tXCBT_Short	Max(200ns, 5tCK)		Max(200ns, 5tCK)			2
	tXCBT_Middle	Max(200ns, 5tCK)		Max(200ns, 5tCK)			2
	tXCBT_Long	Max(250ns, 5tCK)		Max(250ns, 5tCK)			2

**Note:**

1. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
2. Exit command bus training mode to next valid command delay time depends on value of V<sub>REF(CA)</sub> setting: MR12 OP[5:0] and VREF(CA) range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally exit command bus training mode to next valid command delay time may affect V<sub>REF(DQ)</sub> setting. Settling time of V<sub>REF(DQ)</sub> level is same as V<sub>REF(CA)</sub> level.

## 7.9 CA Rx Voltage and Timing

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 20. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in Figure 21 is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

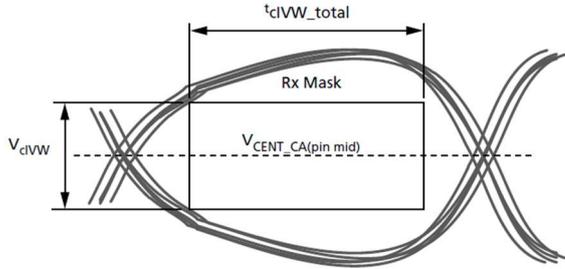


Figure 20 - CA Receiver (Rx) Mask

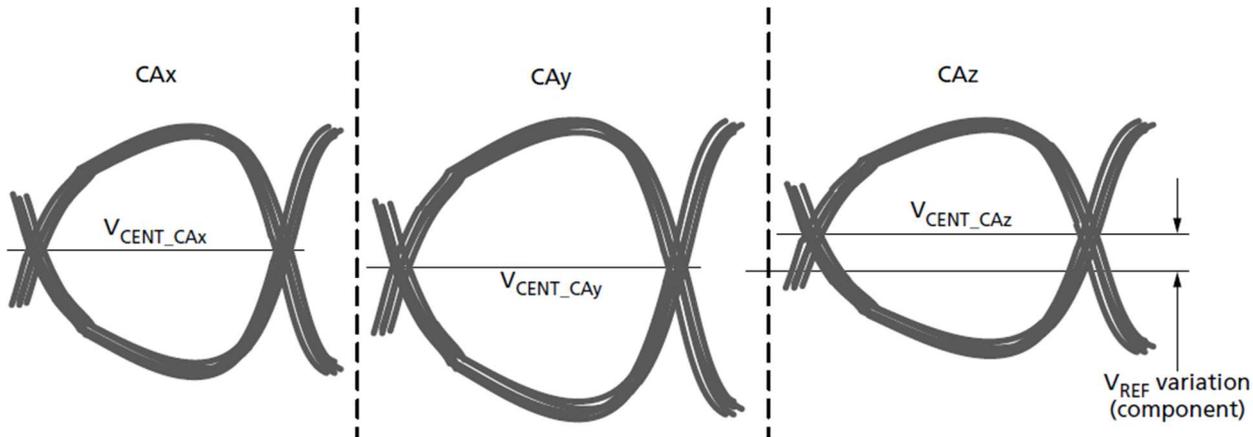
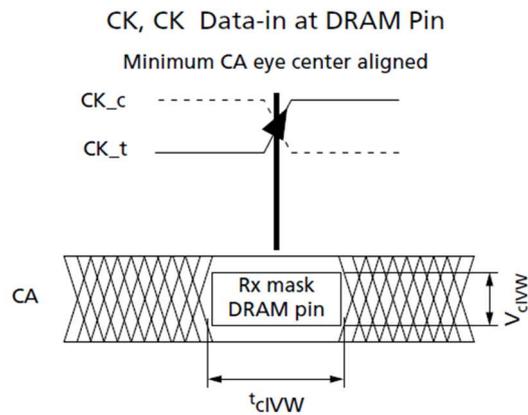


Figure 21 - Across Pin  $V_{REFC_A}$  Voltage Variation

$V_{cent\_CA}(\text{pin mid})$  is defined as the midpoint between the largest  $V_{cent\_CA}$  voltage level and the smallest  $V_{cent\_CA}$  voltage level across all CA and CS pins for a given DRAM component. Each CA  $V_{CENT}$  level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level  $V_{REF}$  will be set by the system to account for RON and ODT settings.



$T_{cIVW}$  for all CA signals is defined as centered on the  $CK_t/CK_c$  crossing at the DRAM pin.

Figure 22 - CA Timing at the DRAM Pins

**Note:**

1. All of the timing terms in above figure are measured from the  $CK_t/CK_c$  to the center (midpoint) of the  $T_{cIVW}$  window taken at the  $V_{cIVW\_total}$  voltage levels centered around  $V_{CENT\_CA}(\text{pin mid})$ .

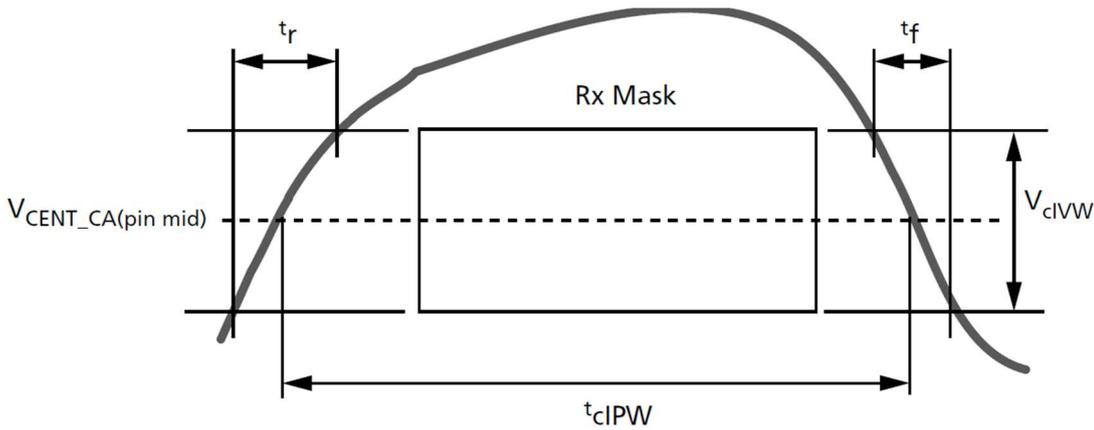


Figure 23 - CA tCIPW and SRIN\_cIVW Definition (for Each Input pulse)

Note:

1.  $SRIN\_cIVW = VdIVW\_total / (tr \text{ or } tf)$ ; signal must be monotonic within  $tr$  and  $tf$  range.

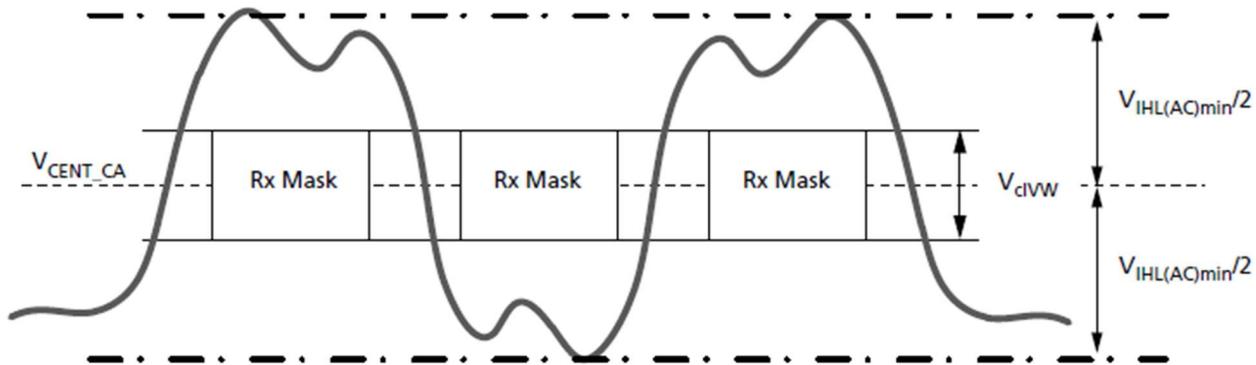


Figure 24 - CA VIH\_AC Definition (for Each Input Pulse)

Table 44 - DRAM CMD/ADDR, CS

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Rx Mask Voltage p-p	VcIVW	-	155	-	145	mV	1,2,3,4
Rx Timing Window	TcIVW	-	0.3	-	0.3	UI	1,2,3,4,9
CAAC Input Pulse Amplitude pk-pk	VIHL_AC	190	-	180	-	mV	1,5,8
CA Input Pulse Width	TcIPW	0.6		0.6		UI	2,6,9
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	V/ns	1,7

Note:

1. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example: the TcIVW(ps) = 450ps at or below 1333 operating frequencies.
2. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
3. Rx mask voltage VcIVW total(max) must be centered around Vcent\_CA(pin mid).
4. Vcent\_CA must be within the adjustment range of the CA internal Vref.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIH AC at any point over the total UI. No timing requirement above level. VIH AC is the peak to peak voltage centered around Vcent\_CA(pin mid) such that VIH\_AC/2 min must be met both above and below Vcent\_CA.
6. CA only minimum input pulse width defined at the Vcent\_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent\_CA(pin mid).
8. VIH\_AC does not have to be met when no transitions are occurring.
9.  $UI = CK(avg)min$

## 7.10 DRAM Data Timing

### 7.10.1 DQ Tx Voltage and Timing

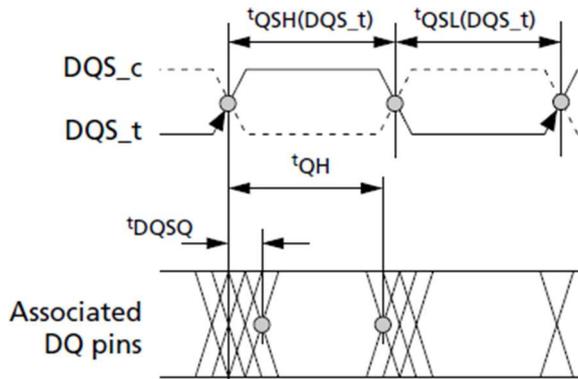


Figure 25 - Read Data Timing Definitions  $t_{QH}$  and  $t_{DQSQ}$  across all DQ Signals per DQS Group

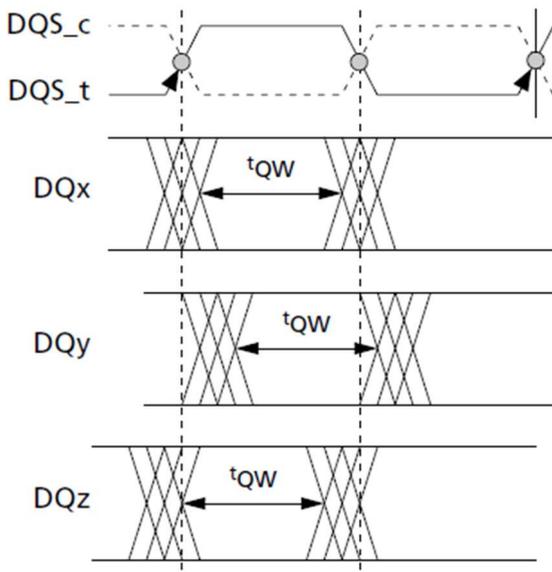


Figure 26 - Read Data Timing  $t_{QW}$  Valid Window Defined per DQ Signal

### 7.10.2 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown Figure 27 is applied per pin. The "total" mask ( $V_{dIVW\_total}$ ,  $T_{dIVW\_total}$ ) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

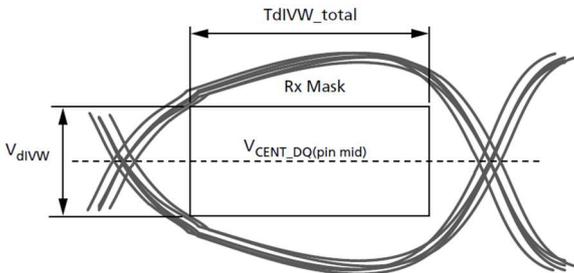


Figure 27 - DQ Receiver (Rx) Mask

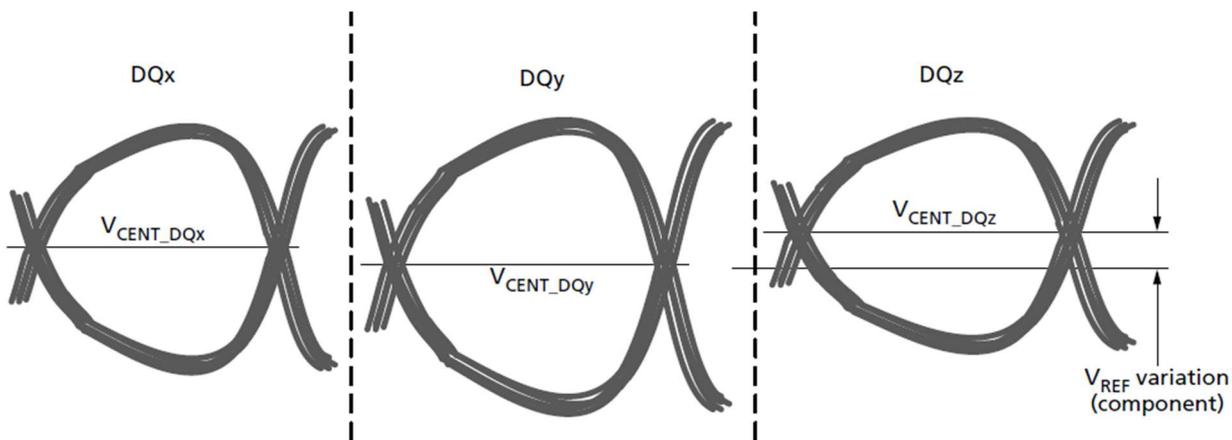


Figure 28 - Across Pin  $V_{REF}$  DQ Voltage Variation

$V_{cent\_DQ(pin\_mid)}$  is defined as the midpoint between the largest  $V_{cent\_DQ}$  voltage level and the smallest  $V_{cent\_DQ}$  voltage level across all DQ pins for a given DRAM component. Each DQ  $V_{cent}$  is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 29. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level  $V_{REF}$  will be set by the system to account for  $R_{on}$  and ODT settings.

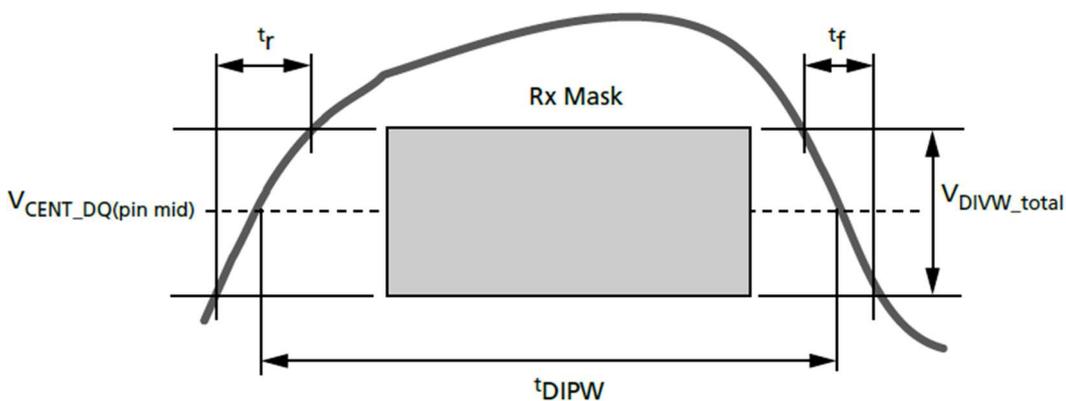


Figure 29 - DQ  $t_{DIPW}$  and  $SRIN_{dIPW}$  Definition for Each Input Pulse

Note:

1.  $SRIN_{dIVW} = V_{dIVW\_total}/(t_r \text{ or } t_f)$  signal must be monotonic within  $t_r$  and  $t_f$  range.

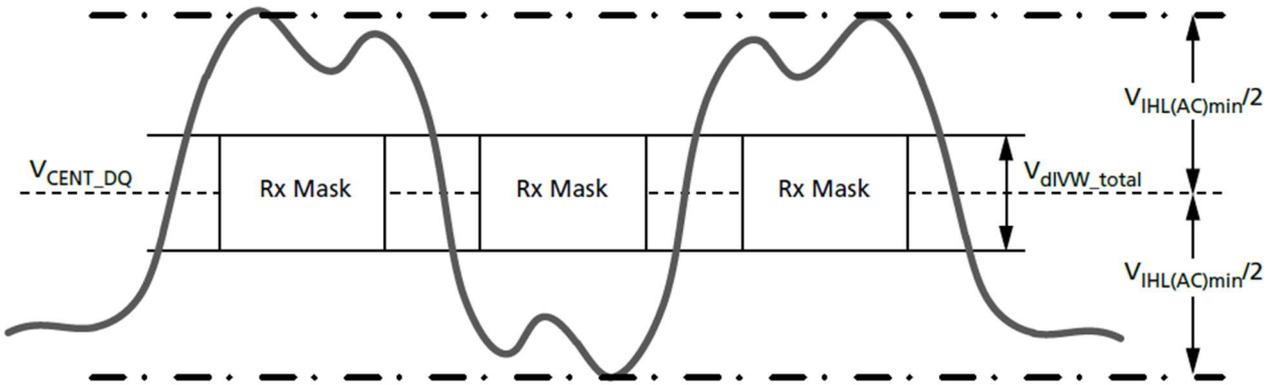


Figure 30 - DQ VIH(AC) Definition (for Each Input Pulse)

Table 45 - DQ in Receive Mode

Parameter	Symbol	3733		4266		Unit	Note
		Min	Max	Min	Max		
Rx Mask Voltage p-p	VdIVW_total	-	140	-	120	mV	1,2,3
CAAC Input Pulse Amplitude pk-pk	VIHL_AC	180	-	170	-	mV	5,7
Input Slew Rate over VdIVW_total	SRIN_dIVW	1	7	1	7	V/ns	6

**Note:**

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx mask voltage VdIVW\_total(MAX) must be centered around VCENT\_DQ(pin\_mid).
3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the internal VREFDQ range irrespective of the input signal common mode.
4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.
5. DQ-only input pulse amplitude into the receiver must meet or exceed VIH(AC) at any point over the total UI. No timing requirement above level. VIH(AC) is the peak-to-peak voltage centered around VCENT\_DQ(pin\_mid), such that VIH(AC)/2 (MIN) must be met both above and below VCENT\_DQ.
6. Input slew rate over VdIVW mask centered at VCENT\_DQ(pin\_mid).