IM8G08D3FFD
8Gbit DDR3 SDRAM
8 Bank x 64Mbit x 8 x 2 Rank

	125	**107**
	DDR3-1600	DDR3-1866
Clock Cycle Time (t_{CK5}, CWL=5)	3.0 ns	-
Clock Cycle Time (t_{CK6}, CWL=5)	2.5 ns	2.5 ns
Clock Cycle Time (t_{CK7}, CWL=6)	1.875 ns	1.875 ns
Clock Cycle Time (t_{CK8}, CWL=6)	1.875 ns	1.875 ns
Clock Cycle Time (t_{CK9}, CWL=7)	1.5 ns	1.5 ns
Clock Cycle Time (t_{CK10}, CWL=7)	1.5 ns	1.5 ns
Clock Cycle Time (t_{CK11}, CWL=8)	1.25 ns	1.25 ns
Clock Cycle Time (t_{CK12}, CWL=8)	-	1.25 ns
Clock Cycle Time (t_{CK13}, CWL=9)	-	1.07 ns
System Frequency ($f_{CK(MAX)}$)	800 MHz	933 MHz

Specification

- Density: 8Gbits
- Organization: 8 Bank x 64Mbit x 8 x 2 Rank
- Data rate: 1866Mbps, 1600Mbps
- $\overline{\text{CAS}}$ Latency (CL): 5, 6, 7, 8, 9, 10, 11, 12, 13
- $\overline{\text{CAS}}$ Write Latency (CWL): 5, 6, 7, 8, 9
- Additive Latency (AL): 0, CL-1, CL-2
- Power supply: VDD, VDDQ = 1.35V (1.283V to 1.45V)
  - Backward compatible: VDD, VDDQ = 1.5V ± 0.075V
- Package: 78-ball FBGA
  - Lead-free and Halogen-free
- 1KB Page size
  - Row address: A0 to A15
  - Column address: A0 to A9
- 8 internal banks for concurrent operation
- Burst Length: 4, 8
- Burst Type: Sequential, Interleave
- Driver Strength: RZQ/7, RZQ/6, (RZQ = 240Ω)
- Precharge: Auto precharge option for each burst access
- Refresh: Auto-refresh, Self-refresh
- Refresh Cycle:
  - 7.8µs at -40℃ ≤ T_{CASE} ≤ +85℃
  - 3.9µs at +85℃ ≤ T_{CASE} ≤ +95℃
- Operating Temperature Range
  - Commercial: 0℃ ≤ T_{CASE} ≤ +95℃
  - Industrial: -40℃ ≤ T_{CASE} ≤ +95℃

Option	***Marking***
• Configuration	
- 512Mbit x 8 x 2 Rank	8G08
• Package	
- 78-Ball FBGA (2CS)	D
• RoHS Compliance	
- RoHS Compliance	G
- Leaded	[Blank]
• Speed	
- DDR3-1866 CL13 (1.07ns)	107
- DDR3-1600 CL11 (1.25ns)	125
• Temperature (T_{CASE})	
- Commercial Temperature (0℃ to 95℃)	[Blank]
- Industrial Temperature (-40℃ to 95℃)	I
• Automotive Grade	
- Non-Automotive Grade	[Blank]

Example Part Number: IM8G08D3FFDG-107I

Features

- Double-Data-Rate architecture (Two data transfers per clock cycle)
- The high-speed data transfer is realized by the 8 bits prefetch pipe-lined architecture
- Bi-directional Differential Data Strobe (DQS and $\overline{\text{DQS}}$) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential Clock Inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; Data and Data Mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Posted $\overline{\text{CAS}}$ by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi-Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{\text{RESET}}$ pin for Power-up sequence and reset function
- SRT Range: Normal / Extended
- Programmable Output Driver Impedance Control

Part Number Information

IM 8G 08 D3 F F D G - 107 (I) ()

Intelligent Memory

DRAM Density
8G = 8Gbit

DRAM I/O width
08 = x8

Memory Type
D3 = DDR3 SDRAM

Voltage
F = 1.35V (DDR3L, 1.5V tolerant)

DRAM Revision
F = Revision F

Automotive Grade
Blank = Non-Automotive Grade

Temperature
Blank = Commercial Temp 0℃ to +95℃ T_{CASE}
I = Industrial Temp -40℃ to +95℃ T_{CASE}
Note: *The refresh rate must be doubled when the T_{CASE} operating temperature exceeds +85℃*

Speed
107 = DDR3-1866 CL13
125 = DDR3-1600 CL11

RoHS Compliance
G = RoHS Compliance
Blank = Leaded

Package
D = FBGA (2 Chip-Select)

8Gbit DDR3 SDRAM Addressing

Configuration	512Mb x 8 x 2 Rank
No. of Bank	8
Bank Address	BA0 ~ BA2
Row Address	A0 ~ A15
Column Address	A0 ~ A9
Auto precharge	A10/AP
BC switch on the fly	A12/$\overline{BC}$
Page size	1KB

Pin Configuration

78-Ball FBGA (x8 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{SS}	V_{DD}	NC				NC	V_{SS}	V_{DD}	A
B	V_{SS}	V_{SSQ}	DQ0				DM	V_{SSQ}	V_{DDQ}	B
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}	C
D	V_{SSQ}	DQ6	$\overline{DQS}$				V_{DD}	V_{SS}	V_{SSQ}	D
E	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}	E
F	ODT1	V_{SS}	$\overline{RAS}$				CK	V_{SS}	CKE1	F
G	ODT0	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE0	G
H	$\overline{CS1}$	$\overline{CS0}$	$\overline{WE}$				A10/AP	ZQ0	ZQ1	H
J	V_{SS}	BA0	BA2				A15	V_{REFCA}	V_{SS}	J
K	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	K
L	V_{SS}	A5	A2				A1	A4	V_{SS}	L
M	V_{DD}	A7	A9				A11	A6	V_{DD}	M
N	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	N

Ball Location (x8)

- ● Populated ball
- ✚ Ball not populated

Top view
(See the balls through the package)

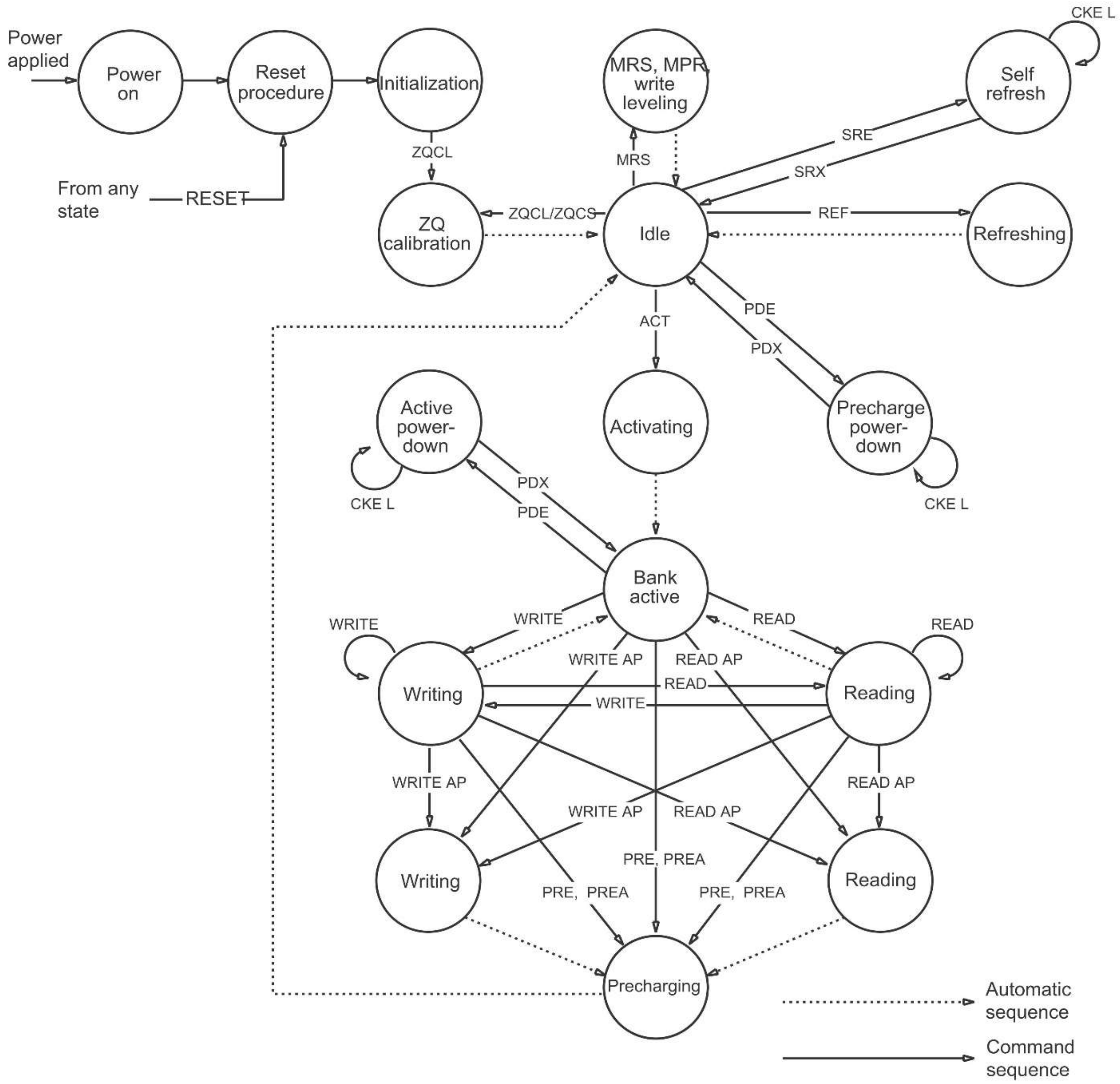
	1	2	3	4	5	6	7	8	9
A	●	●	●	✚	✚	✚	●	●	●
B	●	●	●	✚	✚	✚	●	●	●
C	●	●	●	✚	✚	✚	●	●	●
D	●	●	●	✚	✚	✚	●	●	●
E	●	●	●	✚	✚	✚	●	●	●
F	●	●	●	✚	✚	✚	●	●	●
G	●	●	●	✚	✚	✚	●	●	●
H	●	●	●	✚	✚	✚	●	●	●
J	●	●	●	✚	✚	✚	●	●	●
K	●	●	●	✚	✚	✚	●	●	●
L	●	●	●	✚	✚	✚	●	●	●
M	●	●	●	✚	✚	✚	●	●	●
N	●	●	●	✚	✚	✚	●	●	●

Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self-refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power- down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT0, ODT1	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM. The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable RTT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Autoprecharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop:** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/ Output	**Data Input / Output:** Bi-directional data bus
DQS, $\overline{DQS}$	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals $\overline{DQS}$ respectively, to provide differential pair signaling to the system during read and write. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.35V, 1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation.
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference Voltage for DQ
V_{REFCA}	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT and $\overline{RESET}$) do not supply termination.

Simplified State Diagram



ACT = Activate
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = Precharge

PREA = Precharge All
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = Refresh
RESET = Start Reset Procedure
SRE = Self Refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ Long Calibration
ZQCS = ZQ Short Calibration

Basic Functionality

Read and write operations to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode “on the fly” (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

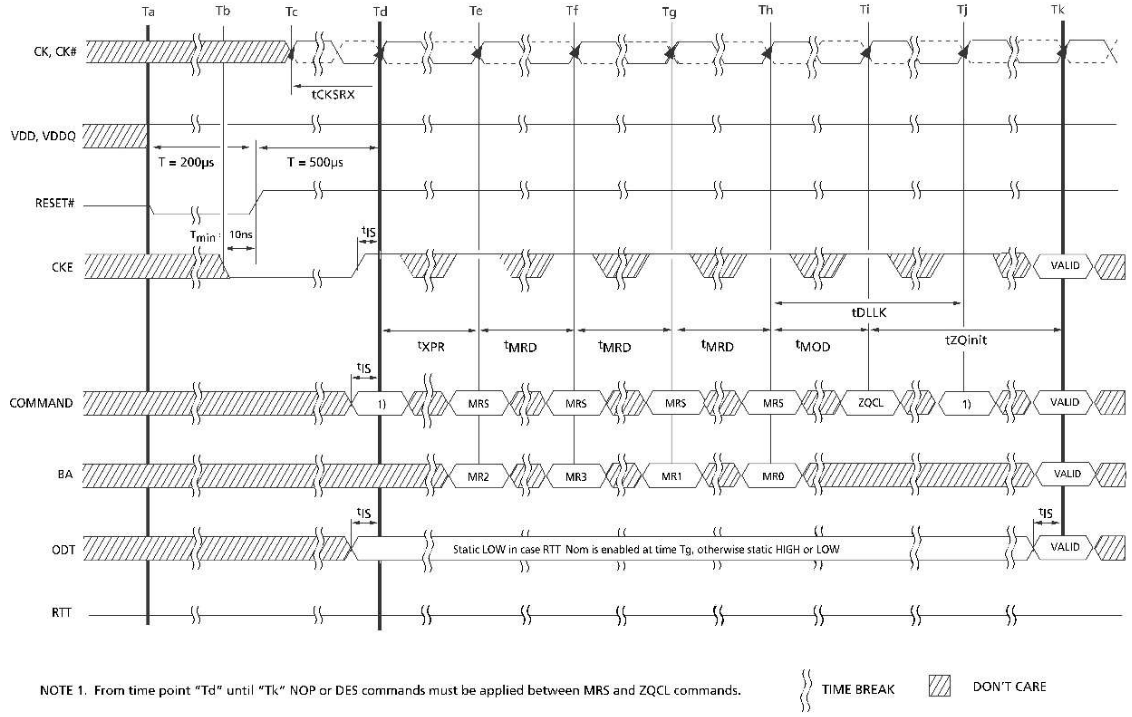
RESET and Initialization Procedure

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below 0.2 x V_{DD} (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200μs with stable power. CKE is pulled “Low” anytime before $\overline{\text{RESET}}$ being de-asserted (min time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no longer than 200ms; and during the ramp, $V_{DD} > V_{DDQ}$ and $V_{DD} - V_{DDQ} < 0.3$ volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output,
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95V max once power ramp is finished,
   - V_{REF} tracks $V_{DDQ}/2$.

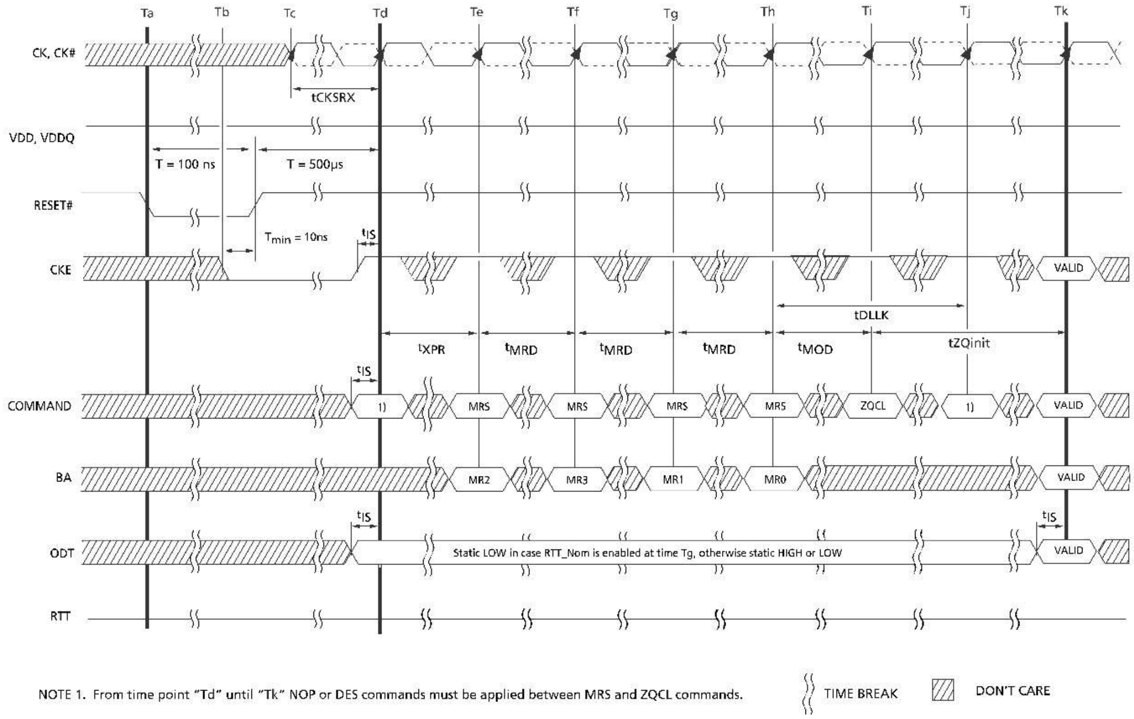
   OR
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK,$\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5t_{CK} (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequences finished, including expiration of t_{DLLK} and t_{ZQinit}.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{DLLK} and t_{ZQinit}.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, t_{XPR}, before issuing the first MRS command to load mode register. (t_{XPR}=Max(t_{XS}, 5t_{CK})].
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue ”DLL Enable” command, provide “Low” to A0, ”High” to BA0 and “Low” to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both t_{DLLK} and t_{ZQ} init completed.
12. The DDR3 SDRAM is now ready for normal operation.



Reset and Initialization with Stable Power

The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization.

1. Assert $\overline{\text{RESET}}$ below 0.2 x V_{DD} anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 100ns. CKE is pulled low before $\overline{\text{RESET}}$ being de-asserted (minimum time 10ns).
2. Follow Power-Up initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, $\overline{CAS}$ latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.

	BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address Field	BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register0	0[*1]	0	0	0[*1]	PPD	WR			DLL	TM	CAS_n Latency			RBT	CL	BL	

A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Wirte recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5[*2]
0	1	0	6[*2]
0	1	1	7[*2]
1	0	0	8[*2]
1	0	1	10[*2]
1	1	0	12[*2]
1	1	1	Reserved

CAS_n Latency

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

1. BA2 is reserved for future use and must be programmed to 0 during MRS.
2. WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR}(in ns) by t_{CK}(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/t_{CK}[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin The programmed WR value is used with t_{RP} to determine t_{DAL}.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff.
The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.

Address Field	BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 1	0*1	0	1	0*1	Qoff	TDQS	0*1	Rtt_Nom	0*1	Level	Rtt_Nom	D.I.C	AL	AL	Rtt_Nom	D.I.C	DLL

A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQS, DQS_n

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A9	A6	A2	Rtt_Nom*3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note : RZQ = 240 ohms

*3: In Wirte leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

*4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

A0	DLL Enable
0	Enable
1	Disable

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note : RZQ = 240 ohms

1. BA2, A8, A10, A13-A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	1	0	0*1			Rtt_WR		0*1	SRT	ASR	CWL			PASR*2			Mode Register 2

A7	Self-refresh temperature range (SRT)
0	Normal operating temperature range
1	Extend temperature self-refresh (Optional)

A6	Auto Self-refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0]= 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

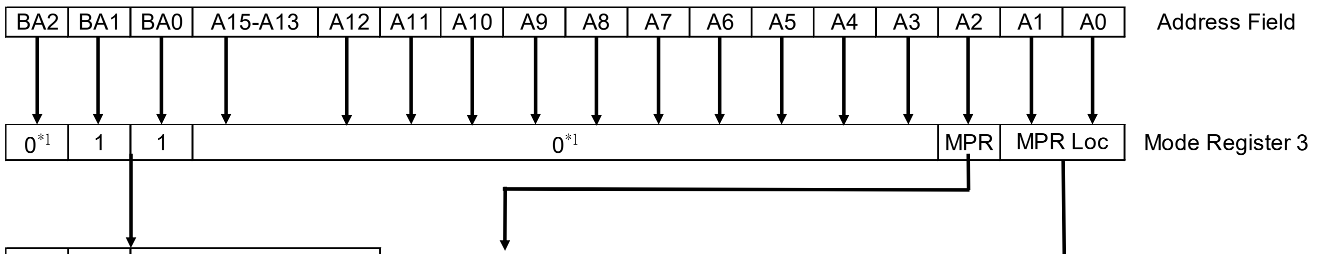
A5	A4	A3	CAS_n write Latency (CWL)
0	0	0	5 (tCK(avg) ≥2.5ns)
0	0	1	6(2.5ns >tCK(avg) ≥1.875ns)
0	1	0	7(1.875ns >tCK(avg) ≥1.5ns)
0	1	1	8(1.5ns >tCK(avg) ≥1.25ns)
1	0	0	9(1.25ns >tCK(avg) ≥1.07ns)
1	0	1	10(1.07ns >tCK(avg) ≥0.938ns)
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

1. BA2, A8, A11-A15 are RFU and must be programmed to 0 during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Mode Register MR3

The Mode Register MR3 controls Multi-Purpose Registers (MPR). The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	PFU
1	0	PFU
1	1	PFU

1. BA2, A3-A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation, MP3 A[2] = 0, MR3 A[1:0] will be ignored.

Burst Length

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read on write command Via A12 ($\overline{BC}$). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of burst length being selected on the fly via A12($\overline{BC}$), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.

Burst Type

[Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (Burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and strobes are in high impedance.
V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X: Don't Care.

Notes:
1. Page length is a function of I/O organization and column addressing
2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

Command Truth Table

a) Note 1,2,3,4 apply to the entire Command truth table
b) Note 5 applies to all Read/Write commands.
[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{\text{BC}}$=Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE Previous Cycle	CKE Current Cycle	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0 - BA2	A13 - A15	A12 / $\overline{\text{BC}}$	A10 / AP	A0 - A9,A11	Notes
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Command Truth Table (cont'd)

Notes:

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependent.
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self-refresh exit is asynchronous.
9. V_{REF} (both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

CKE Truth Table

a. Note 1~7 apply to the entire Command truth table
b. CKE low is allowed only if t_{MRD} and t_{MOD} are satisfied

Current State[2]	CKE Previous Cycle[1] (N-1)	CKE Current Cycle[1] (N)	Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Notes
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self-refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self-refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self-refresh Entry	9, 13, 18
For more details with all signals See “Command Truth Table,” on previous page					10

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on t_{CKEmin} consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKEmin} clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKEmin} + t_{IH}.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-refresh mode can only be entered from the All banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-refresh Exit are NOP and DESELECT only.
13. Self-refresh cannot be entered while Read or Write operations. See ‘Self-Refresh Operation” and ‘Power-Down Modes” on later section for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. ‘Idle state’ means that all banks are closed (t_{RP},t_{DAL},etc. satisfied) and CKE is high and all timings from previous operations are satisfied (t_{MRD},t_{MOD},t_{RFC},t_{ZQinit},t_{ZQoper},t_{ZQCS},etc)as well as all SRF exit and Power Down exit parameters are satisfied (t_{XS},t_{XP},t_{XPDLL},etc)

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 ~ 1.8	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 ~ 1.8	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.8	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

Operating Temperature Condition

Symbol	Parameter	Rating		Units	Notes
		Min.	Max.		
T_{CASE}	Case operating temperature for commercial temperature product	0	95	°C	1,2,3
T_{CASE}	Case operating temperature for industrial temperature product	-40	95	°C	1,2,3

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation this temperature range must be maintained under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions applies:
   (a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9μs. (This double refresh requirement may not apply for some devices.
   (b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions

Symbol	Parameter	Operation Voltage	Rating			Units	Notes
			Min.	Typ.	Max.		
V_{DD}	Supply voltage	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3
V_{DDQ}	Supply voltage for Output	1.35	1.283	1.35	1.45	V	1,2,3
		1.5	1.425	1.5	1.575	V	1,2,3

Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. V_{DD} and V_{DDQ} rating are determined by operation voltage.

AC and DC Input Levels for Single-Ended Signals

Single-Ended AC and DC Input Levels for Command and Address (1.35V)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHCA} (DC90)	DC input logic high	V_{REF} + 0.090	V_{DD}	V	1,5(a)
V_{ILCA} (DC90)	DC input logic low	V_{SS}	V_{REF} - 0.090	V	1,6(a)
V_{IHCA} (AC160)	DDR3L-1600	V_{REF} + 0.160	-	V	1,2
V_{IHCA} (AC135)	DDR3L-1866,1600	V_{REF} + 0.135	-	V	1,2
V_{IHCA} (AC125)	DDR3L-1866,1600	V_{REF} + 0.125	-	V	1,2
V_{ILCA} (AC160)	DDR3L-1600	-	V_{REF} - 0.160	V	1,2
V_{ILCA} (AC135)	DDR3L-1866,1600	-	V_{REF} - 0.135	V	1,2
V_{ILCA} (AC125)	DDR3L-1866,1600	-	V_{REF} - 0.125	V	1,2
V_{REFCA} (DC)	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Notes:

1. For input only pins except $\overline{\text{RESET}}$: V_{REF} = V_{REFCA} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFCA} (DC) by more than ±1% V_{DD} (for reference: approx. ±15 mV).
4. For reference: approx. V_{DD}/2 ±15 mV.
5. V_{IH}(dc) is used as a simplified symbol for $V_{IH.CA}$(a) 1.35V : DC90, b) 1.5V : DC100)
6. V_{IL}(dc) is used as a simplified symbol for $V_{IL.CA}$(a) 1.35V : DC90, b) 1.5V : DC100)
7. V_{IH}(ac) is used as a simplified symbol for $V_{IH.CA}$(AC175) and $V_{IH.CA}$(AC150); $V_{IH.CA}$(AC175) value is used when V_{REF} + 175mV is referenced and $V_{IH.CA}$(AC150) value is used when V_{REF} + 150mV is referenced.
8. V_{IL}(ac) is used as a simplified symbol for $V_{IL.CA}$(AC175) and $V_{IL.CA}$(AC150); $V_{IL.CA}$(AC175) value is used when V_{REF} - 175mV is referenced and $V_{IL.CA}$(AC150) value is used when V_{REF} - 150mV is referenced.

Single-Ended AC and DC Input Levels for DQ and DM (1.35V)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHDQ} (DC90)	DC input logic high	V_{REF} + 0.090	V_{DD}	V	1,5(a)
V_{ILDQ} (DC90)	DC input logic low	V_{SS}	V_{REF} - 0.090	V	1,6(a)
V_{IHDQ} (AC160)	DDR3L-1600	V_{REF} + 0.160	-	V	1,2
V_{IHDQ} (AC135)	DDR3L-1866,1600	V_{REF} + 0.135	-	V	1,2
V_{IHDQ} (AC130)	DDR3L-1866,1600	V_{REF} + 0.130	-	V	1,2
V_{ILDQ} (AC160)	DDR3L-1600	-	V_{REF} - 0.160	V	1,2
V_{ILDQ} (AC135)	DDR3L-1866,1600	-	V_{REF} - 0.135	V	1,2
V_{ILDQ} (AC130)	DDR3L-1866,1600	-	V_{REF} - 0.130	V	1,2
V_{REFDQ} (DC)	Reference voltage for DQ, DM inputs	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Notes:

1. For DQ and DM: V_{REF} = V_{REFDQ} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFDQ} (DC) by more than ±1% V_{DD} (for reference: approx. ±15 mV).
4. For reference: approx. V_{DD}/2 ±15 mV.
5. V_{IH}(dc) is used as a simplified symbol for $V_{IH.DQ}$(a) 1.35V : DC90, b) 1.5V : DC100)
6. V_{IL}(dc) is used as a simplified symbol for $V_{IL.DQ}$(a) 1.35V : DC90, b) 1.5V : DC100)
7. V_{IH}(ac) is used as a simplified symbol for $V_{IH.DQ}$(AC175), $V_{IH.DQ}$(AC150) ; $V_{IH.DQ}$(AC175) value is used when V_{REF} + 175mV is referenced, $V_{IH.DQ}$(AC150) value is used when V_{REF} + 150mV is referenced.
8. V_{IL}(ac) is used as a simplified symbol for $V_{IL.DQ}$(AC175), $V_{IL.DQ}$(AC150) ; $V_{IL.DQ}$(AC175) value is used when V_{REF} - 175mV is referenced, $V_{IL.DQ}$(AC150) value is used when V_{REF} - 150mV is referenced.

Single-Ended AC and DC Input Levels for Command and Address (1.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHCA} (DC100)	DC input logic high	V_{REF} + 0.100	V_{DD}	V	1, 5(b)
V_{ILCA} (DC100)	DC input logic low	V_{SS}	V_{REF} - 0.100	V	1, 6(b)
V_{IHCA} (AC175)	DDR3-1600	V_{REF} + 0.175	-	V	1,2
V_{IHCA} (AC150)	DDR3-1600	V_{REF} + 0.150	-	V	1,2
V_{IHCA} (AC135)	DDR3-1866	V_{REF} + 0.135	-	V	1,2
V_{IHCA} (AC125)	DDR3-1866	V_{REF} + 0.125	-	V	1,2
V_{ILCA} (AC175)	DDR3-1600	-	V_{REF} - 0.175	V	1,2
V_{ILCA} (AC150)	DDR3-1600	-	V_{REF} - 0.150	V	1,2
V_{ILCA} (AC135)	DDR3-1866	-	V_{REF} - 0.135	V	1,2
V_{ILCA} (AC125)	DDR3-1866	-	V_{REF} - 0.125	V	1,2
V_{REFCA} (DC)	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Notes:
1. For input only pins except $\overline{\text{RESET}}$: V_{REF} = V_{REFCA} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFCA} (DC) by more than ±1% V_{DD} (for reference: approx. ±15 mV).
4. For reference: approx. V_{DD}/2 ±15 mV.
5. V_{IH}(dc) is used as a simplified symbol for $V_{IH.CA}$(a) 1.35V : DC90, b) 1.5V : DC100)
6. V_{IL}(dc) is used as a simplified symbol for $V_{IL.CA}$(a) 1.35V : DC90, b) 1.5V : DC100)
7. V_{IH}(ac) is used as a simplified symbol for $V_{IH.CA}$(AC175) and $V_{IH.CA}$(AC150); $V_{IH.CA}$(AC175) value is used when V_{REF} + 175mV is referenced and $V_{IH.CA}$(AC150) value is used when V_{REF} + 150mV is referenced.
8. V_{IL}(ac) is used as a simplified symbol for $V_{IL.CA}$(AC175) and $V_{IL.CA}$(AC150); $V_{IL.CA}$(AC175) value is used when V_{REF} - 175mV is referenced and $V_{IL.CA}$(AC150) value is used when V_{REF} - 150mV is referenced.

Single-Ended AC and DC Input Levels for DQ and DM (1.5V)

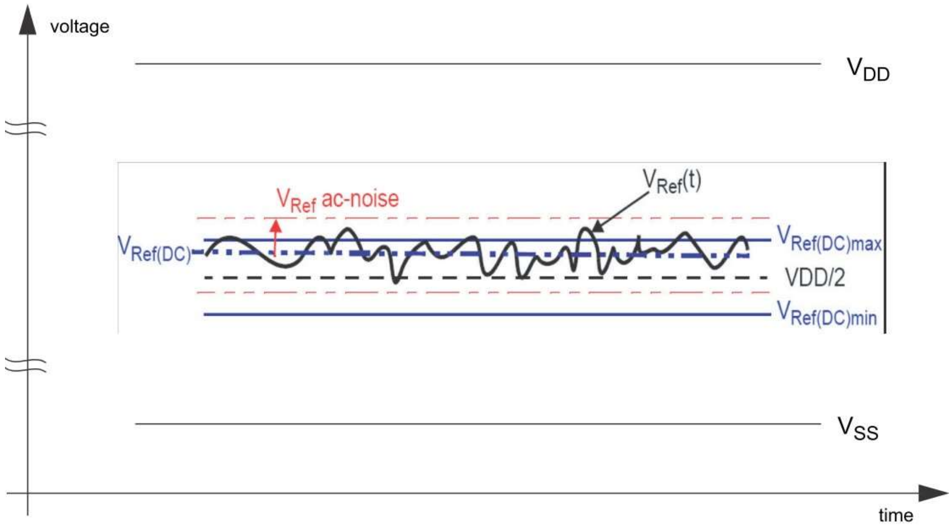
Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHDQ} (DC100)	DC input logic high	V_{REF} + 0.100	V_{DD}	V	1,5(b)
V_{ILDQ} (DC100)	DC input logic low	V_{SS}	V_{REF} - 0.100	V	1,6(b)
V_{IHDQ} (AC150)	DDR3-1600	V_{REF} + 0.150	-	V	1,2
V_{IHDQ} (AC135)	DDR3-1866	V_{REF} + 0.135	-	V	1,2
V_{ILDQ} (AC150)	DDR3-1600	-	V_{REF} - 0.150	V	1,2
V_{ILDQ} (AC135)	DDR3-1866	-	V_{REF} - 0.135	V	1,2
V_{REFDQ} (DC)	Reference voltage for DQ, DM inputs	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Notes:
1. For DQ and DM: V_{REF} = V_{REFDQ} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFDQ} (DC) by more than ±1% V_{DD} (for reference: approx. ±15 mV).
4. For reference: approx. V_{DD}/2 ±15 mV.
5. V_{IH}(dc) is used as a simplified symbol for $V_{IH.DQ}$(a) 1.35V : DC90, b) 1.5V : DC100)
6. V_{IL}(dc) is used as a simplified symbol for $V_{IL.DQ}$(a) 1.35V : DC90, b) 1.5V : DC100)
7. V_{IH}(ac) is used as a simplified symbol for $V_{IH.DQ}$(AC175), $V_{IH.DQ}$(AC150) ; $V_{IH.DQ}$(AC175) value is used when V_{REF} + 175mV is referenced, $V_{IH.DQ}$(AC150) value is used when V_{REF} + 150mV is referenced.
8. V_{IL}(ac) is used as a simplified symbol for $V_{IL.DQ}$(AC175), $V_{IL.DQ}$(AC150) ; $V_{IL.DQ}$(AC175) value is used when V_{REF} - 175mV is referenced, $V_{IL.DQ}$(AC150) value is used when V_{REF} - 150mV is referenced.

V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated in figure V_{REF}(DC) tolerance and V_{REF} AC-Noise limits. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of “Single-Ended AC and DC Input Levels for Command and Address”. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than +/- 1% V_{DD}.



V_{REF}(DC) tolerance and V_{REF} AC-Noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

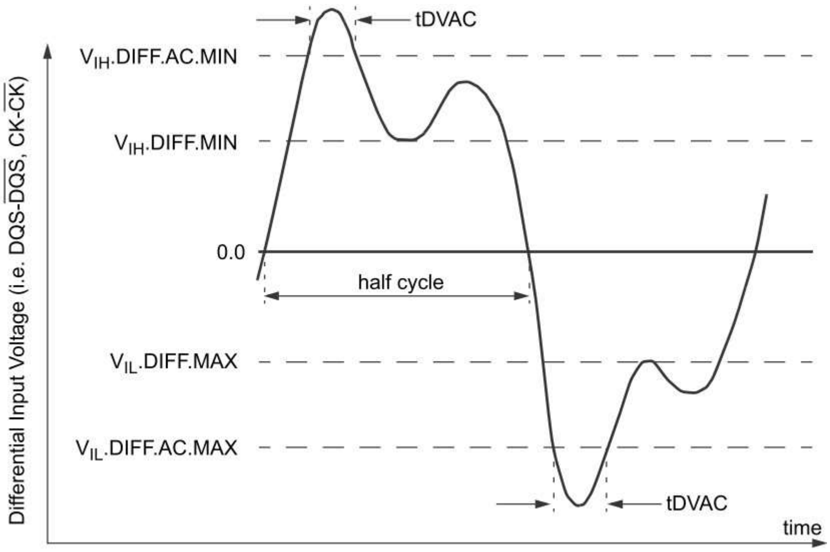
"V_{REF}" shall be understood as V_{REF}(DC), as defined in figure above, V_{REF}(DC) tolerance and V_{REF} AC- Noise limits.

This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and volt- age associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/- 1% of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" t_{DVAC}

Differential swing requirement for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels (1.35V)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHdiff}	Differential input high	+0.18	NOTE 3	V	1
V_{ILdiff}	Differential input low	NOTE 3	-0.18	V	1
$V_{IHdiff}(AC)$	Differential input high AC	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
$V_{ILdiff}(AC)$	Differential input low AC	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Differential AC and DC Input Levels (1.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHdiff}	Differential input high	+0.2	NOTE 3	V	1
V_{ILdiff}	Differential input low	NOTE 3	-0.2	V	1
$V_{IHdiff}(AC)$	Differential input high AC	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
$V_{ILdiff}(AC)$	Differential input low AC	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use V_{IH}/V_{IL}(AC) of address/command and V_{REFCA}; for strobes (DQS, $\overline{DQS}$) use V_{IH}/V_{IL}(AC) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC) min for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specification".

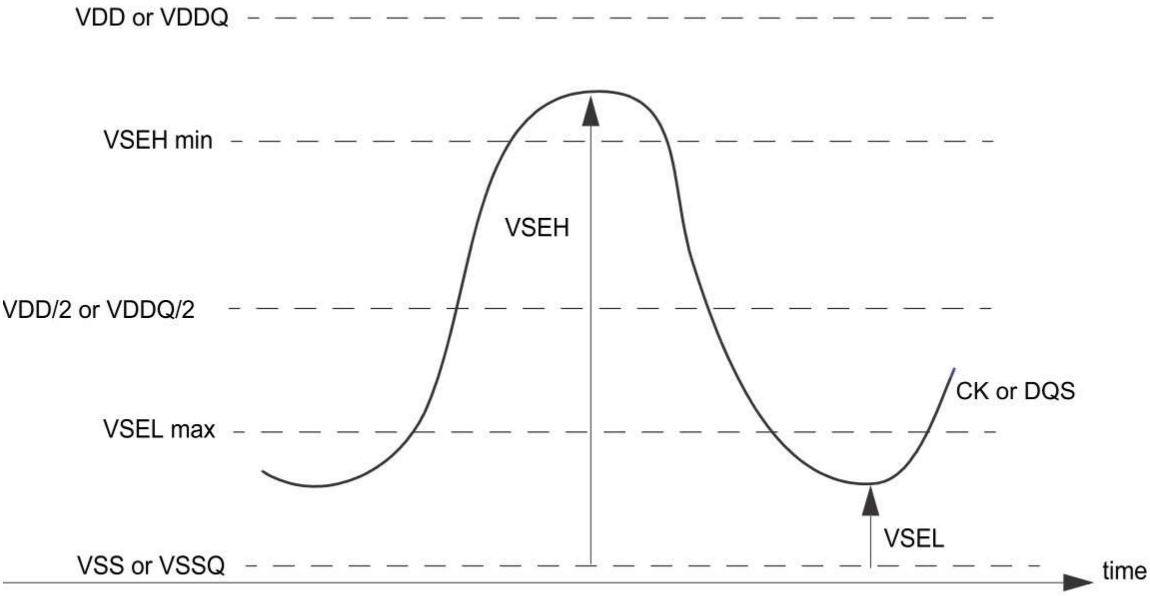
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach V_{SEH} min / V_{SEL} max [approximately equal to the AC-levels (V_{IH}(AC) / V_{IL}(AC)) for Address/command signals] in every half-cycle.

DQS,$\overline{DQS}$ have to reach V_{SEH} min / V_{SEL} max [approximately the ac-levels (V_{IH}(AC) / V_{IL}(AC)) for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if V_{IH150}(AC) / V_{IL150}(AC) is used for Address/command signals, then these AC-levels apply also for the single-ended components of differential CK and $\overline{CK}$



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single- ended components of differential signals the requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

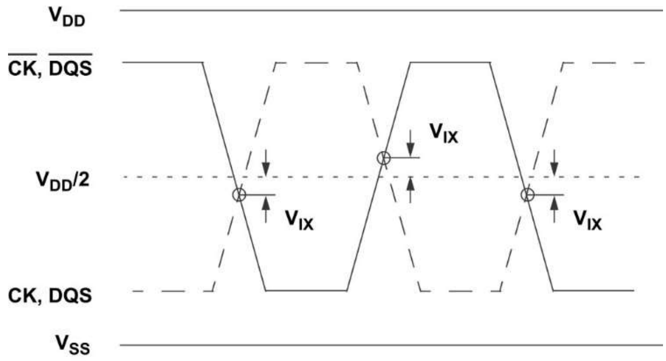
Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	Min.	Max.	Units	Notes
V_{SEH}	Single-ended high-level for strobes	$(V_{DD}/2) + 0.175$	NOTE 3	V	1,2
	Single-ended high-level for CK, $\overline{CK}$	$(V_{DD}/2) + 0.175$	NOTE 3	V	1,2
V_{SEL}	Single-ended low-level for strobes	NOTE 3	$(V_{DD}/2) - 0.175$	V	1,2
	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	$(V_{DD}/2) - 0.175$	V	1,2

Notes:

1. For CK, $\overline{CK}$ use $V_{IH}/V_{IL}(AC)$ of address/command; for strobes (DQS, $\overline{DQS}$) use $V_{IH}/V_{IL}(AC)$ of DQs.
2. $V_{IH}(AC)/V_{IL}(AC)$ for DQs is based on V_{REFDQ}; $V_{IH}(AC)/V_{IL}(AC)$ for address/command is based on V_{REFCA}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended components of differential signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot specifications”.

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid-level between V_{DD} and V_{SS}.



Differential Input Cross Point Voltage

Cross point voltage for differential input signals (CK, DQS): 1.35V

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IX}	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, $\overline{CK}$	-150	150	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, $\overline{DQS}$	-150	150	mV	

Notes:
1. The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following.
   $(V_{DD}/2) + V_{IX}(Min) – V_{SEL} >= 25mV$
   $V_{SEH} – ((V_{DD}/2) + V_{IX}(Max)) >= 25mV$

Cross point voltage for differential input signals (CK, DQS): 1.5V

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IX}	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, $\overline{DQS}$	-150	150	mV	

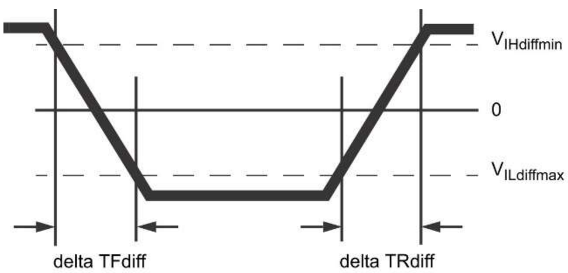
Notes: Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing V_{SEL} / V_{SEH} of at least V_{DD}/2 +/- 250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for V_{SEL} and V_{SEH} standard values.

Slew Rate Definitions for Differential Input Signals

Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	V_{ILdiff} (max)	V_{IHdiff} (min)	$\frac{V_{IHdiff}(min) - V_{ILdiff}(max)}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	V_{IHdiff} (min)	V_{ILdiff} (max)	$\frac{V_{IHdiff}(min) - V_{ILdiff}(max)}{\text{Delta TFdiff}}$

Note: The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate definition for DQS,$\overline{DQS}$ and CK,$\overline{CK}$

Single-ended AC & DC Output Levels

Symbol	Parameter	DDR3-1866,1600	Units	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes: The swing of +/-0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT}=V_{DDQ}/2.

Differential AC & DC Output Levels

Symbol	Parameter	DDR3-1866,1600	Units	Notes
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.2 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.2 x V_{DDQ}	V	1

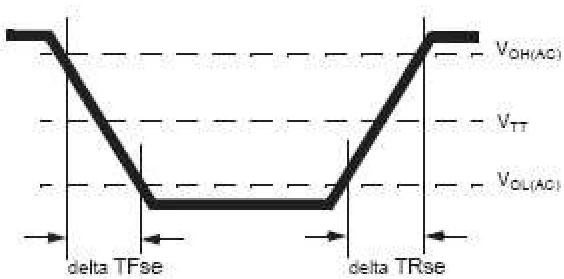
Notes: The swing of +/-0.2xVDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT=VDDQ/2 at each of the differential outputs.

Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	$\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TRse}}$
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	$\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TFse}}$

Note: Output slew rate is verified by design and characterization and may not be subject to production test.



Single-ended Output Slew Rate definition

Parameter	Symbol	Voltage	DDR3-1866,1600		Units
			Min	Max	
Single ended output slew rate	SRQse	1.35V	1.75	5[(1)]	V/ns
		1.5V	2.5	5	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
SE: Single-ended Signals
For Ron = RZQ/7 setting

Notes: In two case, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

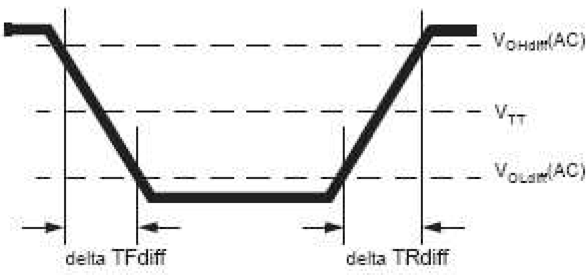
- Case (1) is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low of low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
- Case (2) is defined for a single DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maxi- mum limit of 5 V/ns applies.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff}(AC) and V_{OHdiff}(AC) for differential signals.

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	V_{OHdiff}(AC)-V_{OLdiff}(AC) Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	V_{OHdiff}(AC)-V_{OLdiff}(AC)) Delta TFdiff

Note: Output slew rate is verified by design and characterization and may not be subject to production test.



Differential Output Slew Rate definition

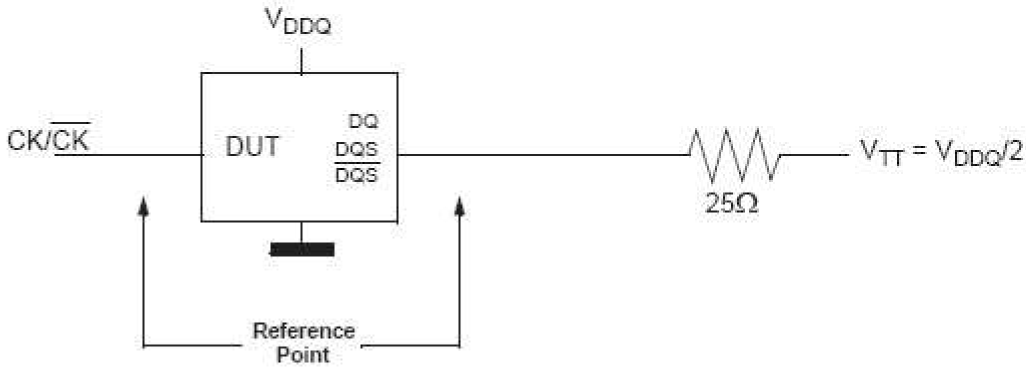
Parameter	Symbol	Voltage	DDR3-1866,1600		Units
			Min	Max	
Differential output slew rate	SRQdiff	1.35V	3.5	12	V/ns
		1.5V	5	12	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment, or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

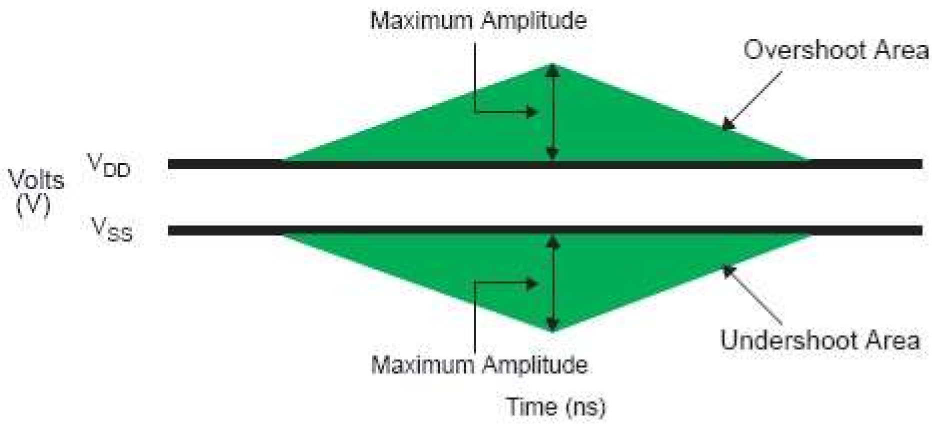


Reference Load for AC Timing and Output Slew Rate

Overshoot and Undershoot Specification

Address and Control Overshoot and Undershoot specifications

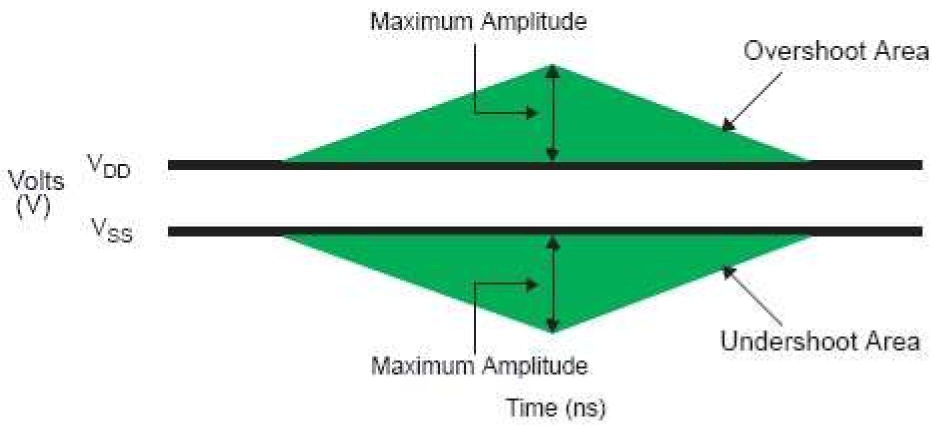
Parameter	Specification DDR3-1866,1600	Unit
Maximum peak amplitude allowed for overshoot area	0.4V	V
Maximum peak amplitude allowed for undershoot area	0.4V	V
Maximum overshoot area above V_{DD}	0.28V-ns	V-ns
Maximum undershoot area below V_{SS}	0.28V-ns	V-ns



Address and Control Overshoot and Undershoot Definition

Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Parameter	Specification DDR3-1866,1600	Unit
Maximum peak amplitude allowed for overshoot area	0.4V	V
Maximum peak amplitude allowed for undershoot area	0.4V	V
Maximum overshoot area above V_{DD}	0.11V-ns	V-ns
Maximum undershoot area below V_{SS}	0.11V-ns	V-ns



Clock, Data, Strobe, Mask Overshoot and Undershoot Definition

I_{DD} Specification

V_{DD}, V_{DDQ} = 1.35V (1.283V to 1.45V)

Conditions	Symbol	Data rate (Mbps)	IDD max	Units
			x8	
Operating One Bank Active-Precharge Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD0}	1866	75	mA
Operating One Bank Active-Read-Precharge Current; CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD1}	1866	95	mA
Precharge Power-Down Current Slow Exit; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	I_{DD2P0}	1866	16	mA
Precharge Power-Down Current Fast Exit; CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	I_{DD2P1}	1866	24	mA
Precharge Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD2N}	1866	52	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: stable at 0; Data IO: FLOAT- ING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD2Q}	1866	52	mA
Active Power-Down Current; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD3P}	1866	54	mA
Active Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD3N}	1866	58	mA

Conditions	Symbol	Data rate (Mbps)	I_{DD} max	Units
			x8	
Operating Burst Read Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD4R}	1866	136	mA
Operating Burst Write Current; CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	I_{DD4W}	1866	211	mA
Burst Refresh Current; CKE: High; External clock: On; t_{CK}, CL, nRFC: see timing used table; BL: 8; AL: 0; $\overline{CS}$: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD5B}	1866	268	mA
Self Refresh Current: Normal Temperature Range; Tcase: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	I_{DD6}	1866	24	mA
Self Refresh Current: Extended Temperature Range; Tcase: 0-95°C; Auto Self-Re- fresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see timing used table; BL: 8; AL: 0; $\overline{CS}$, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	I_{DD6ET}	1866	32	mA
Operating Bank Interleave Read Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; $\overline{CS}$: High be- tween ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	I_{DD7}	1866	171	mA
RESET Low Current; RESET: Low; External clock: off; CK and $\overline{CK}$: LOW; CKE: FLOAT- ING; $\overline{CS}$, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	I_{DD8}	1866	20	mA

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3. Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM
7. Read Burst type: Nibble Sequential, set MR0 A[3]=0B

Timing used for I_{DD} and I_{DDQ} Measured - Loop Patterns

Speed		DDR3-1866	DDR3-1600	Units
CL-nRCD-nRP		13-13-13	11-11-11	
t_{CK}(min)		1.07	1.25	ns
CL		13	11	nCK
nRCD		13	11	nCK
nRC		45	39	nCK
nRAS		32	28	nCK
nRP		13	11	nCK
nFAW	1KB Page size	26	24	nCK
nRRD	1KB Page size	5	5	nCK
nRFC		243	208	nCK

Capacitance

(V_{DD} = 1.35V, T_{OPER} = 25℃)

Symbol	Parameter	DDR3L-1866		DDR3L-1600		Unit	Note
		Min	Max	Min	Max		
C_{IO}	Input/Output Capacitance (DQ, DM, DQS, $\overline{DQS}$)	1.4	2.1	1.4	2.2	pF	1,2,3
C_{CK}	Input Capacitance (CK and $\overline{CK}$)	0.8	1.3	0.8	1.4	pF	2,3
C_{DCK}	Input Capacitance Delta (CK and $\overline{CK}$)	0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/Output Capacitance Delta (DQS and $\overline{DQS}$)	0	0.15	0	0.15	pF	2,3,5
C_I	Input Capacitance (CTRL, AMD, CMD input-only pins)	0.75	1.2	0.75	1.2	pF	2,3,6
C_{DI_CTRL}	Input Capacitance Delta (all CTRL input-only pins)	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
$C_{DI\_ADD\_CMD}$	Input/Output Capacitance Delta (all ADD, CMD input-only pins)	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
C_{DIO}	Input/Output Capacitance Delta (DQ, DM, DQS, $\overline{DQS}$)	-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/Output Capacitance of ZQ pin	-	3	-	3.0	pF	2,3,12

Note:

1. Although the DM pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. V_{DD}=V_{DDQ}=1.35, V_{BIAS}=V_{DD}/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute values of CCK-$C\overline{CK}$.
5. Absolute values of CIO(DQS)-CIO($\overline{DQS}$).
6. CI applies to ODT, $\overline{CS}$,CKE,A0-A12,BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CDI_CTRL applies to ODT, $\overline{CS}$,CKE
8. CDI_CTRL=CDI(CTRL)-0.5*(CI(CK)+CI($\overline{CK}$))
9. CDI_ADD_CMD applies to A0-A12,BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
10. CDI_ADD_CMD=CI(ADD_CMD)–0.5*(CI(CK)+CI($\overline{CK}$)).
11. CDIO=CIO(DQ,DM)-0.5*(CIO(DQS)+CIO($\overline{DQS}$)).
12. Maximum external load capacitance on ZQ pin: 5pF

DDR3-1866 Speed Bins

Speed Bin				107 (DDR3-1866)		Units	Notes
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min.	Max.		
Internal read command to first data			t_{AA}	13.91 (13.125)	20	ns	5,9
Active to read or write delay time			t_{RCD}	13.91 (13.125)	-	ns	5,9
Precharge command period			t_{RP}	13.91 (13.125)	-	ns	5,9
Active to active/auto-refresh command time			t_{RC}	47.91 (47.125)	-	ns	5,9
Active to precharge command period			t_{RAS}	34	9 * t_{REFI}	ns	7
Average Clock Cycle Time	CL = 6	CWL = 5	t_{CK}(avg)	2.5	3.3	ns	1,2,3,6
		CWL = 6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,6
	CL = 8	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
	CL = 10	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5,6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 8	t_{CK}(avg)	1.25	1.5	ns	1,2,3,6
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 12	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 9	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 13	CWL = 5,6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 9	t_{CK}(avg)	1.07	1.25	ns	1,2,3
Supported CL setting				6, 7, 8, 9, 10, 11, 13		nCK	
Supported CWL setting				5, 6, 7, 8, 9		nCK	

DDR3-1600 Speed Bins

Speed Bin				125 (DDR3-1600)		Units	Notes
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	Min.	Max.		
Internal read command to first data			t_{AA}	13.75 (13.125)	20	ns	5,9
Active to read or write delay time			t_{RCD}	13.75 (13.125)	-	ns	5,9
Precharge command period			t_{RP}	13.75 (13.125)	-	ns	5,9
Active to active/auto-refresh command time			t_{RC}	48.75 (48.125)	-	ns	5,9
Active to precharge command period			t_{RAS}	35	9 * t_{REFI}	ns	7
Average Clock Cycle Time	CL = 5	CWL = 5	t_{CK}(avg)	3.0	3.3	ns	1,2,3,6
		CWL = 6,7	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL=6	CWL=5	t_{CK}(avg)	2.5	3.3	ns	1,2,3,6
		CWL=6,7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7,8	t_{CK}(avg)	Reserved	Reserved	ns	1,2,3,6
	CL = 8	CWL = 5	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 6	t_{CK}(avg)	1.875	2.5	ns	1,2,3,6
		CWL = 7,8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 10	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.5	1.875	ns	1,2,3,6
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5,6	t_{CK}(avg)	Reserved	Reserved	ns	4
		CWL = 7	t_{CK}(avg)	1.25	1.5	ns	1,2,3,6
		CWL = 8	t_{CK}(avg)	Reserved	Reserved	ns	4
Supported CL setting				5,6,7,8,9,10,11		nCK	
Supported CWL setting				5, 6, 7, 8		nCK	

Speed Bin Table Notes

1. The CL setting and CWL setting result in t_{CK}(avg) Min and t_{CK}(avg) Max requirements. When making a selection of t_{CK}(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. t_{CK}(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard t_{CK}(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = t_{AA} [ns] / t_{CK}(avg) [ns], rounding up to the next "Supported CL".
3. t_{CK}(avg) Max limits: Calculate t_{CK}(avg) = t_{AA} Max / CL Selected and round the resulting t_{CK}(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is t_{CK}(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. ‘Optional’ settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier’s data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. t_{REFI} depends on operating case temperature (T_{CASE}).
8. For devices supporting optional down binning to CL=7 and CL=9, t_{AA}/ t_{RCD}/ t_{RP}min must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125ns in SPD bytes for t_{AA}min (byte16), t_{RCD}min (Byte18) and t_{RP}min (byte20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1066F should program 13.125ns in SPD bytes for t_{AA}min (byte16), t_{RCD}min (Byte18) and t_{RP}min (byte20). Once t_{RP} (Byte20) is programmed to 13.125ns, t_{RC} min (Byte21,23) also should be programmed accordingly. For example, 49.125ns (t_{RAS}min + t_{RP}min = 36ns + 13.125ns) for DDR3-1333H and 48.125ns (t_{RAS}min + t_{RP}min = 35ns + 13.125ns) for DDR3-1600K.
9. For devices supporting optional down binning to CL=11, CL=9 and CL=7, t_{AA} / t_{RCD} / t_{RPmin} must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866M devices supporting down binning to DDR3-1600K or DDR3-1333H or 1066F should program 13.125ns in SPD bytes for t_{AA}min (byte 16), t_{RCD}min(byte18) and t_{RP}min (byte 20). Once t_{RP} (byte 20) is programmed to 13.125ns, t_{RC}min (byte 21, 23) also should be programmed accordingly. For example, 47.125ns (t_{RAS}min + t_{RP}min = 34ns+13.125ns).

AC Characteristics

Parameter	Symbol	107 (DDR3-1866) Min.	107 (DDR3-1866) Max.	Units	Notes
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins		ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period for 1KB page size	t_{RRD}	5	-	ns	
		4	-	Nck	
Active Bank A to Active Bank B command period for 2KB page size	t_{RRD}	6	-	ns	
		4	-	Nck	
Four activate window for 1KB page size	t_{FAW}	27	-	ns	
Four activate window for 2KB page size	t_{FAW}	35	-	ns	
Address and Control input hold time (V_{IH}/V_{IL} (DC) levels)	**1.35V**				
	t_{IH}(base) DC90	110	-	ps	16
	1.5V				
	t_{IH}(base) DC100	100	-	ps	16
Address and Control input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{IS}(base) AC125	150	-	ps	16
	1.5V				
	t_{IS}(base) AC125	150	-	ps	16
Address and Control input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{IS}(base) AC135	65	-	ps	16
	1.5V				
	t_{IS}(base) AC150	65	-	ps	16,24
DQ and DM input setup time (V_{IH}/V_{IL} (DC) levels)	**1.35V**				
	t_{DH}(base) DC90	75	-	ps	17
	1.5V				
	t_{DH}(base) DC100	70	-	ps	17
DQ and DM input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{DS}(base) AC130	70	-	ps	17
	1.5V				
	t_{DS}(base) AC135	68	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	535	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	320	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	195	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-390	195	ps	13,14

Parameter	Symbol	107 (DDR3-1866)		Units	Notes
		Min.	Max.		
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	t_{DQSQ}	-	85	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	Nck	
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	t_{CK}(avg)	12,13
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-195	195	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.27	0.27	t_{CK}(avg)	
DQS falling edge hold time from rising CK, $\overline{CK}$	t_{DSH}	0.18	-	t_{CK}(avg)	29
DQS falling edge setup time to rising CK, $\overline{CK}$	t_{DSS}	0.18	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	Nck	
Mode register set command update delay	t_{MOD}	15	-	ns	
		12	-	Nck	
Read preamble time	t_{RPRE}	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	t_{CK}(avg)	1
Write postamble time	tWPST	0.3	-	tCK(avg)	1
Write recovery time	tWR	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [t_{RP} / t_{CK}(avg)]		Nck	
Multi-purpose register recovery time	t_{MPRR}	1	-	Nck	22
Internal write to read command delay	t_{WTR}	7.5	-	ns	18
		4	-	Nck	18
Internal read to precharge command delay	t_{RTP}	7.5	-	ns	
		4	-	Nck	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min)+1Nck	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	ns	
Valid clock requirement before Self- refresh exit or Power-down exit	tCKSRX	10	-	ns	
		5	-	Nck	
Exit Self-refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10	-	ns	
		5	-	Nck	
Exit Self-refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	Nck	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	110	-	ns	

Parameter	Symbol	107 (DDR3-1866)		Units	Notes
		Min.	Max.		
Average Periodic Refresh Interval 0°C ≤ Tcase ≤ +85°C	t_{REFI}	-	7.8	µs	
Average Periodic Refresh Interval +85°C < Tcase ≤ +105°C	t_{REFI}	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	5	-	ns	
		3	-	Nck	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min)+10	-	ns	
		5	-	Nck	
DLL locking time	t_{DLLK}	512	-	Nck	
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	ns	2
		10	-	Nck	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	ns	
		3	-	Nck	
Command pass disable delay	t_{CPDED}	2	-	Nck	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	Nck	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	Nck	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	Nck	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [t_{WR}/t_{CK}(avg)]		Nck	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [t_{WR}/t_{CK}(avg)]		Nck	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL+4+WR+1	-	Nck	10
Timing of WRA command to Power-down entry (BC4MRS)	t_{WRPDEN}	WL+2+WR+1	-	Nck	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	Nck	20,21
Timing of MRS command to Power-down entry	$t_{WRSPDEN}$	t_{MOD}(min)	-		
RTT turn-on	t_{AON}	-195	195	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	t_{CK}(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	Nck	
ODT high time with Write command and BL8	ODTH8	6	-	Nck	
RTT dynamic change skew	t_{ADC}	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{Zqinit}	512	-	Nck	
Normal operation full calibration time	t_{Zqoper}	256	-	Nck	

Parameter	Symbol	107 (DDR3-1866)		Units	Notes
		Min.	Max.		
Normal operation short calibration time	t_{ZQCS}	64	-	Nck	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	Nck	3
DQS, $\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	Nck	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	140	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	140	-	ps	
Write leveling output delay	t_{WLO}	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	ns	
Absolute clock period	t_{CK}(abs)	t_{CK}(avg)min + t_{JIT}(per)min	t_{CK}(avg)max + t_{JIT}(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-60	60	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-50	50	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	120	ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	100	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-88	88	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-105	105	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-117	117	ps	
Cumulative error across 5 cycles	t_{ERR} (5per)	-126	126	ps	
Cumulative error across 6 cycles	t_{ERR} (6per)	-133	133	ps	
Cumulative error across 7 cycles	t_{ERR} (7per)	-139	139	ps	
Cumulative error across 8 cycles	t_{ERR} (8per)	-145	145	ps	
Cumulative error across 9 cycles	t_{ERR} (9per)	-150	150	ps	
Cumulative error across 10 cycles	t_{ERR} (10per)	-154	154	ps	
Cumulative error across 11 cycles	t_{ERR} (11per)	-158	158	ps	
Cumulative error across 12 cycles	t_{ERR} (12per)	-161	161	ps	
Cumulative error across n = 13,14,…49,50 cycles	t_{ERR} (nper)	t_{ERR} (nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max		ps	32

Parameter	Symbol	125 (DDR3-1600)		Units	Notes
		Min.	Max.		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins		ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period for 1KB page size	t_{RRD}	6	-	ns	
		4	-	Nck	
Active Bank A to Active Bank B command period for 2KB page size	t_{RRD}	7.5	-	ns	
		4	-	Nck	
Four activate window for 1KB page size	t_{FAW}	30	-	ns	
Four activate window for 2KB page size	t_{FAW}	40	-	ns	
Address and Control input hold time (V_{IH}/V_{IL} (DC) levels)	**1.35V**				
	t_{IH}(base) DC90	130	-	ps	16
	1.5V				
	t_{IH}(base) DC100	120	-	ps	16
Address and Control input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{IS}(base) AC160	60	-	ps	16
	1.5V				
	t_{IS}(base) AC175	45	-	ps	16
Address and Control input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{IS}(base) AC135	185	-	ps	16
	1.5V				
	t_{IS}(base) AC150	170	-	ps	16,24
DQ and DM input setup time (V_{IH}/V_{IL} (DC) levels)	**1.35V**				
	t_{DH}(base) DC90	55	-	ps	17
	1.5V				
	t_{DH}(base) DC100	45	-	ps	17
DQ and DM input setup time (V_{IH}/V_{IL} (AC) levels)	**1.35V**				
	t_{DS}(base) AC135	25	-	ps	17
	1.5V				
	t_{DS}(base) AC150	10	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	560	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	360	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	225	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-450	225	ps	13,14

Parameter	Symbol	125 (DDR3-1600)		Units	Notes
		Min.	Max.		
DQS, $\overline{DQS}$ to DQ Skew, per group, per access	t_{DQSQ}	-	100	ps	12,13
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	Nck	
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	t_{CK}(avg)	12,13
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-225	225	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.27	0.27	t_{CK}(avg)	
DQS falling edge hold time from rising CK, $\overline{CK}$	t_{DSH}	0.18	-	t_{CK}(avg)	29
DQS falling edge setup time to rising CK, $\overline{CK}$	t_{DSS}	0.18	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	Nck	
Mode register set command update delay	t_{MOD}	15	-	ns	
		12	-	Nck	
Read preamble time	t_{RPRE}	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	t_{CK}(avg)	1
Write postamble time	tWPST	0.3	-	tCK(avg)	1
Write recovery time	tWR	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [t_{RP} / t_{CK}(avg)]		Nck	
Multi-purpose register recovery time	t_{MPRR}	1	-	Nck	22
Internal write to read command delay	t_{WTR}	7.5	-	ns	18
		4	-	Nck	18
Internal read to precharge command delay	t_{RTP}	7.5	-	ns	
		4	-	Nck	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min)+1nCK	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	ns	
Valid clock requirement before Self- refresh exit or Power-down exit	tCKSRX	10	-	ns	
		5	-	Nck	
Exit Self-refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10	-	ns	
		5	-	Nck	
Exit Self-refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	Nck	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-	ns	

Parameter	Symbol	125 (DDR3-1600)		Units	Notes
		Min.	Max.		
Average Periodic Refresh Interval 0°C ≤ Tcase ≤ +85°C	t_{REFI}	-	7.8	µs	
Average Periodic Refresh Interval +85°C < Tcase ≤ +105°C	t_{REFI}	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	5	-	ns	
		3	-	Nck	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min)+10	-	ns	
		5	-	Nck	
DLL locking time	t_{DLLK}	512	-	Nck	
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	ns	2
		10	-	Nck	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	ns	
		3	-	Nck	
Command pass disable delay	t_{CPDED}	1	-	Nck	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	Nck	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	Nck	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	Nck	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [t_{WR}/t_{CK}(avg)]		Nck	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [t_{WR}/t_{CK}(avg)]		Nck	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL+4+WR+1	-	Nck	10
Timing of WRA command to Power-down entry (BC4MRS)	t_{WRPDEN}	WL+2+WR+1	-	Nck	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	Nck	20,21
Timing of MRS command to Power-down entry	$t_{WRSPDEN}$	t_{MOD}(min)	-		
RTT turn-on	t_{AON}	-225	225	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	t_{CK}(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	Nck	
ODT high time with Write command and BL8	ODTH8	6	-	Nck	
RTT dynamic change skew	t_{ADC}	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{Zqinit}	512	-	Nck	
Normal operation full calibration time	t_{Zqoper}	256	-	Nck	

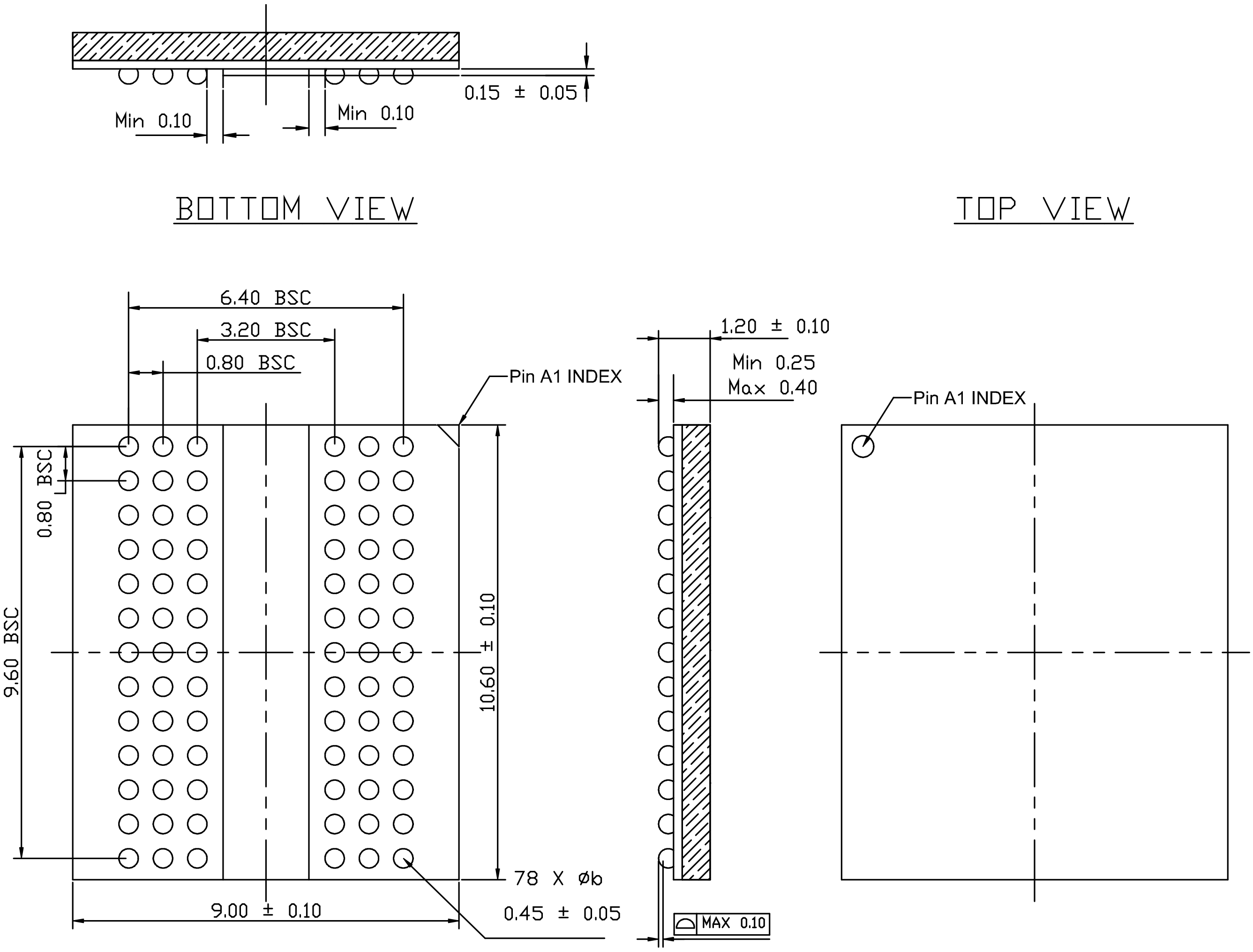
Parameter	Symbol	125 (DDR3-1600)		Units	Notes
		Min.	Max.		
Normal operation short calibration time	t_{ZQCS}	64	-	Nck	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	Nck	3
DQS, $\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	Nck	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	165	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	165	-	ps	
Write leveling output delay	t_{WLO}	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	ns	
Absolute clock period	t_{CK}(abs)	t_{CK}(avg)min + t_{JIT}(per)min	t_{CK}(avg)max + t_{JIT}(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-70	70	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-60	60	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	140	ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	120	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-103	103	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-122	122	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-136	136	ps	
Cumulative error across 5 cycles	t_{ERR} (5per)	-147	147	ps	
Cumulative error across 6 cycles	t_{ERR} (6per)	-155	155	ps	
Cumulative error across 7 cycles	t_{ERR} (7per)	-163	163	ps	
Cumulative error across 8 cycles	t_{ERR} (8per)	-169	169	ps	
Cumulative error across 9 cycles	t_{ERR} (9per)	-175	175	ps	
Cumulative error across 10 cycles	t_{ERR} (10per)	-180	180	ps	
Cumulative error across 11 cycles	t_{ERR} (11per)	-184	184	ps	
Cumulative error across 12 cycles	t_{ERR} (12per)	-188	188	ps	
Cumulative error across n = 13,14,…49,50 cycles	t_{ERR} (nper)	t_{ERR} (nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max		ps	32

Notes for AC Electrical Characteristics

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
7. ODT turn on time (min) is when the device leaves high impedance and ODT resistance begins to turn on.
   ODT turn on time (max) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min) is when the device starts to turn-off ODT resistance. ODT turn-off time (max) is when the bus is in high impedance. Both are measured from ODTLoff.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and t_{HZ}(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of t_{LZ}(DQS), t_{LZ}(DQ), t_{HZ}(DQS), t_{HZ}(DQ) Notes for definition and measurement method.
15. t_{REFI} depends on operating case temperature (Tcase).
16. t_{IS}(base) and t_{IH}(base) values are for 1V/ns command/addresss single-ended slew rate and 2V/ns CK, $\overline{\text{CK}}$ differential slew rate, Note for DQ and DM signals, V_{REF}(DC) = V_{REFDQ}(DC). For input only pins except $\overline{\text{RESET}}$, V_{REF}(DC) = V_{REFCA}(DC). See Address / Command Setup, Hold and Derating section.
17. t_{DS}(base) and t_{DH}(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{\text{DQS}}$ differential slew rate. Note for DQ and DM signals,V_{REF}(DC)= V_{REFDQ}(DC). For input only pins except RESET, V_{REF}(DC) = V_{REFCA}(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows;
    For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by t_{LZDQS}(min) on the left side and t_{DQSCK}(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down I_{DD} spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN}$(min) is satisfied, there are cases where additional time such as t_{XPDLL}(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 Nck for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:
    $$\frac{\text{ZQCorrection}}{(\text{Tsens x Tdriftrate}) + (\text{Vsens x Vdriftrate})}$$
    where Tsens = max(dRTTdT, dRONdTM) and Vsens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
24. The t_{IS}(base) AC150 specifications are adjusted from the t_{IS}(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 Mv and another 25 ps to account for the earlier reference point [(175 mv – 150 Mv) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of V_{REF}(DC) and the consecutive crossing of V_{REF}(DC).
26. t_{DQSL} describes the instantaneous differential input low pulse width on DQS – $\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.
27. t_{DQSH} describes the instantaneous differential input high pulse width on DQS – $\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.
28. t_{DQSH},act + t_{DQSL},act = 1 t_{CK},act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.
29. t_{DSH},act + t_{DSS},act = 1 t_{CK},act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.
30. t_{CH}(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. t_{CL}(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
33. $T_{CASE} \leq 85°C$.
34. Required for operation at $T_{CASE} > 85°C$.

Package Diagram

78-Ball Fine Pitch Ball Grid Array Outline



Note: All dimensions are in millmeter.

Version History

Version	History	Date	Remarks
0.1	First Release	Oct, 2022	
1.0	1. Update IDD table 2. Update Datasheet format	Oct, 2022	