IM4G16D3FDB
4Gbit DDR3 SDRAM
8Bank x 32Mbit x 16

	125	107	093
	DDR3-1600	DDR3-1866	DDR4-2133
Clock Cycle Time (CL=5; CWL=5)	2.5ns	-	-
Clock Cycle Time (CL=6; CWL=5)	2.5ns	2.5ns	2.5ns
Clock Cycle Time (CL=7; CWL=6)	1.875ns	1.875ns	1.875ns
Clock Cycle Time (CL=8; CWL=6)	1.875ns	1.875ns	1.875ns
Clock Cycle Time (CL=9; CWL=7)	1.5ns	1.5ns	1.5ns
Clock Cycle Time (CL=10; CWL=7)	1.5ns	1.5ns	1.5ns
Clock Cycle Time (CL=11; CWL=8)	1.25ns	1.25ns	1.25ns
Clock Cycle Time (CL=13; CWL=9)	-	1.07ns	1.07ns
Clock Cycle Time (CL=14; CWL=10)	-	-	0.938ns
System Frequency ($f_{CK(MAX)}$)	800MHz	933MHz	1066MHz

Specifications

- Density: 4Gbits
- Organization: 8Bank x 32Mbit x 16
- Package: 96-Ball FBGA
- Max Date rate: 2133Mbps
- Power Supply:
  - V_{DD} & V_{DDQ} = 1.35V (1.283V – 1.45V)
    **Backward compatible to 1.5V ± 0.075V*
  - V_{DD} & V_{DDQ} = 1.5V ± 0.075V
- Operating Temperature:
  - C-temp: 0℃ ≤ T_{CASE} ≤ 95℃
  - I-temp: -40℃ ≤ T_{CASE} ≤ 95℃
  - H-temp: -40℃ ≤ T_{CASE} ≤ 105℃
- 8 Internal Banks
- CAS Latency (CL): 5,6,7,8,9,10,11,12,13,14
- CAS Write Latency (CWL): 5,6,7,8,9,10
- Additive Latency (AL): 0, CL-2, CL-1
- Double Data Rate Architecture
- Bi-directional Data Strobe (DQS & DQS#)
- Differential Clock (CK & CK#)
- Burst Type: Sequential / Interleave
- Burst Length (BL): 8,4
- Refresh: Auto and Self
- Average Refresh Period:
  - 7.8us at -40°C ≤ T_{CASE} ≤ +85°C
  - 3.9us at +85°C ≤ T_{CASE} ≤ +95°C
  - 1.95us at +95°C ≤ T_{CASE} ≤ +105°C
- 8n-bit prefetch architecture
- Precharge & Active Power Down
- Output Driver Impedance Control
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- RoHS Compliant

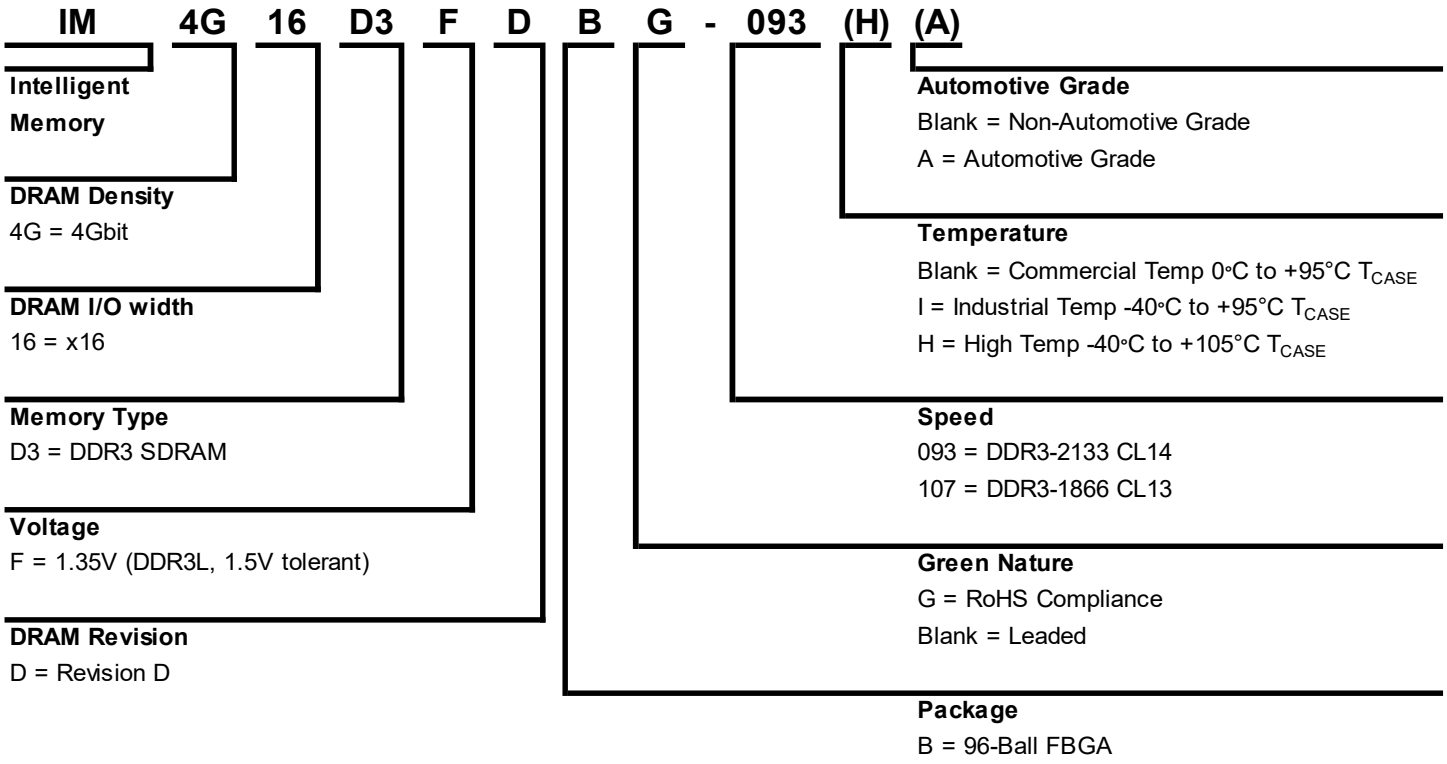
Option — *Marking*

- Capacity
  - 4Gbit — 4G
- DRAM I/O Width
  - x16 — 16
- Voltage
  - 1.35V (/1.5V) — F
- Package
  - 96-Ball FBGA — B
- RoHS Compliance
  - RoHS Compliance — G
  - Leaded — [Blank]
- Speed
  - DDR3-1866 (1.07ns) — 107
  - DDR3-2133 (0.938ns) — 093
- Temperature (T_{CASE})
  - Commercial Temperature (0℃ to 95℃) — [Blank]
  - Industrial Temperature (-40℃ to 95℃) — I
  - High Temperature (-40℃ to 105℃) — H
- Automotive Grade
  - Non-Automotive Grade — [Blank]
  - Automotive Grade — A

Version History

Version	History	Date	Remarks
1.0	First Release	Mar, 2020	
2.0	1. Remove “DDR3-1333”, “DDR3-1600” speed 2. Revise the Speed bin table of DDR3-1866 and DDR3-2133 3. Revise the Part Number Information 4. Revise Recommended DC Operating Condition	Feb, 2021	
3.0	1. Remove Automotive Grade 2. Update datasheet format	Nov,2022	
4.0	1. Add “High Temperature” and Automotive grade 2. Update datasheet format	Nov, 2024	
4.1	1. Revise the dimension drawing	Dec, 2024	

Part Number Information



DDR3 SDRAM Addressing

Configuration	DDR3
Memory Density	4Gbit
No of Bank	8
Bank address	BA0 ~ BA2
Row Address	A0 ~ A14
Column Address	A0 ~ A9
Page size	2KB

Pin Configuration

96-ball FBGA (x16 configuration)

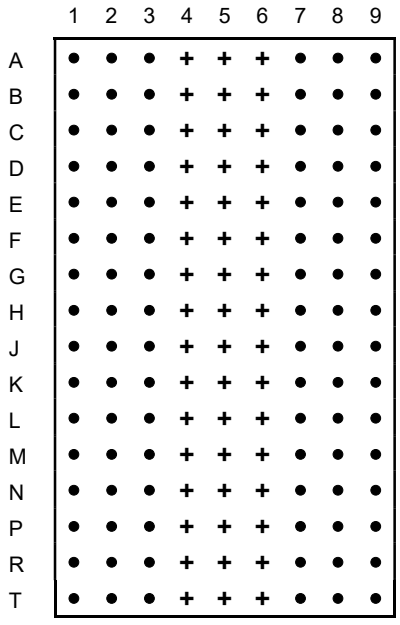
	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				DQSU#	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	DQSL#				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	RAS#				CK	V_{SS}	NC	J
K	ODT0	V_{DD}	CAS#				CK#	V_{DD}	CKE0	K
L	NC	CS0#	WE#				A10/AP	ZQ0	NC	L
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	RESET#	A13				A14	A8	V_{SS}	T

Top View

(See the ball through the package)

Ball Location (x16)

- ● Populated ball
- \+ Ball not populated



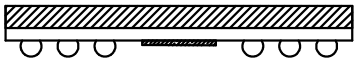
Signal Pin Description

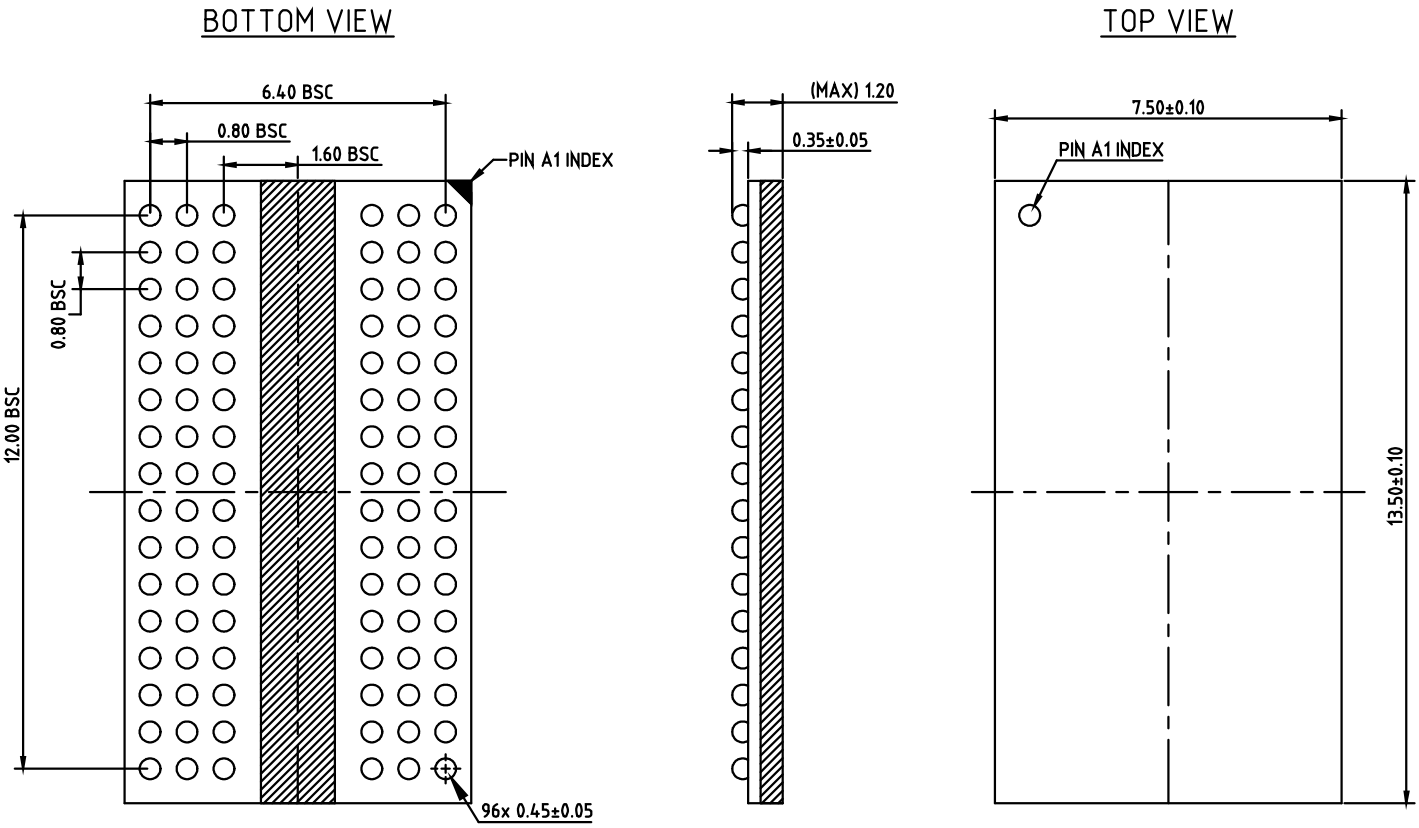
Pin	Type	Function
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	**Clock Enable**: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After V_{REFCA} and Internal DQ V_{REF} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	**Chip Select:** All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQSU, DQS#, DQSL, DQSL#, DMU and DML signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
RAS#, CAS#, WE#	Input	**Command Inputs:** RAS#, CAS# and WE# (along with CS#) define the command being entered.
DMU, DML	Input/ Output	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 ~ BA2	Input	**Bank Address Inputs :** BA0 – BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 ~ A14	Input	**Address Inputs:** Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Auto-precharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	**Burst Chop:** A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
DQU, DQL, DQU#, DQL#	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		**No connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.35V (1.283V ~ 1.45V); compatible to 1.5V±0.075V operation
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.35V (1.283V ~ 1.45V); compatible to 1.5V±0.075V operation
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference voltage for DQ**
V_{REFCA}	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**

Note: Input only pins (BA0-BA2, A0-12, RAS#, CAS#, WE#, CS#, CKE, ODT and RESET#) do not supply termination.

Package Diagram

96-Ball Fine Pitch Ball Grid Array Outline





Note: All dimensions are in millimeters.

1 IDD and IDDQ Specification Parameters and Test Conditions

1.1 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

Figure 1 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-average currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN ≤ VIL.AC(max).
- "1" and "HIGH" is defined as VIN ≥ VIH.AC(min).
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD}/2$.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 49 through Table 56 in JEDEC JESD79-3F.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting:

RON	=	RZQ/7 (34Ω in MR1)
Qoff	=	0_B (Output Buffer enabled in MR1)
RTT_Nom	=	RZQ/6 (40Ω in MR1)
RTT_WR	=	RZQ/2 (120Ω in MR2)

Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Define D = {CS#, RAS#, CAS#, WE#} = {HIGH, LOW, LOW, LOW}
- Define D# = {CS#, RAS#, CAS#, WE#} = {HIGH, HIGH, HIGH, HIGH}

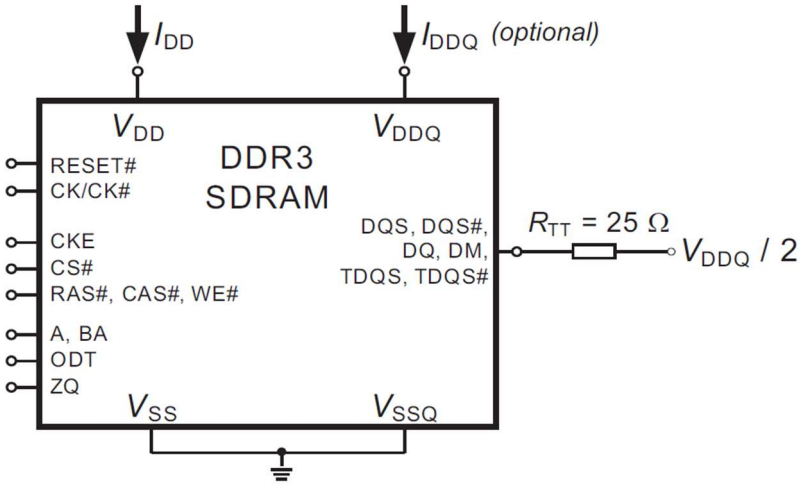


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ(optional) Measurements

Note:

1. DIMM level output test load condition may be different from above.

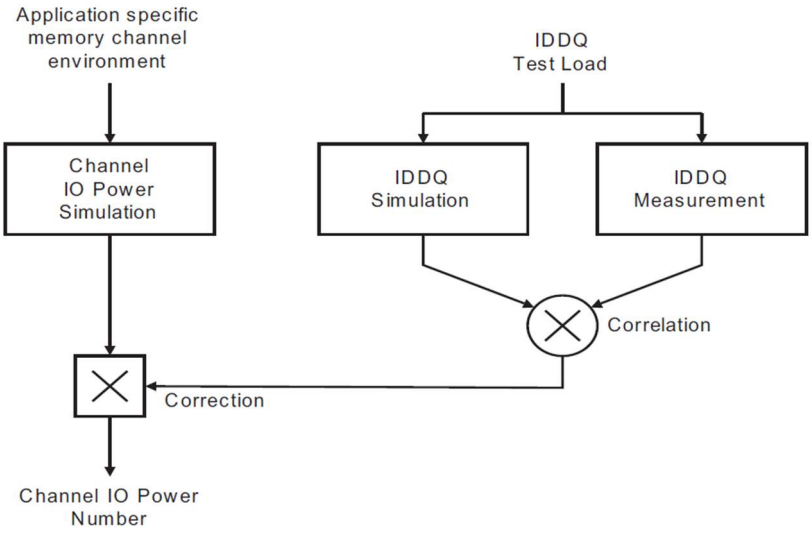


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 - Timing used for IDD and IDDQ Measured-Loop Patterns

Symbol		DDR3-1600	DDR3-1866	DDR3-2133	Unit
		11-11-11	13-13-13	14-14-14	
tCK		1.25	1.071	0.938	ns
CL		11	13	14	nCK
nRCD		11	13	14	nCK
nRC		39	45	50	nCK
nRAS		28	32	36	nCK
nRP		11	13	14	nCK
nFAW	1KB Page size	24	26	27	nCK
	2KB Page size	32	33	38	nCK
nRRD	1KB Page size	5	5	6	nCK
	2KB Page size	6	6	7	nCK
nRFC 4Gb		208	243	279	nCK

Table 2 - Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** CKE: High; External clock: On; tCK, nRC, nRAS, CL: BL: 8[1]; AL: 0; CS#: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0.
IDD1	**Operating One Bank Active-Read-Precharge Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: BL: 8[1,7]; AL:0; CS#: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0.
IDD2N	**Precharge Standby Current** CKE: High; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0
IDD2NT	**Precharge Standby ODT Current** CKE: High; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL;DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: toggling
IDDQ2NT	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2P0	**Precharge Power-Down Current Slow Exit** CKE: Low; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pecharge Power Down Mode: Slow Exit[3]
IDD2P1	**Precharge Power-Down Current Fast Exit** CKE: Low; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pecharge Power Down Mode: Fast Exit[3]
IDD2Q	**Precharge Quiet Standby Current** CKE: High; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD3N	**Active Standby Current** CKE: High; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD3P	**Active Power-Down Current** CKE: Low; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD4R	**Operating Burst Read Current** CKE: High; External clock: On; tCK, CL: BL: 8[1,7]; AL: 0; CS#: High between RD; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one according to; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** CKE: High; External clock: On; tCK, CL: BL: 8[1]; AL: 0; CS#: High between WR; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one according to; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at HIGH

Symbol	Description
IDD5B	**Burst Refresh Current** CKE: High; External clock: On; tCK, CL, nRFC: BL: 8(1); AL: 0; CS#: High between REF; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL;DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0
IDD6	**Self Refresh Current: Normal Temperature Range** *T*CASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled(4); Self-Refresh Temperature Range (SRT): Normal(5); CKE: Low; External clock: Off; CK and CK#: LOW; CL: BL: 8(1); AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL;DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: MID-LEVEL
IDD6ET	**Self-Refresh Current: Extended Temperature Range (optional)** *T*CASE: 0 - 95°C; Auto Self-Refresh (ASR): Disabled(4); Self-Refresh Temperature Range (SRT): Extended(5); CKE: Low; External clock: Off; CK and CK#: LOW; CL: see Table 46 on page 141; BL: 8(1); AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL;DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: BL: 8(1,7); AL: CL-1; CS#: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0
IDD8	**RESET Low Current** RESET: LOW; External clock: Off; CK and CK#: LOW; CKE: FLOATING; CS#, Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.

Note:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_WR enable: set MR2 A[10,9] = 10B
3. Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
7. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

1.2 IDD Specifications

IDD Values are for full operating range of voltage and temperature unless otherwise noted.

Table 3 - IDD Specification for C-temp

Speed Grade Bin	DDR3-1600	DDR3-1866	DDR3-2133	Unit
Operating Temp	0°C ~ 95°C	0°C ~ 95°C	0°C ~ 95°C	
Voltage	1.35V	1.35V	1.35V	
Symbol	Max	Max	Max	
IDD0	57	59	61	mA
IDD1	81	84	87	mA
IDD2P0	8	8	8	mA
IDD2P1	14	16	18	mA
IDD2N	24	26	28	mA
IDD2NT	31	33	35	mA
IDD2Q	24	26	28	mA
IDD3P	26	28	30	mA
IDD3N	38	40	42	mA
IDD4R	155	165	175	mA
IDD4W	155	165	175	mA
IDD5B	235	242	249	mA
IDD6	12	12	12	mA
IDD6ET	16	16	16	mA
IDD7	190	200	210	mA
IDD8	10	10	10	mA

Note:

1. Some data retains the possibility of future updates.

Table 4 - IDD Specification for H-temp

Speed Grade Bin	DDR3-1600	DDR3-1866	Unit
Operating Temp	-40°C ~ 105°C	-40°C ~ 105°C	
Voltage	1.35V	1.35V	
Symbol	Max	Max	
IDD0	156	169	mA
IDD1	182	208	mA
IDD2P0	68	68	mA
IDD2P1	102	111	mA
IDD2N	111	117	mA
IDD2NT	124	130	mA
IDD2Q	111	117	mA
IDD3P	111	117	mA
IDD3N	143	150	mA
IDD4R	286	312	mA
IDD4W	286	312	mA
IDD5B	260	270	mA
IDD6	90	90	mA
IDD7	364	390	mA
IDD8	39	39	mA

Note:

1. Some data retains the possibility of future updates.

2 Functional Description

2.1 Simplified State Diagram

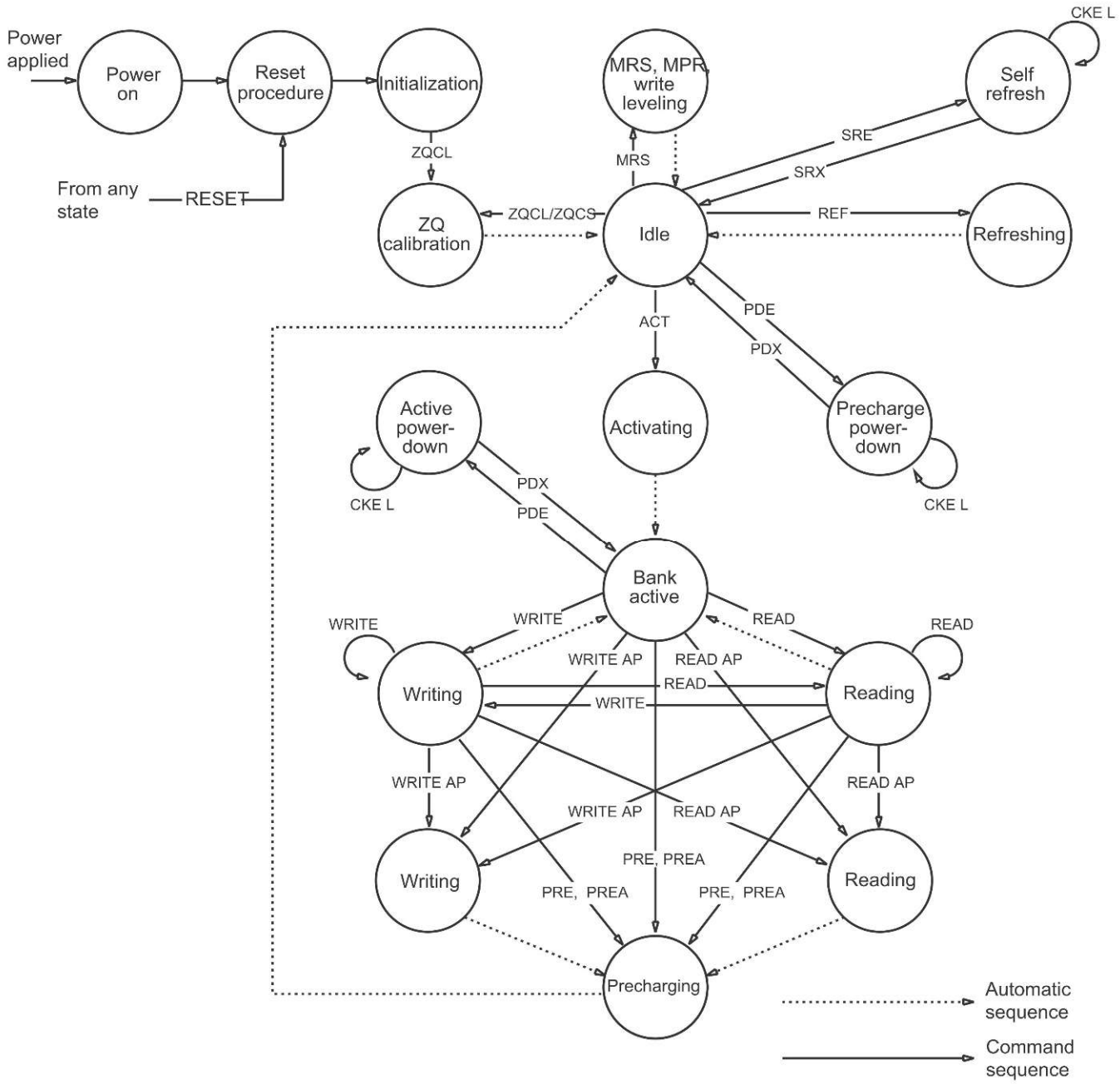


Figure 3 - Simplified State Diagram

Table 5 - State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA,RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

Note: See “Command Truth Table” for more details.

2.2 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" on page 15 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

2.3 RESET and Initialization Procedure

2.3.1 Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x V_{DD}; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to V_{DD}min must be no greater than 200 ms; and during the ramp, $V_{DD} > V_{DDQ}$ and (V_{DD} - V_{DDQ}) < 0.3 volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output,
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95 V max once power ramp is finished, AND
   - V_{REF} tracks V_{DDQ}/2.

   OR
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

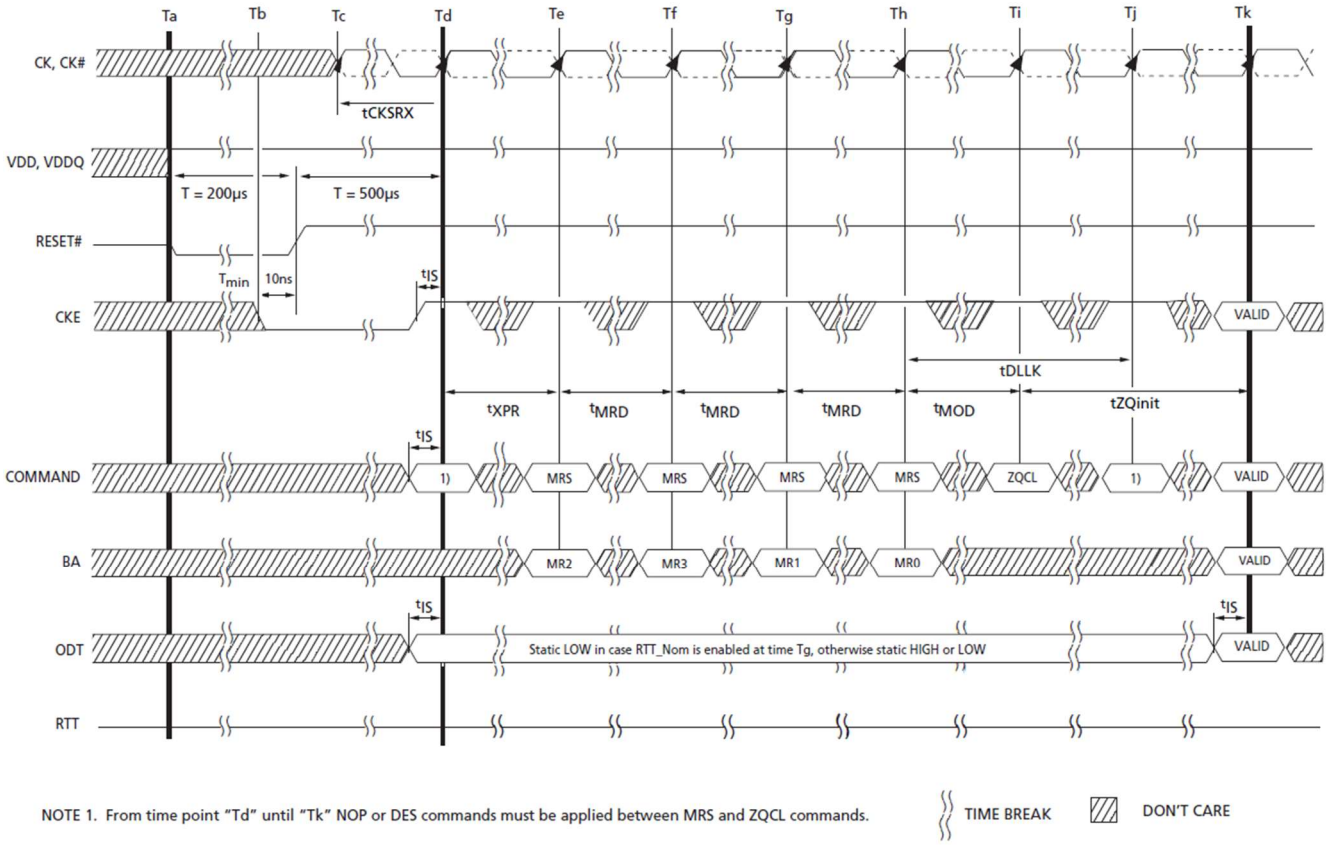


Figure 4 - Reset and Initialization Sequence at Power-on Ramping

2.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * V_{DD} anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled “LOW” before RESET being deasserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

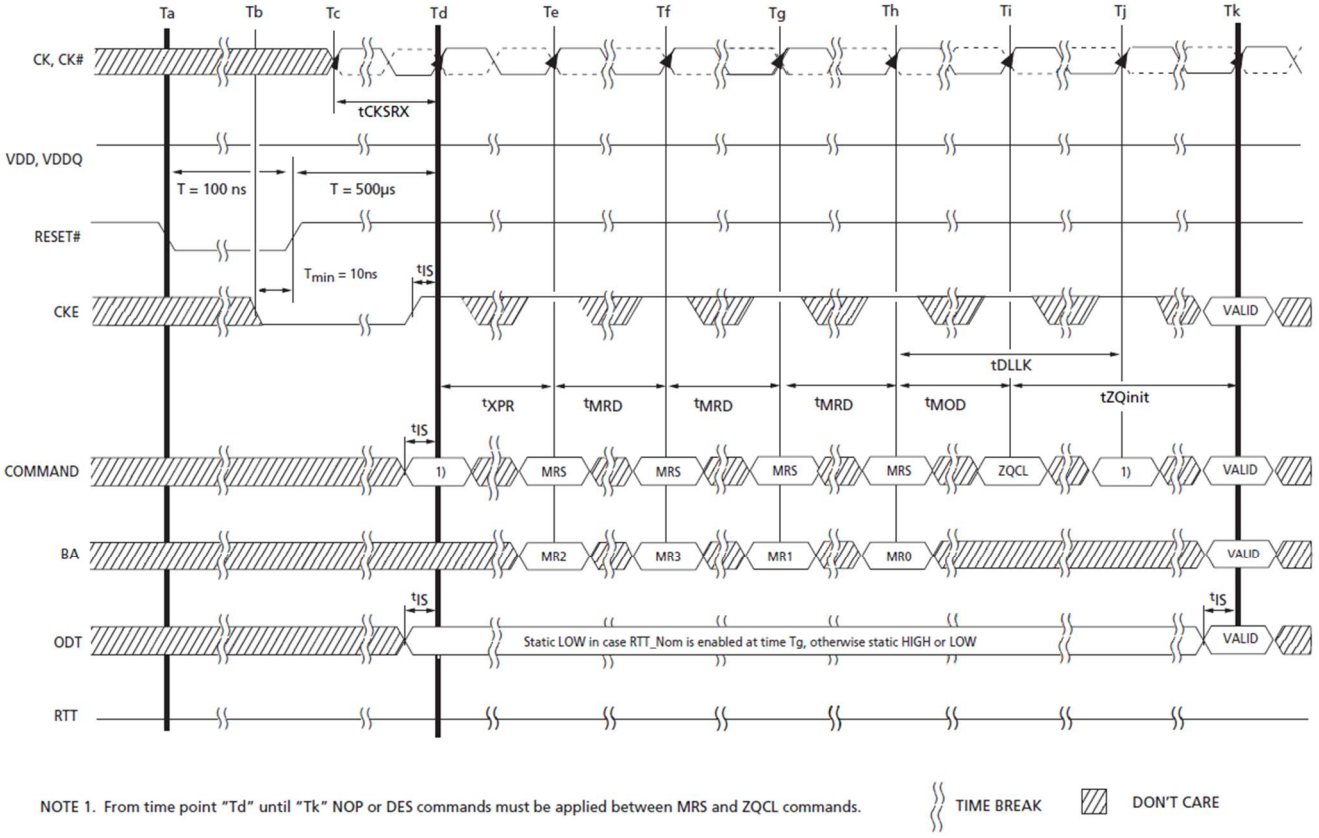


Figure 5 - Reset Procedure at Power Stable Condition

2.4 Register Definition

2.4.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 6.

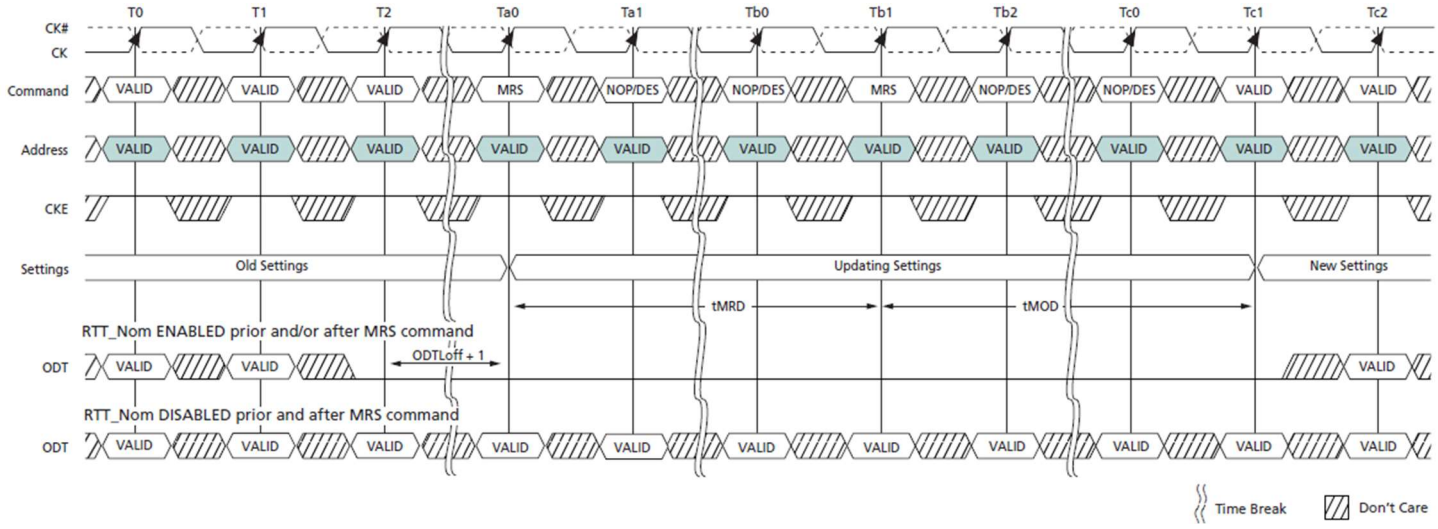


Figure 6 - tMRD timing

The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 7.

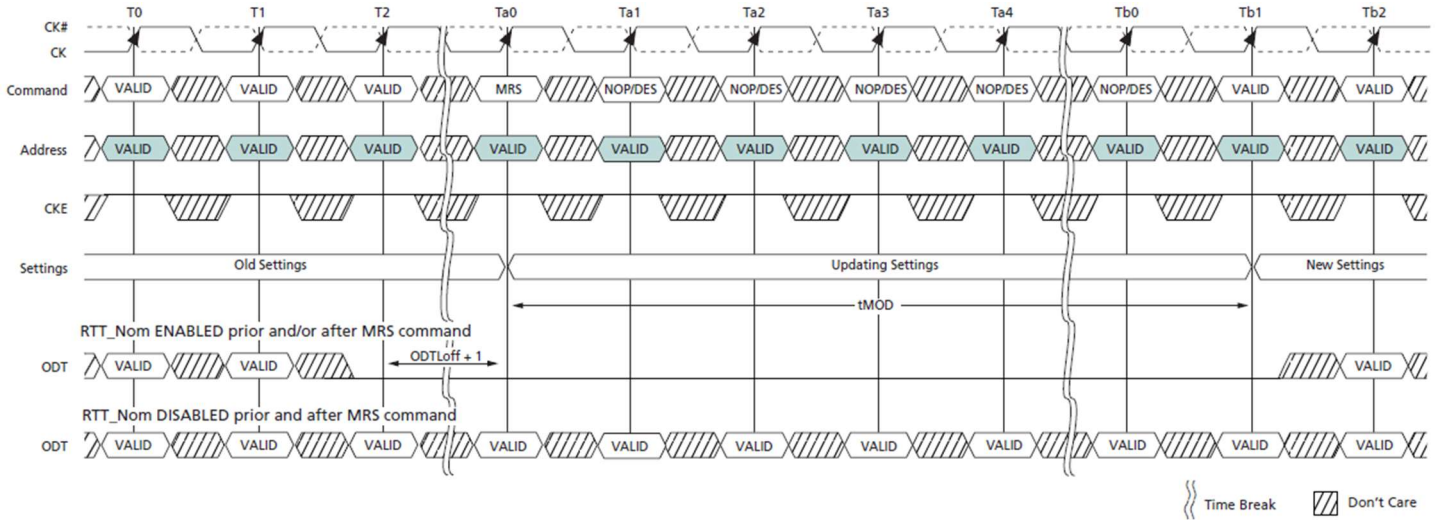


Figure 7 - tMOD timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

2.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to Figure 8.

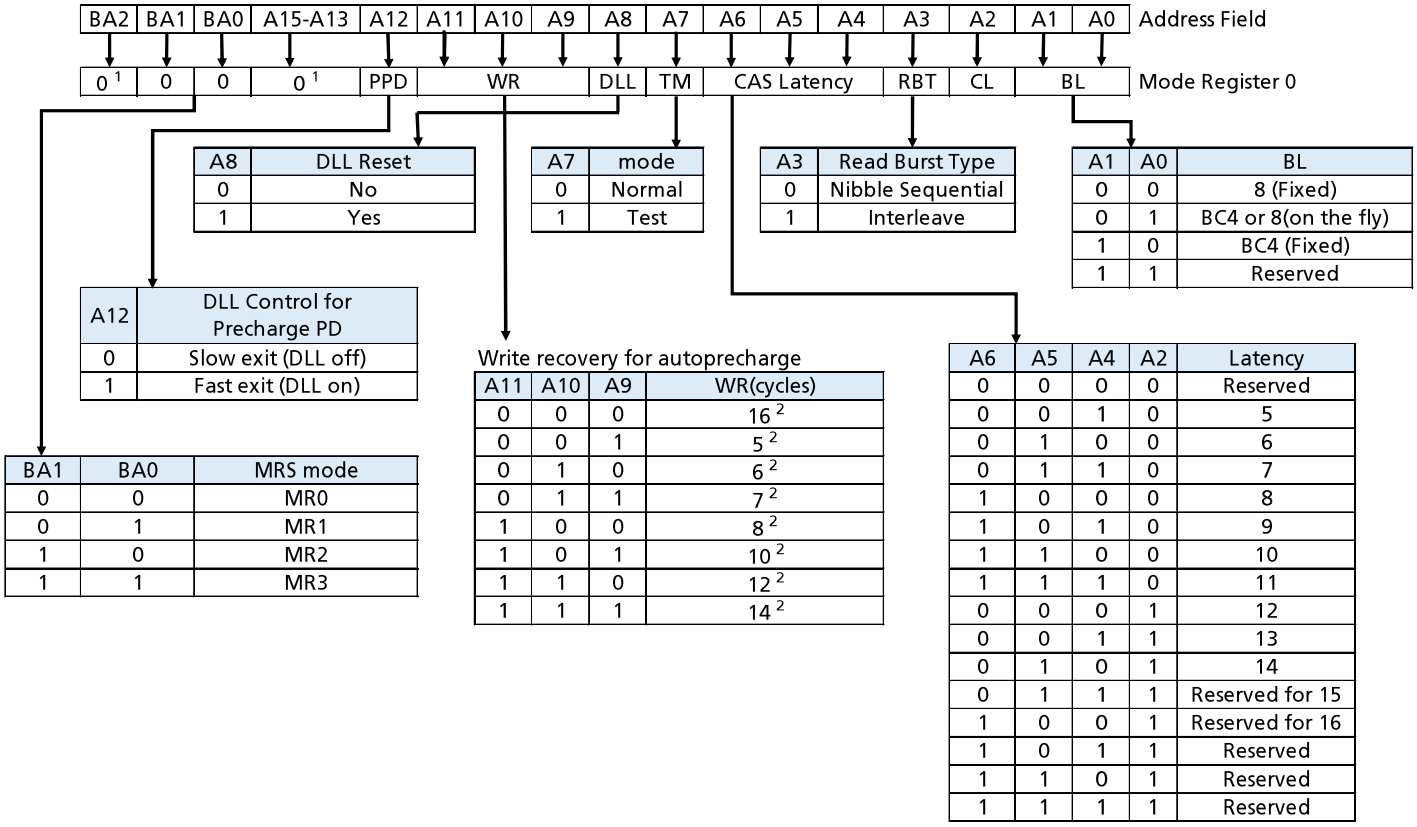


Figure 8 - MR0 Definition

Note:

1. BA2 and A13 ~ A15 are RFU and must be programmed to 0 during MRS.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency
4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

2.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 8. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 6. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Table 6 - Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A2, A1, A0)	Burst type = Sequential (Decimal) A3=0	Burst type = Interleaved (Decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0 V V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 V V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V V V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Note:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

2.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins". For detailed Read operation, refer to "READ Operation".

2.4.2.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 6. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

2.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

2.4.2.5 Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

2.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

2.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 9.

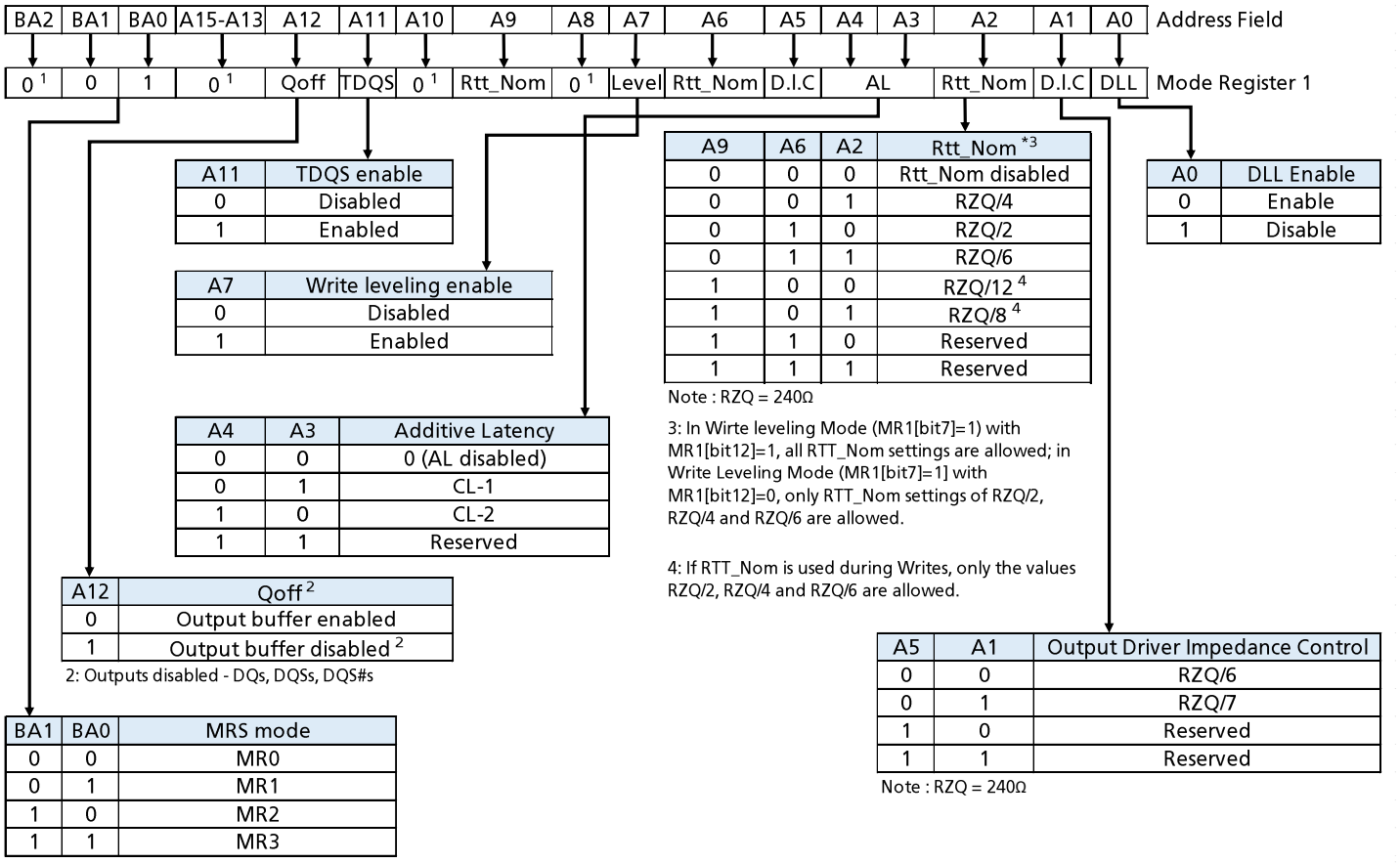


Figure 9 - MR1 Definition

Note: 1. BA2, A8, A10 and A13 ~ A15 are RFU and must be programmed to 0 during MRS.

2.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode”.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

2.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 9.

2.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

2.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 7.

Table 7 - Additive Latency (AL) Setting

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Note: AL has a value of CL-1 or CL-2 as per the CL values programmed in the MR0 register

2.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See section "Write Leveling" for more details.

2.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 9. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

2.4.3.7 TDQS, TDQS#

TDQS (Termination Data Strobe) is a feature of x8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/TDQS# pins that is applied to the DQS/DQS# pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. See Table 8 for details.

The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

Table 8 - TDQS, TDQS# Function Matrix

MR1 (A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	TDQS#

Note:
1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.
3. TDQS function is only available for X8 DRAM and must be disabled for x4 and x16.

2.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
																	Address Field
0 [1]	1	0	0 [1]			Rtt_WR		0 [1]	SRT	ASR	CWL			PASR [2]			Mode Register 2

A7	Self-refresh temperature range (SRT)
0	Normal operating temperature range
1	Extend (optional) operating temperature range

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A10	A9	Rtt_WR [2]
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0]= 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥2.5ns)
0	0	1	6 (2.5ns >tCK(avg) ≥1.875ns)
0	1	0	7 (1.875ns >tCK(avg) ≥1.5ns)
0	1	1	8 (1.5ns >tCK(avg) ≥1.25ns)
1	0	0	9 (1.25ns >tCK(avg) ≥1.07ns)
1	0	1	10 (1.07ns >tCK(avg) ≥0.935ns)
1	1	0	11 (0.935ns >tCK(avg) ≥0.833ns)
1	1	1	12 (0.833ns >tCK(avg) ≥0.75ns)

Figure 10 - MR2 Definition

Note:

1. BA2, A5, A8, A11 ~ 15 are RFU and must be programmed to 0 during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

2.4.4.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 10 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

2.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 10. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins”. For detailed Write operation refer to “WRITE Operation”.

2.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

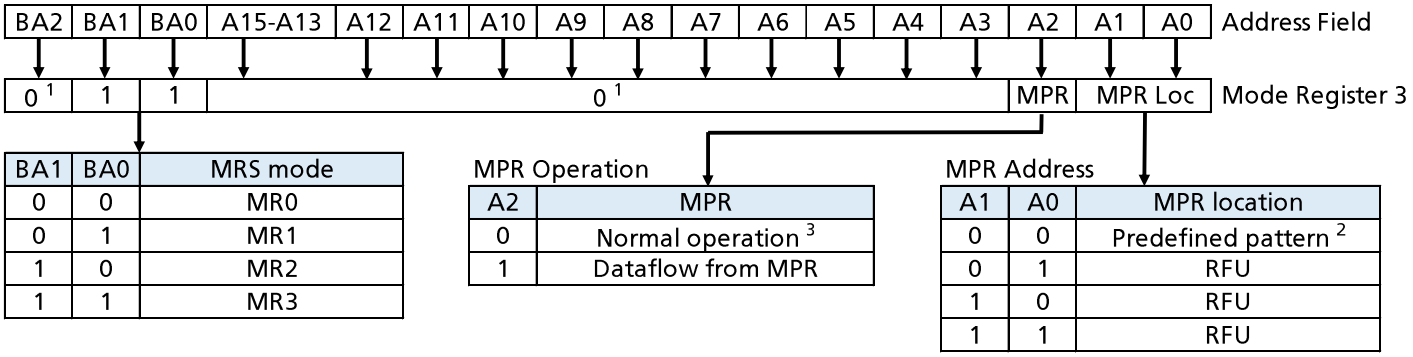
Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to “Extended Temperature Usage”. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

2.4.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT”.

2.4.5 Mode Register MR3

The Mode Register MR3 controls multi-purpose registers. Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

MPR Operation

A2	MPR
0	Normal operation [3]
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern [2]
0	1	RFU
1	0	RFU
1	1	RFU

Figure 11 - MR3 Definition

Note:

1. BA2, A3 ~ A15 are RFU and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

2.4.5.1 Multi-Purpose Register (MPR)

The Multi-Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi-Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to “Multi-Purpose Register”.

3 DDR3 SDRAM Command Description and Operation

3.1 Command Truth Table

a. Note 1,2,3 and 4 apply to the entire Command Truth Table.

b. Note 5 applies to all Read/Write commands.

[BA = Bank Address, RA = Row Address, CA = Column Address, BC# = Burst Chop, X = Don't Care, V = Valid]

Table 9 - Command Truth Table

Function	Abbrev	CKE		CS#	RAS#	CAS#	WE#	BA0 - BA2	A13 - A15	A12/ BC#	A10/ AP	A0 - A9,A11	Note
		Previous cycle	Current cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 / BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 / BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 / BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 / BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Note:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.

9. V_{REF}(Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. V_{REFDQ} supply may be turned OFF and V_{REFDQ} may take any value between V_{SS} and V_{DD} during Self Refresh operation, provided that V_{REFDQ} is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

3.2 CKE Truth Table

a. Note 1-7 apply to the entire CKE Truth Table.
b. For Power-down entry and exit parameters, see “Power Down Modes”.
c. CKE low is allowed only if tMRD and tMOD are satisfied.

Table 10 - CKE Truth Table

Current State[2]	CKE		Command (N)[3] RAS#,CAS#,WE#,CS#	Action (N)[3]	Note
	Previous Cycle [1] (N-1)	Current Cycle [1] (N-1)			
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Bank Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Sellf-Refresh	9,13,18
For more detail with all signals, see “Command Truth Table”.					10

Note:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh cannot be entered during Read or Write operations. For a detailed list of restrictions See “Self-Refresh Operation” and see “Power-Down Modes”.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around V_{REF}) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation. V_{REFDQ} supply may be turned OFF and V_{REFDQ} may take any value between V_{SS} and V_{DD} during Self Refresh operation, provided that V_{REFDQ} is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

3.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

3.4 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

3.5 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for susequent operations until A0 bit is set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change”.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram (CL=6, BL=8):

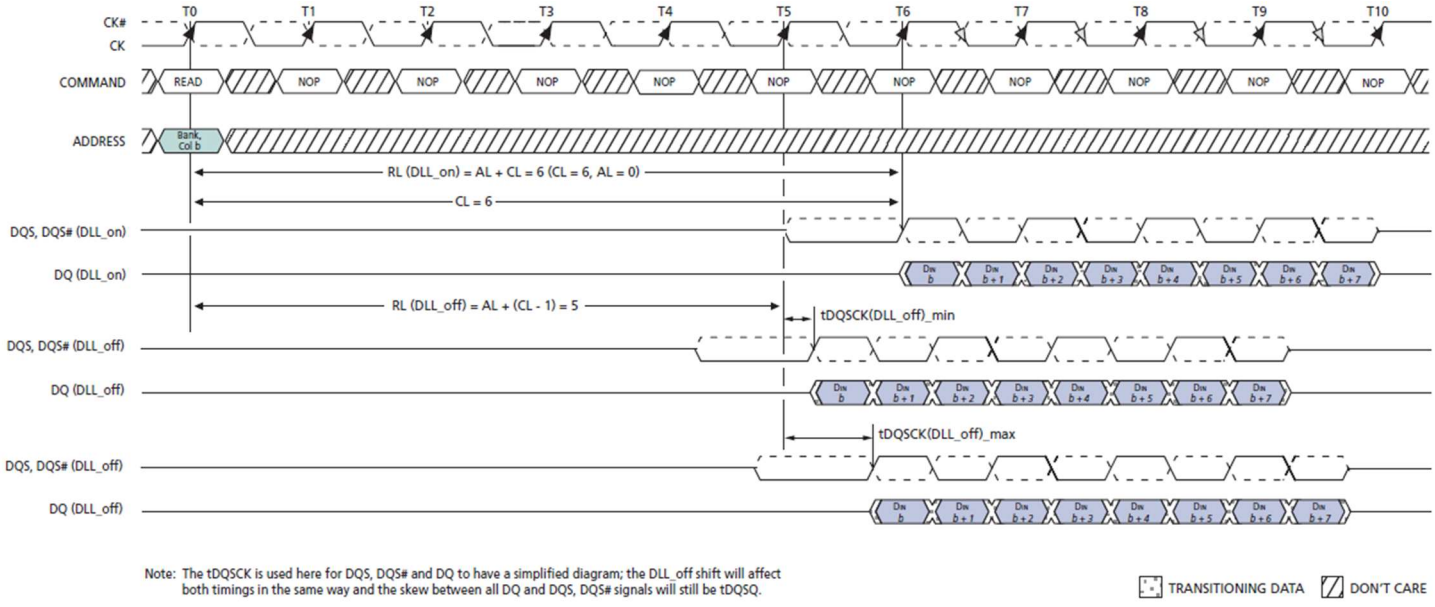


Figure 12 - DLL-off mode READ Timing Operation

3.6 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit is set back to “0”.

3.6.1 DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with “Input clock frequency change”.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.

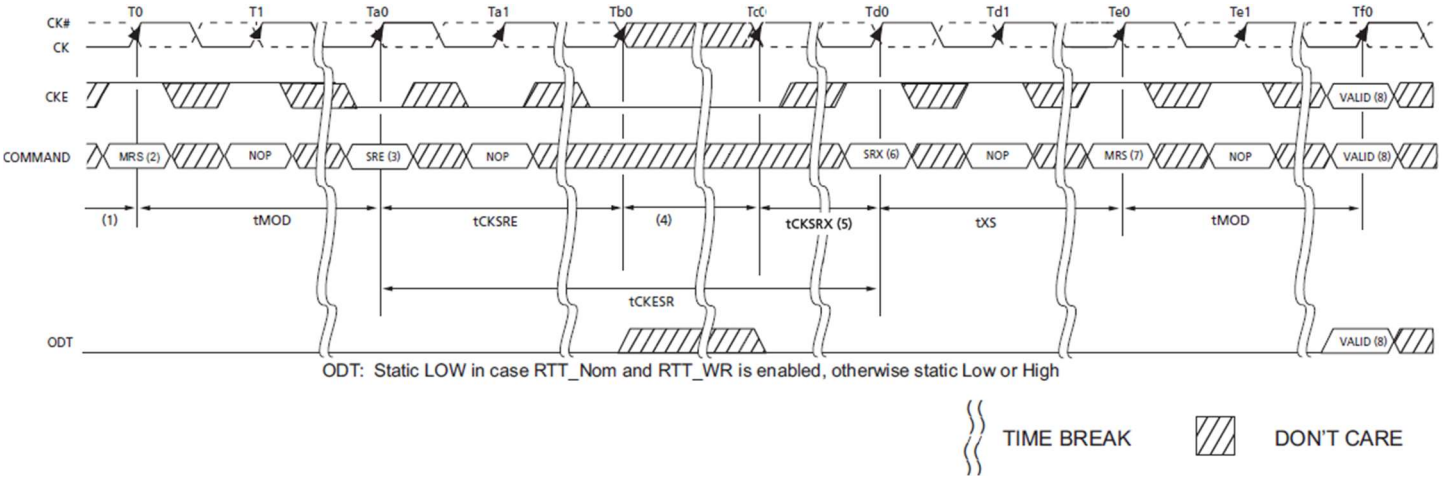


Figure 13 - DLL Switch Sequence from DLL-on to DLL-off

Note:

1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

3.6.2 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change".
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to “0” to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

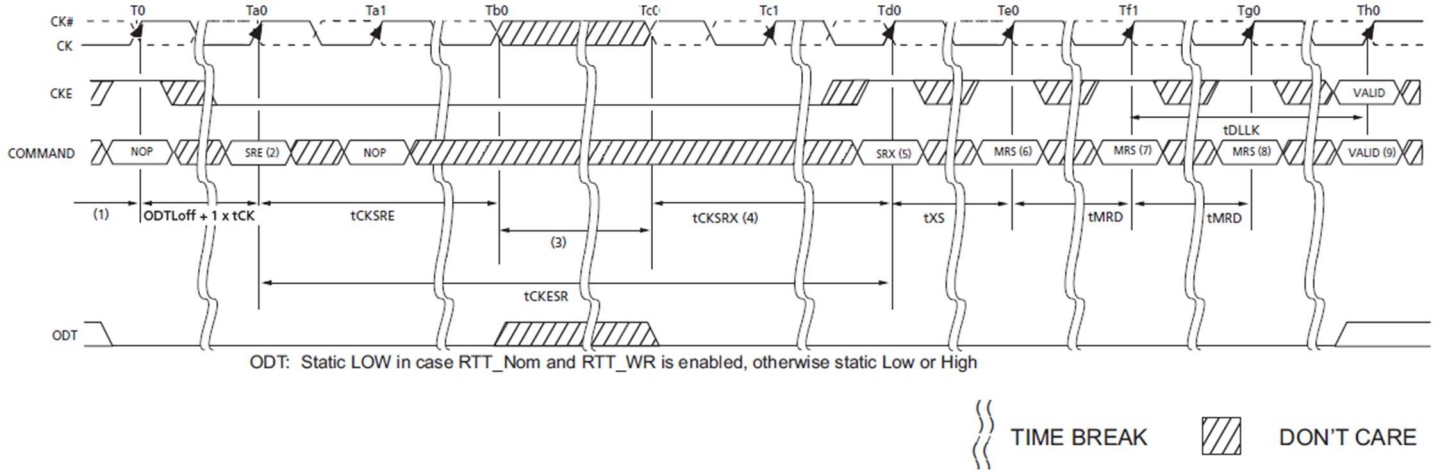


Figure 14 - DLL Switch Sequence from DLL-off to DLL-on

Note:

1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL on by MR1 A0 = 0
7. Start DLL Reset by MR0 A8 = 1
8. Update Mode registers
9. Any valid command

3.7 Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed into Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See “Self-Refresh Operation”. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to “DLL on/off switching procedure”.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 15.

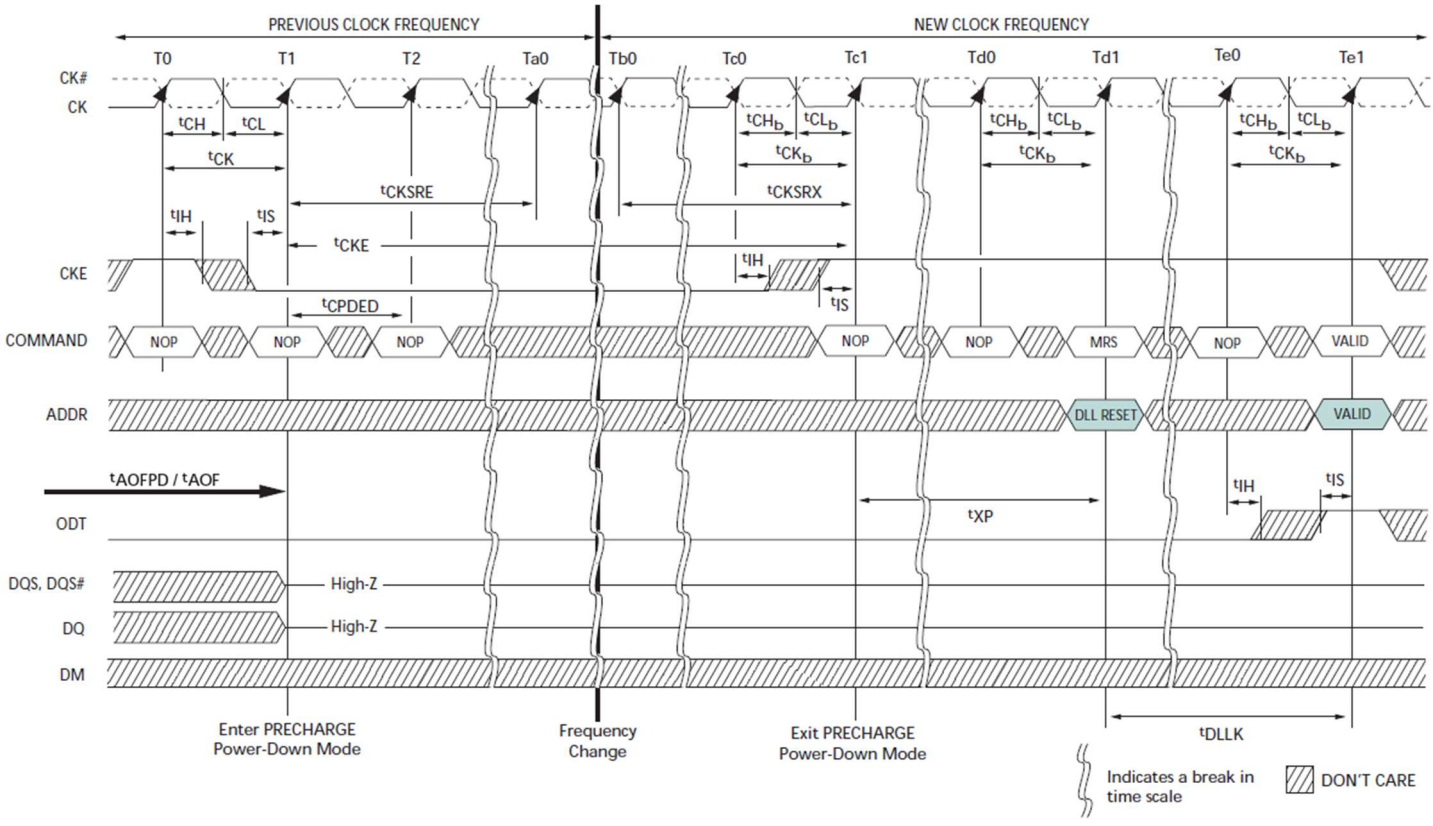


Figure 15 - Change Frequency during Precharge Power-down

Note:

1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down.
2. tAOFPD and tAOF must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements.
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 12. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case

3.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS-DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS-DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 16.

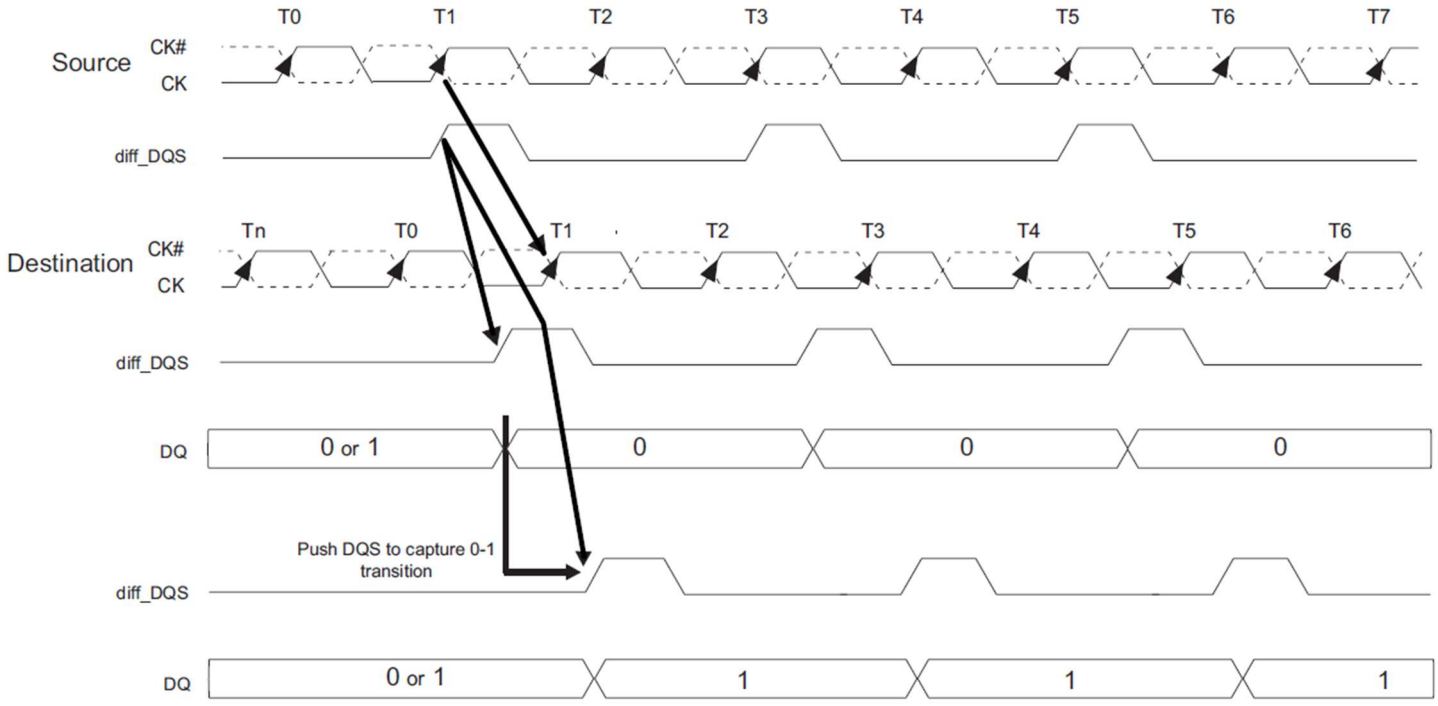


Figure 16 - Write Leveling Concept

DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

3.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 11). Note that in write leveling mode, only DQS/DQS# terminations are activated and deactivated via ODT pin, unlike normal operation (Table 12).

Table 11 - MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 12 - DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/DQS# termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

Note: In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

3.8.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5, and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after tWLO timing. Either one or all data bits ("prime DQ bit(s)") provide the leveling feedback. The DRAM's remaining DQ bits are driven Low statically after the first sampling procedure. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device Figure 17 describes the timing diagram and parameters for the overall Write Leveling procedure.

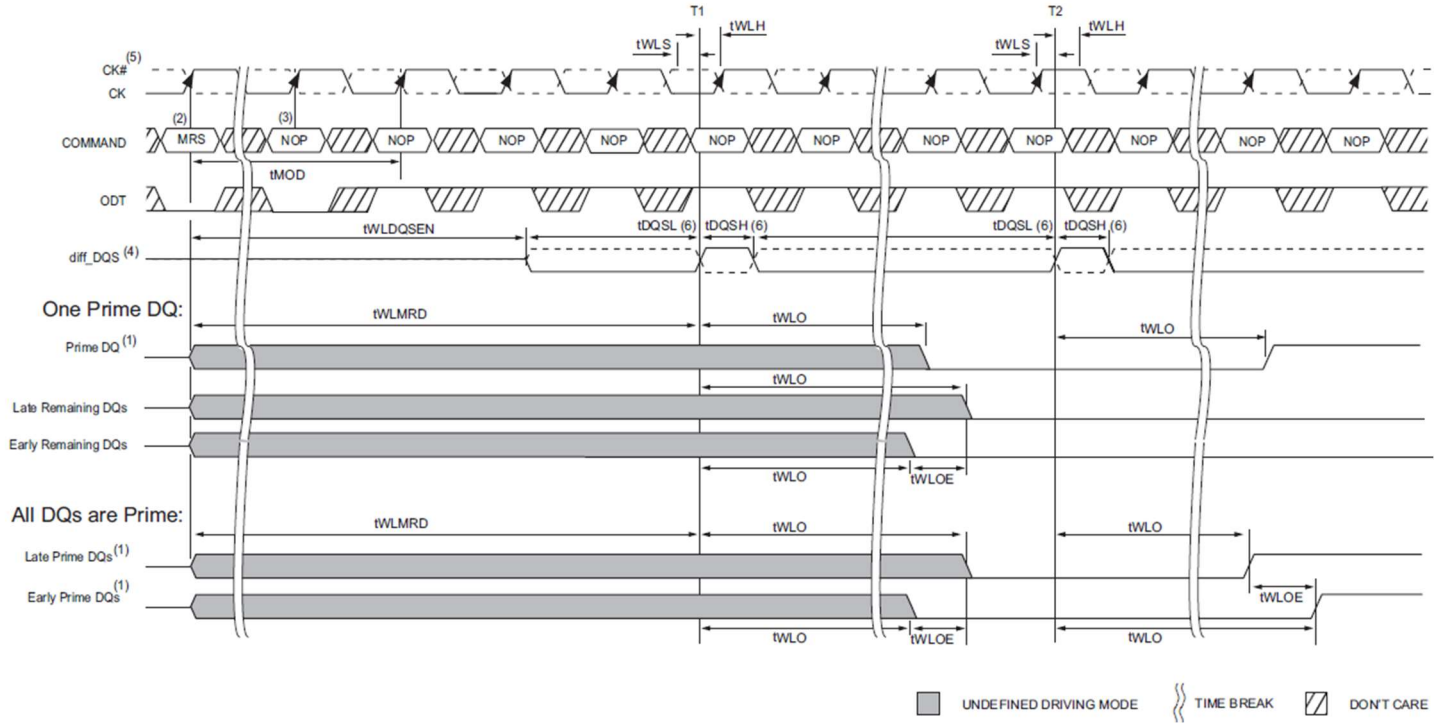


Figure 17 - Timing detail for Write leveling sequence [DQS-DQS# is capturing CK-CK# low at T1 and CK-CK# high at T2

Note:

1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or Deselect.
3. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

3.8.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

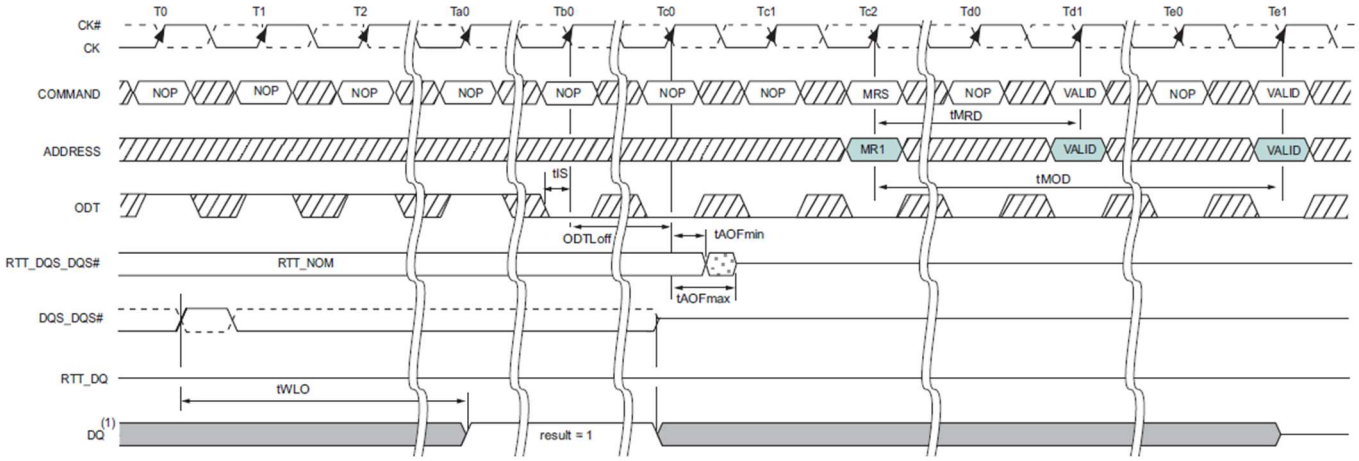


Figure 18 - Timing detail for Write leveling exit

Note:

1. The DQ result = 1 between Ta0 and Tc0 is a result of DQS DQS# signals capturing CK high just after the T0 state.
2. Refer to Figure 11 for specific tWLO timing.

3.9 Extended Temperature Usage

Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material:

a. Auto Self-refresh supported
b. Extended Temperature Range supported
c. Double refresh required for operation in the Extended Temperature Range (applies only for devices supporting the Extended Temperature Range)

Table 13 - Mode Register Description

Field	Bits	Description
ASR	MR2 (A6)	**Auto Self-Refresh (ASR) (Optional)** when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate T_{OPER} during subsequent Self-Refresh operation 0 = Manual SR Reference (SRT) 1 = ASR enable (optional)
SRT	MR2 (A7)	**Self-Refresh Temperature (SRT) Range** If ASR = 0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

3.9.1 Auto Self-Refresh mode - ASR Mode (optional)

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1b and MR2 bit A7 = 0b. The DRAM will manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0b.

If the ASR mode is not enabled (MR2 bit.A6 = 0b), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Please refer to the supplier data sheet and/or the DIMM SPD for Extended Temperature Range and Auto Self-Refresh option availability.

3.9.2 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = 0b, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = 0b, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = 1b then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0b and the DRAM should not be operated outside the Normal Temperature Range.

Table 14 - Self Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 ~ 85°C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal & Extended (0 ~ 95°C)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 ~ 85°C)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent	Normal & Extended (0 ~ 95°C)
1	1	Illegal	-

3.10 Multi-Purpose Register

The Multi-Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 19.

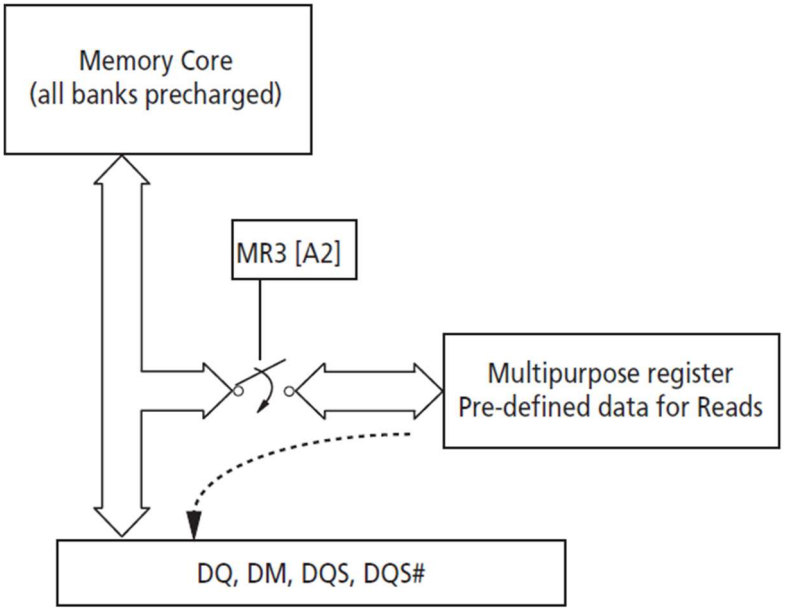


Figure 19 - MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 12. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi-Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 13. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 15 - MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	Don't Care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	Table 14	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

3.10.1 MPR Function Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
  - DQ[0] drives information from MPR.
  - DQ[3:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x8:
  - DQ[0] drives information from MPR.
  - DQ[7:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x16:
  - DQL[0] and DQU[0] drive information from MPR.
  - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *)
  - A[2]=1b, Burst order: 4,5,6,7 *)
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11, A13,... (if available): don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

Note: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

3.10.2 MPR Register Address Definition

Table 16 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi-Purpose Register Read.

Table 16 - MPR MR3 Register Address Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order: 0,1,2,3,4,5,6,7 Pre-defined Data Pattern: [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order: 0,1,2,3 Pre-defined Data Pattern: [0,1,0,1]
			BC4	100b	Burst order: 4,5,6,7 Pre-defined Data Pattern: [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7

Note: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

3.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi-Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to “Electrical Characteristics & AC Timing for DDR3-800 to DDR3-2133”.

3.10.4 Protocol Example

Read out predetermined read-calibration pattern. (This is one example)

Description: Multiple reads from Multi-Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode “A2 = 1b“ and “A[1:0] = 00b“
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
  - A[1:0] = ‘00’b (Data burst order is fixed starting at nibble, always 00b here)
  - A[2] = ‘0’b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12/BC = 1 (use regular burst length of 8)
  - All other address pins (including BA[2:0] and A10/AP): don’t care
- After RL = AL + CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode “A2 = 0b“ and “A[1:0] = valid data but value are don’t care“
- All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with “regular” DRAM commands, like activate a memory bank for regular read or write access,...

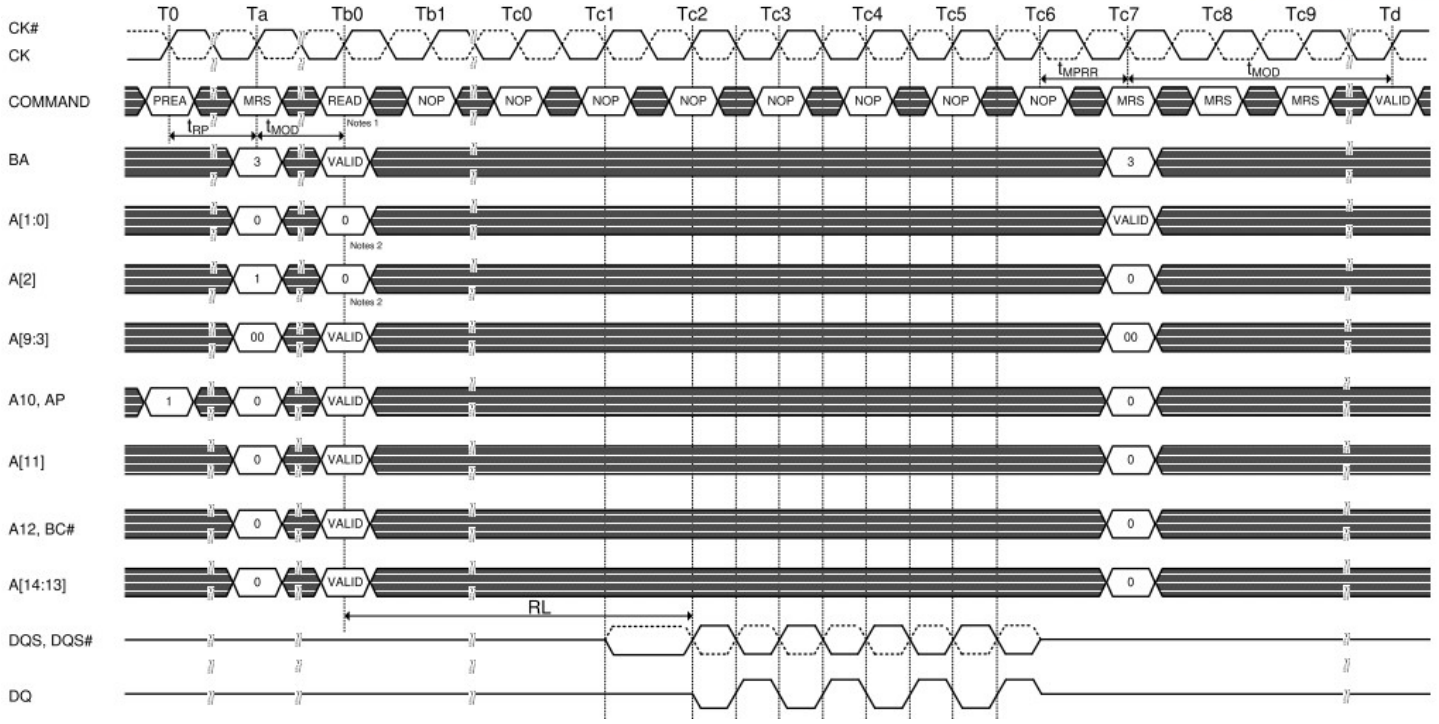


Figure 20 - MPR Readout of predefined pattern, BL8 fixed burst order, single readout

TIME BREAK Don't Care

Note:

1. RD with BL8 either MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

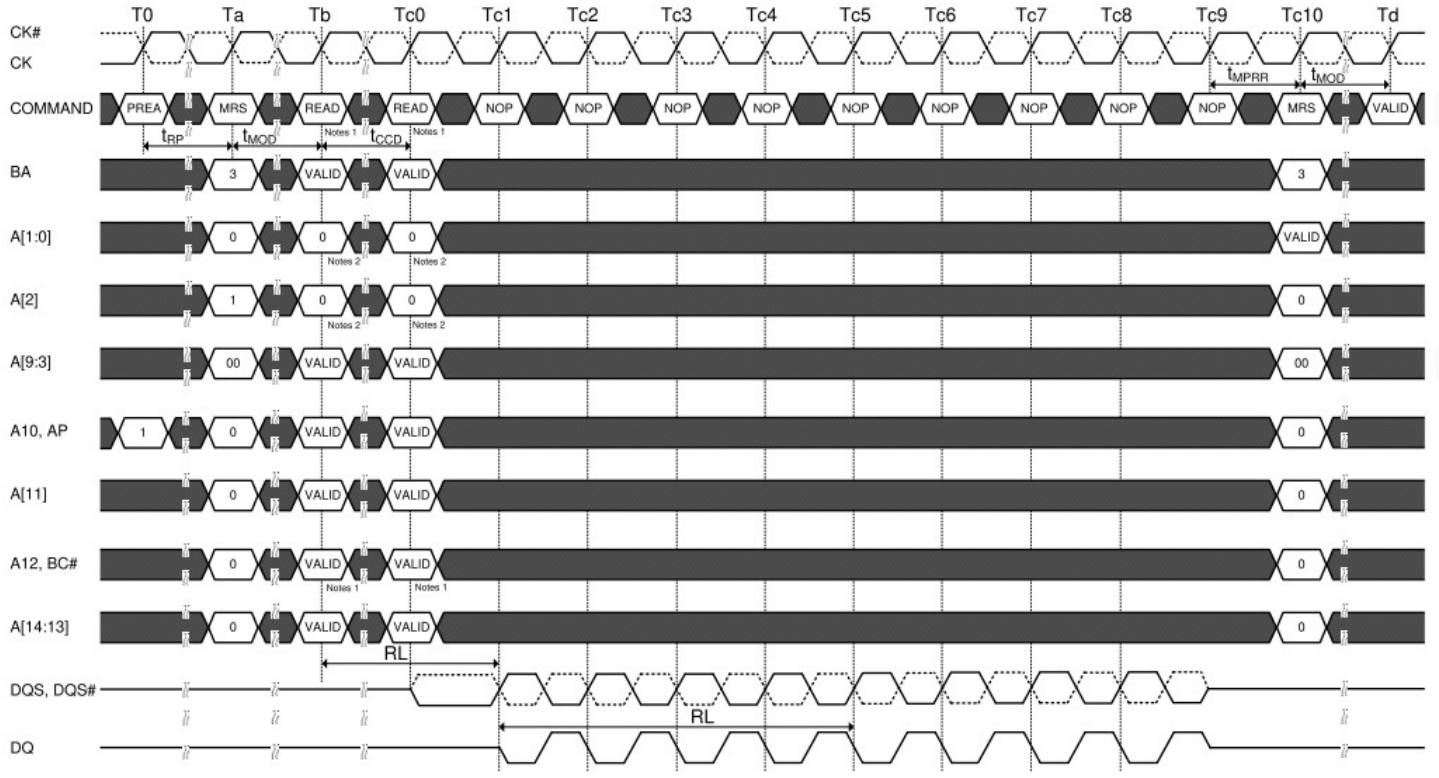


Figure 21 - MPR Readout of predefined pattern, BL8 fixed burst order, back to back readout

TIME BREAK Don't Care

Note:

1. RD with BL8 either MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

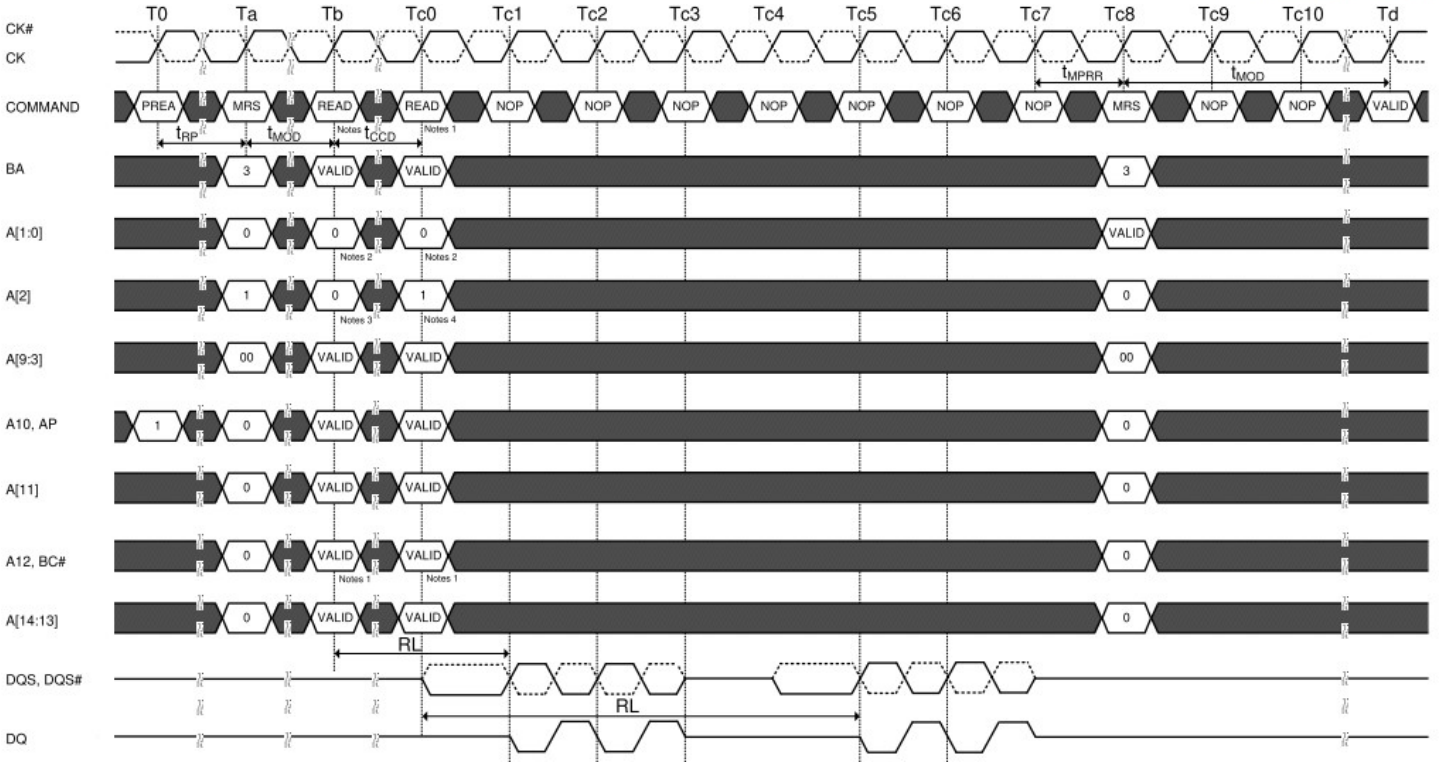


Figure 22 - MPR Readout of predefined pattern, BC4 lower nibble then upper nibble

TIME BREAK Don't Care

Note:

1. RD with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0]
3. A[2]=0 selects lower 4 nibble bits 0…3.
4. A[2]=1 selects upper 4 nibble bits 4…7.

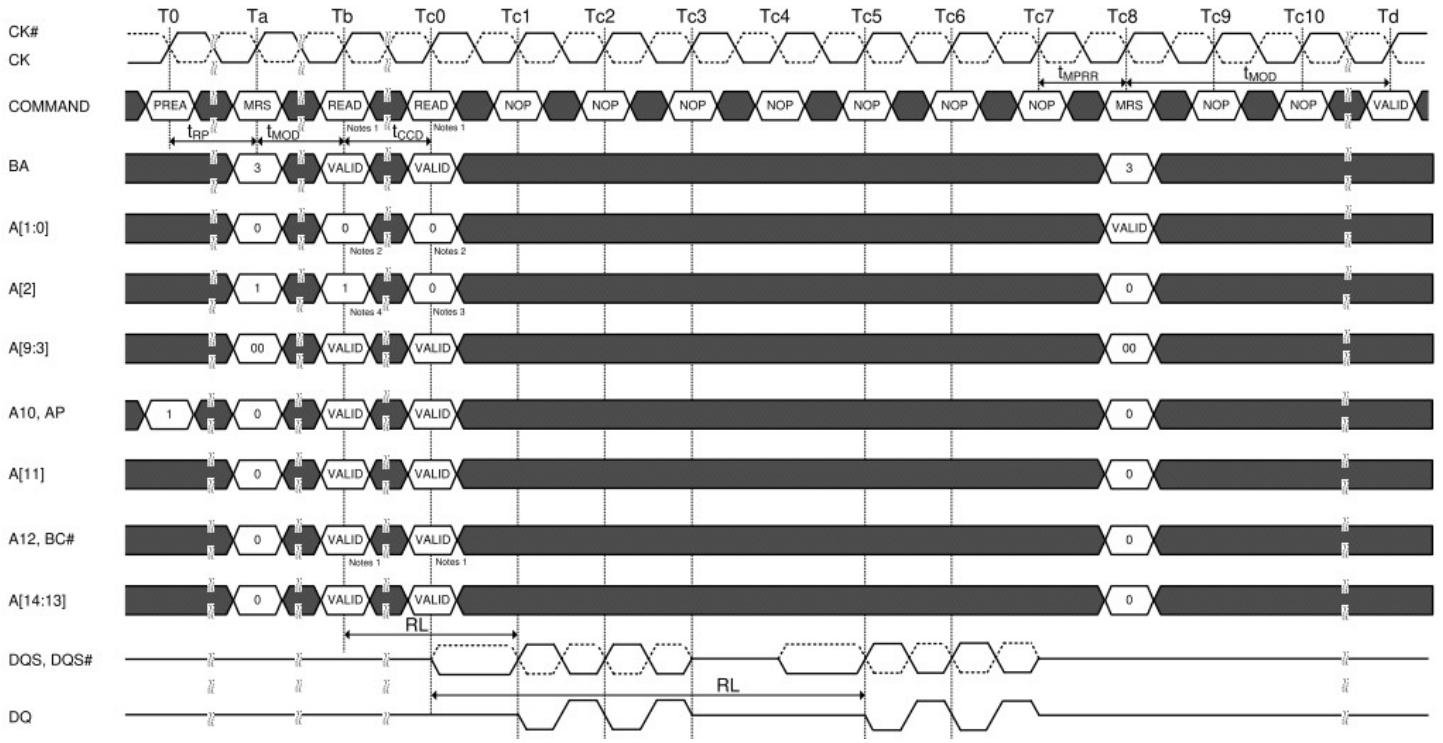


Figure 23 - MPR Readout of predefined pattern, BC4 upper nibble then lower nibble

TIME BREAK Don't Care

Note:

1. RD with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0]
3. A[2]=0 selects lower 4 nibble bits 0…3.
4. A[2]=1 selects upper 4 nibble bits 4…7.

3.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

3.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

3.13 READ Operation

3.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
A12 = 1, BL8
A12 is used only for burst length control, not as a column address.

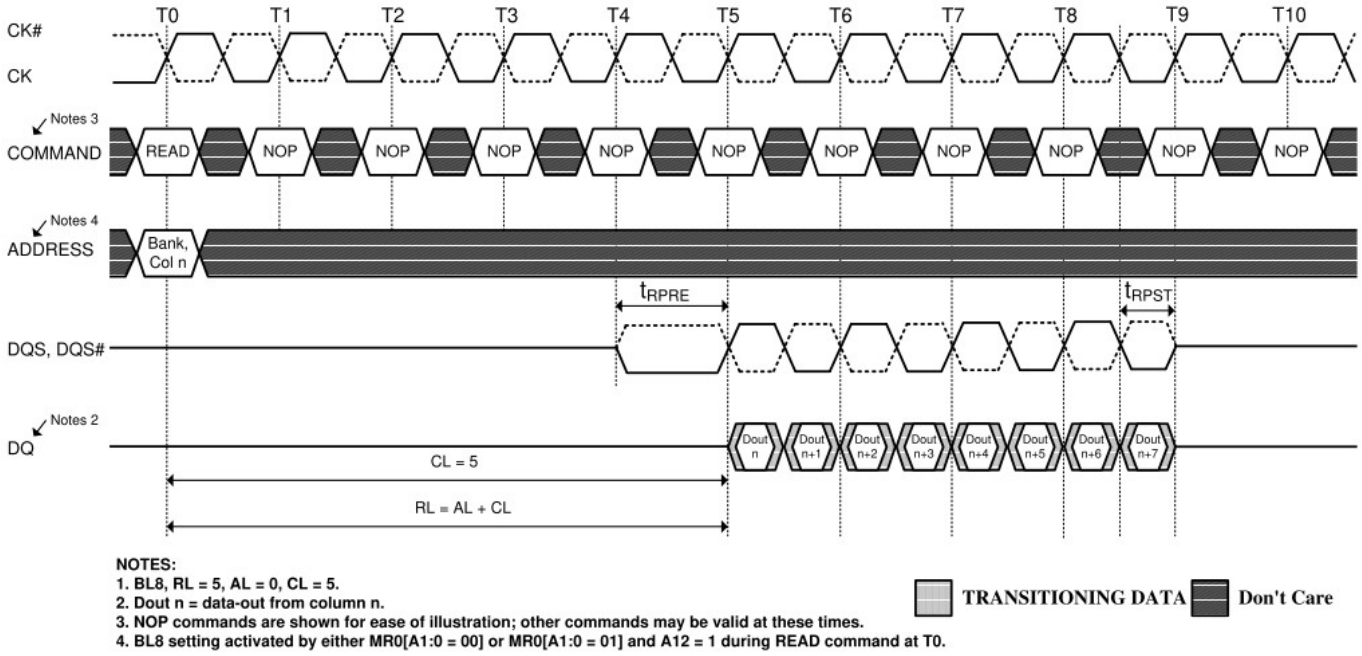


Figure 24 - READ Burst Operation RL=5 (AL=0, CL=5, BL8)

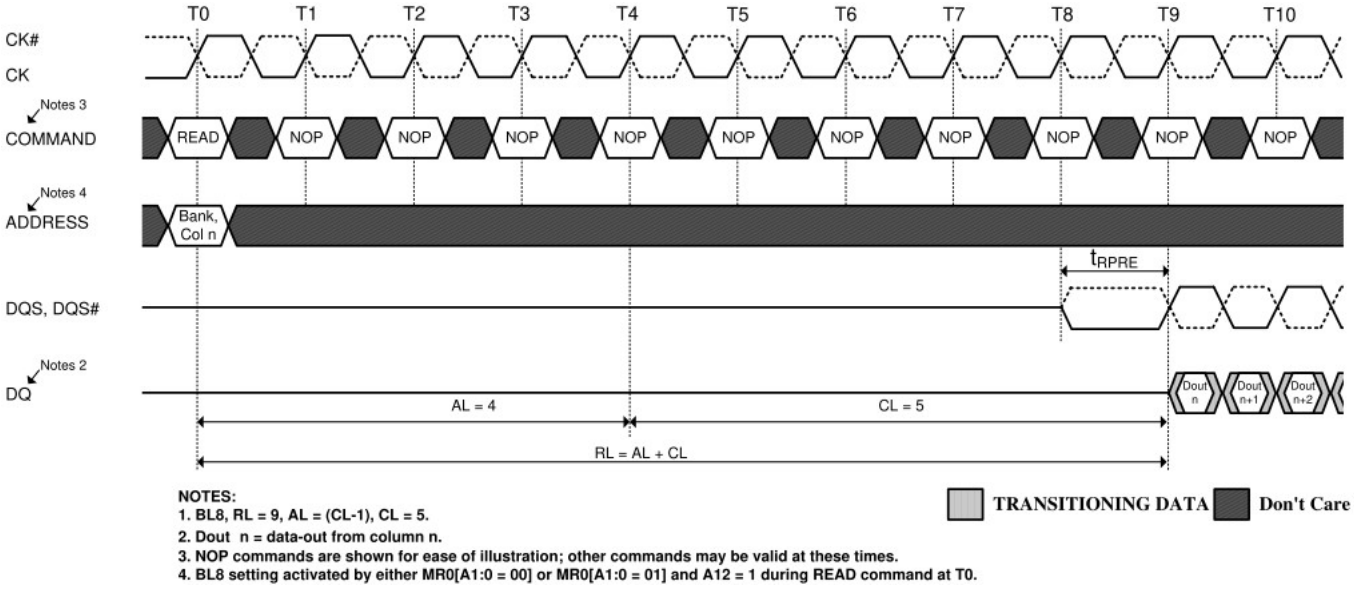


Figure 25 - READ Burst Operation RL=9 (AL=4, CL=5, BL8)

3.13.2 READ Timing Definitions

Read timing is shown in Figure 26 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the DQS, DQS# differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, DQS# differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined.

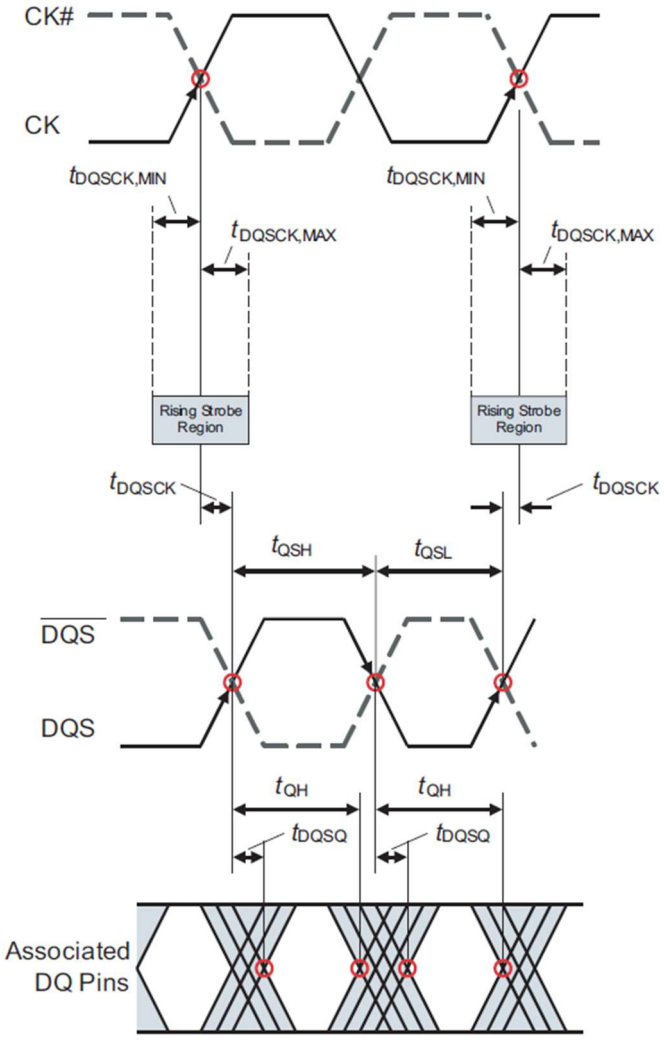


Figure 26 - READ Timing Definition

3.13.2.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 27 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS), tHZ(DQS) for preamble/postamble

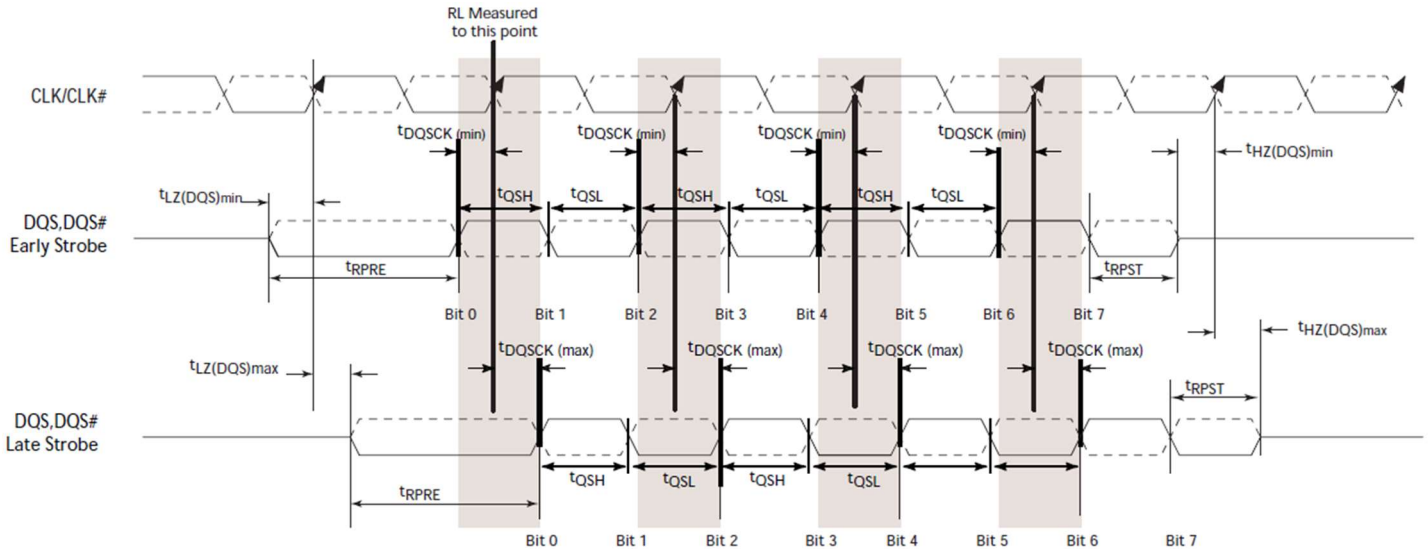


Figure 27 - Clock to Data Strobe Relationship

Note:

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:
   if tDQSCK(n+1) < 0
   tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - | tDQSCK(n+1) |
3. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
4. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).
5. The minimum pulse width of read preamble is defined by tRPRE(min).
6. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
7. The minimum pulse width of read postamble is defined by tRPST(min).
8. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

3.13.2.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 28 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined.

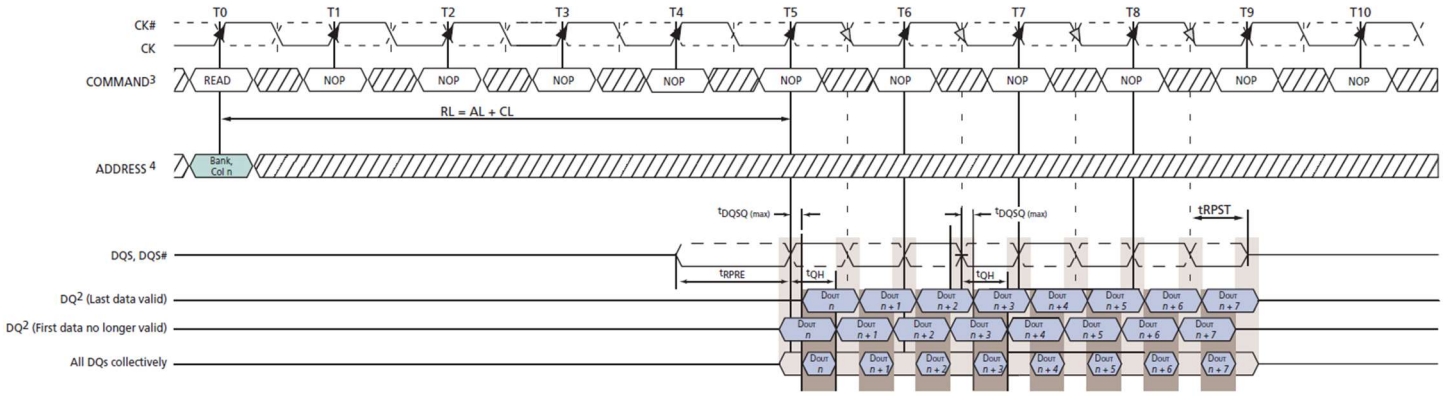


Figure 28 - Data Strobe to Data Relationship

Note:

1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS,DQS# to Data and does not define DQS,DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

4.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 30 shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

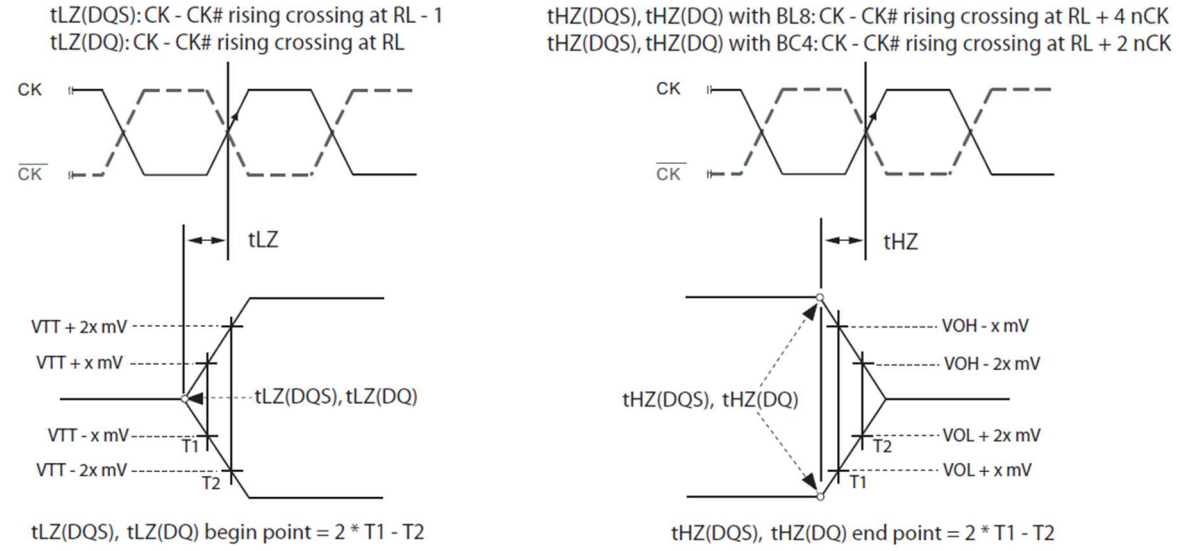


Figure 29 - tLZ and tHZ method for calculating transitions and endpoints

3.14 WRITE Operation

3.14.1 DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
A12 = 1, BL8
A12 is used only for burst length control, not as a column address.

3.14.2 WRITE Timing Violations

3.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain minor violations, that the DRAM is guaranteed not to “hang up,” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

3.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command.

3.14.2.3 Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

3.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge)

3.14.2.5 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, consistent with the implementation on DDR2 SDRAMs. It has identical timings on write operations as the data bits, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM of x8 bit organization can be used as TDQS during write cycles if enabled by the MR1[A11] setting. See “TDQS, TDQS#” on for more details on TDQS vs. DM operations.

3.15 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS#, RAS# and CAS# are held Low and WE# High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min). Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI. At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI. Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

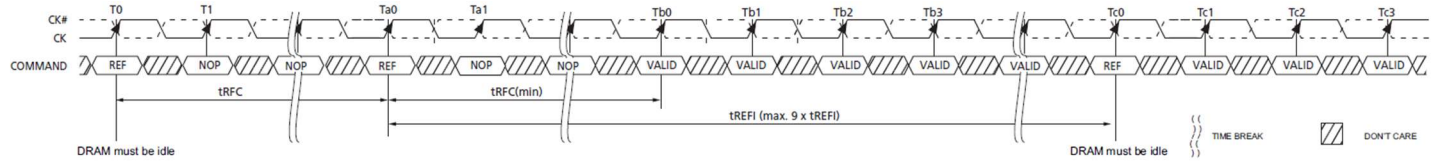


Figure 30 - Refresh Command Timing

Note:

1. Only NOP/DES commands allowed after Refresh command registered until tRFC(min) expires.
2. Time interval between 2 Refresh commands maybe extended tp a maximum of 9 x tREFI.

3.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit,tZQoper, tZQCS, etc.) Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is

automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{REFCA} and V_{REFDQ}) must be at valid levels. V_{REFDQ} supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that V_{REFDQ} is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied. Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands" on page 107. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL for proper operation. However, if the DDR3 SDRAM is placed into Self-Refresh mode before tXSDLL is met, ODT may turn don't care in accordance with once the DDR3 SDRAM has entered Self-Refresh mode.

3.17 Power-Down Modes

3.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but powerdown IDD spec will not be applied until finishing those operations. Timing diagrams are shown for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Table 17 - Power-Down Entry Definition

Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	0	Off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, REF, MRS, PRE or PREA. tXPDLL to commands that need the DLL to operate, such as RD, RDA or ODT control line.
Precharged (All banks Precharged)	1	On	Fast	tXP to any valid command

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device. The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined in the AC specifications table.

4 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM for x4 and x8 configuration (and TDQS, TDQS# for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document:

- The ODT control modes are described in below
- The ODT synchronous mode is described in below
- The dynamic ODT feature is described in below
- The ODT asynchronous mode is described in below
- The transitions between ODT synchronous and asynchronous are described in below

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 31.

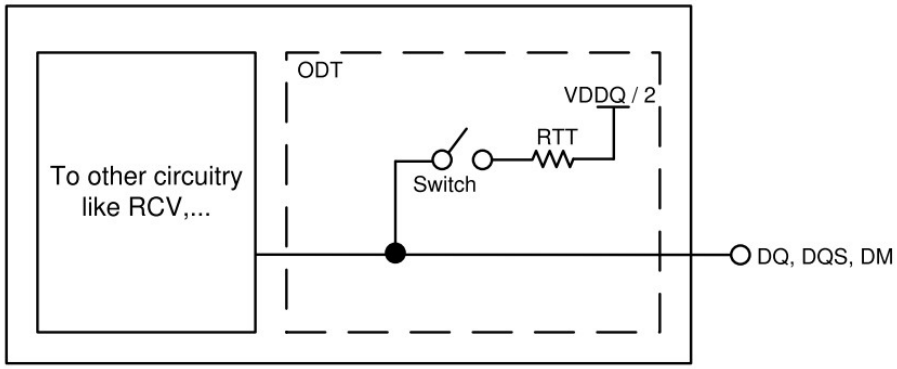


Figure 31 - Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT, and in self-refresh mode.

4.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if any of MR1 {A9, A6, A2} or MR2 {A10, A9} are non-zero. In this case, the value of RTT is determined by the settings of those bits.

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (unless ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 18.

Table 18 - Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 [A9,A6,A2] and MR2 [A10,A9] in general)

4.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL - 2 .

4.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to the ODT Timing Parameters.

4.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply: ODTLon, ODTLoff, *t*AON,min,max, *t*AOF,min,max.

Minimum RTT turn-on time (*t*AONmin) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (*t*AONmax) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (*t*AOFmin) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (*t*AOFmax) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 77). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

4.2.3 ODT during Reads

As the DDR3L SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the following figure. DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e. tHZ is early), then tAONmin time may apply. If DRAM stops driving late (i.e. tHZ is late), then DRAM complies with tAONmax timing.

4.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3L SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

4.3.1 Functional Description

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ‘1’. The function is described as follows:

Two RTT values are available: RTT_Nom and RTT_WR.

- The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.
- The value for RTT_WR is preselected via bits A[10,9] in MR2.

During operation without write commands, the termination is controlled as follows:

- Nominal termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.

When a Write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:

- A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
- A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set RTT_WR, MR2 [A10,A9 = [0,0], to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the Write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of Write command until ODT is register low.

Table 19 - Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr	Defined from	Defined to	Definition for all Speed bin	Unit
ODT turn-on Latency	ODTLon	Registering external ODT signal high	Turning termination on	WL-2	tCK
ODT turn-off Latency	ODTLoff	Registering external ODT signal low	Turning termination off	WL-2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_Nom to RTT_WR	WL-2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=4)	ODTLcwn4	Registering external write command	change RTT strength from RTT_WR to RTT_Nom	4+ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=8)	ODTLcwn8	Registering external write command	change RTT strength from RTT_WR to RTT_Nom	6+ODTLoff	tCK(avg)
Minimum ODT high time after ODT assertion	ODTH4	Registering ODT high	ODT registered low	4	tCK(avg)
Minimum ODT high time after Write (BL=4)	ODTH4	Registering write with ODT high	ODT registered low	4	tCK(avg)
Minimum ODT high time after Write (BL=8)	ODTH8	Registering write with ODT high	ODT registered low	6	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT Valid	Min: 0.3tCK(avg) Max: 0.7tCK(avg)	tCK(avg)

Note:

1. tAOF, nom and tADC, nom are 0.5tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn).

4.4 Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12. In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply: tAONPD min/max, tAOFPD min/max.

Minimum RTT turn-on time (tAONPD min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tAONPD max) is the point in time when the ODT resistance is fully on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPDmin) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tAOFPDmax) is the point in time when the on-die termination has reached high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being sample low.

4.4.1 Synchronous to Asynchronous ODT Mode Transitions

Table 20 - ODT timing parameters for Power Down (with DLL frozen) entry and exit

Description	Min	Max
ODT to RTT Turn-on delay	Min(ODTLon*tCK + tAONmin; tAONPDmin) Min((WL-2)*tCK + tAONmin; tAONPDmin)	Max(ODTLon*tCK + tAONmax; tAONPDmax) Max((WL-2)*tCK + tAONmax; tAONPDmax)
ODT to RTT Turn-off delay	Min(ODTLoff*tCK + tAOFmin; tAOFPDmin) Min((WL-2)*tCK + tAOFmin; tAOFPDmin)	Max(ODTLoff*tCK + tAOFmax; tAOFPDmax) Max((WL-2)*tCK + tAOFmax; tAOFPDmax)
Tanpd	WL-1	

4.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3L SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min). If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min). Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end point at tCPDED(min) and tRFC(min, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT changes as early as the smaller of tAONPDmin and (ODTLon*tck+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff*tCK+tAOFmax). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

4.4.3 Asynchronous to Synchronous ODT Mode transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3L SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered high. ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODTLon* tCK+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT deassertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODToff*tCK+tAOFmax). Note that if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

4.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case, the response of the DDR3L SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD entry transition period to the end of the PD exit transition period (even if the entry ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case, the response of the DDR3L SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD exit transition period to the end of the PD entry transition period. Note that in the following figure, it is assumed that there was no Refresh command in progress when Idle state was entered.

4.5 ZQ Calibration Commands

4.5.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron and ODT values. DDR3L SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows calibration of output driver and on-die termination values.

Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon selfrefresh exit, DDR3L SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between ranks.

4.5.2 ZQ Calibration Timing

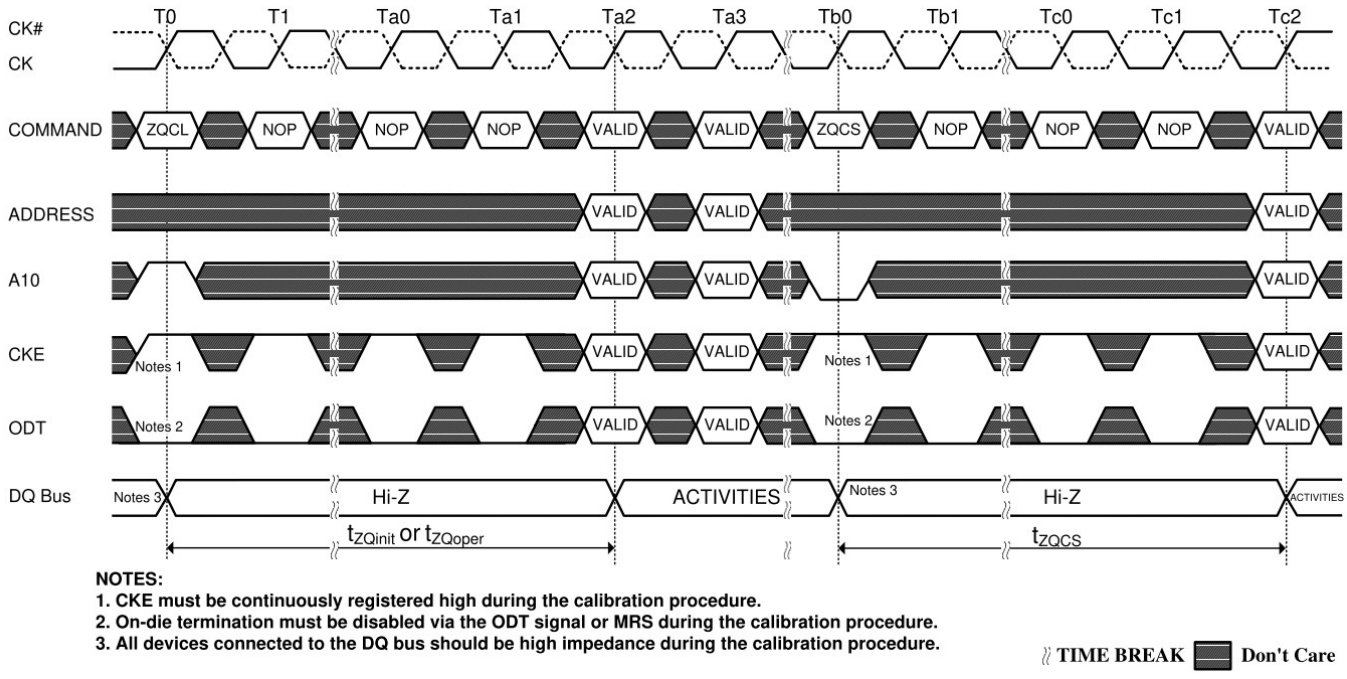


Figure 32 - ZQ Calibration Timing

4.5.3 ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ calibration function, a 240 ohm ±1% tolerance external resistor connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.

5 Absolute Maximum Rating

5.1 Absolute Maximum DC Rating

Table 21 - Absolute Maximum DC Rating

Symbol	Parameter	Rating	Unti	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 ~ 1.80	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 ~ 1.80	V	1,3
V_{IN} , V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.80	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300 mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500 mV; V_{REF} may be equal to or less than 300 mV

5.2 DRAM Component Operating Temperature Range

Table 22 - Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range	85 ~ 95	°C	1,3
	Industrial Operating Temperature Range	-40 ~85	°C	1,2
	Extended Temperature Range	85 ~ 95	°C	1,3
	High Operating Temperature Range	-40 ~ 105	°C	1,3,4

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b. In 95°C to 105°C, with Refresh commands must be quadrupled in frequency, therefore, reducing the Refresh interval tREFI to 1.95us.
   c. Supporting extended temperature Self-Refresh entry via the control of MR2 bit A7. When T_{CASE} > 95°C, self refresh mode is not available.
4. During high temperature operation range, the DRAM case temperature must be maintained between -40°C ~ 105°C under all operating conditions.

6 AC & DC Operating Condition

6.1 Recommended DC Operating Conditions

Table 23 - Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min	Typ	Max		
V_{DD}	Supply Voltage	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for output	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDD(t) over a long period of time (e.g., 1 sec).
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.
6. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.

7 AC & DC Input Measurement Levels

7.1 AC and DC Logic Input Level for Single-ended Signals

7.1.1 AC and DC Input Levels for Single-ended Command and Address Signals

Table 24 - Single-ended AC and DC Input Level for Command and Address

Symbol	Parameter	DDR3L-1600		DDR3L-1866,2133		Unit	Note
		Min	Max	Min	Max		
VIH.CA(DC90)	DC input logic high	V_{REF}+0.090	V_{DD}	V_{REF}+0.090	V_{DD}	V	1
VIL.CA(DC90)	DC input logic low	V_{SS}	V_{REF}-0.090	V_{SS}	V_{REF}-0.090	V	1
VIH.CA(AC160)	AC input logic high	V_{REF}+0.160	Note 2	-	-	V	1,2,5
VIL.CA(AC160)	AC input logic low	Note 2	V_{REF}-0.160	-	-	V	1,2,5
VIH.CA(AC135)	AC input logic high	V_{REF}+0.135	Note 2	V_{REF}+0.135	Note 2	V	1,2,5
VIL.CA(AC135)	AC input logic low	Note 2	V_{REF}-0.135	Note 2	V_{REF}-0.135	V	1,2,5
VIH.CA(AC125)	AC input logic high	-	-	V_{REF}+0.125	Note 2	V	1,2,5
VIL.CA(AC125)	AC input logic low	-	-	Note 2	V_{REF}-0.125	V	1,2,5
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Symbol	Parameter	DDR3-1600		DDR3-1866,2133		Unit	Note
		Min	Max	Min	Max		
VIH.CA(DC100)	DC input logic high	V_{REF}+0.100	V_{DD}	V_{REF}+0.100	V_{DD}	V	1,6
VIL.CA(DC100)	DC input logic low	V_{SS}	V_{REF}-0.100	V_{SS}	V_{REF}-0.100	V	1,7
VIH.CA(AC175)	AC input logic high	V_{REF}+0.175	Note 2	-	-	V	1,2,8
VIL.CA(AC175)	AC input logic low	Note 2	V_{REF}-0.175	-	-	V	1,2,9
VIH.CA(AC150)	AC input logic high	V_{REF}+0.150	Note 2	-	-	V	1,2,8
VIL.CA(AC150)	AC input logic low	Note 2	V_{REF}-0.150	-	-	V	1,2,9
VIH.CA(AC135)	AC input logic high	-	-	V_{REF}+0.135	Note 2	V	1,2,8
VIL.CA(AC135)	AC input logic low	-	-	Note 2	V_{REF}-0.135	V	1,2,9
VIH.CA(AC125)	AC input logic high	-	-	V_{REF}+0.125	Note 2	V	1,2,8
VIL.CA(AC125)	AC input logic low	-	-	Note 2	V_{REF}-0.125	V	1,2,9
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4,10

Note:

1. For input only pins except RESET#. V_{REF} = $V_{REFCA(DC)}$.
2. See “Overshoot and Undershoot Specifications”.
3. The AC peak noise on V_{REF} may not allow VREF to deviate from $V_{REF(DC)}$ by more than ± 1% V_{DD} (for reference: DDR3L: approx. ± 13.5mV; DDR3: approx. ± 15mV).
4. For reference: DDR3 has approx. VDD/2 ± 15mV, DDR3L has approx. VDD/2 ± 13.5mV.
5. These levels apply for 1.35V operation only. If the device is operated at 1.5V, the respective levels in JESD79 -3F (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) apply. The 1.5V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) do not apply when the device is operated in the 1.35 voltage range.
6. VIH(DC) is used as a simplified symbol for VIH.CA(DC100).
7. VIL(DC) is used as a simplified symbol for VIL.CA(DC100).
8. VIH(AC) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC175) value is used when V_{REF} + 0.175V is referenced, VIH.CA(AC150) value is used when V_{REF} + 0.15V is referenced, VIH.CA(AC135) value is used when V_{REF} + 0.135V is referenced, and VIH.CA(AC125) value is used when V_{REF} + 0.125V is referenced.
9. VIL(AC) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC125); VIL.CA(AC175) value is used when V_{REF} - 0.175V is referenced, VIL.CA(AC150) value is used when V_{REF} - 0.15V is referenced, VIL.CA(AC135) value is used when V_{REF} - 0.135V is referenced, and VIL.CA(AC125) value is used when V_{REF} - 0.125V is referenced.
10. $V_{REFCA(DC)}$ is measured relative to VDD at the same point in time on the same device.

7.1.2 AC and DC Input Levels for Single-ended Data Signal

Table 25 - Single-ended AC and DC Input Level for DQ and DM

Symbol	Parameter	DDR3L-1600		DDR3L-1866,2133		Unit	Note
		Min	Max	Min	Max		
VIH.DQ(DC90)	DC input logic high	V_{REF}+0.090	V_{DD}	V_{REF}+0.090	V_{DD}	V	1
VIL.DQ(DC90)	DC input logic low	V_{SS}	V_{REF}-0.090	V_{SS}	V_{REF}-0.090	V	1
VIH.DQ(AC135)	AC input logic high	V_{REF}+0.135	Note 2	-	-	V	1,2,5
VIL.DQ(AC135)	AC input logic low	Note 2	V_{REF}-0.135	-	-	V	1,2,5
VIH.DQ(AC130)	AC input logic high	-	-	V_{REF}+0.130	Note 2	V	1,2,5
VIL.DQ(AC130)	AC input logic low	-	-	Note 2	V_{REF}-0.130	V	1,2,5
$V_{REFDQ(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Symbol	Parameter	DDR3-1600		DDR3-1866,2133		Unit	Note
		Min	Max	Min	Max		
VIH.DQ(DC100)	DC input logic high	V_{REF}+0.100	V_{DD}	V_{REF}+0.100	V_{DD}	V	1,6
VIL.DQ(DC100)	DC input logic low	V_{SS}	V_{REF}-0.100	V_{SS}	V_{REF}-0.100	V	1,7
VIH.DQ(AC150)	AC input logic high	V_{REF}+0.150	Note 2	-	-	V	1,2,8
VIL.DQ(AC150)	AC input logic low	Note 2	V_{REF}-0.150	-	-	V	1,2,9
VIH.DQ(AC135)	AC input logic high	V_{REF}+0.135	Note 2	V_{REF}+0.135	Note 2	V	1,2,8
VIL.DQ(AC135)	AC input logic low	Note 2	V_{REF}-0.135	Note 2	V_{REF}-0.135	V	1,2,9
$V_{REFDQ(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4,10

Note:

1. For input only pins except RESET#, V_{REF} = $V_{REFDQ(DC)}$.
2. See “Overshoot and Undershoot Specifications”.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFDQ(DC)}$ by more than ± 1% VDD (for reference: DDR3L: approx. ± 13.5mV; DDR3: approx. ± 15mV).
4. For reference: DDR3 has approx. V_{DD}/2 ± 15mV, and DDR3L has approx. V_{DD}/2 ± 13.5mV.
5. These levels apply for 1.35V operation only. If the device is operated at 1.5V, the respective levels in JESD79-3F (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) apply. The 1.5V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.35 voltage range.
6. VIH(DC) is used as a simplified symbol for VIH.DQ(DC100).
7. VIL(DC) is used as a simplified symbol for VIL.DQ(DC100).
8. VIH(AC) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when V_{REF} + 0.175V is referenced, VIH.DQ(AC150) value is used when V_{REF} + 0.15V is referenced, and VIH.DQ(AC135) value is used when VREF + 0.135V is referenced.
9. VIL(AC) is used as a simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC175) value is used when V_{REF} - 0.175V is referenced, VIL.DQ(AC150) value is used when V_{REF} - 0.15V is referenced, and VIL.DQ(AC135) value is used when V_{REF} - 0.135V is referenced.
10. $V_{REFDQ(DC)}$ is measured relative to VDD at the same point in time on the same device.

7.2 V_{REF} Tolerances

The DC-Tolerance limits and AC-Noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated in Figure 33. It shows a valid reference voltage $V_{REF(t)}$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirement. Furthermore $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% V_{DD}.

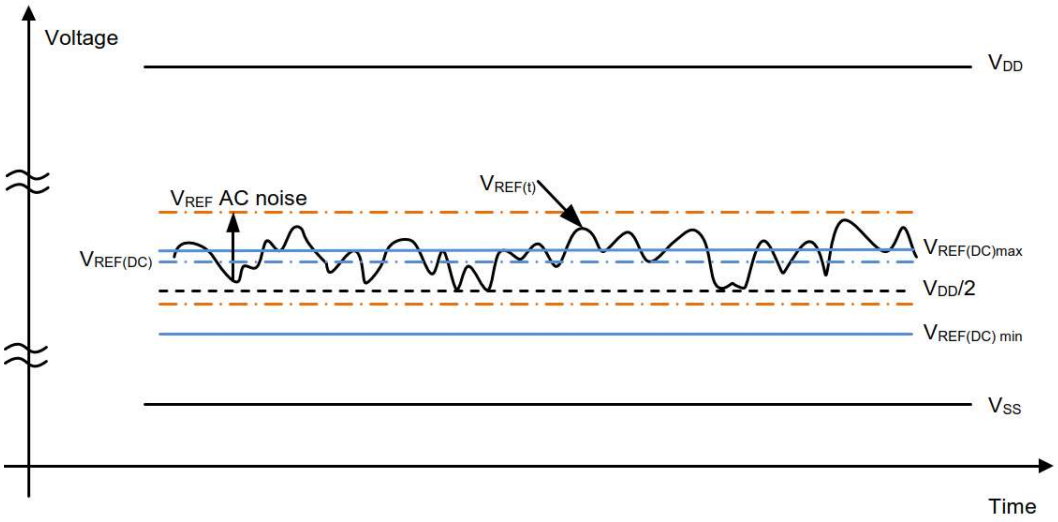


Figure 33 - Illustration of VREF(DC) Tolerance and VREF AC-Noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on V_{REF}. "V_{REF}" should be understood as $V_{REF(DC)}$.

This clarifies that DC-Variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level, and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-Noise. Timing and voltage effects due to AC-Noise on V_{REF} up to the specified limit (± 1% of V_{DD}) are included in DRAM timings and their associated deratings.

7.3 AC and DC Logic Input Levels for Differential Signals

7.3.1 Differential Signals Definition

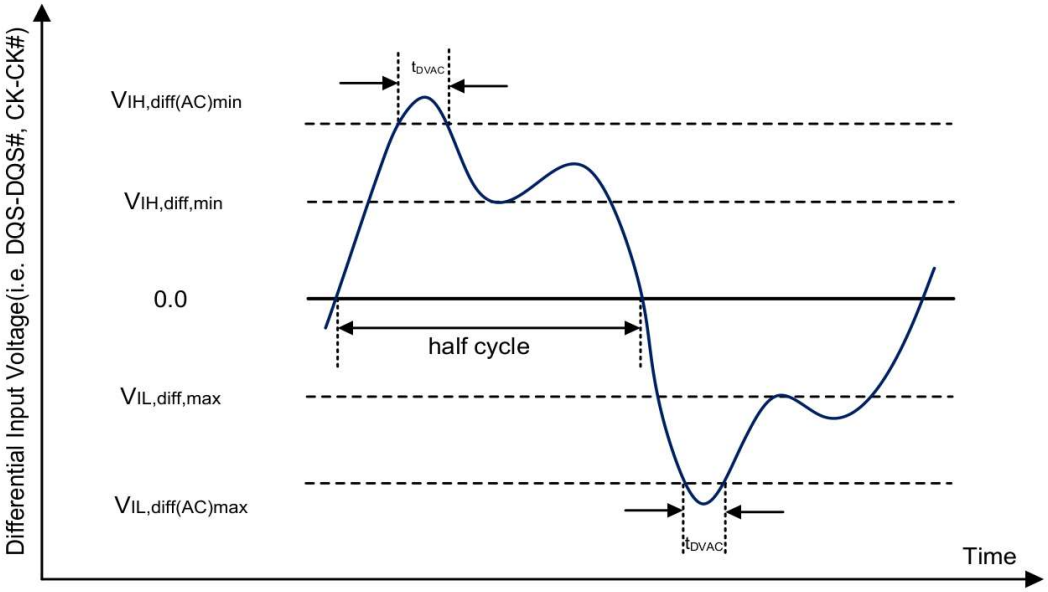


Figure 34 - Definition of Differential AC-Swing and "Time above AC-Level" tDVAC

7.3.2 Differential Swing Requirements for Clock (CK - CK#) and strobe (DQS - DQS#)

Table 26 - Differential AC and DC Input Level Table 25 – Single-ended AC and DC Input Level for DQ and DM

Symbol	Parameter	DDR3-1600,1866,2133				Unit	Note
		1.35V		1.5V			
		Min	Max	Min	Max		
VIH.diff	Differential Input High	+0.18	Note 3	+0.20	Note 3	V	1
VIL.diff	Differential Input Low	Note 3	-0.18	Note 3	-0.20	V	1
VIH.diff(AC)	Differential Input High AC	2x(VIH(AC) – V_{REF})	Note 3	2x(VIH(AC) – V_{REF})	Note 3	V	2
VIL.diff(AC)	Differential Input Low AC	Note 3	2x(VIL(AC) – V_{REF})	Note 3	2x(VIL(AC) – V_{REF})	V	2

Note:

1. Used to define a differential signal slew-rate.
2. For CK - CK# use VIH/VIL(AC) of ADD/CMD and V_{REFCA}; for DQS - DQS#, DQSL - DQSL#, DQSU - DQSU# use VIH/VIL(AC) of DQS and V_{REFDQ}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 27 - Allowed Time before Ringback (tDVAC) for CK-CK# and DQS-DQS# (1.35V).

Slew Rate (V/ns)	DDR3L-1600				DDR3L-1866,2133					
	tDVAC(ps) (VIH/L.diff=320mV)		tDVAC(ps) (VIH/L.diff=270mV)		tDVAC(ps) (VIH/L.diff=270mV)		tDVAC(ps) (VIH/L.diff=250mV)		tDVAC(ps) (VIH/L.diff=260mV)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	Note	-	44	-	5	-	22	-	24	-
1.0	Note	-	Note	-	Note	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIH,diff(AC) level and falling input signal shall become equal to or less than VIL,diff(AC) level.

Table 28 - Allowed Time before Ringback (tDVAC) for CK-CK# and DQS-DQS# (1.5V).

Slew Rate (V/ns)	DDR3L-1600						DDR3L-1866,2133			
	tDVAC(ps) (VIH/L.diff=350mV)		tDVAC(ps) (VIH/L.diff=300mV)		tDVAC(ps) (VIH/L.diff=DQS-DQS# only)		tDVAC(ps) (VIH/L.diff=300mV)		tDVAC(ps) (VIH/L.diff=CK-CK# only)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	75	-	175	-	214	-	134	-	139	-
4.0	57	-	170	-	214	-	134	-	139	-
3.0	50	-	167	-	191	-	112	-	118	-
2.0	38	-	119	-	146	-	67	-	77	-
1.8	34	-	102	-	131	-	52	-	63	-
1.6	29	-	81	-	113	-	33	-	45	-
1.4	22	-	54	-	88	-	9	-	23	-
1.2	Note	-	19	-	56	-	Note	-	Note	-
1.0	Note	-	Note	-	11	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIH,diff(AC) level and falling input signal shall become equal to or less than VIL,diff(AC) level.

7.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin/VSELmax (approximately equal to the AC-Levels (VIH(AC)/VIL(AC)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin/VSELmax (approximately the AC-Levels (VIH(AC)/VIL(AC)) for DQ signal) in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK and CK#.

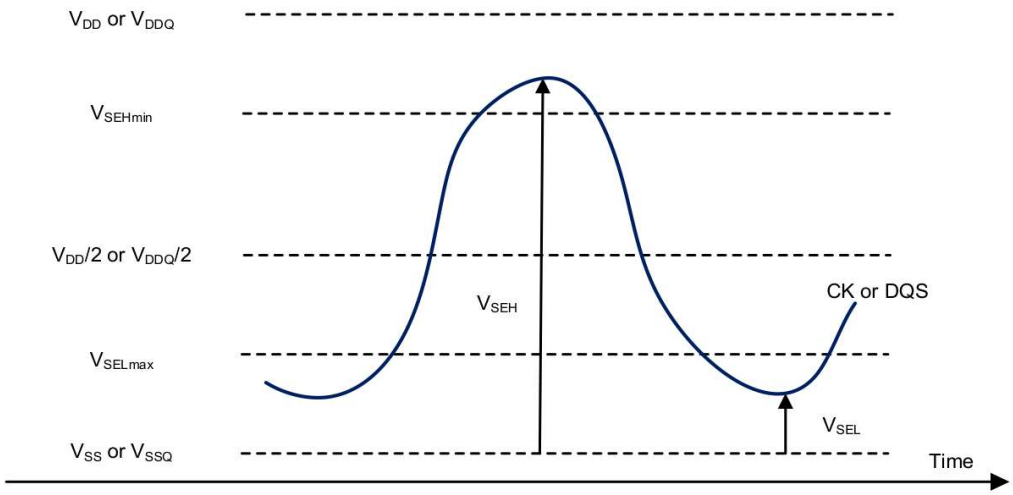


Figure 35 - Single-ended Requirement for Differential Signals

Note that, while ADD/CMD and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$, this is nominally the same. The transition of single-ended signals through the AC-Levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 29 - Single-ended Level for CK, CK#, DQS, DQS#, DQSI, DQSL#, DQSU, DQSU#

Symbol	Parameter	DDR3-1600,1866,2133		Unit	Note
		Min	Max		
VSEH	Single-ended High-level for Strobes	(V_{DD}/2)+0.175	Note 3	V	1,2
	Single-ended High-level for CK, CK#	(V_{DD}/2)+0.175	Note 3	V	1,2
VSEL	Single-ended Low-level for Strobes	Note 3	(V_{DD}/2)-0.175	V	1,2
	Single-ended Low-level for CK, CK#	Note 3	(V_{DD}/2)-0.175	V	1,2

Note:

1. For CK, CK# use VIH/VIL(AC) of ADD/CMD; for storbes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(AC) of DQS.
2. VIH(AC)/VIL(AC) for DQ is based on V_{REFDQ}; VIH(AC)/VIL(AC) for ADD/CMD is based on V_{REFCA}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

7.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross-point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 30 and Table 31. The differential input cross point voltage VIX is measured from the actual cross-point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

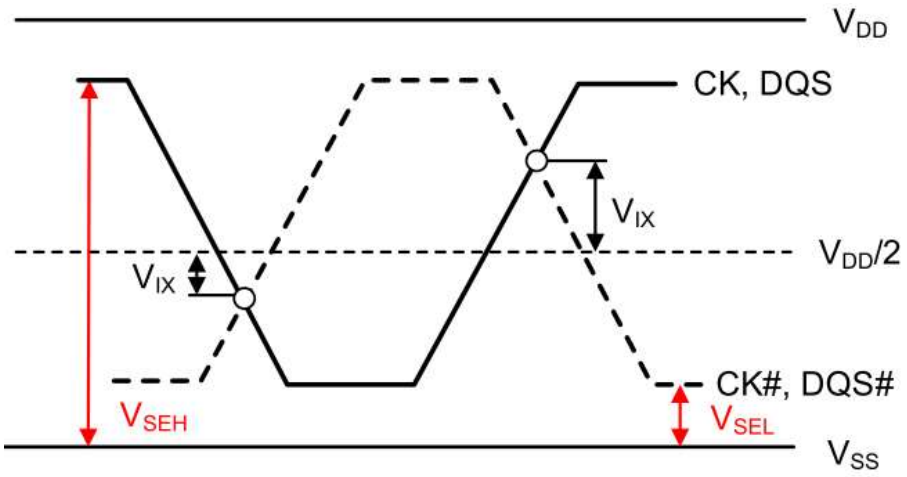


Figure 36 - VIX Definition

Table 30 - Cross Point Voltage for Differential Input Signal (CK, DQS) for 1.35V

Symbol	Parameter	DDR3-1600,1866,2133		Unit	Note
		Min	Max		
VIX(CK)	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, CK#	-150	150	mV	1
VIX(DQS)	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, DQS#	-150	150	mV	

Note:

1. The relation between VIX(min/max) and VSEL/VSEH should satisfy following.
   V_{DD}/2 + VIX(min) – VSEL ≥ 25mV
   VSEH – (V_{DD}/2 + VIX(max)) ≥ 25mV

Table 31 - Cross Point Voltage for Differential Input Signal (CK, DQS) for 1.5V

Symbol	Parameter	DDR3-1600,1866,2133		Unit	Note
		Min	Max		
VIX(CK)	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK, CK#	-150	150	mV	2
		-175	175	mV	1
VIX(DQS)	Differential Input Cross Point Voltage relative to V_{DD}/2 for DQS, DQS#	-150	150	mV	2

Note:

1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL/VSEH of at least V_{DD}/2 ± 250mV, and when the differential slew rate of CK - CK# is larger than 3V/ns.
2. The relation between VIX(min/max) and VSEL/VSEH should satisfy following.
   V_{DD}/2 + VIX(min) – VSEL ≥25mV
   VSEH - (V_{DD}/2 + VIX(max)) ≥25mV

7.5 Slew Rate Definitions for Single-ended Input Signals

See section “Address/Command Setup, Hold and Derating” single-ended slew rate definitions for address and command signals.

See section “Data Setup, Hold and Slew Rate Derating” single-ended slew rate definitions for data signals.

7.6 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK#, and DQS, DQS#) are defined and measured as shown in Table 32 and Figure 37.

Table 32 – Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential Input Slew Rate for Rising edge (CK-CK# and DQS-DQS#)	VIL.diff.max	VIH.diff.min	(VIH.diff.min – VIL.diff.max) / DeltaTRdiff
Differential Input Slew Rate for Falling edge (CK-CK# and DQS-DQS#)	VIH.diff.min	VIL.diff.max	(VIH.diff.min – VIL.diff.max) / DeltaTFdiff

Note:

1. The differential signal (i.e. CK-CK# and DQS-DQS#) must be linear between these thresholds.

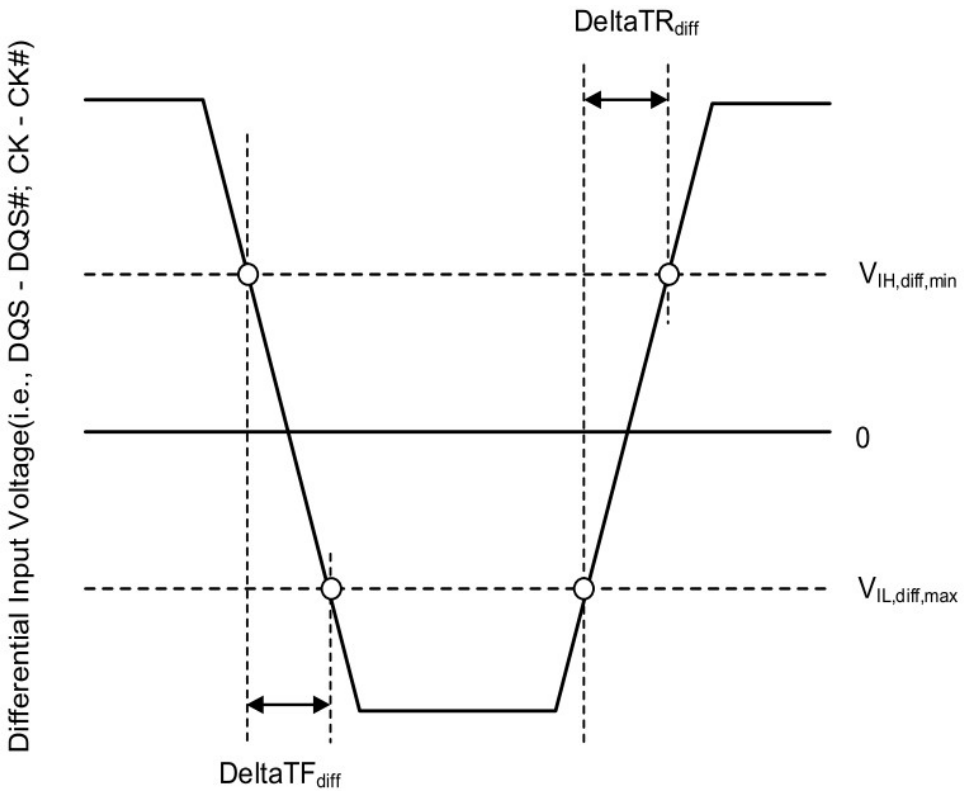


Figure 37 – Differential Input Slew Rate Definition for DQS,DQS# and CK,CK#

8 AC & DC Output Measurement Level

8.1 Single-ended AC and DC Output Level

Table 33 – Single-ended AC and DC Output Level

Symbol	Parameter	Value	Unit	Note
VOH(DC)	DC Output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
VOM(DC)	DC Output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
VOL(DC)	DC Output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
VOH(AC)	DC Output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
VOL(AC)	DC Output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2.

8.2 Differential AC and DC Output Level

Table 34 – Differential AC and DC Output Level

Symbol	Parameter	Value	Unit	Note
VOH.diff(AC)	AC Differential Output high measurement level (for output SR)	+0.2 x V_{DDQ}	V	1
VOL.diff(AC)	AC Differential Output low measurement level (for output SR)	-0.2 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

8.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals as shown in Table 35 and Figure 38.

Table 35 – Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended Output Slew Rate for Rising edge	VOL(AC)	VOH(AC)	(VOH(AC) – VOL(AC)) / DeltaTRse
Single-ended Output Slew Rate for Falling edge	VOH(AC)	VOL(AC)	(VOH(AC) – VOL(AC)) / DeltaTFse

Note:

1. Output slew rate is verified by design and characterization and may not be subject to production test.

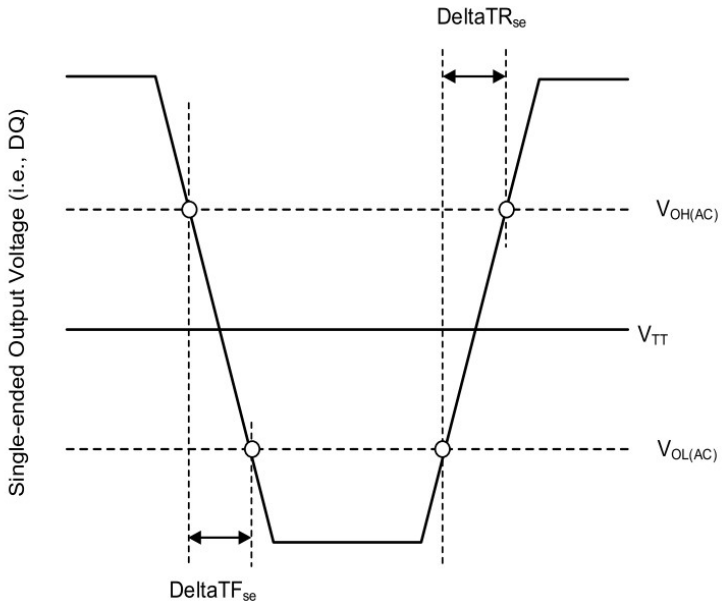


Figure 38 - Single-ended Output Slew Rate Definition

Table 36 – Single-ended Output Slew Rate

Parameter	Symbol	Operation Voltage	DDR3-1600,1866,2133		Unit
			Min	Max	
Single-ended Output Slew Rate	SEQse	1.35V	1.75	5[1]	V/ns
		1.5V	2.5	5	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For RON = RZQ/7 Setting

Note:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.
   - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from LOW to HIGH or HIGH to LOW respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies).

8.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL,diff(AC) and VOH,diff(AC) for differential signals as shown in Table 37 and Figure 39.

Table 37 – Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential Output Slew Rate for Rising edge	VOL.diff(AC)	VOH.diff(AC)	(VOH.diff(AC) – VOL.diff(AC)) / DeltaTRdiff
Differential Output Slew Rate for Falling edge	VOH.diff(AC)	VOL.diff(AC)	(VOH.diff(AC) – VOL.diff(AC)) / DeltaTFdiff

Note:

1. Output slew rate is verified by design and characterization and may not be subject to production test.

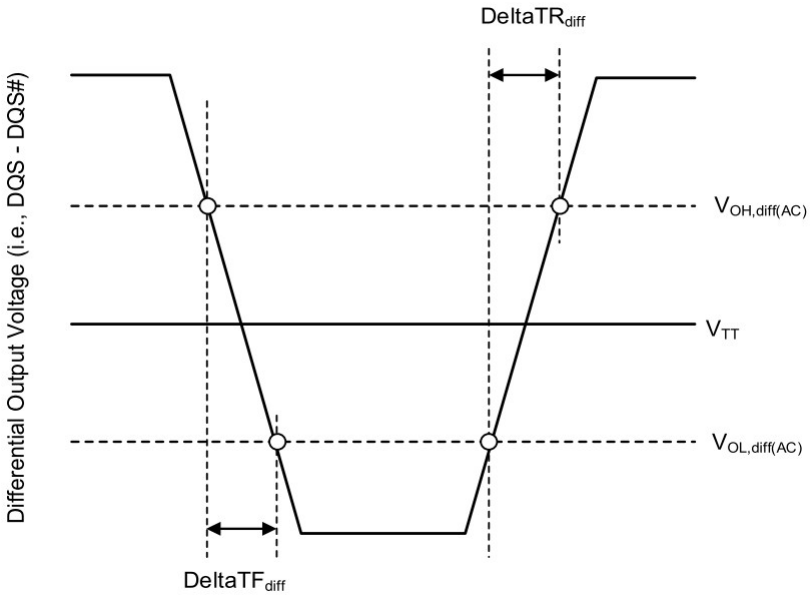


Figure 39 – Differential Output Slew Rate Definition

Table 38 – Differential Output Slew Rate

Parameter	Symbol	Operation Voltage	DDR3-1600		DDR3-1866,2133		Unit
			Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	1.35V	3.5	12	3.5	12	V/ns
		1.5V	5	10	5	12	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For RON = RZQ/7 Setting

8.5 Reference Load for AC Timing and Output Slew Rate

Figure 40 represents the effective reference load of 25Ω used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

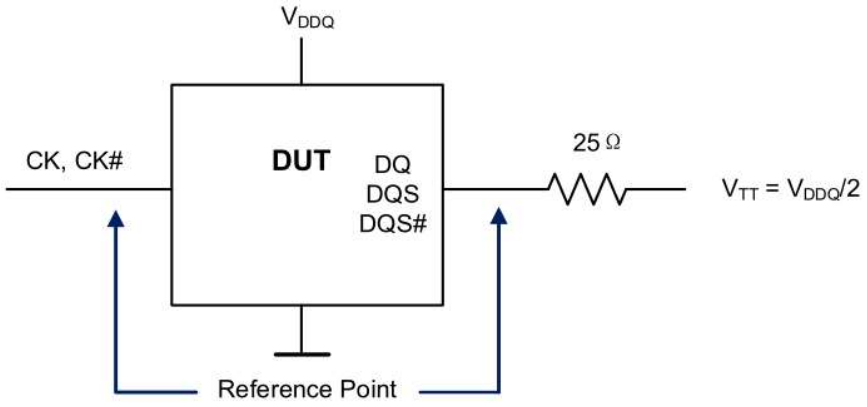


Figure 40 – Reference Load for AC Timing and Output Slew Rate

8.6 Overshoot and Undershoot Specification

8.6.1 Address and Control Overshoot and Undershoot Specification

Table 39 – AC Overshoot/Undershoot Specification for Address and Control Pins

	DDR3-1600	DDR3-1866	DDR3-2133	Unit
Maximum Peak Amplitude allowed for overshoot area[1]	0.4	0.4	0.4	V
Maximum Peak Amplitude allowed for undershoot area[2]	0.4	0.4	0.4	V
Maximum overshoot area above V_{DD}	0.33	0.28	0.25	V-ns
Maximum undershoot area below V_{SS}	0.33	0.28	0.25	V-ns
A0-A15, BA0-BA2, CS#, RAS#, CAS#, WE#, CKE, ODT				

Note:

1. The sum of the applied voltage (V_{DD}) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of the applied voltage (V_{DD}) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

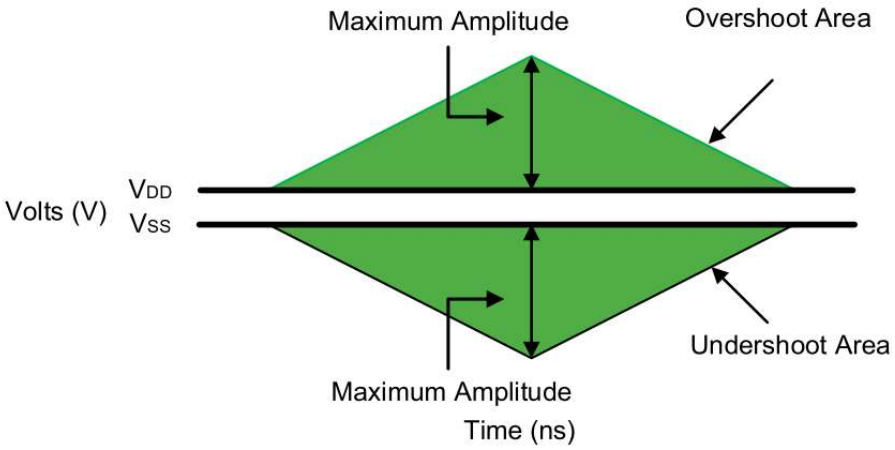


Figure 41 – Address and Control Overshoot and Undershoot Specification

8.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specification

Table 40 – AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

	1600	1866	2133	Unit
Maximum Peak Amplitude allowed for overshoot area[1]	0.4	0.4	0.4	V
Maximum Peak Amplitude allowed for undershoot area[2]	0.4	0.4	0.4	V
Maximum overshoot area above V_{DDQ}	0.13	0.11	0.10	V-ns
Maximum undershoot area below V_{SSQ}	0.13	0.11	0.10	V-ns
CK, CK#, DQ, DQS, DQS#, DM				

Note:

1. The sum of the applied voltage (V_{DD}) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of the applied voltage (V_{DD}) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

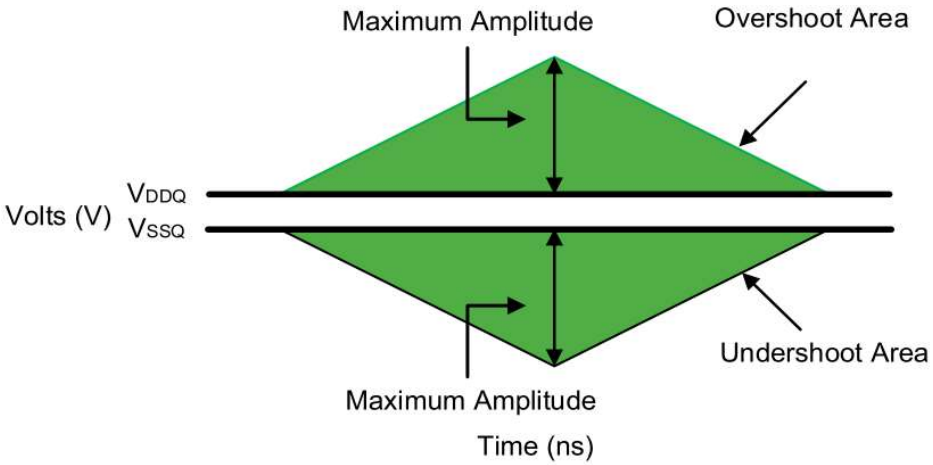


Figure 42 – Clock, Data, Strobe and Mask Overshoot and Undershoot Specification

8.7 34Ω Output Driver DC Electronic Characteristics

A functional representation of the output buffer is shown Figure 43. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:

RON34 = RZQ/7 (Nominal 34.3Ω ± 10% with nominal RZQ = 240Ω).

The individual pull-up and pull-down resistors RON(Pu) and RON(Pd) are defined as follows:

under the condition that RON(Pd) is turned off.
under the condition that RON(Pu) is turned off.

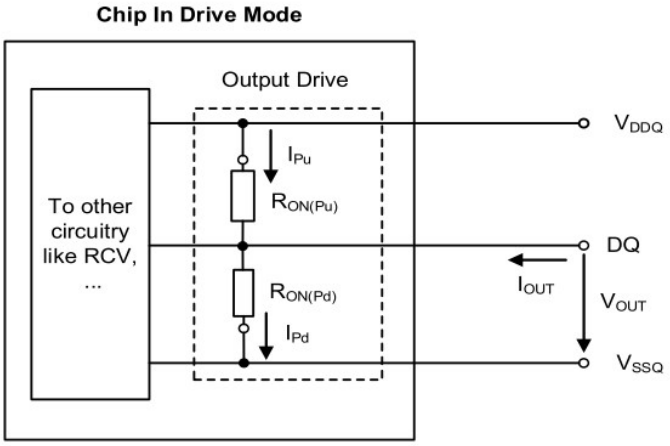


Figure 43 – Output Driver: Definition of Voltages and Currents

Table 41 – Output Driver DC Electrical Characteristics, assuming RZQ=240Ω; entire operating temperature range; after proper ZQ calibration

RON,Nom	Resistor	V_{OUT}	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
34Ω	$R_{ON.34Pd}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/7	1,2,3
		VOM(DC) = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/7	1,2,3
		VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/7	1,2,3
	$R_{ON.34Pu}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/7	1,2,3
		VOM(DC) = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/7	1,2,3
		VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/7	1,2,3
40Ω	$R_{ON.40Pd}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/6	1,2,3
		VOM(DC) = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/6	1,2,3
		VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/6	1,2,3
	$R_{ON.34Pu}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/6	1,2,3
		VOM(DC) = 0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/6	1,2,3
		VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/6	1,2,3
Mismatch between Pull-up and Pull-down, MM_{PuPd}		VOM(DC) = 0.5 x V_{DDQ}	-10	-	+10	+10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
   Measure RON(Pu) and RON(Pd), both at 0.5 × V_{DDQ}:

8.7.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 42 and Table 43.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$.

Note:
1. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 42 – Output Driver Sensitivity Definition

Item	Min	Max	Unit
$R_{ON(Pu)}@V_{OH(DC)}$	$0.6 – dR_{ON}dTH \times \lvert \Delta T \rvert - dR_{ON}dVH \times \lvert \Delta V \rvert$	$1.1 + dR_{ON}dTH \times \lvert \Delta T \rvert - dR_{ON}dVH \times \lvert \Delta V \rvert$	RZQ/7
$R_{ON}@V_{OM(DC)}$	$0.9 – dR_{ON}dTM \times \lvert \Delta T \rvert - dR_{ON}dVM \times \lvert \Delta V \rvert$	$1.1+ dR_{ON}dTM \times \lvert \Delta T \rvert - dR_{ON}dVM \times \lvert \Delta V \rvert$	RZQ/7
$R_{ON(Pd)}@V_{OL(DC)}$	$0.6 – dR_{ON}dTL \times \lvert \Delta T \rvert - dR_{ON}dVL \times \lvert \Delta V \rvert$	$1.1 + dR_{ON}dTL \times \lvert \Delta T \rvert - dR_{ON}dVL \times \lvert \Delta V \rvert$	RZQ/7

Table 43 – Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-1600,1866,2133		Unit
Item	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.13	%/mV

Note:
1. These parameters may not be subject to production test. They are verified by design and characterization.

8.8 On-Die Termination (ODT) Levels and I-V Characteristics

8.8.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register. ODT is applied to the DQ, DM, DQS /DQS# pins.

A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTT(Pu) and RTT(Pd)) are defined as follows:

under the condition that RTT(Pd) is turned off.
under the condition that RTT(Pu) is turned off.

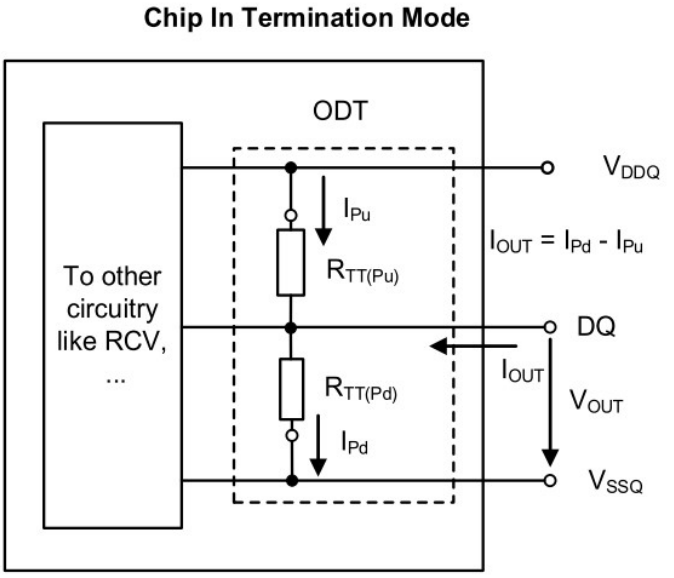


Figure 44 – On-Die Termination: Definition of Voltages and Currents

8.8.2 ODT DC Electrical Characteristic

Table 44 provides an overview of the ODT DC electrical characteristics. Their values for RTT60(Pd120), RTT60(Pu120), RTT120(Pd240), RTT120(Pu240), RTT40(Pd80), RTT40(Pu80), RTT30(Pd60), RTT30(Pu60), RTT20(Pd40), RTT20(Pu40) are not specification requirements, but can be used as design guidelines.

Table 44 – ODT DC Electristics, assuming RZQ=240Ω ± 1% entire operating temperature range; after proper ZQ calibration

MR1 (A9,A6,A2)	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
0,1,0	120Ω	$R_{TT120(Pd240)}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ	1,2,3,4
		$R_{TT120(Pu240)}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ	1,2,3,4
		R_{TT120}	VIL(AC) to VIH(AC)	0.9	1.0	1.65	1.6	RZQ/2	1,2,5
0,0,1	60Ω	$R_{TT60(Pd120)}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/2	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/2	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/2	1,2,3,4
		$R_{TT60(Pu120)}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/2	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/2	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/2	1,2,3,4
		R_{TT60}	VIL(AC) to VIH(AC)	0.9	1.0	1.65	1.6	RZQ/4	1,2,5

MR1 (A9,A6,A2)	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
0,1,1	40Ω	$R_{TT40(Pd80)}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/3	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/3	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/3	1,2,3,4
		$R_{TT40(Pu80)}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/3	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/3	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/3	1,2,3,4
		R_{TT40}	VIL(AC) to VIH(AC)	0.9	1.0	1.65	1.6	RZQ/6	1,2,5
1,0,1	30Ω	$R_{TT30(Pd60)}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/4	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/4	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/4	1,2,3,4
		$R_{TT30(Pu60)}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/4	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/4	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/4	1,2,3,4
		R_{TT30}	VIL(AC) to VIH(AC)	0.9	1.0	1.65	1.6	RZQ/8	1,2,5
1,0,0	20Ω	$R_{TT20(Pd40)}$	VOL(DC) = 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/6	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/6	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/6	1,2,3,4
		$R_{TT20(Pu40)}$	VOL(DC) = 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	RZQ/6	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	RZQ/6	1,2,3,4
			VOH(DC) = 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	RZQ/6	1,2,3,4
		R_{TT20}	VIL(AC) to VIH(AC)	0.9	1.0	1.65	1.6	RZQ/12	1,2,5
Deviation of V_M w.r.t $V_{DDQ}/2$, ΔVM				-5	-	+5	+5	%	1,2,5,6

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
   Apply VIH(AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

6. Measurement definition for VM and ΔVM : ΔMeasure Voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100$$

8.8.3 ODT DC Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 45 and Table 46

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$.

Table 45 – ODT Sensitivity Definition

	Min	Max	Unit
R_{TT}	$0.9 – dR_{TT}dT \times \lvert\Delta T\rvert - dR_{TT}dV \times \lvert\Delta V\rvert$	$1.6 + dR_{TT}dT \times \lvert\Delta T\rvert + dR_{TT}dV \times \lvert\Delta V\rvert$	RZQ /2,4,6,8,12

Table 46 – ODT Voltage and Temperature Sensitivity

	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

Note:

1. These parameters may not be subject to production test. They are verified by design and characterization.

8.9 ODT Timing Definitions

8.9.1 Test Load for ODT Timing

Different than for timing measurements, the reference load for ODT timings is defined in Figure 45.

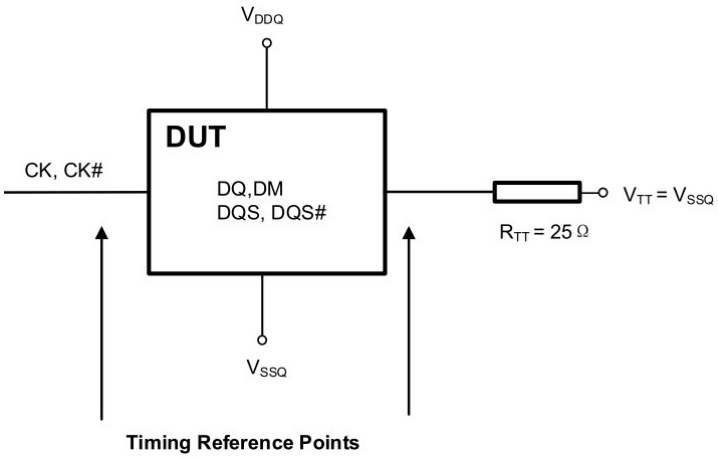


Figure 45 – ODT Timing Reference Load

8.9.2 ODT Timing Definitions

Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in Table 47. Measurement reference settings are provided in Table 48.

Table 47 – ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK-CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	46
tAONPD	Rising edge of CK-CK# with ODT being first registered HIGH	Extrapolated point at V_{SSQ}	47
tAOF	Rising edge of CK-CK# defined by the end point of ODTLoff	End point: Extrapolated point at $V_{RTT.Nom}$	48
tAOFPD	Rising edge of CK-CK# with ODT being first registered LOW	End point: Extrapolated point at $V_{RTT.Nom}$	49
tADC	Rising edge of CK-CK# defined by the end point of ODTLcnw, ODTLcwn4 of ODTLcwn8	End point: Extrapolated point at $V_{RTT(WR)}$ and $V_{RTT.Nom}$ respectively	50

Table 48 – Reference Settings for ODT Timing Measurements

Measured Parameter		$R_{TT.Nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1} (V)	V_{SW2} (V)
tAON		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
tAONPD		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
tAOF		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
tAOFPD		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
tADC	DDR3L (1.35V)	RZQ/12	RZQ/2	0.20	0.25
	DDR3 (1.5V)	RZQ/12	RZQ/2	0.20	0.30

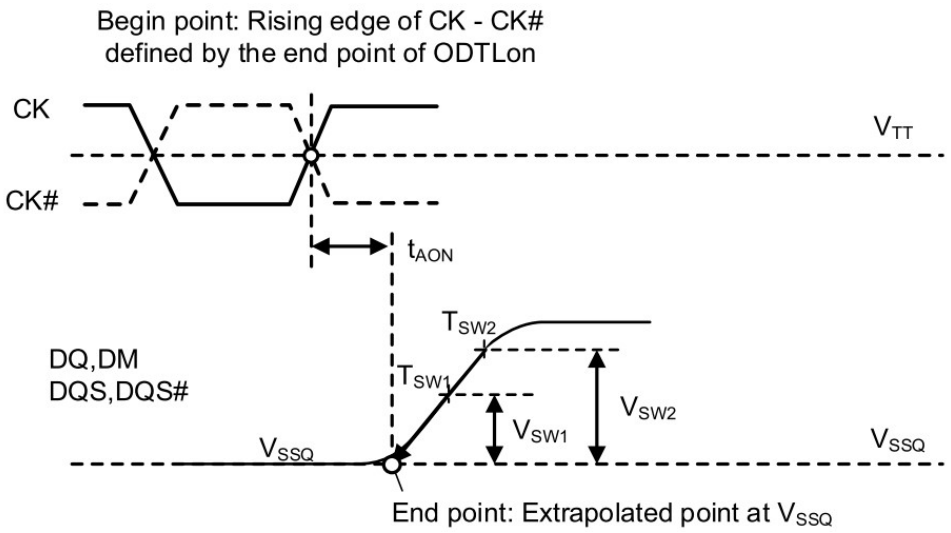


Figure 46 – Definition of tAON

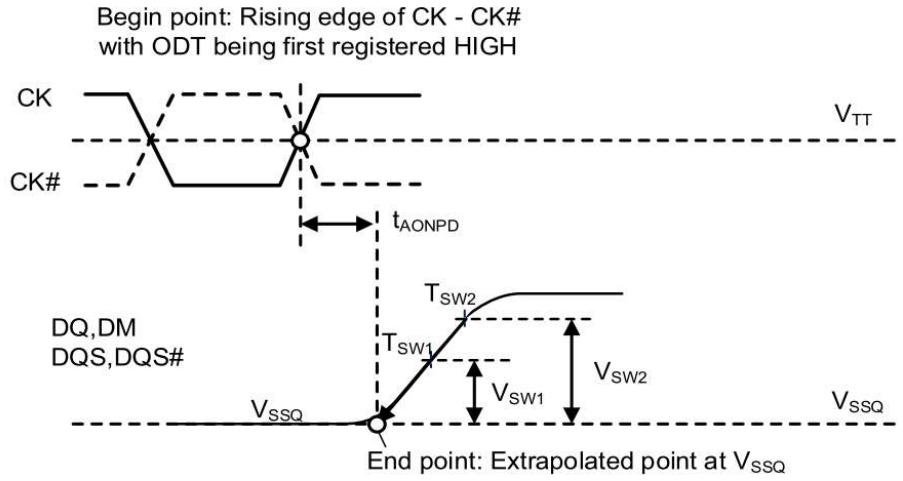


Figure 47 – Definition of tAONPD

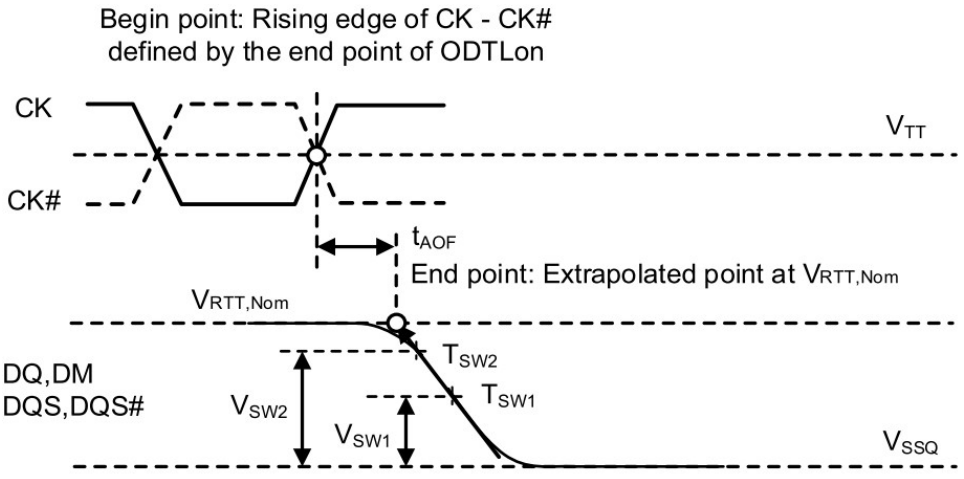


Figure 48 – Definition of tAOF

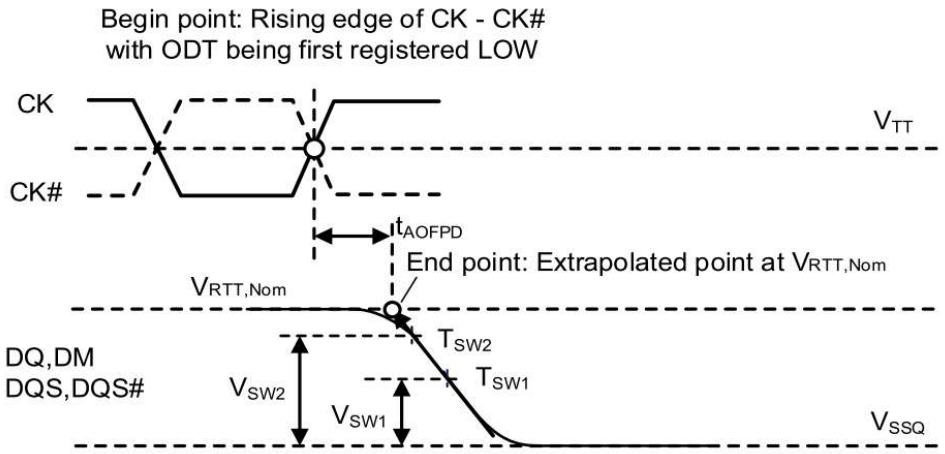


Figure 49 – Definition of tAOFPD

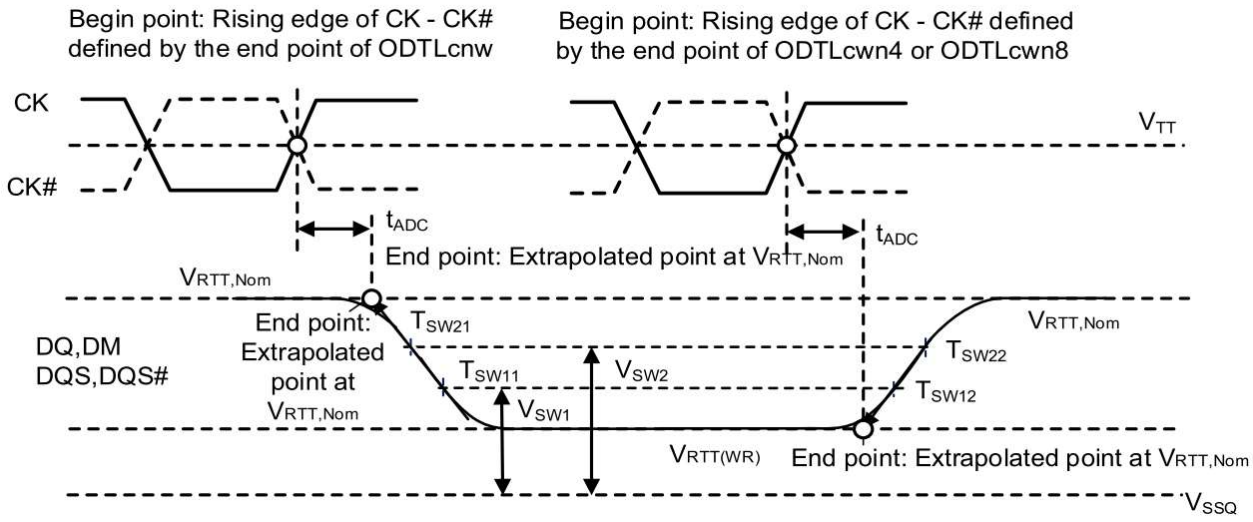


Figure 50 – Definition of tADC

9 Input/Output Capacitance

9.1 Input/Output Capacitance

Table 49 - Input/Output Capacitance for 1.5V

Parameter	Symbol	1600		1866		2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
Input/Output Capacitance, DQ, DM, DQS, DQS#, TDQS, TDQS#	CIO	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input Capacitance, CK and CK#	CCK	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
Input Capacitance delta, CK and CK#	CDCK	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/Output Capacitance delta, DQS, DQS#	CDDQS	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input Capacitance, CTRL, ADD, CMD input-only pins	CI	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,6
Input Capacitance delta, all CTRL input-only pins	CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input/Output Capacitance, all ADD/CMD input-only pins	CDI_ADD_CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/Output Capacitance delta, DQ, DM, DQS, DQS#, TDQS, TDQS#	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/Output Capacitance of ZQ pin	CZQ	-	3	-	3	-	3	pF	2,3,12

Table 50 - Input/Output Capacitance for 1.35V

Parameter	Symbol	1600		1866		2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
Input/Output Capacitance, DQ, DM, DQS, DQS#, TDQS, TDQS#	CIO	1.4	2.2	1.4	2.1	1.4	2.1	pF	1,2,3
Input Capacitance, CK and CK#	CCK	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
Input Capacitance delta, CK and CK#	CDCK	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/Output Capacitance delta, DQS, DQS#	CDDQS	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input Capacitance, CTRL, ADD, CMD input-only pins	CI	0.75	1.2	0.75	1.2	0.75	1.2	pF	2,3,6
Input Capacitance delta, all CTRL input-only pins	CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input/Output Capacitance, all ADD/CMD input-only pins	CDI_ADD_CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/Output Capacitance delta, DQ, DM, DQS, DQS#, TDQS, TDQS#	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/Output Capacitance of ZQ pin	CZQ	-	3	-	3	-	3	pF	2,3,12

Note:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK#
5. Absolute value of CIO(DQS)-CIO(DQS#)
6. CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CDI_CTRL applies to ODT, CS# and CKE
8. CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI(CLK#))
9. CDI_ADD_CMD applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#
10. CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI(CLK#))
11. CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

10 Electrical Characteristics & AC Timing

10.1 Refresh Parameters by Device Density

Table 51 – Refresh Parameters by Device Density

Parmeter	Symbol		4Gb	Unit	Note
REF Command to ACT and REF Command time	tRFC		260	ns	
Average Periodic Refresh Interval	tREFI	0°C ≤ Tcase ≤85°C	7.8	us	
		85°C ≤ Tcase ≤95°C	3.9	us	
		95°C ≤ Tcase ≤105°C	1.95	us	

10.2 Standard Speed Bins

DDR3-1600 Speed Bin

Table 52 – DDR3-1600 Speed Bins and Operating Conditions

Speed Bin		Symbol	DDR3-1600K		Unit	Note
CL-nRCD-nRP			11-11-11			
Parmeter			Min	Max		
Internal Read Command to First data		tAA	13.75 (13.125)[5,11]	20	ns	
ACT to Internal Read or Write Delay time		tRCD	13.75 (13.125)[5,11]	-	ns	
PRE Command Period		tRP	13.75 (13.125)[5,11]	-	ns	
ACT to ACT or REF Command Period		tRC	48.75 (48.125)[5,11]	-	ns	
ACT to PRE Command Period		tRAS	35	9*tREFI	ns	
CL=5	CWL=5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,8,12,13
	CWL=6,7,8	tCK(AVG)	Reserved		ns	4
CL=6	CWL=5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL=6,7,8	tCK(AVG)	Reserved		ns	1,2,3,4,8
CL=7	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,8
			(Optional)[5,11]			
	CWL=7,8	tCK(AVG)	Reserved		ns	4
CL=8	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,8
	CWL=7,8	tCK(AVG)	Reserved		ns	4
CL=9	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,8
			(Optional)[5,11]			
	CWL=8	tCK(AVG)	Reserved		ns	4
CL=10	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,8
	CWL=8	tCK(AVG)	Reserved		ns	4
CL=11	CWL=5,6,7	tCK(AVG)	Reserved		ns	4
	CWL=8	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Setting			5,6,7,8,9,10,11		nCK	
Supported CWL Setting			5,6,7,8		nCK	

DDR3-1866 Speed Bin

Table 53 – DDR3-1866 Speed Bins and Operating Conditions

Speed Bin		Symbol	DDR3-1866M		Unit	Note
CL-nRCD-nRP			13-13-13			
Parmeter			Min	Max		
Internal Read Command to First data		tAA	13.91 (13.125)[5,11]	20	ns	
ACT to Internal Read or Write Delay time		tRCD	13.91 (13.125)[5,11]	-	ns	
PRE Command Period		tRP	13.91 (13.125)[5,11]	-	ns	
ACT to ACT or REF Command Period		tRC	47.91 (47.125)[5,11]	-	ns	
ACT to PRE Command Period		tRAS	34	9*tREFI	ns	
CL=5	CWL=5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,9
	CWL=6,7,8,9	tCK(AVG)	Reserved		ns	4
CL=6	CWL=5	tCK(AVG)	2.5	3.3	ns	1,2,3,9
	CWL=6,7,8,9	tCK(AVG)	Reserved		ns	4
CL=7	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,9
			(Optional)[5,11]			
	CWL=7,8,9	tCK(AVG)	Reserved		ns	4
CL=8	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,9
	CWL=7,8,9	tCK(AVG)	Reserved		ns	4
CL=9	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,9
			(Optional)[5,11]			
	CWL=8,9	tCK(AVG)	Reserved		ns	4
CL=10	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,9
	CWL=8,9	tCK(AVG)	Reserved		ns	4
CL=11	CWL=5,6,7	tCK(AVG)	Reserved		ns	4
	CWL=8	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CWL=9	tCK(AVG)	Reserved		ns	4
CL=12	CWL=5,6,7,8,9	tCK(AVG)	Reserved		ns	4
CL=13	CWL=5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL=9	tCK(AVG)	1.07	<1.25	ns	1,2,3
Supported CL Setting			6,7,8,9,10,11,13		nCK	
Supported CWL Setting			5,6,7,8,9		nCK	

DDR3-2133 Speed Bin

Table 54 – DDR3-2133 Speed Bins and Operating Conditions

Speed Bin		Symbol	DDR3-2133N		Unit	Note
CL-nRCD-nRP			14-14-14			
Parmeter			Min	Max		
Internal Read Command to First data		tAA	13.09	20	ns	
ACT to Internal Read or Write Delay time		tRCD	13.09	-	ns	
PRE Command Period		tRP	13.09	-	ns	
ACT to ACT or REF Command Period		tRC	46.09	-	ns	
ACT to PRE Command Period		tRAS	33	9*tREFI	ns	
CL=6	CWL=5	tCK(AVG)	2.5	3.3	ns	1,2,3,4,10
	CWL=6,7,8,9,10	tCK(AVG)	Reserved		ns	4
CL=7	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,10
			(Optional)[5,11]			
	CWL=7,8,9,10	tCK(AVG)	Reserved		ns	4
CL=8	CWL=5	tCK(AVG)	Reserved		ns	4
	CWL=6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,10
	CWL=7,8,9,10	tCK(AVG)	Reserved		ns	4
CL=9	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,10
			(Optional)[5,11]			
	CWL=8,9,10	tCK(AVG)	Reserved		ns	4
CL=10	CWL=5,6	tCK(AVG)	Reserved		ns	4
	CWL=7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,10
	CWL=8,9,10	tCK(AVG)	Reserved		ns	4
CL=11	CWL=5,6,7	tCK(AVG)	Reserved		ns	4
	CWL=8	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CWL=9,10	tCK(AVG)	Reserved		ns	4
CL=12	CWL=5,6,7,8,9,10	tCK(AVG)	Reserved		ns	4
CL=13	CWL=5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL=9	tCK(AVG)	1.07	<1.25	ns	1,2,3,4,10
	CWL=10	tCK(AVG)	Reserved		ns	4
CL=14	CWL=5,6,7,8,9	tCK(AVG)	Reserved		ns	4
	CWL=10	tCK(AVG)	0.938	<1.07	ns	1,2,3
Supported CL Setting			5,6,7,8,9,10,11,12,13,14		nCK	
Supported CWL Setting			5,6,7,8,9,10		nCK	

Note:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accodingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
12. DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
13. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
14. For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866M devices supporting down binning to DDR3-1600K or DDR3-1333H or 1066F should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRPmin (byte20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34 ns+ 13.125 ns).

10.3 Timing Parameters

Table 55 – Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	ns	6
Average Clock Period	tCK(AVG)	1.25	<1.5	1.071	<1.25	ns	
Average High Pulse Width	tCH(AVG)	0.47	0.53	0.47	0.53	tCK(AVG)	
Average Low Pulse Width	tCL(AVG)	0.47	0.53	0.47	0.53	tCK(AVG)	
Absolute Clock Period	tCK(ABS)	tCK(AVG)min + tJIT(per)min	tCK(AVG)max + tJIT(per)max	tCK(AVG)min + tJIT(per)min	tCK(AVG)max + tJIT(per)max	ps	
Absolute Clock HIGH pulse width	tCH(ABS)	0.43	-	0.43	-	tCK(AVG)	25
Absolute Clock LOW pulse width	tCL(ABS)	0.43	-	0.43	-	tCK(AVG)	26
Clock Period Jitter	JIT(per)	-70	70	-60	60	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100		ps	
Duty Cycle	tJIT(duty)	-		-		ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	-88	88	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	-105	105	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	-117	117	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	-126	126	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	-133	133	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	-139	139	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	-145	145	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	-150	150	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	-154	154	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	-158	158	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	-161	161	ps	
Cunulative error across n = 13, 14, ..., 49, 50 cycles	tERR(nper)	Min: (1 + 0.68ln(n)) * tJIT(per)_min Max: (1 + 0.68ln(n)) * tJIT(per)_max				ps	24
Data Timing							
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	100	-	85	ps	13
DQ ouput Hold time from DQS,DQS#	tQH	0.38	-	0.38	-	tCK(AVG)	13,g
DQ Low-impedance time from CK,CK#	tLZ((DQ)	-450	225	-390	195	ps	13,14,f
DQ High impedance time from CK,CK#	tHQ(DQ)	-	225	-	195	ps	13,14,f
Data Setup time to DQS,DQS# referenced to VIH(ac)/VILI(ac) level	1.5V						
	tDS(base),AC150	10	-	-	-	ps	d,17
	tDS(base),AC135	-	-	68	-	ps	d,17
	1.35V						
	tDS(base),AC135	25	-	70	-	ps	d,17
Data Setup time to DQS,DQS# referenced to VIH(ac)/VIL(ac) level	1.5V						
	tDS(base),DC100	45	-	70	-	ps	d,17
	1.35V						
	tDS(base),DC90	55	-	75	-	ps	D,17
DQ and DM Input Pulse Width for each input	tDIPW	360	-	320	-	ps	28

10.3 Timing Parameters

Parameter	Symbol	DDR3-1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(AVG)	13,19,g
DQS,DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(AVG)	11,13,g
DQS,DQS# differential output high time	tQSH	0.4	-	0.4	-	tCK(AVG)	13,g
DQS,DQS# differential output low time	tQSL	0.4	-	0.4	-	tCK(AVG)	13,g
DQS,DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(AVG)	1
DQS,DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(AVG)	1
DQS,DQS# rising edge output access time from rising CK,CK#	tDQSCK	-225	225	-195	195	ps	13,f
DQS,DQS# Low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	ps	13,14,f
DQS,DQS# High-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	ps	13,14,f
DQS,DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(AVG)	29,31
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(AVG)	30,31
DQS,DQS# rising edge to CK,CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	tCK(AVG)	c
DQS,DQS# falling edge Setup time to CK,CK# rising edge	tDSS	0.18	-	0.18	-	tCK(AVG)	c,32
DQS,DQS# falling edge Hold time from CK,CK# rising edge	tDSH	0.18	-	0.18	-	tCK(AVG)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command Delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e,18
WRITE Recovery time	tWR	15	-	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-		
ACT to internal Read or Write delay time	tRCD	See Table 52		See Table 53			e
PRE Command period	tRP	See Table 52		See Table 53			e
ACT ot ACT or REF Command period	tRC	See Table 52		See Table 53			e
CAS# to CAS# Command Delay	tCCD	4	-	4	-	nCK	
Auto Precharge Write Recovery + Precharge time	tDAL(min)	WR + roundup(tRP/tCK(AVG))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
Active to Precharge Command Period	tRAS	See Table 52		See Table 53			e
Active to Active Command period for 1KB page size	tRRD	max(4nCK, 6ns)	-	max(4nCK, 5ns)	-	ns	e
Active to Active Command period for 2KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	ns	e
Four Activate Window for 1KB page size	tFAW	30	-	27	-	ns	e
Four Activate Window for 2KB page size	tFAW	40	-	35	-	ns	e
Command and Address Setup time to CK,CK# referenced to VIH(ac)/VIL(ac) level	1.5V						
	tIS(base),AC175	45	-	-	-	ps	b,16
	tIS(base),AC150	170	-	-	-	ps	b,16,27
	tIS(base),AC125	-	-	150	-	ps	b,16

10.3 Timing Parameters

Parameter	Symbol	DDR3-1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
Command and Address Setup time to CK,CK# referenced to VIH(ac)/VIL(ac) level	1.35V						
	tIS(base),AC160	60	-	-	-	ps	b,16
	tIS(base),AC135	185	-	65	-	ps	b,16
	tIS(base),AC125	-	-	150	-	ps	b,16
Command and Address Hold time fomr CK,CK# referenced to VIH(ac)/VIL(ac) levels	1.5V						
	tIS(base),DC100	120	-	100	-	ps	b,16
	1.35V						
	tIS(base),DC90	130	-	110	-	ps	b,16
Contorl and Address Input pulse width for each input	tIPW	560	-	535	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max(512nCK, 640ns)	-	max(512nCK, 640ns)	-		
Normal Operation Full calibration time	tZQoper	max(256nCK, 320ns)	-	max(256nCK, 320ns)	-		
Normal Operation Short calibration time	tZQCS	max(64nCK, 80ns)	-	max(64nCK, 80ns)	-		23
Reset Timing							
Exist Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min)+ 10ns)	-	max(5nCK, tRFC(min)+ 10ns)	-		
Self Refresh Timings							
Exist Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min)+ 10ns)	-	max(5nCK, tRFC(min)+ 10ns)	-		
Exist Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE Low width for Self Refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) to Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) to Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Power Down Timing							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 6ns)	-	max(3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to command requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-		
CKE Minimum Pulse Width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-		
Command pass disable delay	tCPDED	1	-	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	nCK	20
Timing RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF,BL8MRS,BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(AVG))	-	WL+4+ (tWR/tCK(AVG))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF,BL8MRS,BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+ (tWR/tCK(AVG))	-	WL+2+ (tWR/tCK(AVG))	-	nCK	9

10.3 Timing Parameters

Parameter	Symbol	DDR3-1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
Timing of WRA coammd nt oPower Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-		
ODT Timing							
ODT Turn on Latency	ODTLon	WL-2 = CWL+AL-2				nCK	
ODT Turn off Latency	ODTLoff	WL-2 = CWL+AL-2				nCK	
ODT High time without Write command or with Write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-225	225	-195	195	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	Taof	0.3	0.7	0.3	0.7	tCK(AVG)	8,f
RTT Dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(AVG)	f
Write Leveling Timing							
First DQS/DQS# rising edge after Write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after Write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling Setup time from rising CK,CK# crossing to rising DQS,DQS# crossing	tWLS	165	-	140	-	ps	
Write leveling Hold time from rising DQS,DQS# crosing to rising CK,CK# crossing	tWLH	165	-	140	-	ps	
Write leveing output delay	tWLO	0	7.5	0	7.5	ns	
Write leveing output error	tWLOE	0	2	0	2	ns	

10.3 Timing Parameters

Table 56 – Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-2133		Unit	Note
		Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns	6
Average Clock Period	tCK(AVG)	0.938	<1.07	ns	
Average High Pulse Width	tCH(AVG)	0.47	0.53	tCK(AVG)	
Average Low Pulse Width	tCL(AVG)	0.47	0.53	tCK(AVG)	
Absolute Clock Period	tCK(ABS)	tCK(AVG)min + tJIT(per)min	tCK(AVG)max + tJIT(per)max	ps	
Absolute Clock HIGH pulse width	tCH(ABS)	0.43	-	tCK(AVG)	25
Absolute Clock LOW pulse width	tCL(ABS)	0.43	-	tCK(AVG)	26
Clock Period Jitter	JIT(per)	-50	50	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-40	40	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	100		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	80		ps	
Duty Cycle	tJIT(duty)	-		ps	
Cumulative error across 2 cycles	tERR(2per)	-74	74	ps	
Cumulative error across 3 cycles	tERR(3per)	-87	87	ps	
Cumulative error across 4 cycles	tERR(4per)	-97	97	ps	
Cumulative error across 5 cycles	tERR(5per)	-105	105	ps	
Cumulative error across 6 cycles	tERR(6per)	-111	111	ps	
Cumulative error across 7 cycles	tERR(7per)	-116	116	ps	
Cumulative error across 8 cycles	tERR(8per)	-121	121	ps	
Cumulative error across 9 cycles	tERR(9per)	-125	125	ps	
Cumulative error across 10 cycles	tERR(10per)	-128	128	ps	
Cumulative error across 11 cycles	tERR(11per)	-132	132	ps	
Cumulative error across 12 cycles	tERR(12per)	-134	134	ps	
Cunulative error across n = 13, 14, ..., 49, 50 cycles	tERR(nper)	Min: (1 + 0.68ln(n)) * tJIT(per)_min Max: (1 + 0.68ln(n)) * tJIT(per)_max		ps	24
Data Timing					
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	75	ps	13
DQ ouput Hold time from DQS,DQS#	tQH	0.38	-	tCK(AVG)	13,g
DQ Low-impedance time from CK,CK#	tLZ((DQ)	-360	180	ps	13,14,f
DQ High impedance time from CK,CK#	tHQ(DQ)	-	180	ps	13,14,f
Data Setup time to DQS,DQS# referenced to VIH(ac)/VILI(ac) level	1.5V				
	tDS(base),AC135	53	-	ps	17
Data Setup time to DQS,DQS# referenced to VIH(ac)/VIL(ac) level	1.5V				
	tDS(base),DC100	55	-	ps	17
DQ and DM Input Pulse Width for each input	tDIPW	280	-	ps	28
Data Strobe Timing					
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(AVG)	13,19,g
DQS,DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(AVG)	11,13,g
DQS,DQS# differential output high time	tQSH	0.38	-	tCK(AVG)	13,g
DQS,DQS# differential output low time	tQSL	0.38	-	tCK(AVG)	13,g
DQS,DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(AVG)	1
DQS,DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(AVG)	1

10.3 Timing Parameters

Parameter	Symbol	DDR3-2133		Unit	Note
		Min	Max		
Data Strobe Timing					
DQS,DQS# rising edge output access time from rising CK,CK#	tDQSCK	-180	180	ps	13,f
DQS,DQS# Low-impedance time (Referenced from RL-1)	tLZ(DQS)	-360	180	ps	13,14,f
DQS,DQS# High-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	ps	13,14,f
DQS,DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(AVG)	29,31
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(AVG)	30,31
DQS,DQS# rising edge to CK,CK# rising edge	tDQSS	-0.27	0.27	tCK(AVG)	c
DQS,DQS# falling edge Setup time to CK,CK# rising edge	tDSS	0.1	-	tCK(AVG)	c,32
DQS,DQS# falling edge Hold time from CK,CK# rising edge	tDSH	0.18	-	tCK(AVG)	c,32
Command and Address Timing					
DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to PRECHARGE Command Delay	tRTP	max(4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-		e,18
WRITE Recovery time	tWR	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	nCK	
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-		
ACT to internal Read or Write delay time	tRCD	See Table 54			e
PRE Command period	tRP	See Table 54			e
ACT ot ACT or REF Command period	tRC	See Table 54			e
CAS# to CAS# Command Delay	tCCD	4	-		
Auto Precharge Write Recovery + Precharge time	tDAL(min)	WR + roundup(tRP/tCK(AVG))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	22
Active to Precharge Command Period	tRAS	See Table 54			e
Active to Active Command period for 1KB page size	tRRD	max(4nCK, 6ns)	-	ns	e
Active to Active Command period for 2KB page size	tRRD	max(4nCK, 7.5ns)	-	ns	e
Four Activate Window for 1KB page size	tFAW	25	-	ns	e
Four Activate Window for 2KB page size	tFAW	35	-	ns	e
Command and Address Setup time to CK,CK# referenced to VIH(ac)/VIL(ac) level	1.5V				
	tIS(base),AC125	135	-	ps	b,16
Command and Address Hold time form CK,CK# referenced to VIH(ac)/VIL(ac) levels	1.5V				
	tIS(base),DC100	95	-	ps	b,16
Control and Address Input pulse width for each input	tIPW	470	-	ps	28
Calibration Timing					
Power-up and RESET calibration time	tZQinit	max(512nCK, 640ns)	-		
Normal Operation Full calibration time	tZQoper	max(256nCK, 320ns)	-		
Normal Operation Short calibration time	tZQCS	max(64nCK, 80ns)	-		23
Reset Timing					
Exist Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min)+10ns)	-		

10.3 Timing Parameters

Parameter	Symbol	DDR3-2133		Unit	Note
		Min	Max		
Self Refresh Timings					
Exist Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min)+10ns)	-		
Exist Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK	
Minimum CKE Low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) to Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) to Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-		
Power Down Timing					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to command requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-		
CKE Minimum Pulse Width	tCKE	max(3nCK, 5ns)	-		
Command pass disable delay	tCPDED	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK	20
Timing RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF,BL8MRS,BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(AVG))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF,BL8MRS,BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(AVG))	-	nCK	9
Timing of WRA coammd nt oPower Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1		nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1		nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)			
ODT Timing					
ODT Turn on Latency	ODTLon	WL-2 = CWL+AL-2		nCK	
ODT Turn off Latency	ODTLoff	WL-2=CWL+AL-2		nCK	
ODT High time without Write command or with Write command and BC4	ODTH4	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn-off delay (Power Down with DLL frozen)	tAOFPD	2	8.5	ns	
RTT turn-on	tAON	-180	180	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(AVG)	8,f
RTT Dynamic change skew	tADC	0.3	0.7	tCK(AVG)	f

10.3 Timing Parameters

Parameter	Symbol	DDR3-2133		Unit	Note
		Min	Max		
Write Leveling Timing					
First DQS/DQS# rising edge after Write leveling mode is programmed	tWLMRD	40	-	nCK	3
DQS/DQS# delay after Write leveling mode is programmed	tWLDQSEN	25	-	nCK	3
Write leveling Setup time from rising CK,CK# crossing to rising DQS,DQS# crossing	tWLS	125	-	ps	
Write leveling Hold time from rising DQS,DQS# crosing to rising CK,CK# crossing	tWLH	125	-	ps	
Write leveing output delay	tWLO	0	7.5	ns	
Write leveing output error	tWLOE	0	2	ns	

10.3.1 Jitter Note:

a) Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

b) These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

c) These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

d) These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.

e) For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

f) When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993ps and tLZ(DQ),max(derated) = 400 ps + 172ps = + 572 ps. (Caution on the min/max usage!)

Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <=12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

g) When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

10.3.2 Timing Parameter Note:

1. Actual value dependant upon measurement level definitions See Figure 45 — “Method for calculating tWPRE transitions and endpoints” and See Figure — “Method for calculating tWPST transitions and endpoints”.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON See “Timing Parameters”.
8. For definition of RTT turn-off time tAOF See “Timing Parameters”.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure 28 — “Clock to Data Strobe Relationship”
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Address / Command Setup, Hold and Derating”
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 13.6 “Data Setup, Hold and Slew Rate Derating”.
18. Start of internal write transaction is defined as follows:

    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Figure — “Clock to Data Strobe Relationship”
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications - Case 2”
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / oC, VSens = 0.15% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.