IM2G08D2DBB
2Gbit DDR2 SDRAM
8 BANKS X 32Mbit X 8

Ordering Speed Code	-25
	DDR2-800
Clock Cycle Time (t_{CK3})	5 ns
Clock Cycle Time (t_{CK4})	3.75 ns
Clock Cycle Time (t_{CK5})	2.5 ns
Clock Cycle Time (t_{CK6})	2.5 ns
System Frequency (f_{CK} max)	400 MHz

Features

- High speed data transfer rates with system frequency up to 400 MHz
- Programmable $\overline{\text{CAS}}$ Latency: 3, 4, 5 and 6
- Programmable Additive Latency: 0, 1, 2, 3, 4 and 5
- Write Latency = Read Latency -1
- JEDEC Power Supply 1.8V ± 0.1V
- V_{DDQ} = 1.8V ± 0.1V
- Available in 60-ball FBGA for x8 component
- Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- 8 internal banks for concurrent operation
- 4-bit Prefetch Architecture
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 4 and 8
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- ODT (On-Die Termination)
- Weak Strength Data-Output Driver Option
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- $\overline{\text{DQS}}$ can be disabled for single-ended data strobe
- Read Data Strobe (RDQS) supported (x8 only)
- PASR Partial Array Self Refresh
- t_{RAS} lockout supported
- Refresh Interval:
  - Average refresh period:
    7.8 us at -40°C ≤ Tcase ≤ 85°C
    3.9 us at 85°C ≤ Tcase ≤ 95°C
- Operating case temperature range
  - Commercial Tcase = 0°C to 95°C
  - Industrial Tcase = -40°C to 95°C
- RoHS complaint

Option *Marking*

- Configuration
  - 256Mx8 (8 Banks x 32Mbit x 8) — 2G08
- Package
  - 60-ball FBGA (8mm x 10mm) for x8 — B
- Leaded/Lead-free
  - Leaded — <blank>
  - Lead-free/RoHS — G
- Speed/Cycle Time
  - 2.5 ns @ CL5 (DDR2-800) — -25
- Temperature
  - Commercial 0°C to 95°C Tcase — <blank>
  - Industrial -40°C to 95°C Tcase — I

Example Part Number: IM2G08D2DBBG-25I

Description

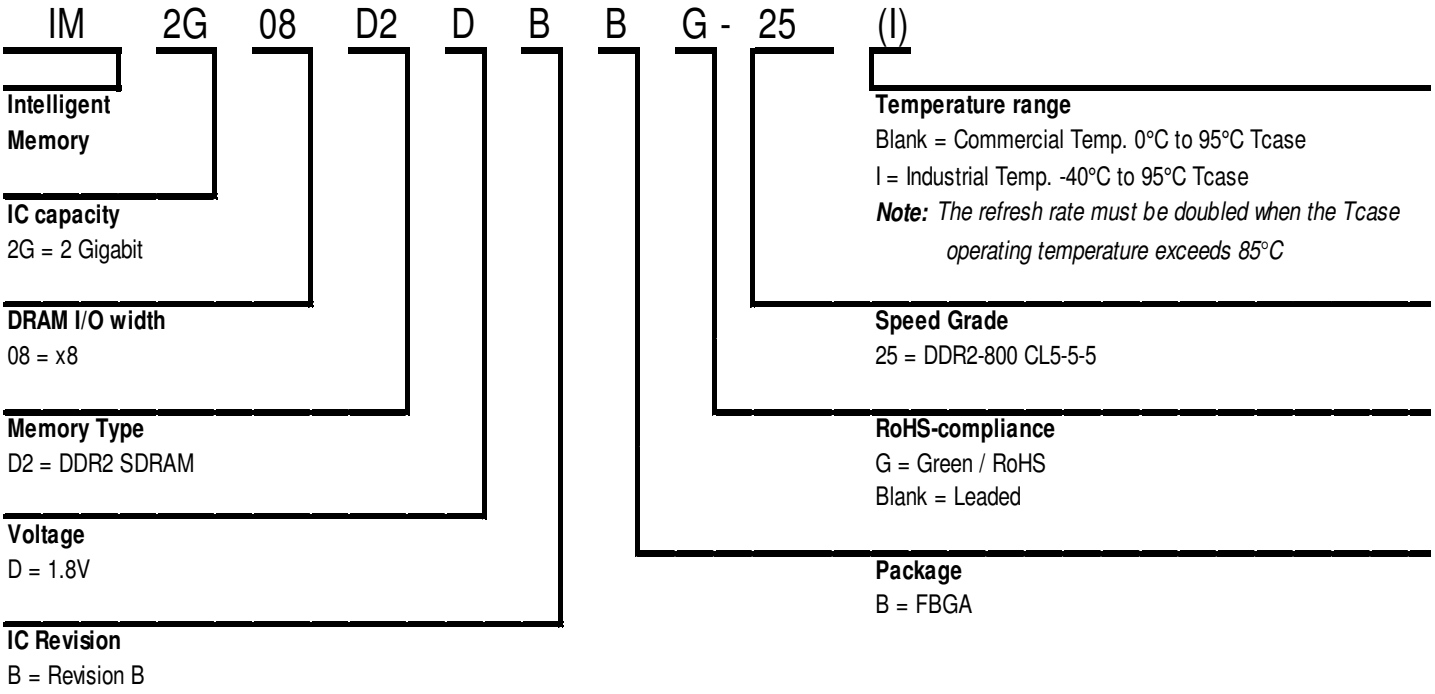
The IM2G08D2DBB is a eight banks DDR2 DRAM organized as 8 banks x 32Mbit x 8. The IM2G08D2DBB achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The chip is designed to comply with the following key DDR2 SDRAM features:(1) posted CAS with additive latency, (2) write latency = read latency-1, (3) On Die Termination.

All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/Os are synchronized with a pair of bidirectional strobes (DQS, $\overline{\text{DQS}}$) in a source synchronous fashion.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Part Number Information



2Gb DDR2 SDRAM Addressing

Configuration	**256Mb x 8**
# of Bank	8
Bank address	BA0 ~ BA2
Auto precharge	A10/AP
Row Address	A0 ~ A14
Column Address	A0 ~ A9
Page size	1 KB

Pin Configurations

60-ball FBGA (x8 configuration)

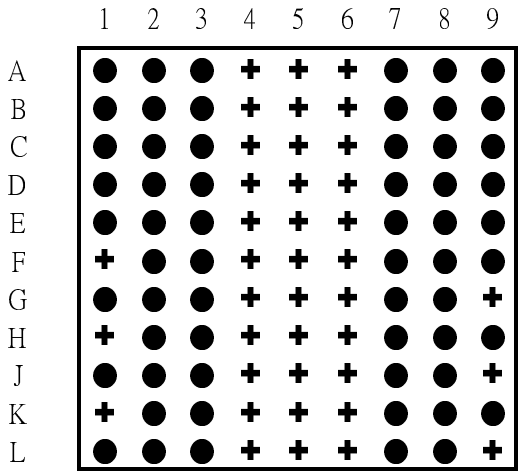
	1	2	3	4	5	6	7	8	9	
A	V_{DD}	NU/$\overline{RDQS}$	V_{SS}				V_{SSQ}	$\overline{DQS}$	V_{DDQ}	A
B	DQ6	V_{SSQ}	DM/RDQS				DQS	V_{SSQ}	DQ7	B
C	V_{DDQ}	DQ1	V_{DDQ}				V_{DDQ}	DQ0	V_{DDQ}	C
D	DQ4	V_{SSQ}	DQ3				DQ2	V_{SSQ}	DQ5	D
E	V_{DDL}	V_{REF}	V_{SS}				V_{SSDL}	CK	V_{DD}	E
F		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT	F
G	BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS}$		G
H		A10/AP	A1				A2	A0	V_{DD}	H
J	V_{SS}	A3	A5				A6	A4		J
K		A7	A9				A11	A8	V_{SS}	K
L	V_{DD}	A12	A14				NC	A13		L

Ball Location (x8)

- ● Populated ball
- ✚ Ball not populated

Top view

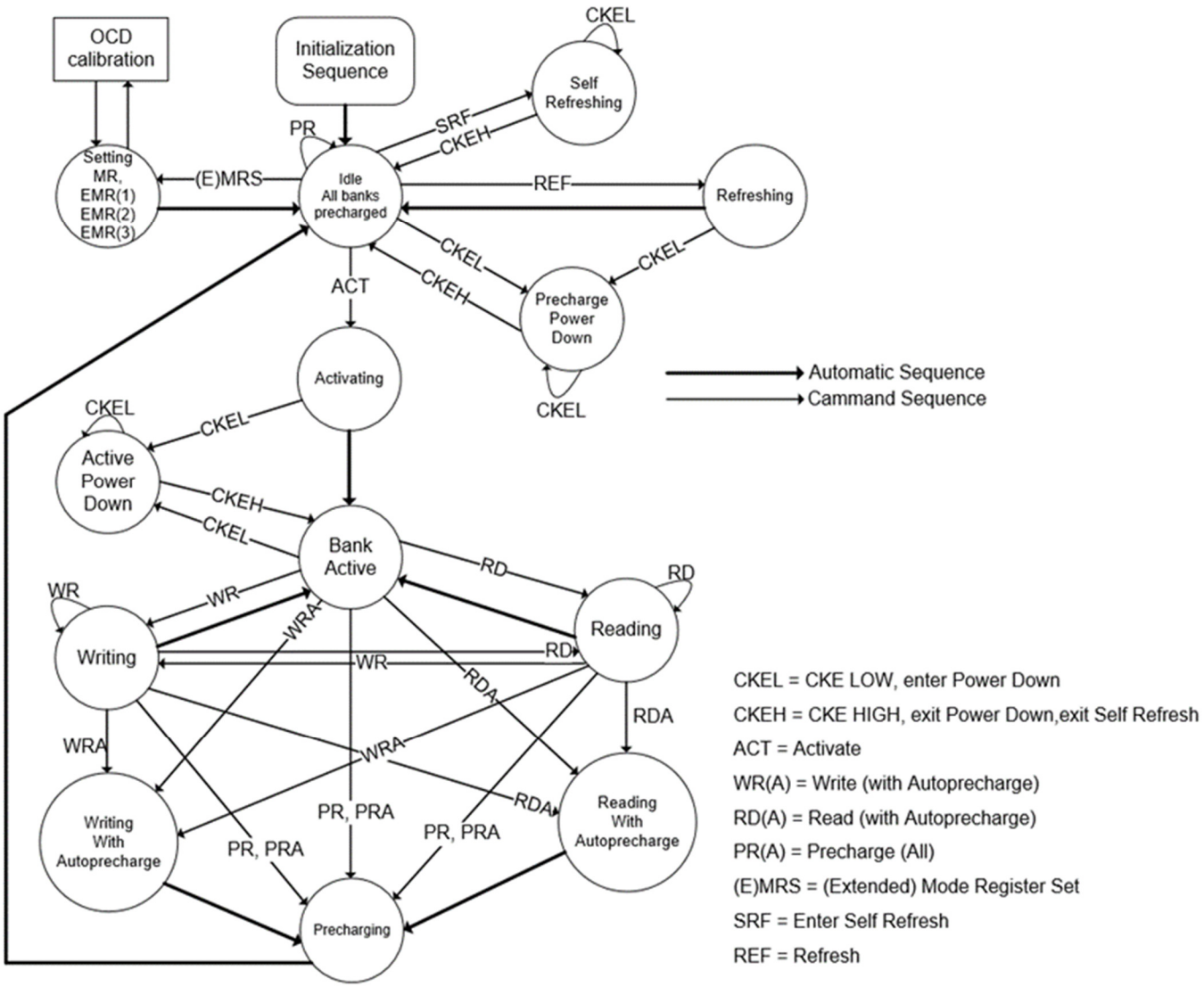
(See the balls through the package)



Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A14	Input	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA14) when sampled at the rising clock edge for x8 device. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends on the SDRAM organization: 256M x 8 DDR CAn = CA9 In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0, BA1 and BA2 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0, BA1 and BA2.
BA0 - BA2	Input	Selects which bank is to be active.
DQx	Input/ Output	Data Input/Output pins operate in the same manner as on conventional DRAMs. DQ0-DQ7 for x8 device.
DQS, $\overline{DQS}$ RDQS, $\overline{RDQS}$	Input/ Output	Data Strobe, output with read data, input with write data. Edge-aligned with read data, centered in write data. For x8 device, an RDQS option using DM pin can be enabled via the EMRS(1) to simply read timing. The data strobes DQS and RDQS may be used in single ended mode or paired with optional complimentary signals $\overline{DQS}$ and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
DM	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled high along with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading is designed to match that of DQ and DQS pins. For x8 device, the function of DM of RDQS/$\overline{RDQS}$ is enabled by EMRS command.
V_{DD}, V_{SS}	Supply	Power and ground for the input buffers and the core logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Input	SSTL Reference Voltage for Inputs.
V_{DDL}, V_{SSDL}	Supply	Isolated power supply and ground for the DLL to provide improved noise immunity.
ODT	Input	On Die Termination Enable. It enables termination resistance internal to the DRAM. ODT is applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ and DM for x8 device. ODT will be ignored if EMRS disable the function.

Simplified State Diagram



Note: Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit – among other things – are not captured in full detail.

Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

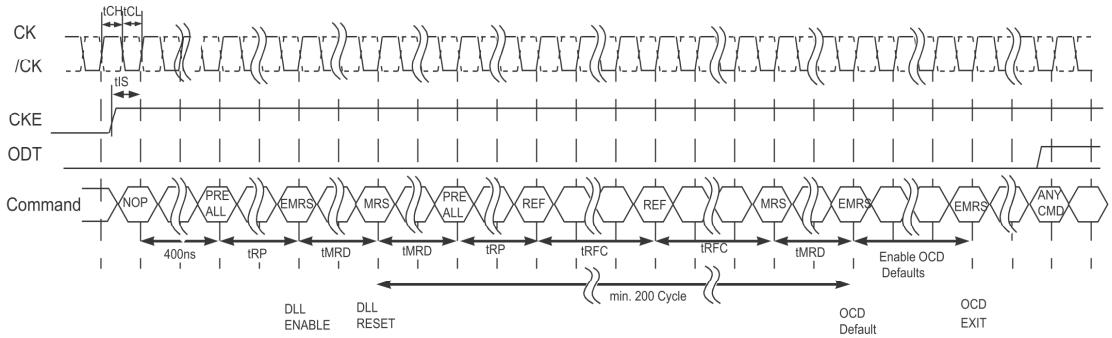
1. Apply power and attempt to maintain CKE below 0.2*V_{DDQ} and ODT[*1] at a low state (all other inputs may be undefined).
   - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output, AND
   - V_{TT} is limited to 0.95V max, AND
   - V_{REF} tracks V_{DDQ}/2.

   or
   - Apply V_{DD} before or at the same time as V_{DDL}.
   - Apply V_{DDL} before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} before or at the same time as V_{TT} & V_{REF}.

   at least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition.
3. For the minimum of 200us after stable power and clock (CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and A12)
8. Issue a Mode Register Set command for “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (To program operating parameters without resetting the DLL)
12. At least 200 clocks after step 8, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

*1 To guarantee ODT off, V_{REF} must be valid and a low level must be applied to the ODT pin.

Initialization Sequence after Power Up



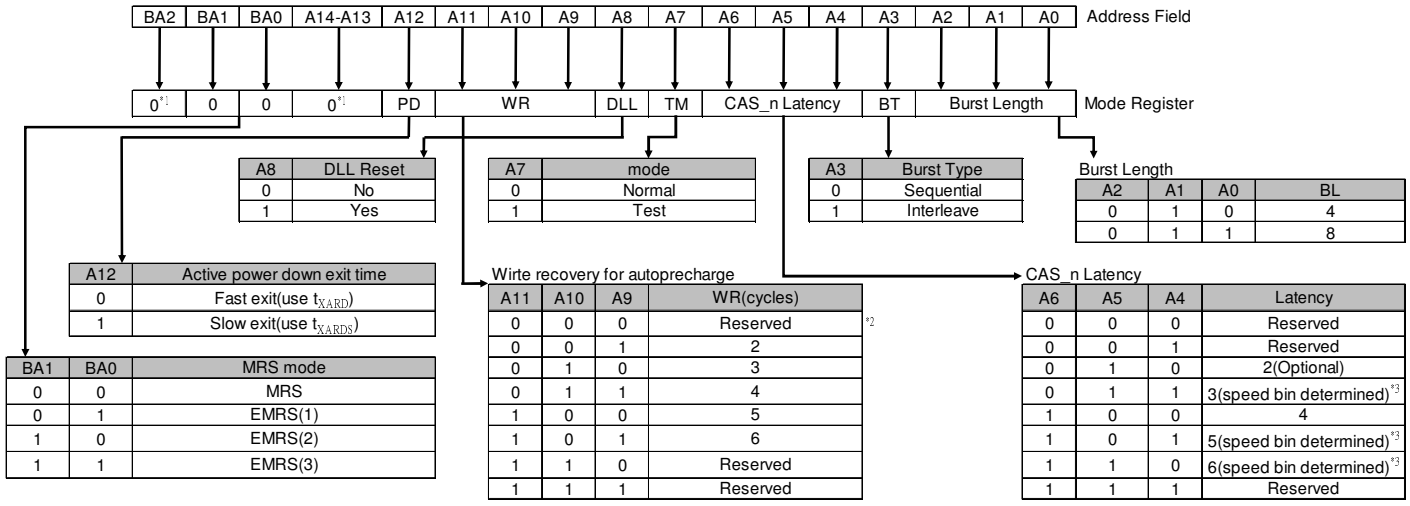
Programming the Mode Register

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time (t_{WR}) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, single-ended strobe and ODT (On Die Termination) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, WR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 - A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{CAS}$ latency is defined by A4 - A6. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A9 - A11. Refer to the table for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit(use t_{XARD})
1	Slow exit(use t_{XARDS})

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3)

Wirte recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved *2
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

CAS_n Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3(speed bin determined) *3
1	0	0	4
1	0	1	5(speed bin determined) *3
1	1	0	6(speed bin determined) *3
1	1	1	Reserved

*1: BA2 and A13-A14 are reserved for future use and must be programmed to 0 when setting the mode register.

*2: WR(write recovery for autoprecharge) min is determined by t_{CK} max and WR max is determined by t_{CK} min.
WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = t_{WR}(ns)/t_{CK}(ns)).

*3: Speed bin determined. Not required on all speed bins.

DDR2 SDRAM Extended Mode Register Set

EMRS(1)

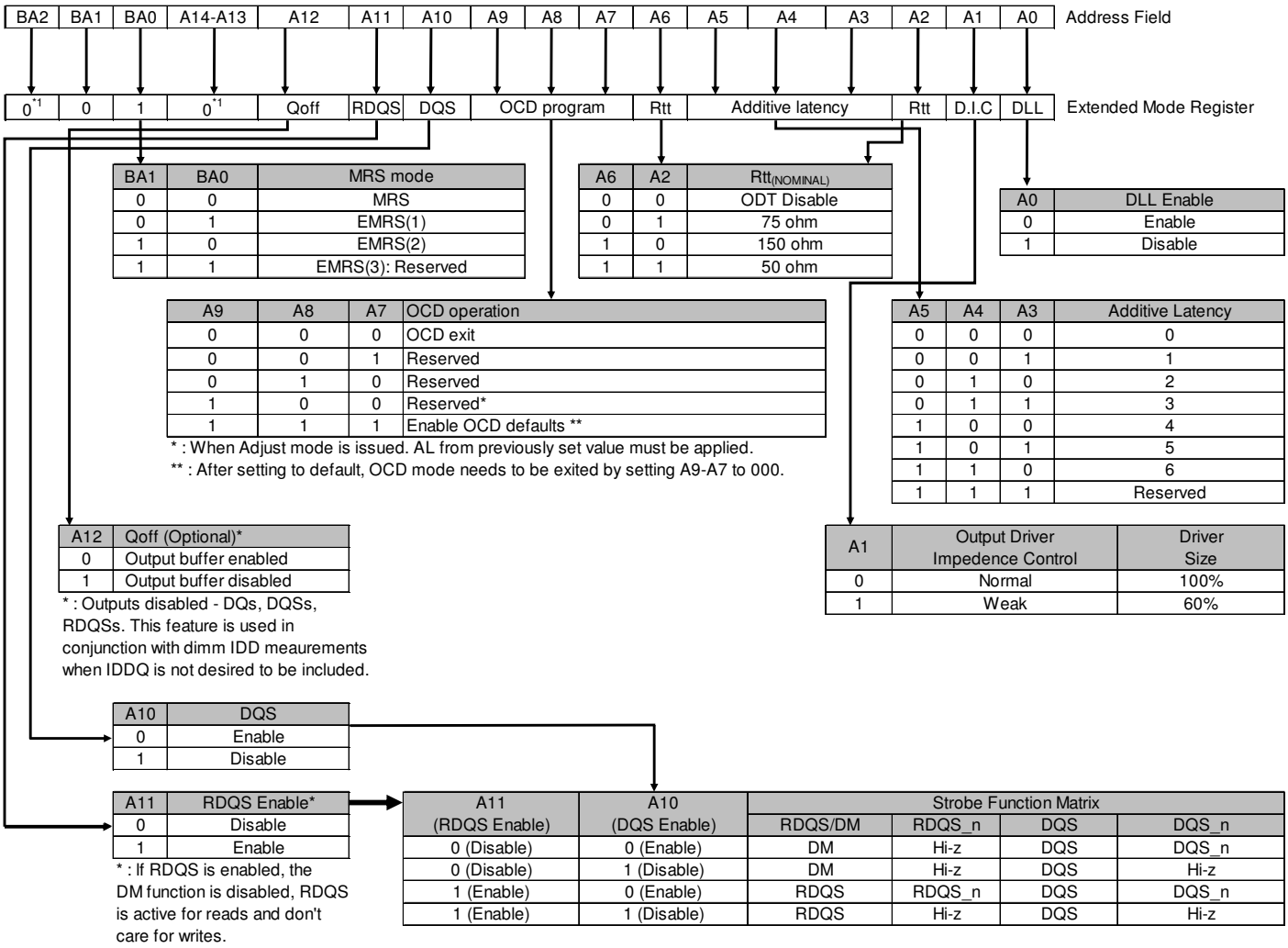
The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. Extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0 and low on BA1, and controlling rest of pins A0 ~ A13.

The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling reduced strength data-output drive. A3 ~ A5 determines the additive latency. A2 and A6 are used for ODT value selection, A7 ~ A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable.

DLL Enable / Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.

EMRS(1) Programming



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

A6	A2	$Rtt_{(NOMINAL)}$
0	0	ODT Disable
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD operation
0	0	0	OCD exit
0	0	1	Reserved
0	1	0	Reserved
1	0	0	Reserved*
1	1	1	Enable OCD defaults **

* : When Adjust mode is issued. AL from previously set value must be applied.
** : After setting to default, OCD mode needs to be exited by setting A9-A7 to 000.

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A12	Qoff (Optional)*
0	Output buffer enabled
1	Output buffer disabled

* : Outputs disabled - DQs, DQSs, RDQSs. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	DQS
0	Enable
1	Disable

A11	RDQS Enable*
0	Disable
1	Enable

* : If RDQS is enabled, the DM function is disabled, RDQS is active for reads and don't care for writes.

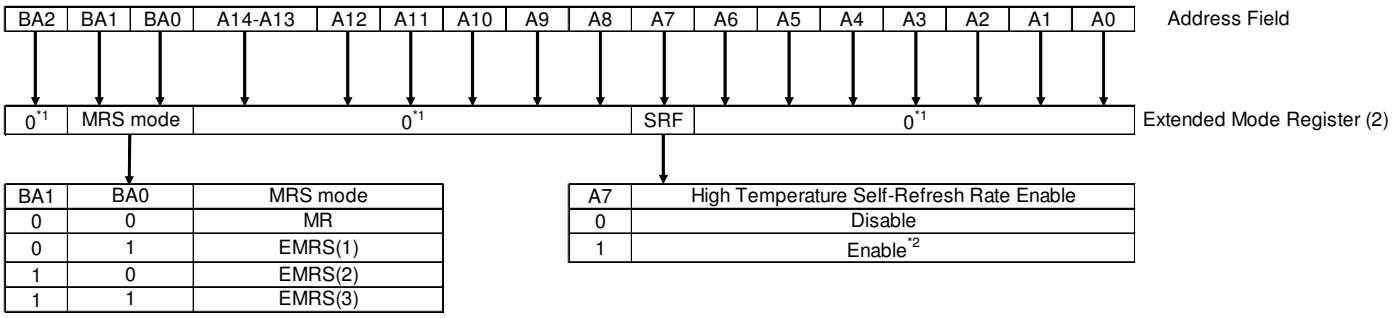
A11 (RDQS Enable)	A10 (DQS Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS_n	DQS	DQS_n
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS_n
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS_n	DQS	DQS_n
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

*1: BA2 and A13-A14 are reserved for future use and must be programmed to 0 when setting the mode register.

EMRS(2)

The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be programmed during initialization for proper operation. The extended mode register(2) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, HIGH on BA1 and LOW on BA0, while controlling the states of address pins A0-A15. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the extended mode register(2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

EMRS(2) Programming



BA1	BA0	MRS mode
0	0	MR
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3)

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable*2

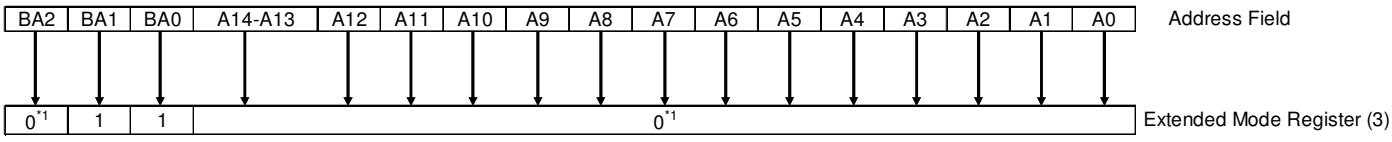
*1: BA2 and A0-A6, A8-A14 are reserved for future use and must be programmed to 0 when setting the mode register.

*2 : As industry adoption of high temperature parts proceeds, users need to determine if a DRAM supports High Temperature Self-Refresh Rate Enable mode before attempting to use it in that mode. JEDEC standard DDR2 SDRAM Module user can look at DDR2 SDRAM Module SPD field Byte 49 bit [0]. If the high temperature self-refresh mode is supported then controller can set the EMR(2)[A7] bit to enable the self-refresh rate in case of higher than 85 oC temperature self-refresh operation. For the loose part user, please refer to DRAM Manufacturer's part number and data sheet to check the high temperature self-refresh rate availability.

EMRS(3)

No function is defined in extended mode register(3). The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

EMRS(3) Programming

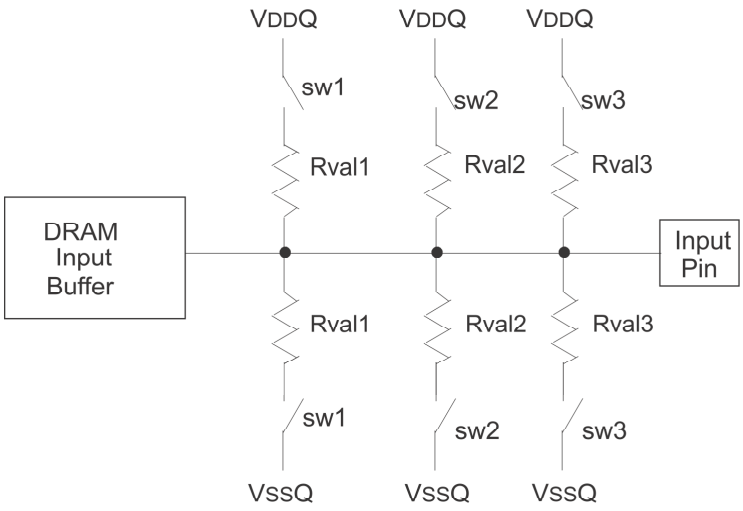


*1: BA2 and A0- A14 are reserved for future use and must be programmed to 0 when setting the mode register.

ODT (on-die termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$ and DM signal for x8 configurations via the ODT control pin.
The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.



Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by “Rtt (nominal)” in EMR.
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

Functional representation of ODT

ODT Truth Table

The ODT Truth Table shows which of the input pins are terminated depending on the state of address bit A10 and A11 in the EMRS. To activate termination of any of these pins, the ODT function has to be enabled in the EMRS by address bits A6 and A2.

Input Pin	EMRS	EMRS
	Address Bit A10	Address Bit A11
x8 components:		
DQ0 ~ DQ7	X	X
DQS	X	X
$\overline{\text{DQS}}$	0	X
RDQS	X	1
$\overline{\text{RDQS}}$	0	1
DM	X	0

X = Don’t Care
0 = Signal Low
1 = Signal High

DC Electrical Characteristics and Operation Conditions:

Parameter / Condition	Symbol	Min.	Nom.	Max.	Units	Notes
Rtt eff. impedance value for EMRS(A6,A2)= 0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt eff. impedance value for EMRS(A6,A2)= 1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt eff. impedance value for EMRS(A6,A2)= 1,1; 50 ohm	Rtt3(eff)	40	50	60	ohm	1,2
Deviation of VM with respect to $V_{DDQ}/2$	delta VM	-6		+6	%	1,3

1) Test condition for Rtt measurements

2) Optional for DDR2-400/533/667, mandatory for DDR2-800.

Measurement Definition for Rtt(eff): Apply $V_{IH}(ac)$ and $V_{IL}(ac)$ to test pin separately, then measure current $I(V_{IH}(ac))$ and $I(V_{IL}(ac))$ respectively. $V_{IH}(ac)$, $V_{IL}(ac)$, and V_{DDQ} values defined in SSTL_18

$$Rtt(eff) = \frac{\mathrm{VIHac} - \mathrm{VILac}}{\mathrm{I(VIHac)} - \mathrm{I(VILac)}}$$

3) Measurement Definition for VM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\left(\frac{2 \times \mathrm{VM}}{\mathrm{VDDQ}}\right) - 1\right) \times 100\%$$

AC Electrical Characteristics and Operation Conditions: For speed 800

Symbol	Parameter / Condition	Min.	Max.	Units	Notes
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	1
t_{AON}	ODT turn-on	t_{AC}(min)	t_{AC}(max) + 0.7	ns	1,3,4
t_{AONPD}	ODT turn-on (Power Down Mode)	t_{AC}(min)+2	2 t_{CK}+ t_{AC}(max)+1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	2,6
t_{AOF}	ODT turn-off	t_{AC}(min)	t_{AC}(max)+0.6	ns	2,5,6
t_{AOFPD}	ODT turn-off (Power Down Mode)	t_{AC}(min)+2	2.5 t_{CK}+ t_{AC}(max)+1	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	X	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8		t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max. is when the ODT resistance is fully on. Both are measured from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn-off ODT resistance.
ODT turn off time max. is when the bus is in high impedance. Both are measured from t_{AOFD}.

3) Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns.

4) When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{ERR}(6-10per) of the input clock.

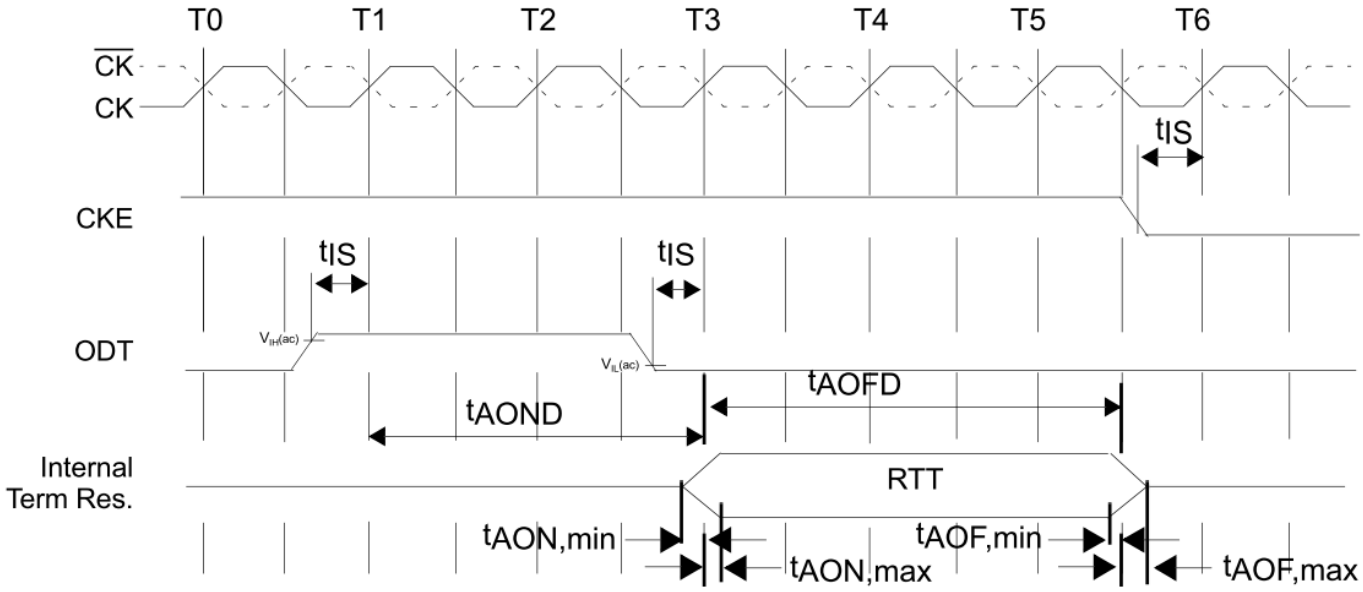
5) When the device is operated with input clock jitter, this parameter needs to be derated by { - t_{JIT}(duty),max - t_{ERR}(6-10per),max } and { - t_{JIT}(duty),min - t_{ERR}(6-10per),min } of the actual input clock.

6) For t_{AOFD} of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assume a t_{CH}(avg), average input clock HIGH pulse width of 0.5 relative to t_{CK}(avg). t_{AOF},min and t_{AOF},max should each be derated by the same amount as the actual amount of t_{CH}(avg) offset present at the DRAM input with respect to 0.5. Note that these deratings are in addition to the t_{AOF} derating per input clock jitter, i.e. t_{JIT}(duty) and t_{ERR}(6-10per). However t_{AC} values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for t_{AOF} are;

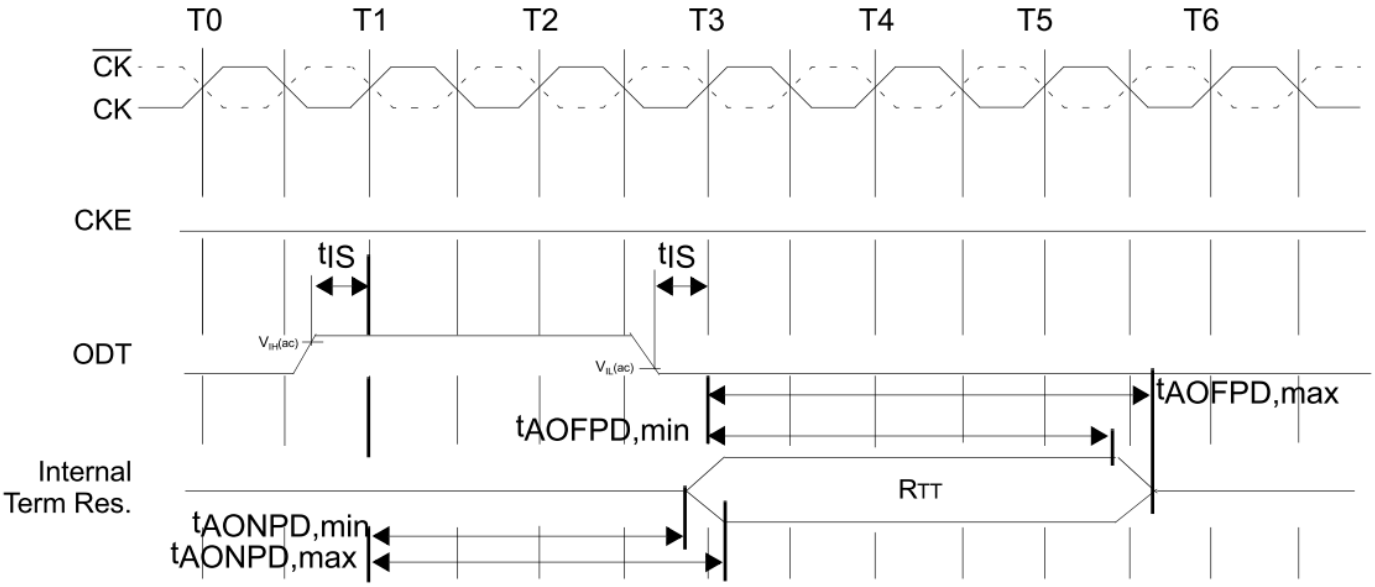
t_{AOF},min(derated_final) = t_{AOF},min(derated) + { - t_{JIT}(duty),max – t_{ERR}(6-10per),max }

t_{AOF},max(derated_final) = t_{AOF},max(derated) + { - t_{JIT}(duty),min – t_{ERR}(6-10per),min }

ODT timing for active/standby mode



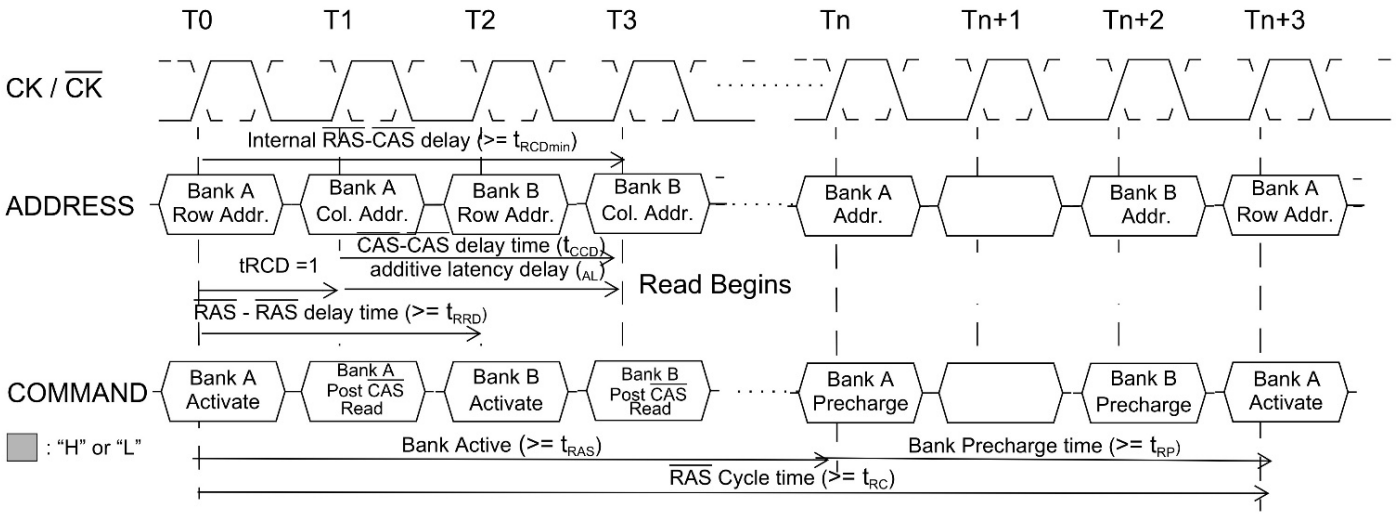
ODT timing for power-down mode



Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses of BA0 - BA2 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for x8 organised components. For x16 components, row addresses A0 through A12 have to be applied.
The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the t_{RCD} min specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure t_{RCD} min is satisfied. Additive latencies of 0,1,2,3,4,5 and 6 are supported.
Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} respectively.
The minimum time interval between successive Bank Activate commands to the same bank is determined (t_{RC}). The minimum time interval between Bank Active commands, to any other bank, is the Bank A to Bank B delay time (t_{RRD}).

Bank Active Command Cycle: t_{RCD} = 3, AL = 2, t_{RP} = 3, t_{RRD} = 2, t_{CCD} = 2



Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a wide variety of fast access modes. The boundary of the burst cycle is restricted to specific segments of the page length.

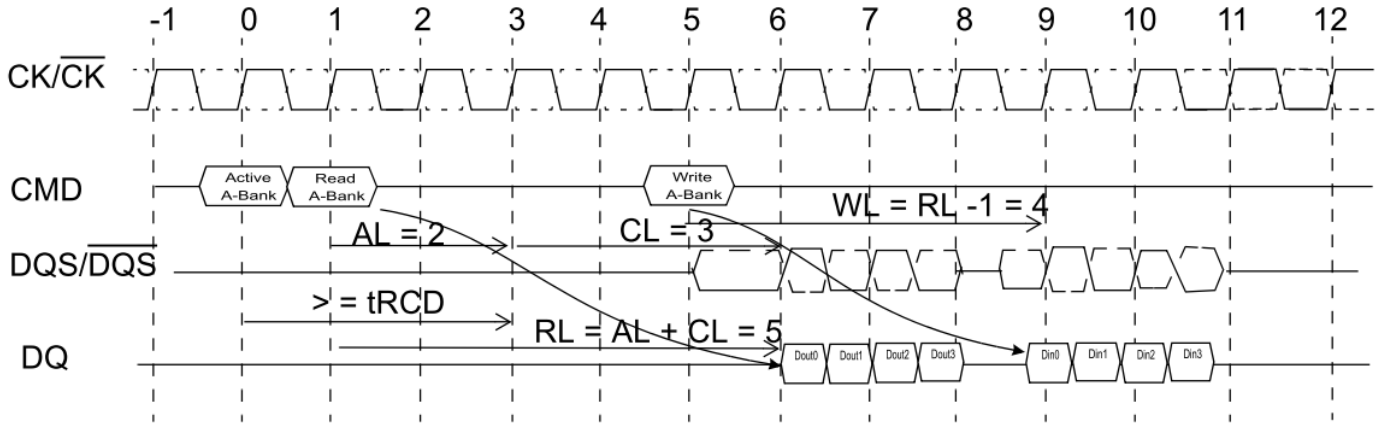
A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is 4 clocks for read or write cycles. Burst interruption is allowed with 8 bit burst operation. For details see the "Burst Interrupt" - Section of this datasheet.

Posted $\overline{CAS}$

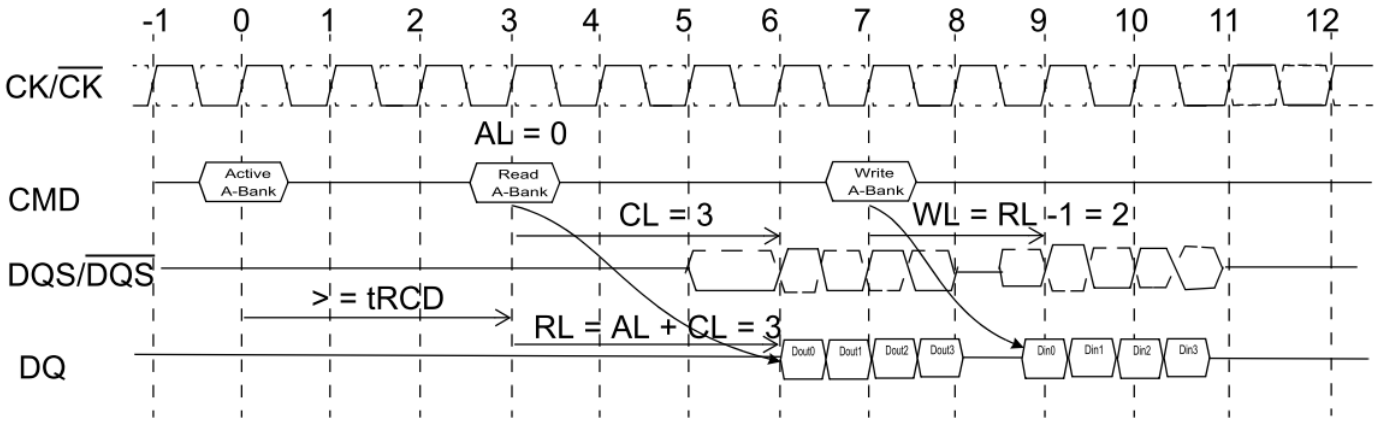
Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the t_{RCD}min, then AL greater than 0 must be written into the EMRS. The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{CAS}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the t_{RCD}min period, the Read Latency is also defined as RL = AL + CL.

Read followed by a write to the same bank,
where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4



[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Read followed by a write to the same bank,
where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4



AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst-mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the “Burst Interruption” section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

Burst length	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4	X 0 0	0, 1, 2, 3	0, 1, 2, 3
	X 0 1	1, 2, 3, 0	1, 0, 3, 2
	X 1 0	2, 3, 0, 1	2, 3, 0, 1
	X 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Notes:

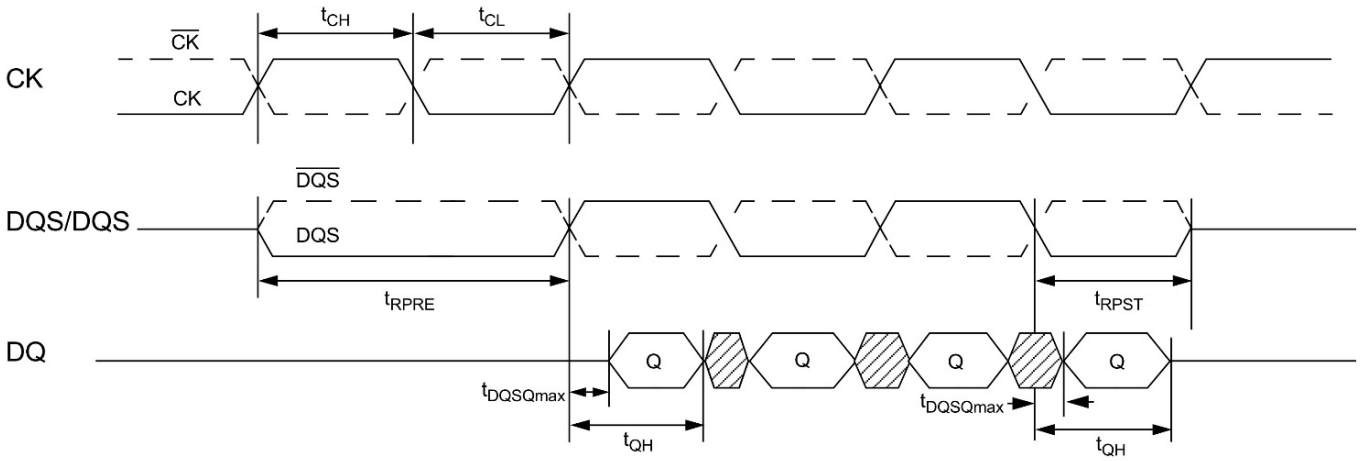
1) Page length is a function of I/O organization and column addressing.

2) Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components.

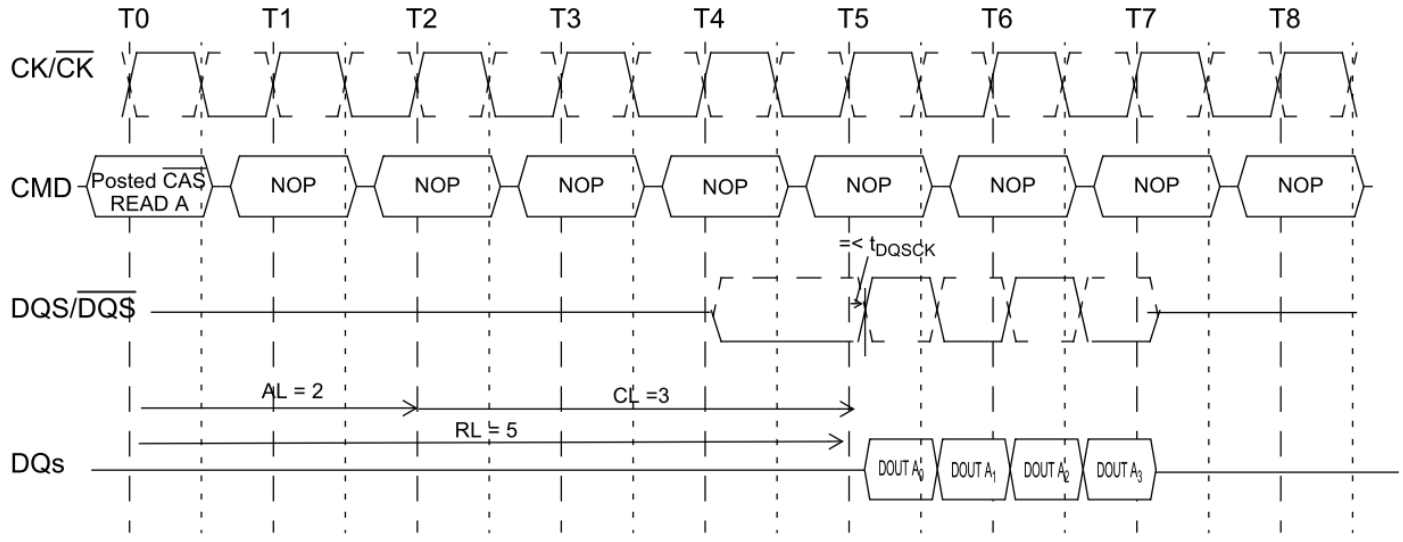
Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each sub-sequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS).

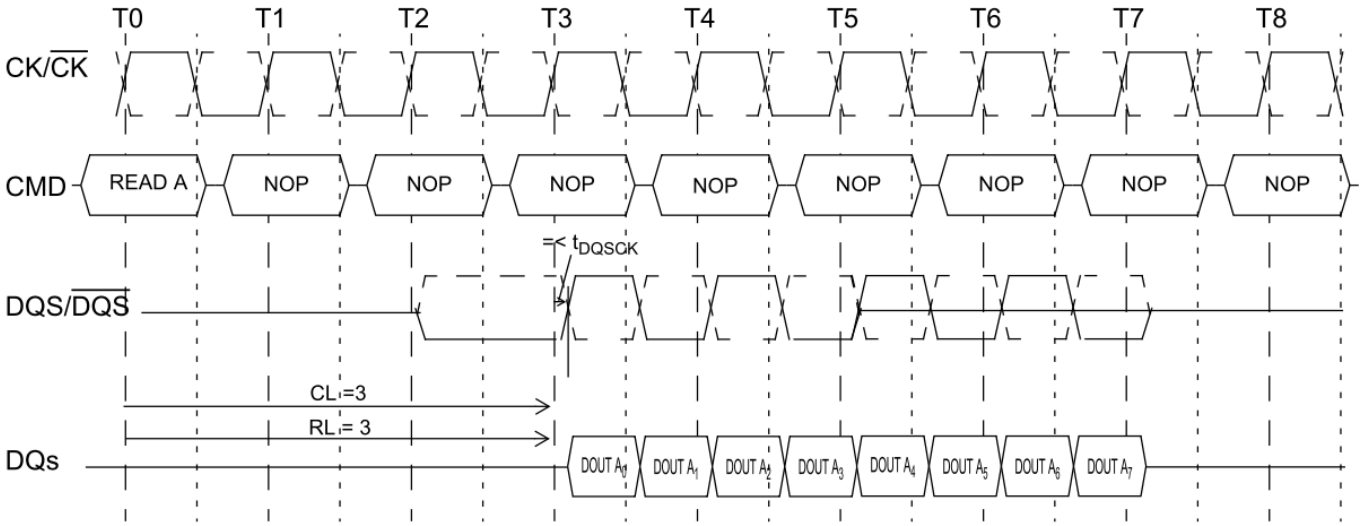
Data output (read) timing



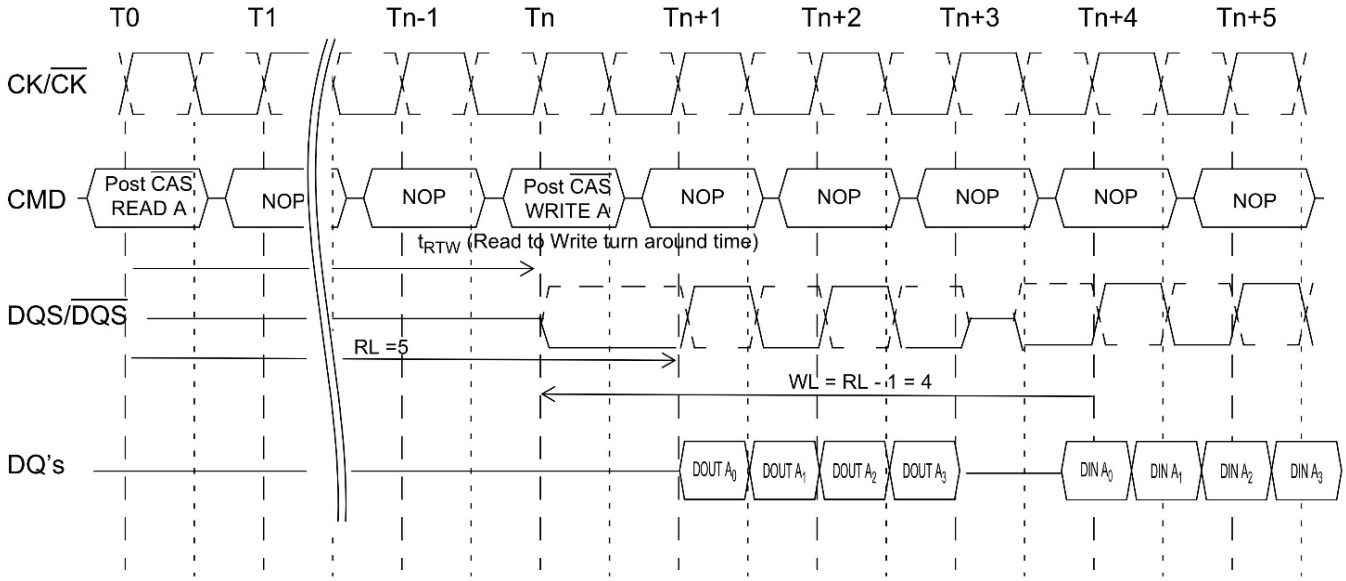
Burst read operation: RL = 5 (AL = 2, CL = 3, BL = 4)



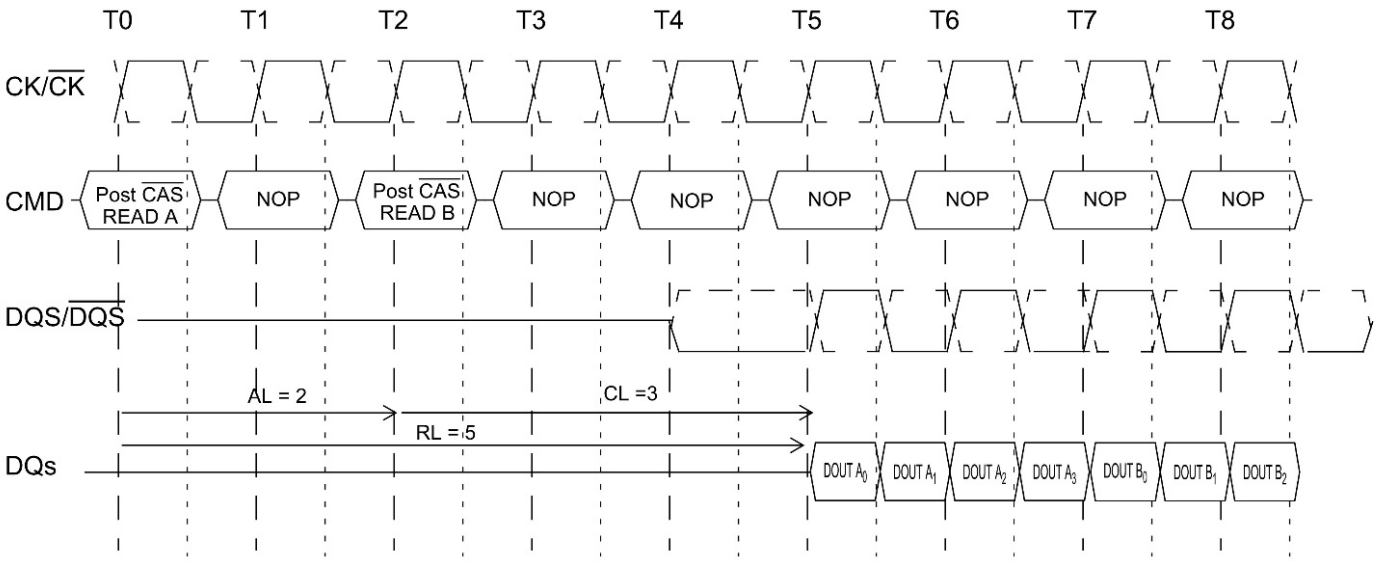
Burst read operation: RL = 3 (AL = 0, CL = 3, BL = 8)



Burst read followed by burst write: RL = 5, WL = (RL-1) = 4, BL = 4



Seamless burst read operation: RL = 5, AL = 2, and CL = 3, BL = 4

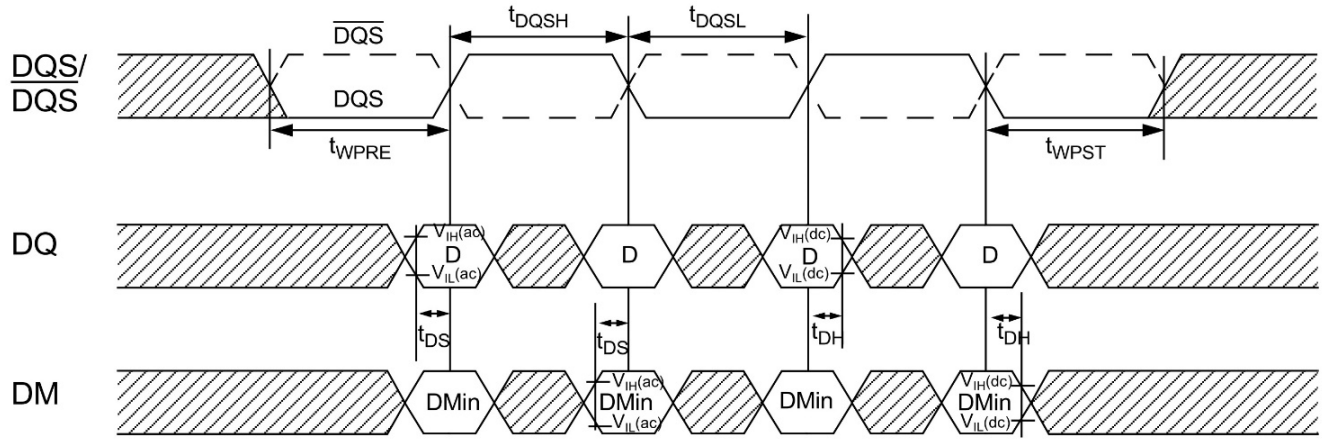


The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

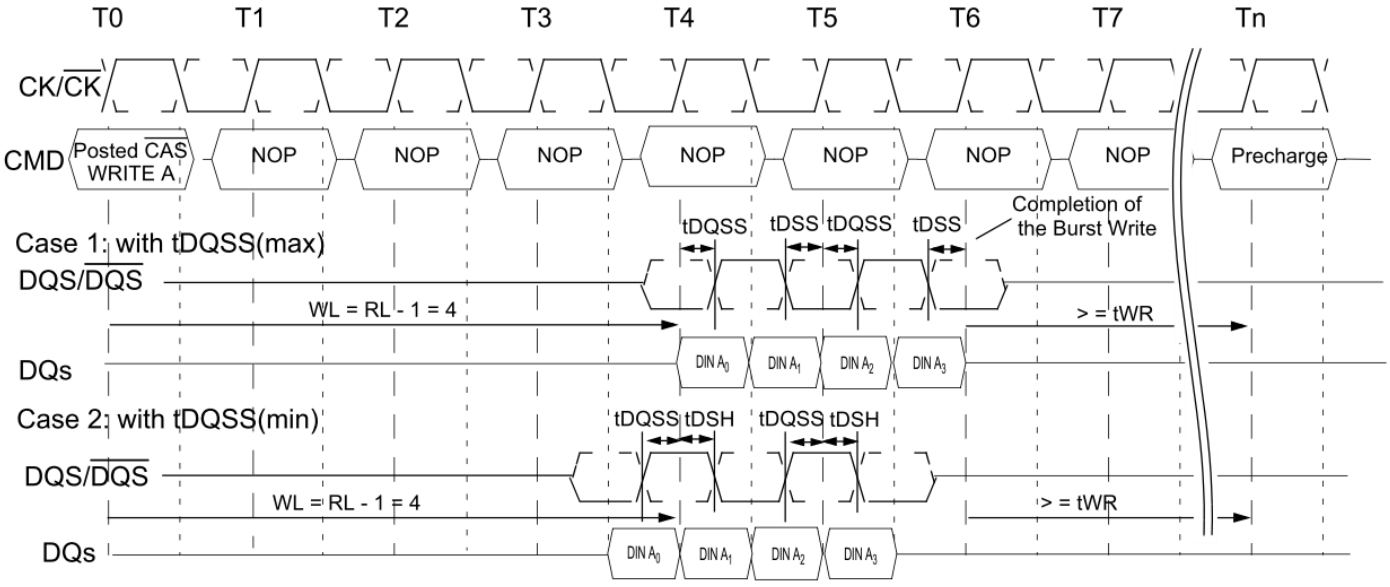
Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named “write recovery time” (t_{WR}) and is the time needed to store the write data into the memory array. t_{WR} is an analog timing parameter (see the AC table in this specification) and is not the programmed value for WR in the MRS.

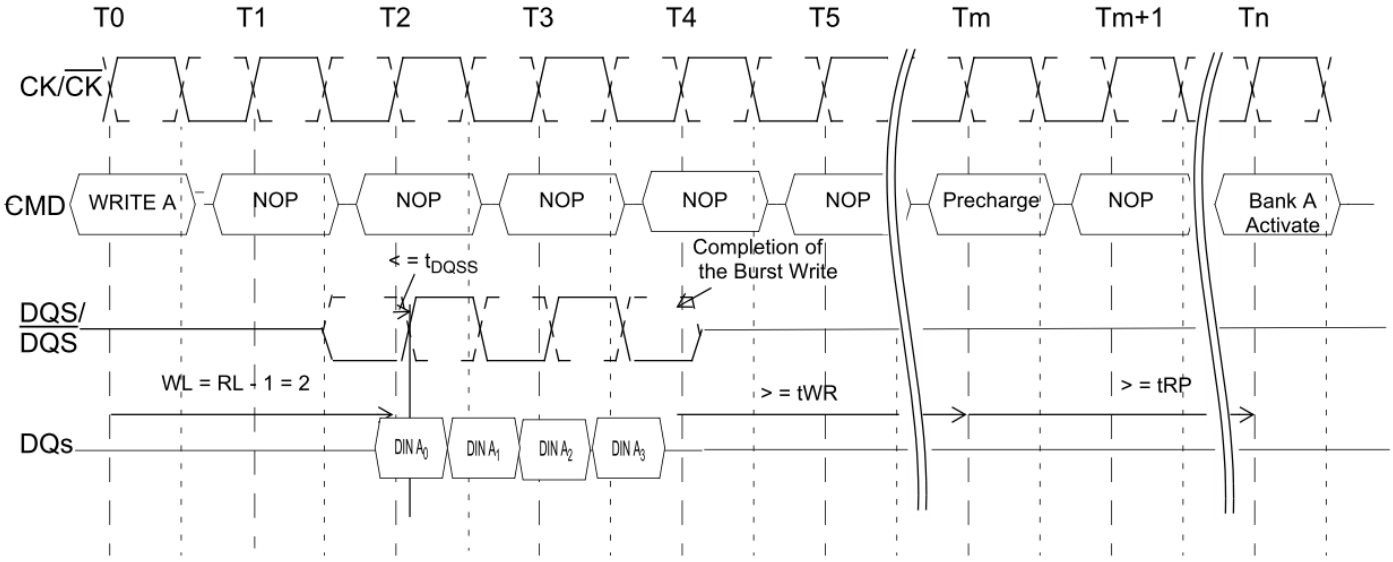
Data input (write) timing



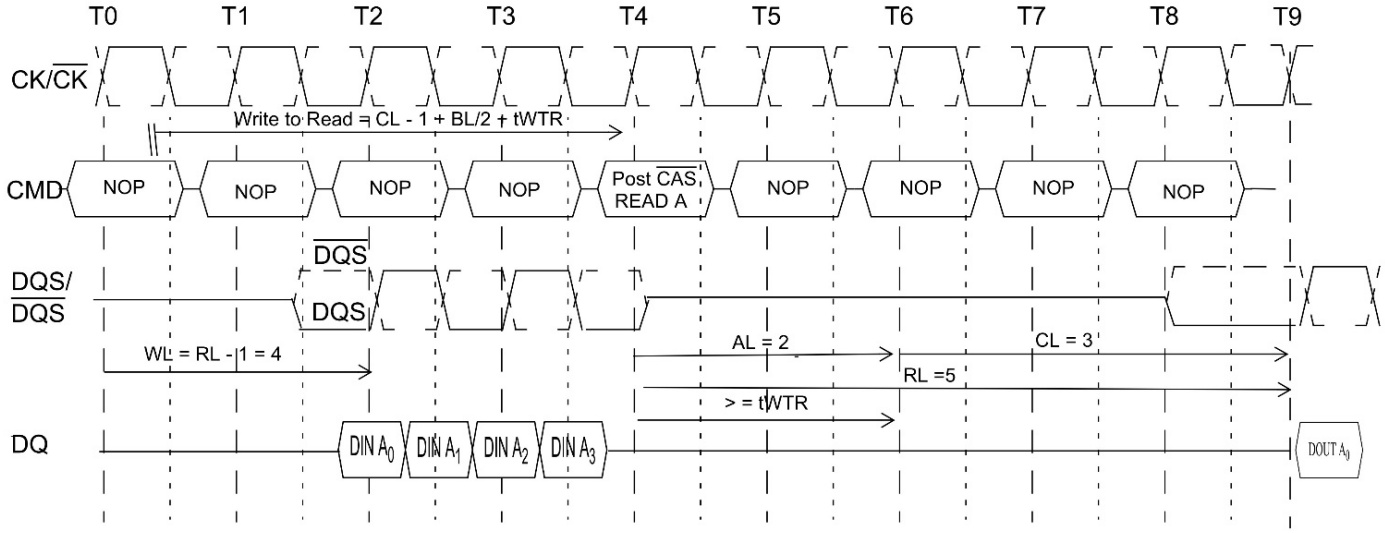
Burst write operation: RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



Burst write operation: RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4

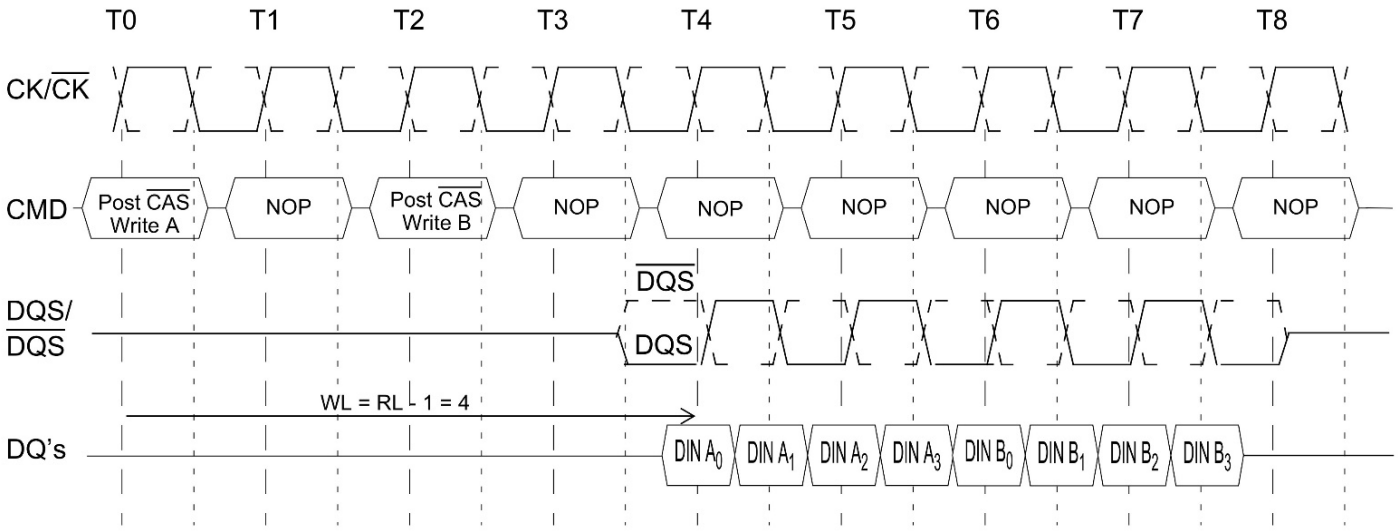


Burst write followed by burst read: RL = 5 (AL = 2, CL = 3), WL = 4, t_{WTR} = 2, BL = 4



The minimum number of clocks from the burst write command to the burst read command is [CL - 1 +BL/2 + t_{WTR}]
This t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

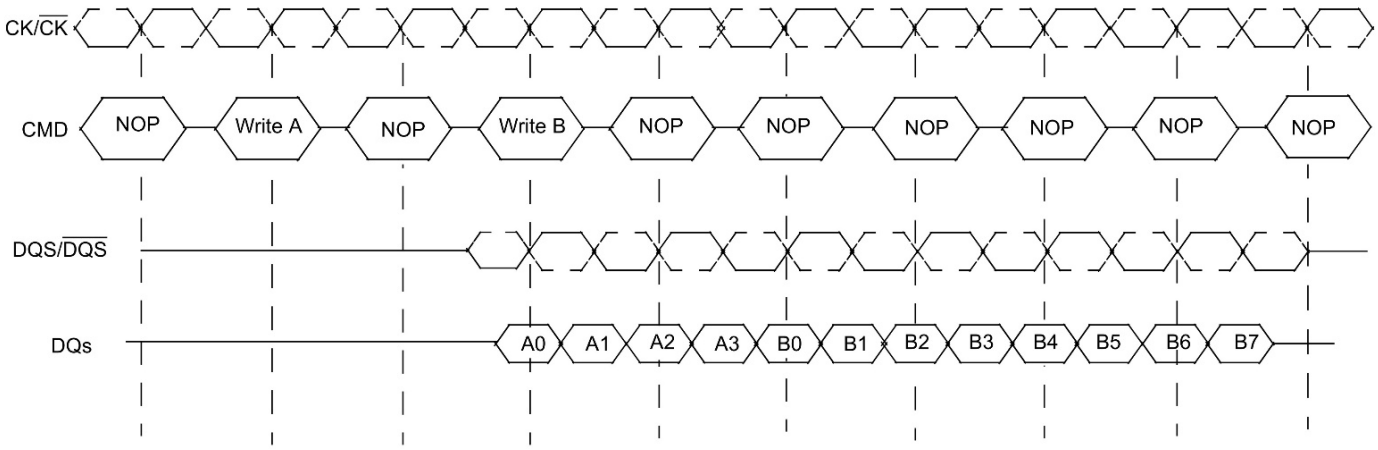
Seamless burst write operation: RL = 5, WL = 4, BL = 4



The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Writes interrupted by a write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

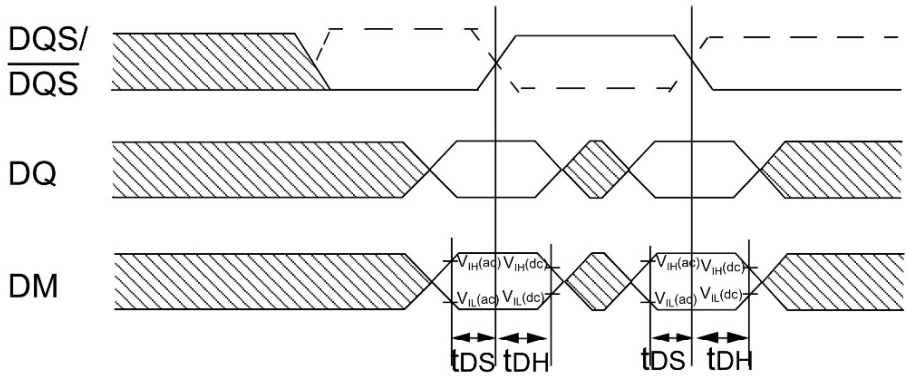


Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command of Precharge command is prohibited.
Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
Write burst interruption is allowed to any bank inside DRAM.
Write burst with Auto Precharge enabled is not allowed to interrupt.
Write burst interruption is allowed by another Write with Auto Precharge command.
All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL + BL/2 + t_{WR} where t_{WR} starts with the rising clock after the uninterrupted burst end and not from the end of actual burst end.

Write Data Mask

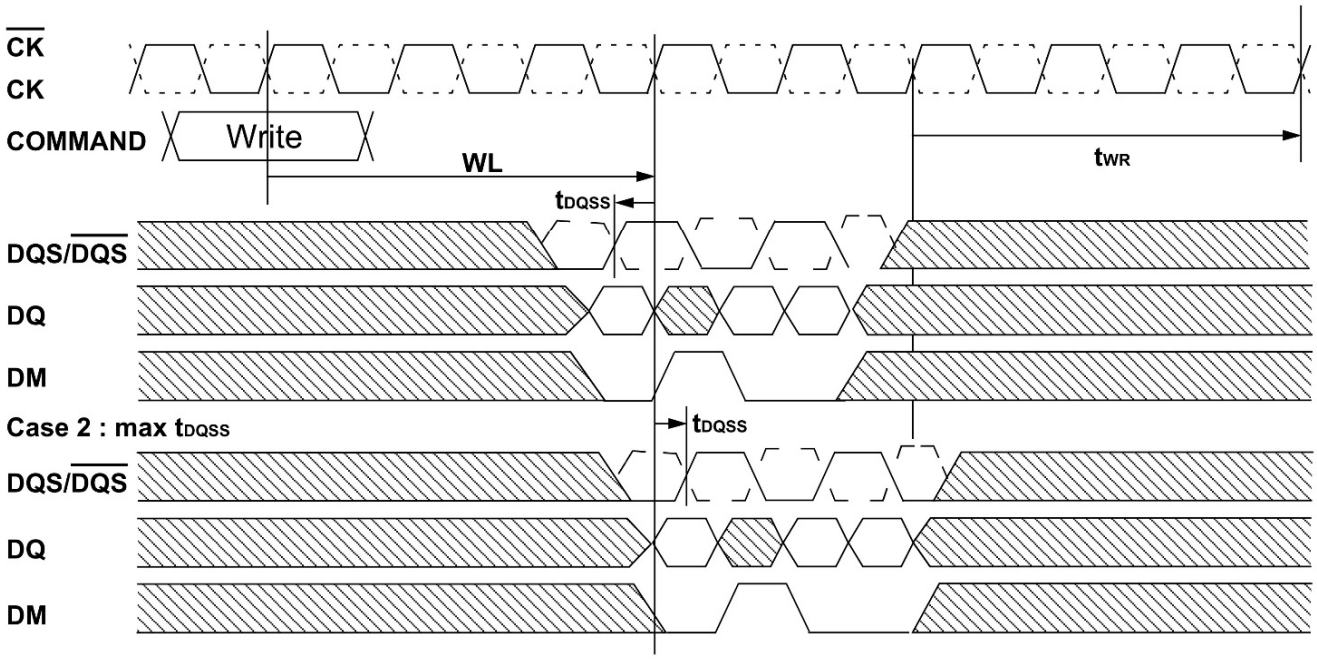
One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a unidirectional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMR(1) setting.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1 : min t_{DQSS}



Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. Four address bits A10, BA2, BA1 and BA0 are used to define which bank to precharge when the command is issued.

Bank selection for precharge by address bits

A10	BA2	BA1	BA0	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1 Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1 Gb and higher
LOW	HIGH	HIGH	LOW	Bank 6 only	1 Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7 only	1 Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

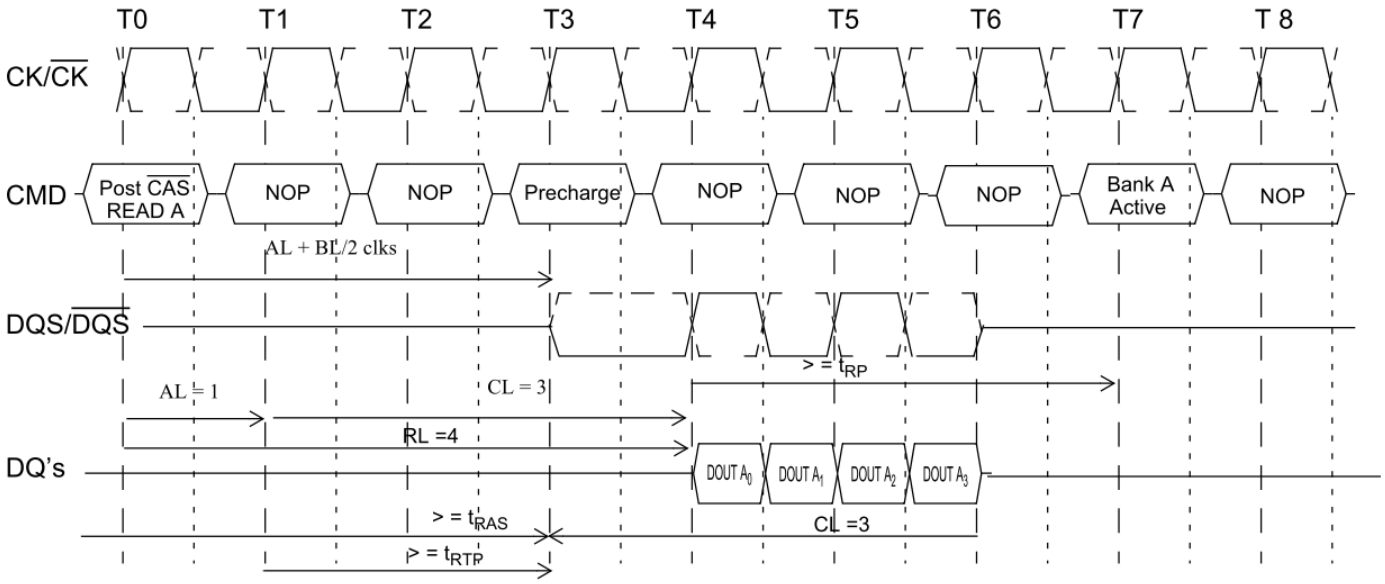
Burst Read Operation Followed by Precharge

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max(RTP, 2) - 2 clocks

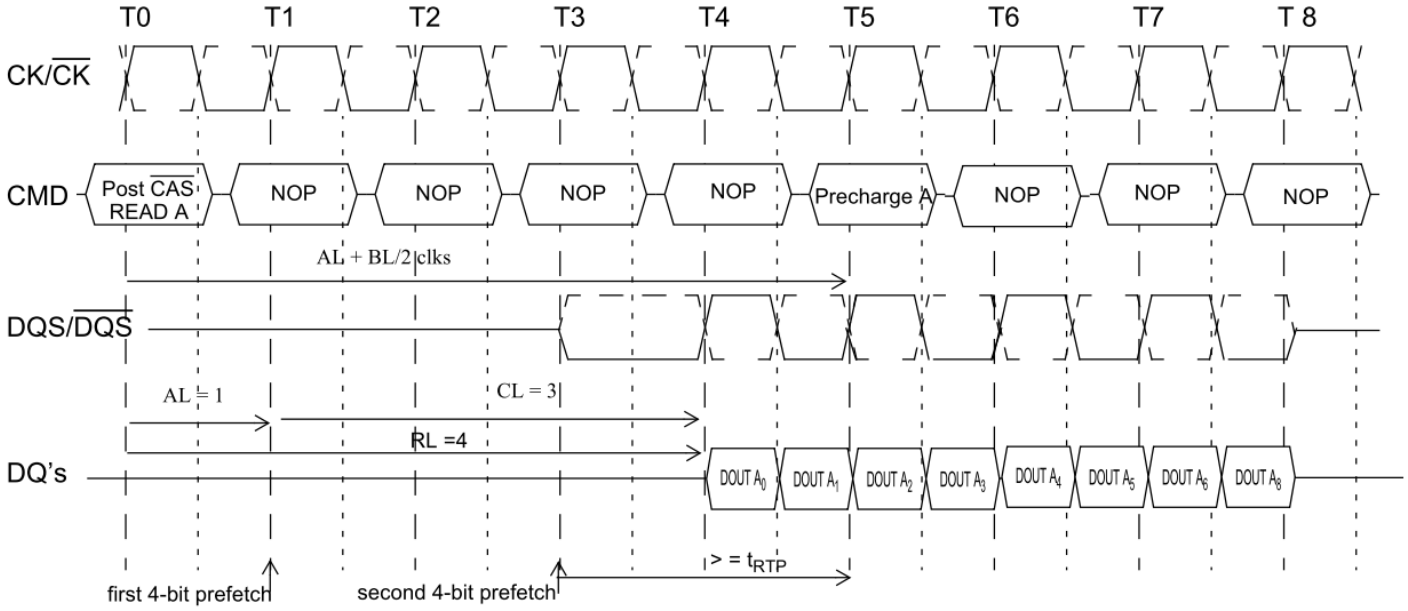
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 + max(RTP, 2) - 2 clocks" after a Read Command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called t_{RTP} (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

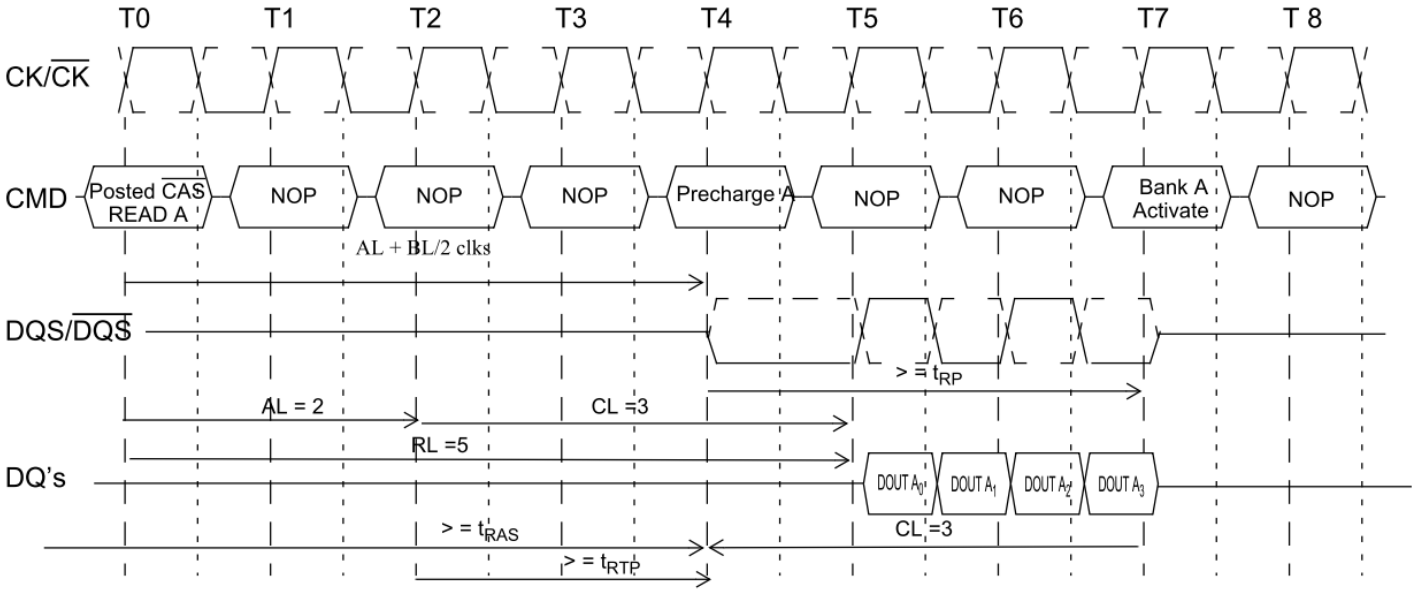
Burst read operation followed by precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks



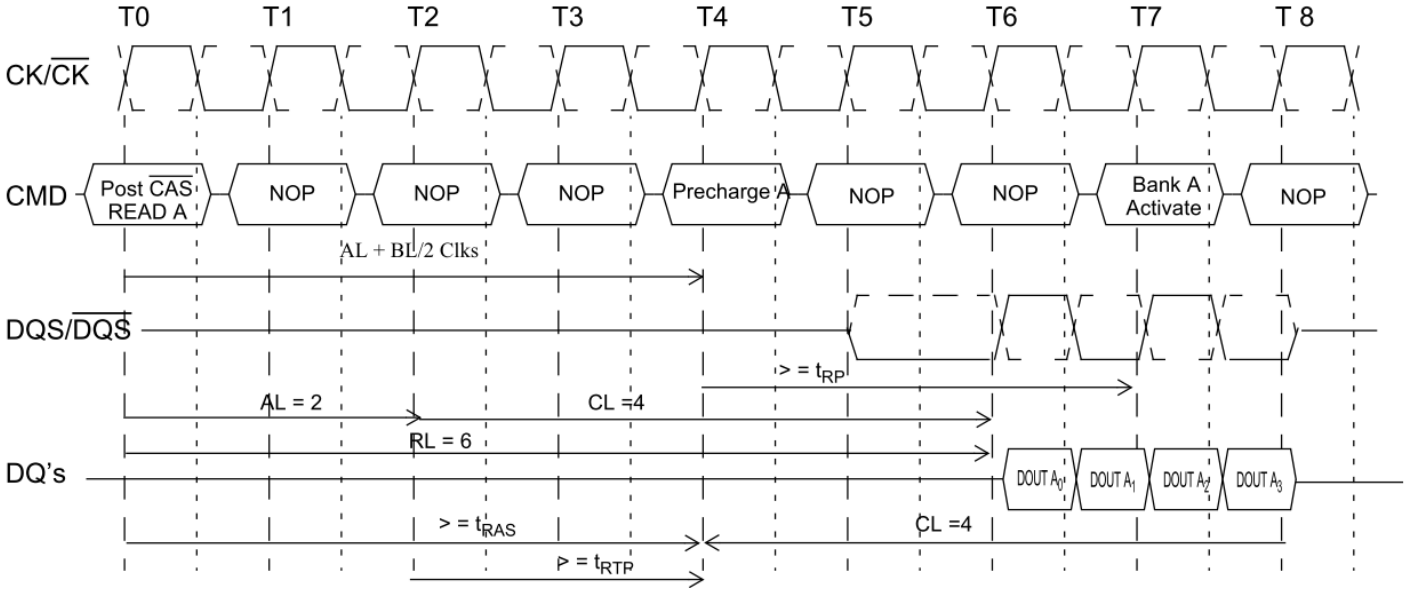
Burst read operation followed by precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks



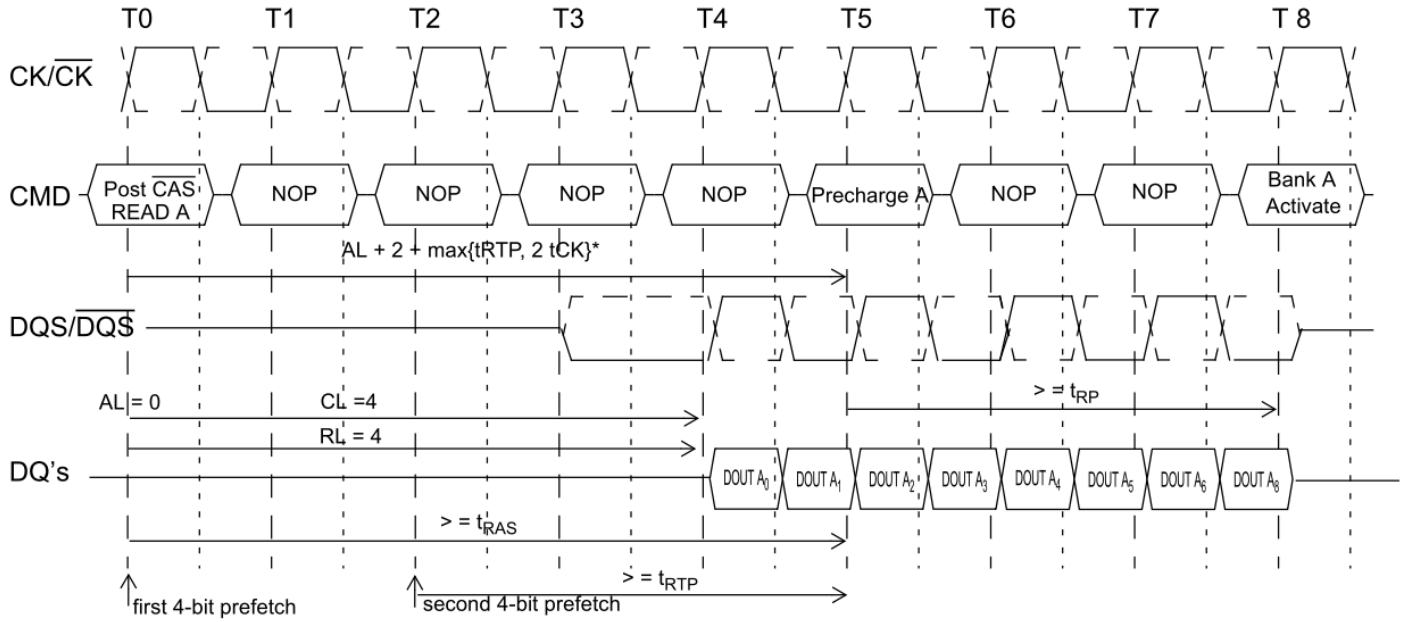
Burst read operation followed by precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks



Burst read operation followed by precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



Burst read operation followed by precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks



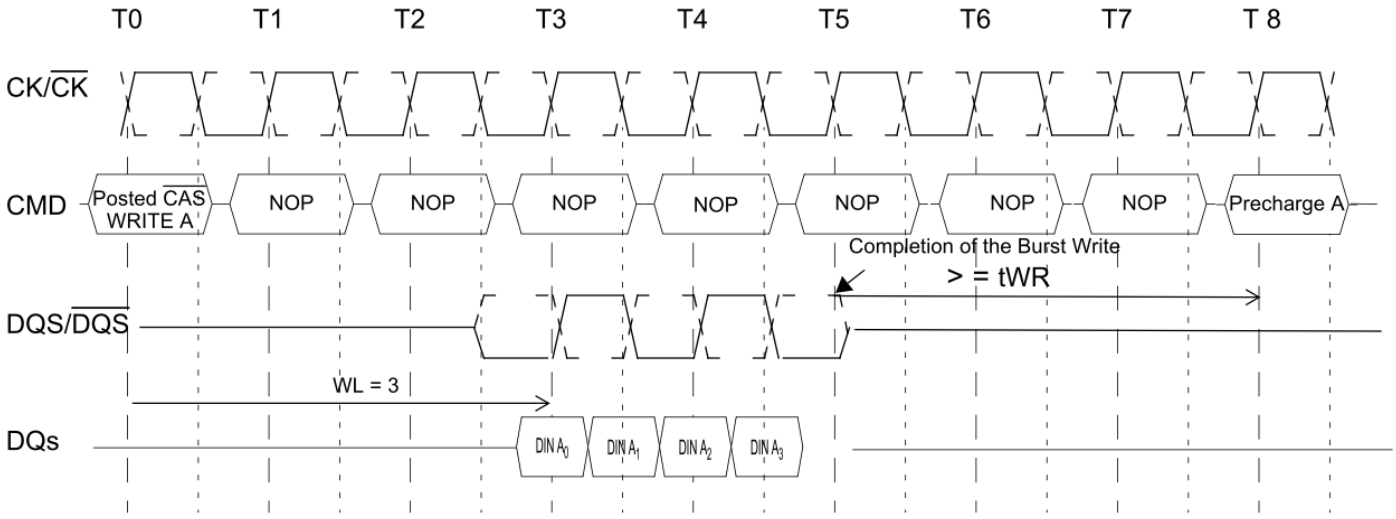
* : rounded to next integer.

Burst Write Followed by Precharge

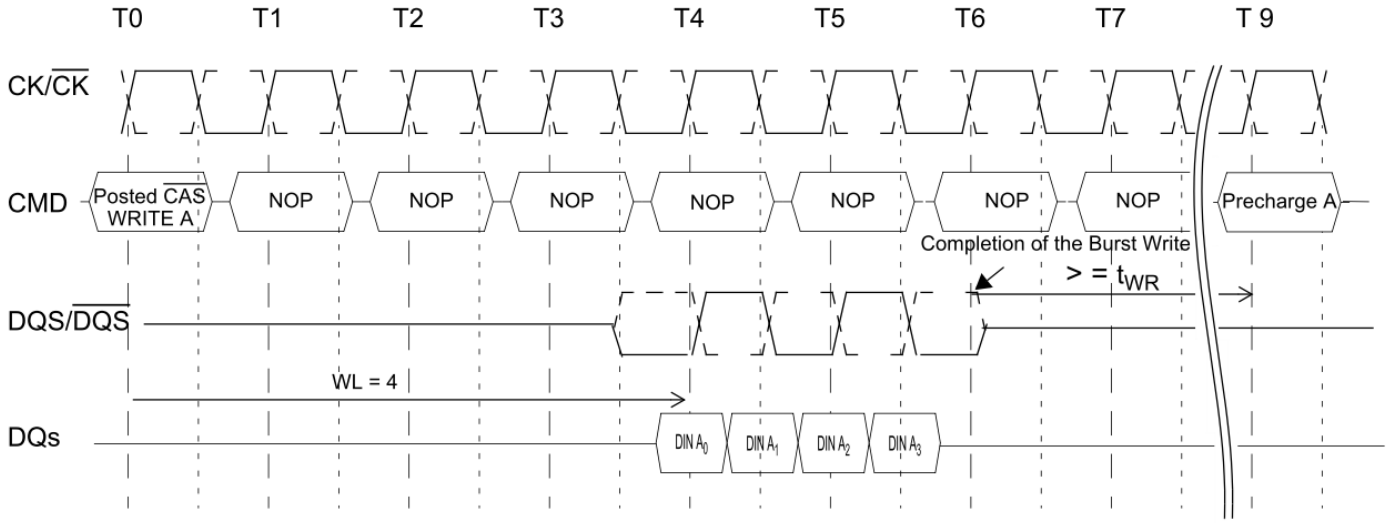
Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + t_{WR}

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the t_{WR} delay.

Burst write followed by precharge: WL = (RL-1) = 3



Burst write followed by precharge: WL = (RL-1) = 4



Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Pre-charge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is $\overline{CAS}$ Latency (CL) clock cycles before the end of the read burst.

Auto-Precharge is also implemented for Write Commands. The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ Latency) thus improving system performance for random data access. The $\overline{RAS}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL /2) cycles later from the Read with AP command if t_{RAS} (min) and t_{RTP} are satisfied.

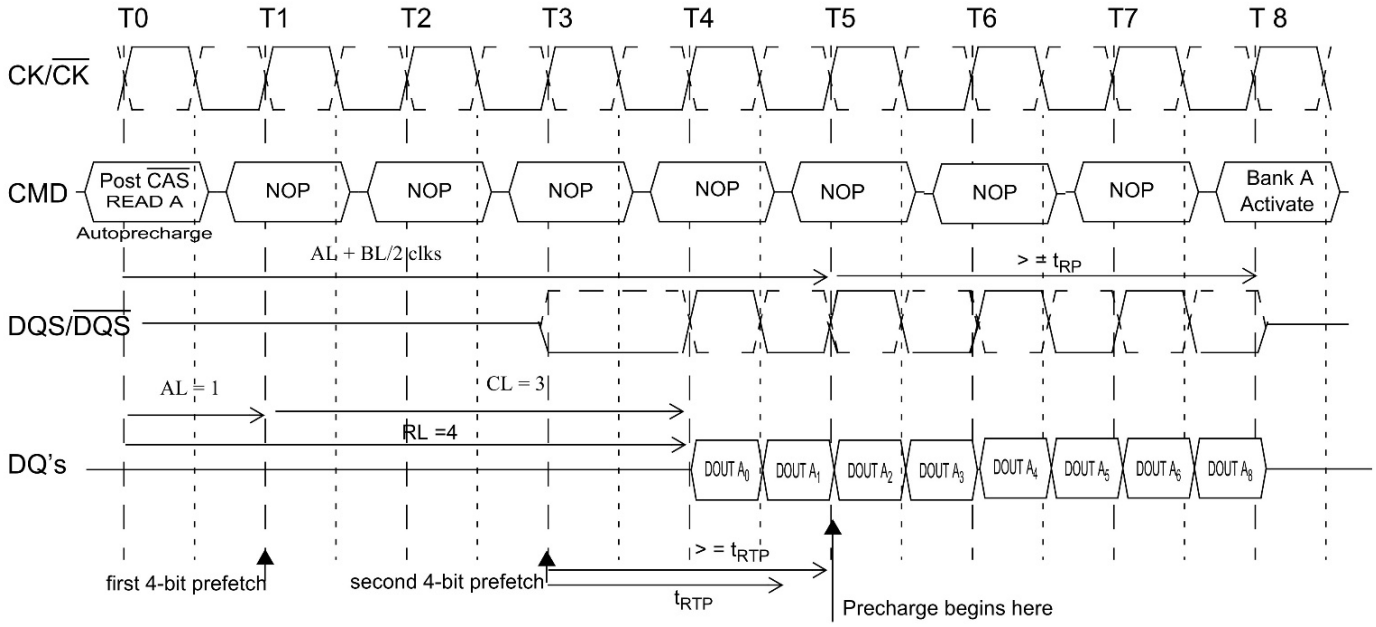
If t_{RAS} (min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RAS} (min) is satisfied.

If t_{RTP} (min) is not satisfied a t the edge, the start point of Auto-precharge operation will be delayed until t_{RTP} (min) is satisfied.

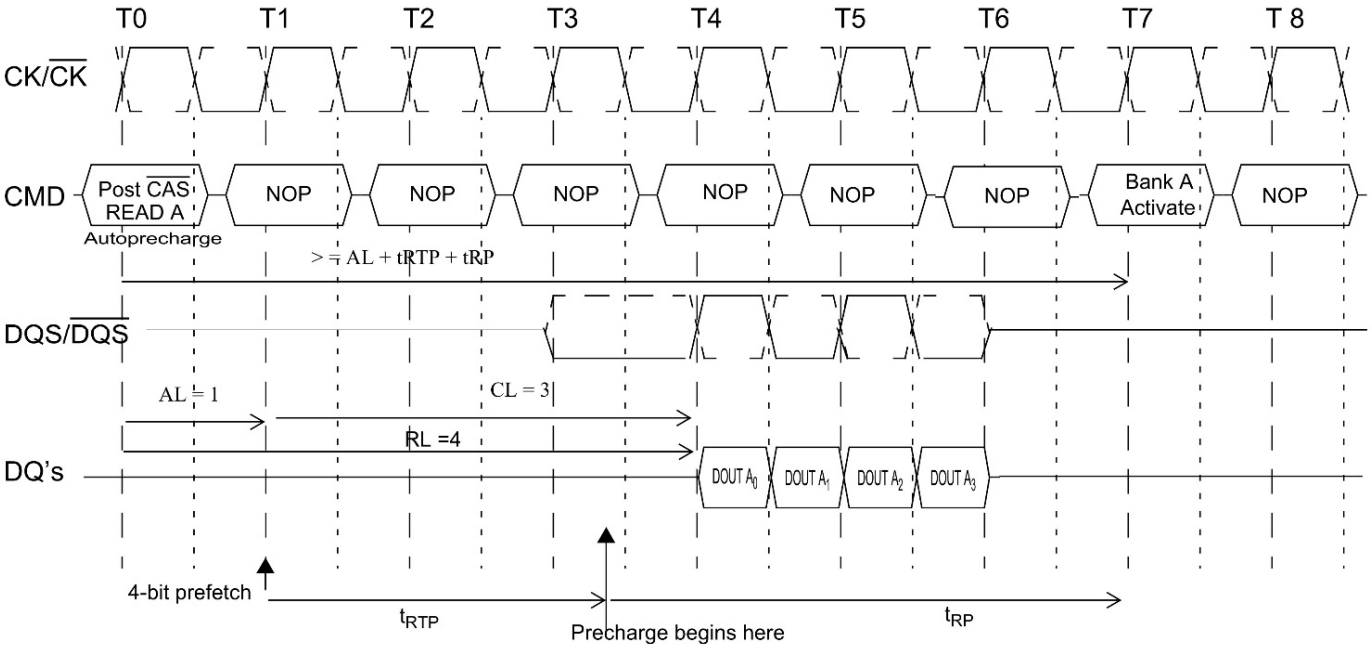
In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal pre charge happens (not the next rising clock edge after this e vent). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RPF} or BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that both parameters t_{RTP} and t_{RP} have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:
a) The $\overline{RAS}$ precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.
b) The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

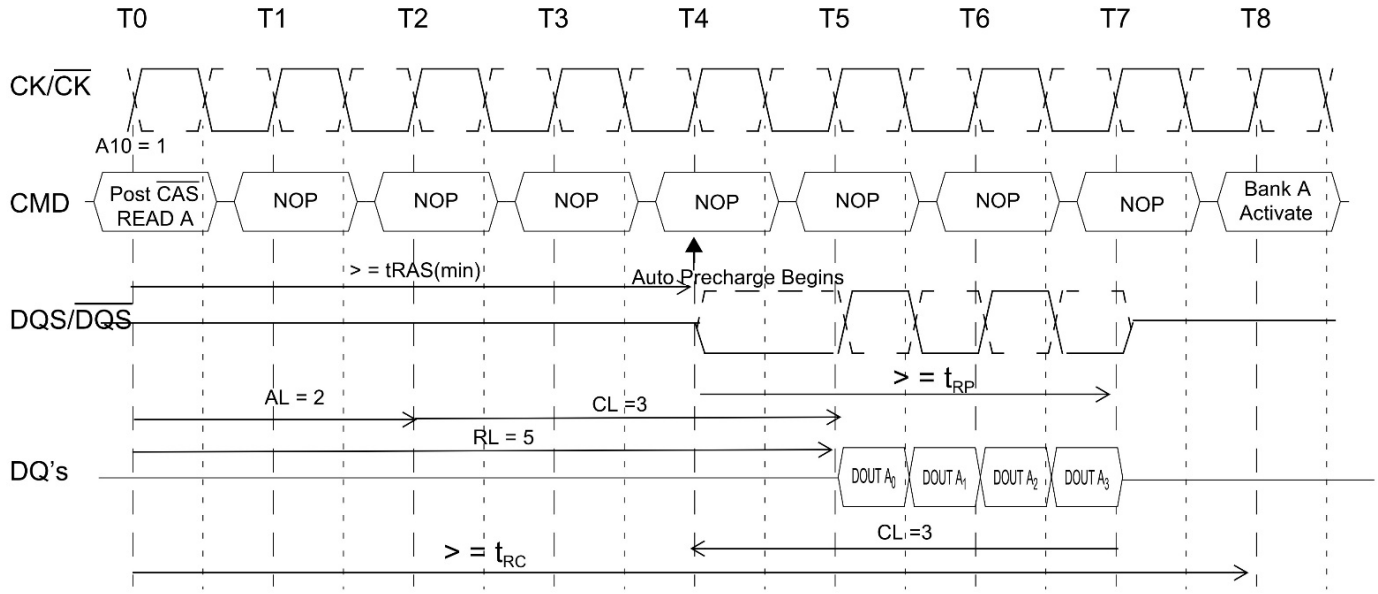
Burst read operation with auto precharge: RL = 4, AL = 1, CL =3, BL = 8, t_{RTP} <= 2 clocks



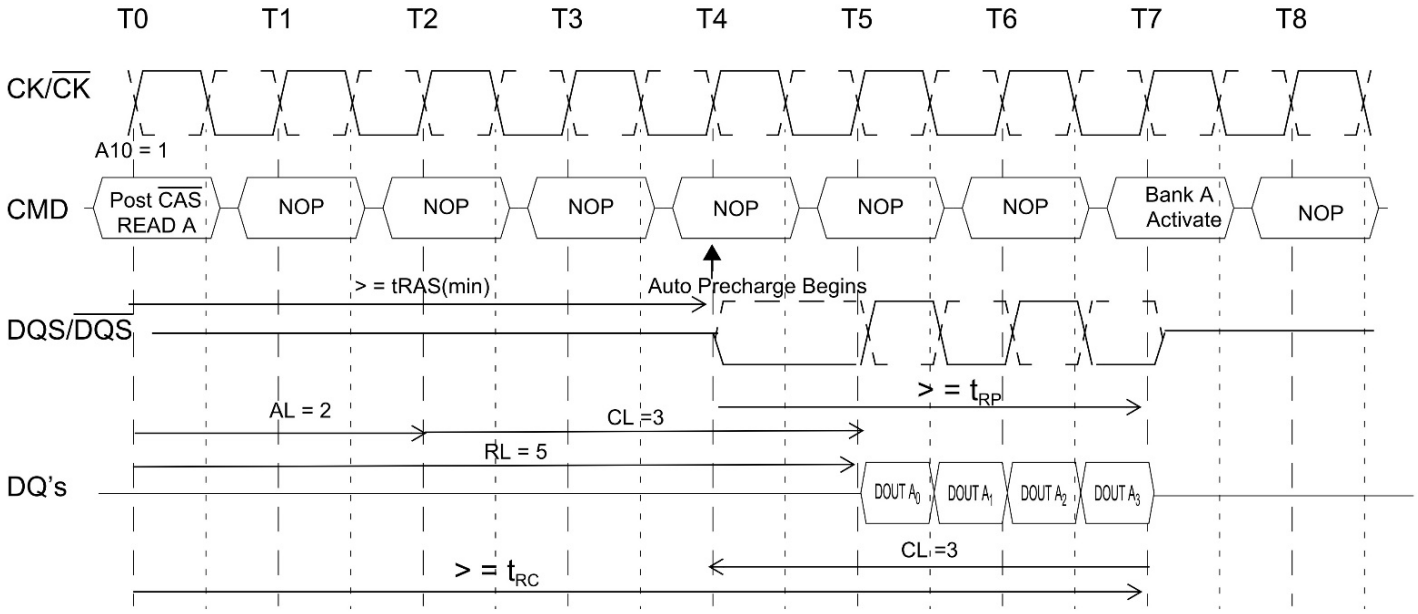
Burst read operation with auto precharge: RL = 4, AL = 1, CL =3, BL = 4, t_{RTP} > 2 clocks



Burst read with auto precharge followed by an activation to the same bank (t_{RC} Limit):
RL = 5 (AL = 2, CL = 3, internal t_{RCD} = 3, BL = 4, t_{RTP} <= 2 clocks)



Burst read with auto precharge followed by an activation to the same bank (t_{RP} Limit):
RL = 5 (AL = 2, CL = 3, internal t_{RCD} = 3, BL = 4, t_{RTP} <= 2 clocks)

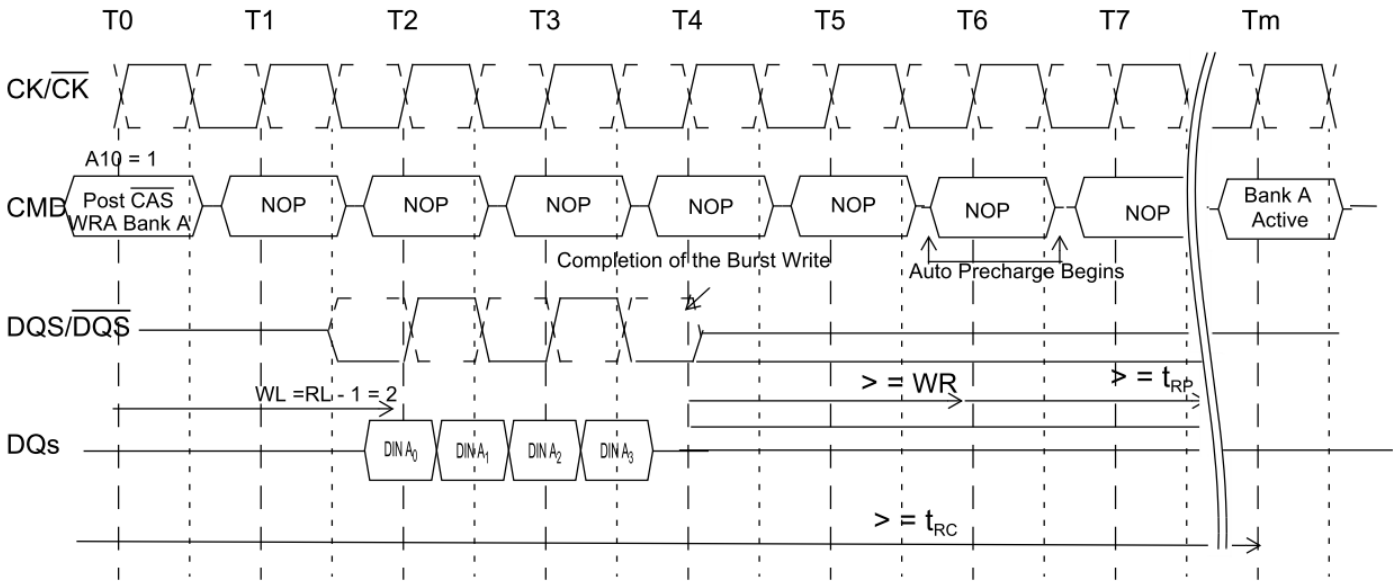


Burst Write with Auto-Precharge

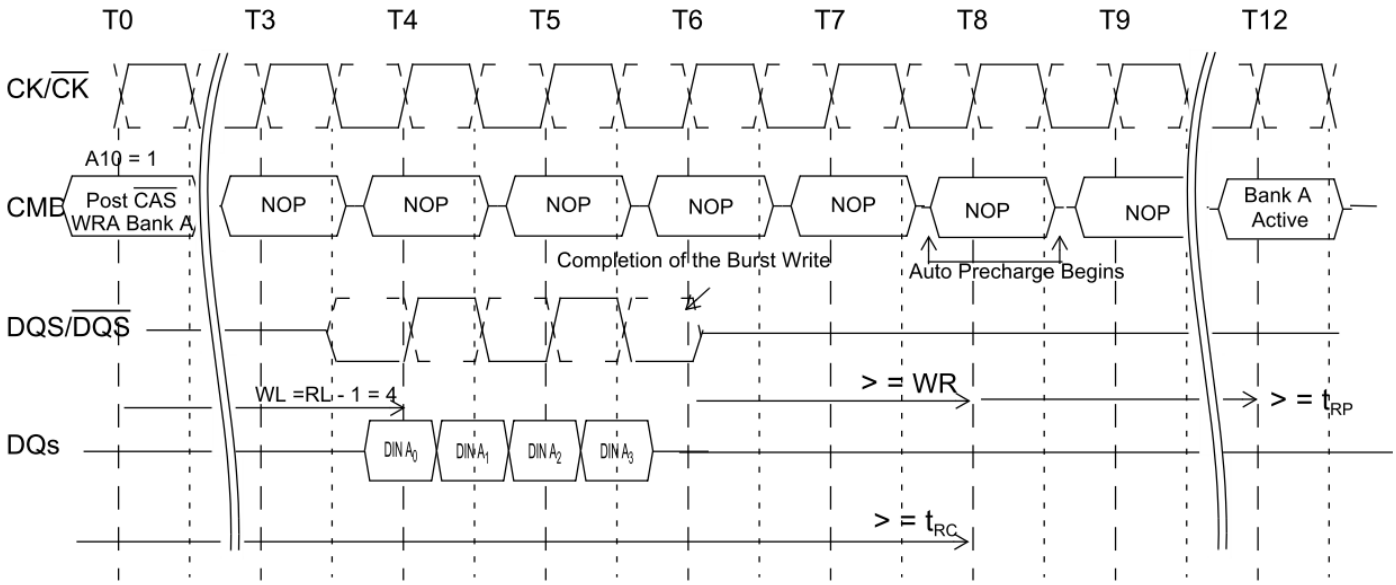
If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register. The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

a) The data-in to bank activate delay time (WR + t_{RP}) has been satisfied.
b) The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

Burst write with auto-precharge (t_{RC} Limit): WL = 2, WR = 2, BL = 4, t_{RP} = 3



Burst write with auto-precharge (WR + t_{RP}): WL = 4, WR = 2, BL = 4, t_{RP} = 3

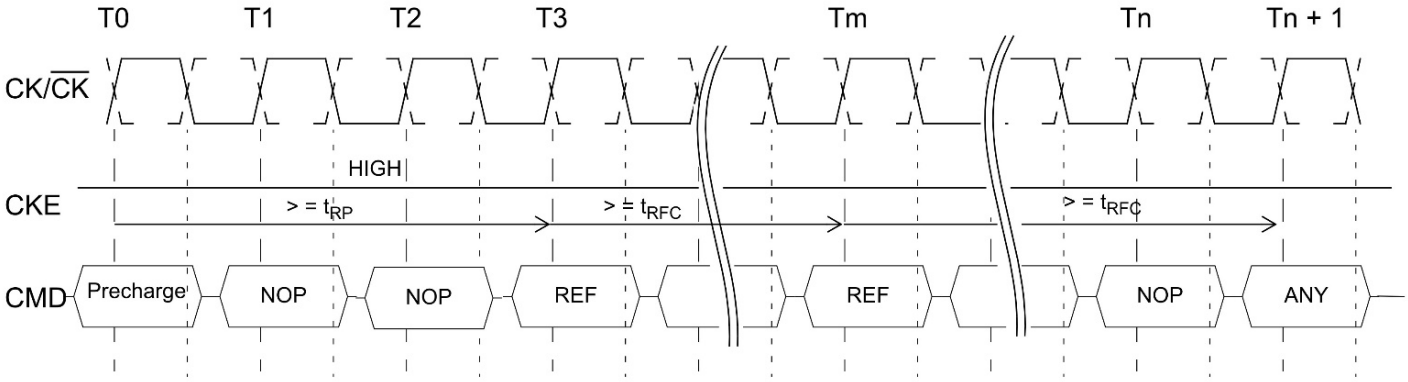


Refresh Command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * t_{REFI}.

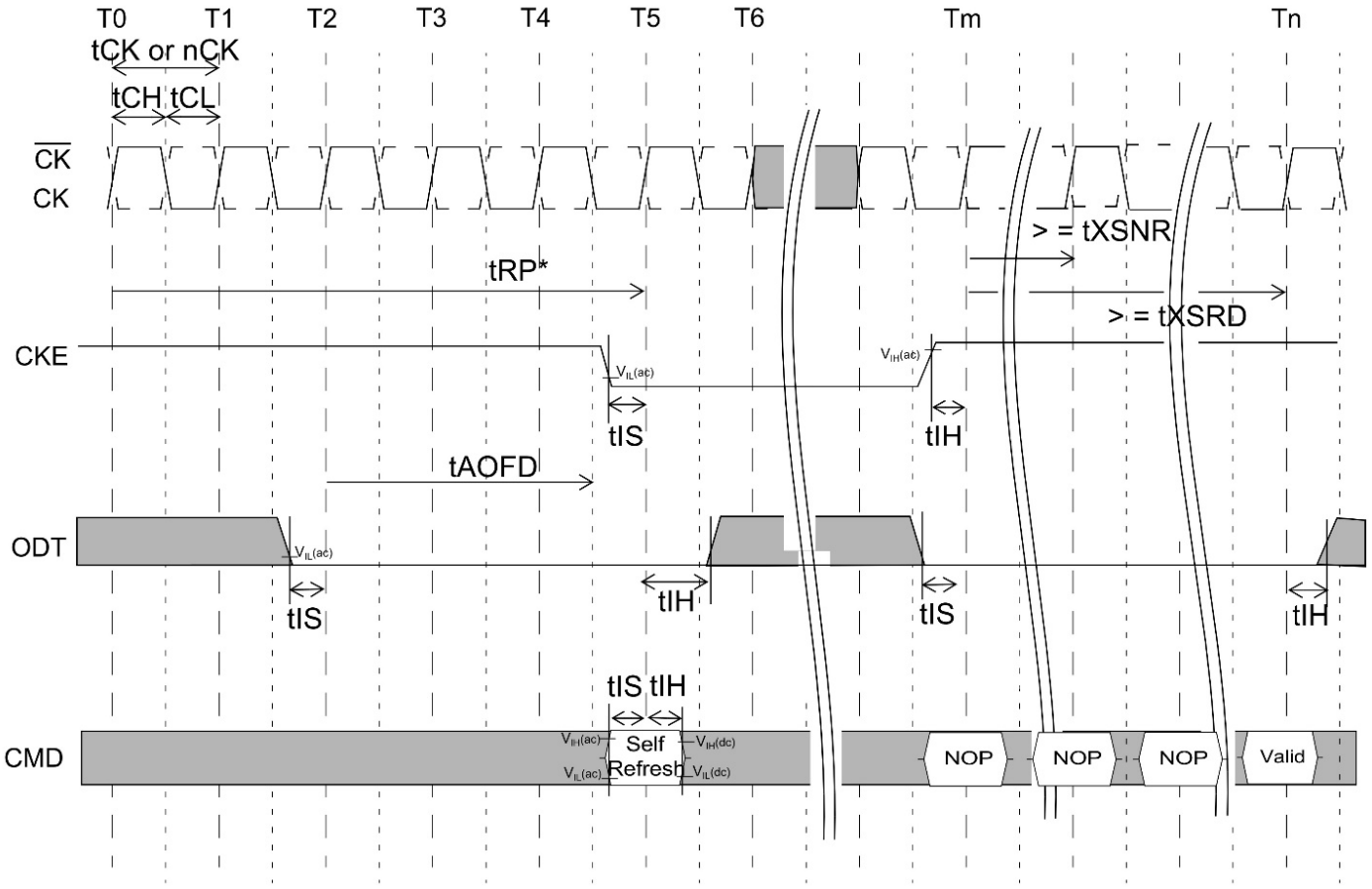


Self refresh operation

The Self -Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self-Refresh Exit command is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self-Refresh exit period t_{XSRD} for proper operation except for self refresh re-entry. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least t_{XSNR} period and issuing one refresh command (refresh period of t_{RFC}). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSRD}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.



Device must be in the “All banks idle” state prior to entering Self Refresh mode.
ODT must be turned off t_{AOFD} before entering Self Refresh mode, and can be turned on again when t_{XSRD} timing is satisfied.
t_{XSRD} is applied for a Read or a Read with autoprecharge command.
t_{XSNR} is applied for any command except a Read or a Read with autoprecharge command.

Power-Down

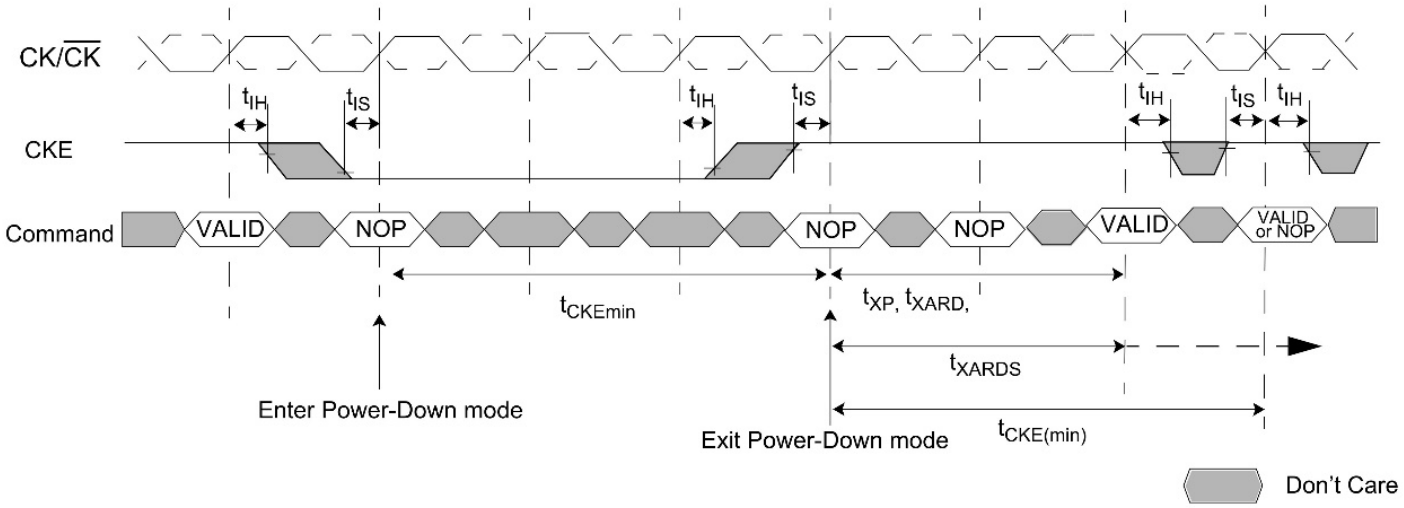
Power-down is synchronously entered when CKE is registered low along with NOP or Deselect command. No read or write operation may be in progress when CKE goes low. These operations are any of the following: read burst or write burst and recovery. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, mode register or extended mode register command time, or autorefresh is in progress. The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For *Active Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to “low” this mode is referred as “standard active power-down mode” and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to “high” this mode is referred as a power saving “low power active power-down mode”. This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied.

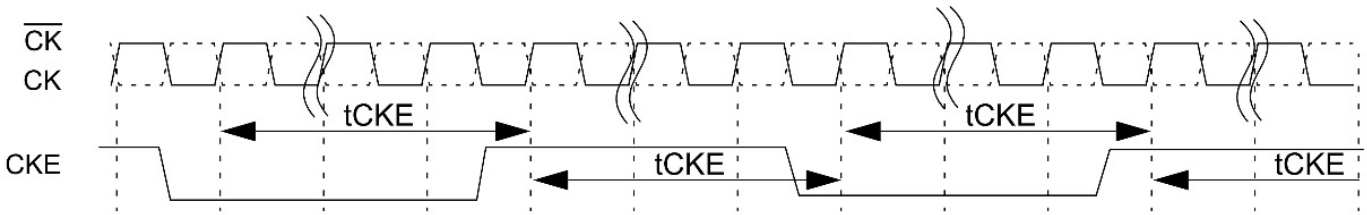
Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are “Don’t Care”. Power-down duration is limited by 9 times t_{REFI} of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Basic power down entry and exit timing diagram

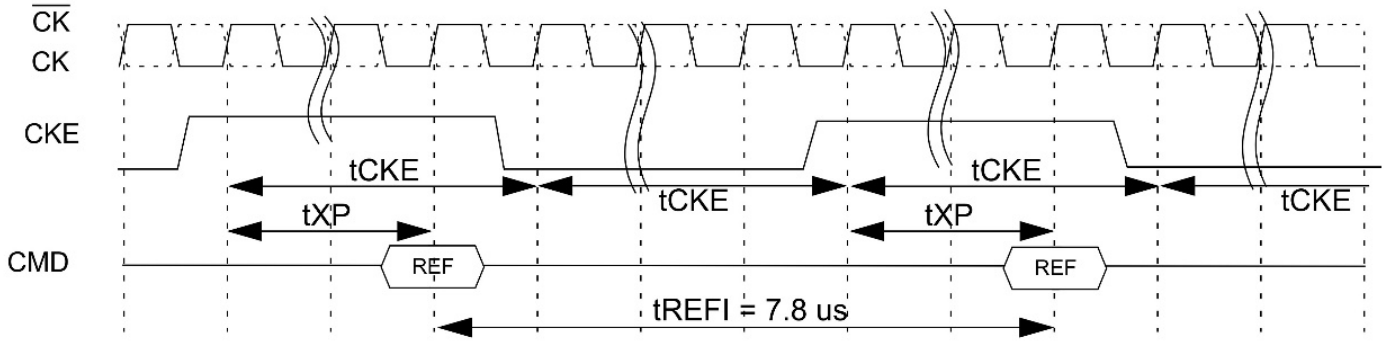


Example 1 of CKE intensive environment



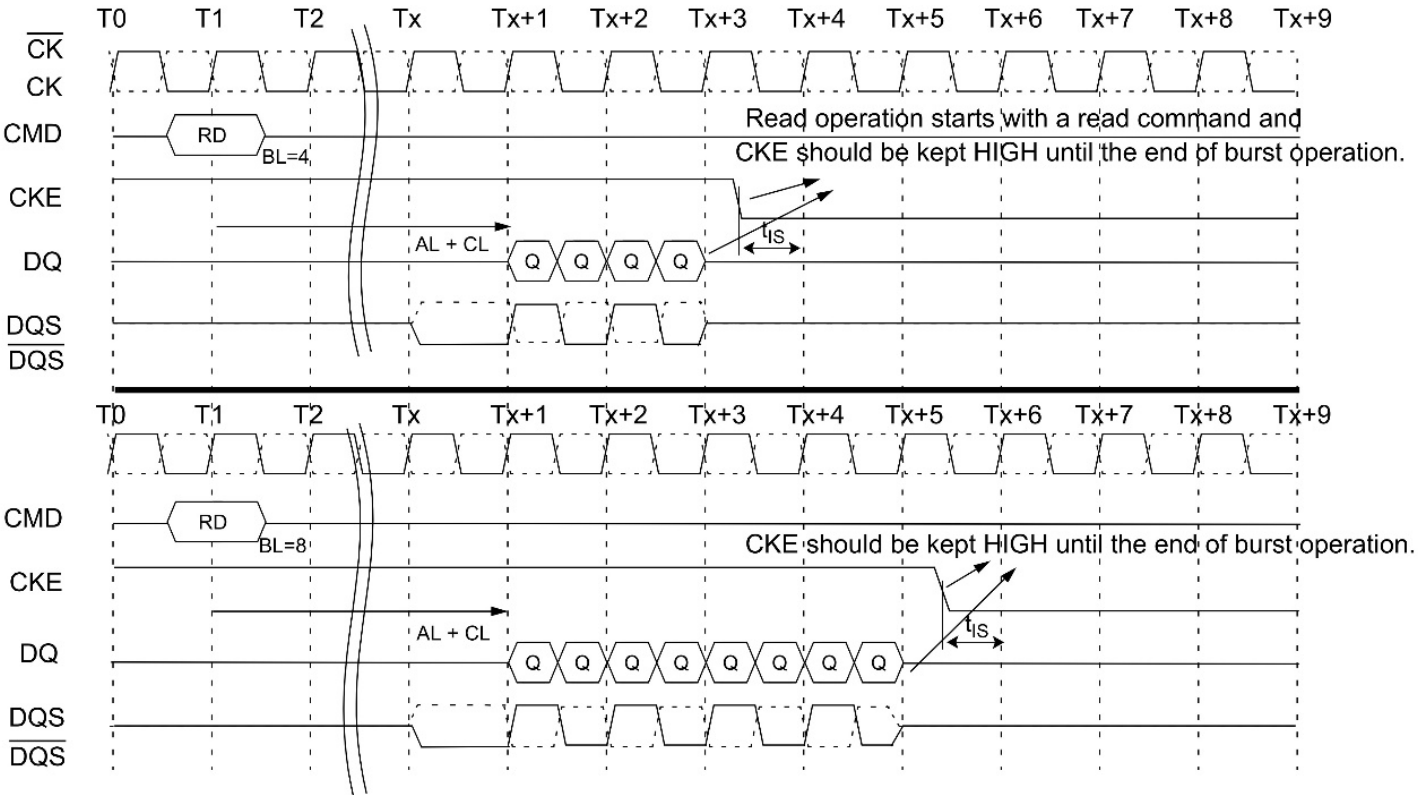
DRAM guarantees all AC and DC timing & voltage specifications and proper DLL operation with intensive CKE operation.

Example 2 of CKE intensive environment

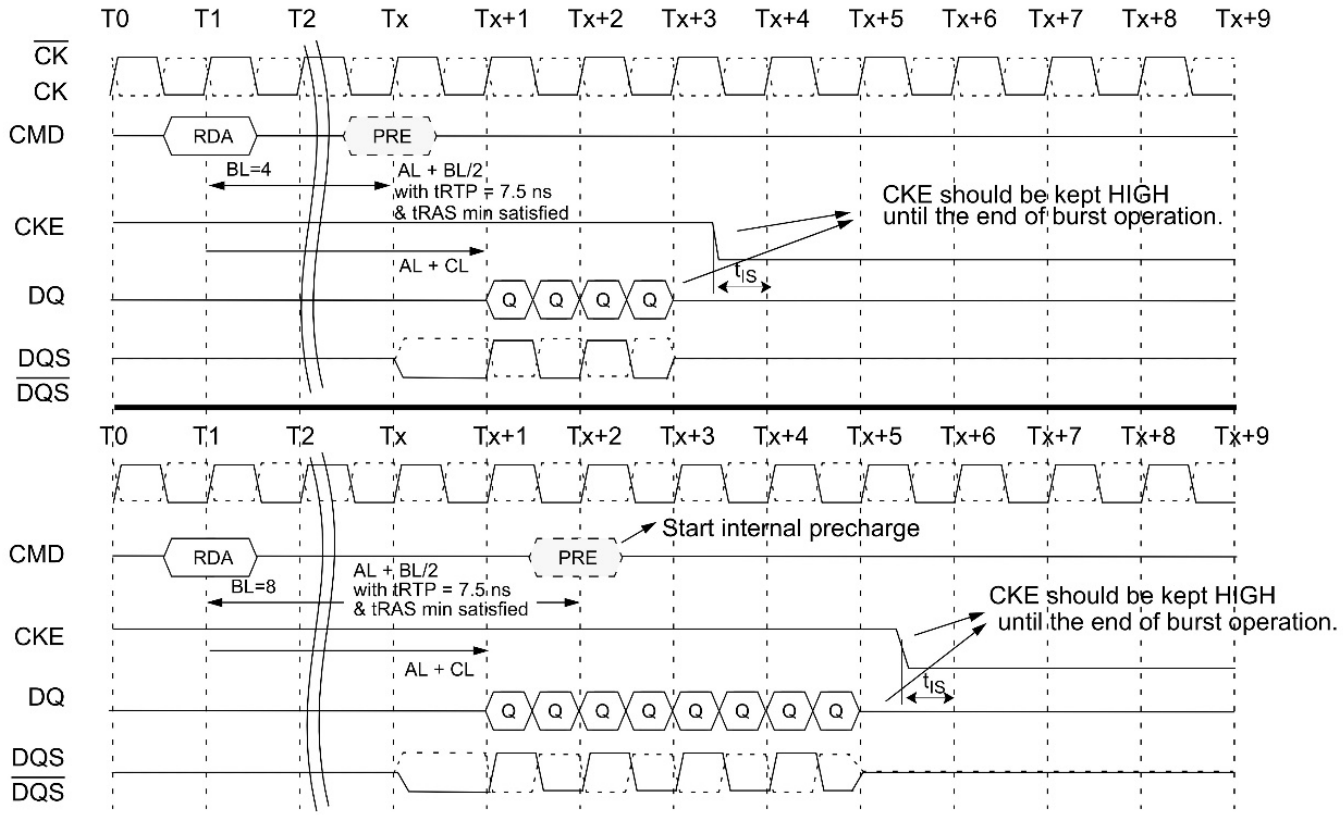


The pattern shown above can repeat over a long period of time. With this pattern, DRAM guarantees all AC and DC timing & voltage specifications and DLL operation with temperature and voltage drift.

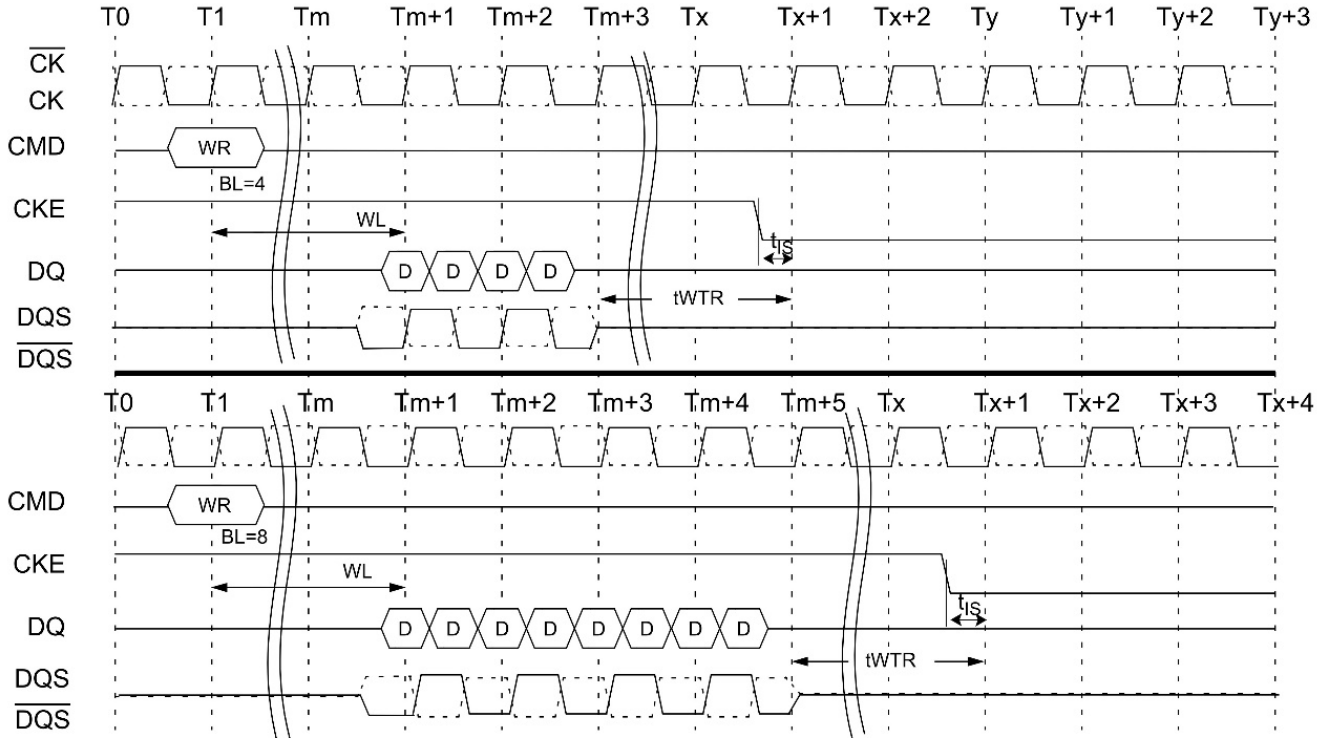
Read to power-down entry



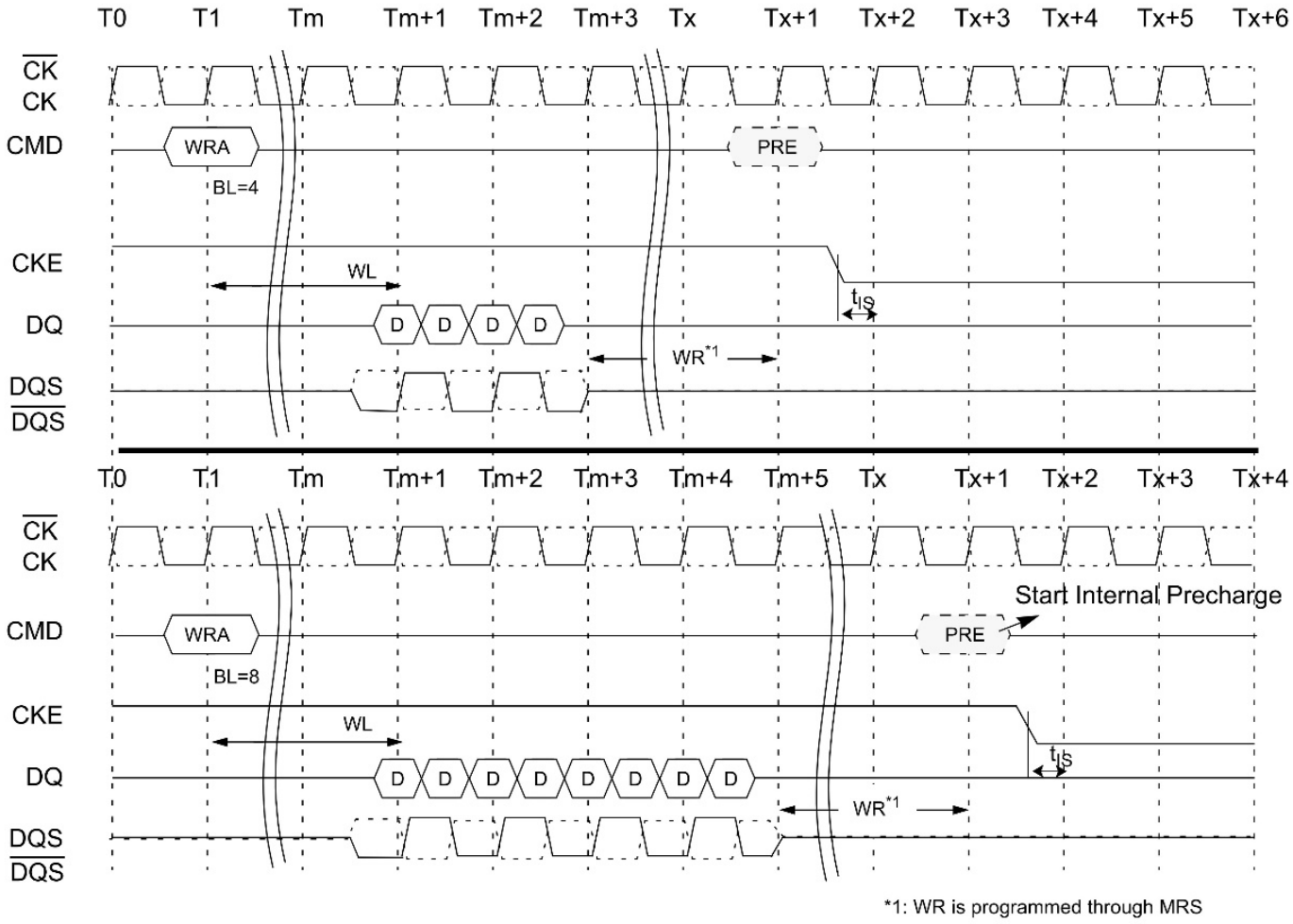
Read with autoprecharge to power-down entry



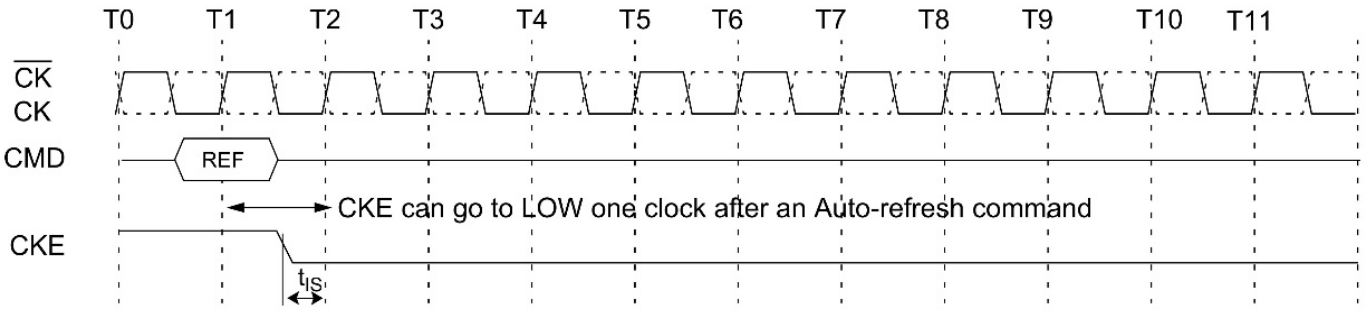
Write to power-down entry



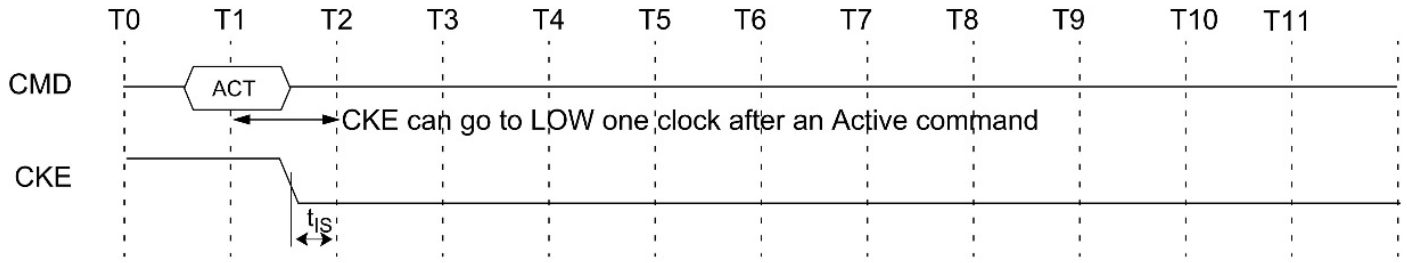
Write with autoprecharge to power-down entry



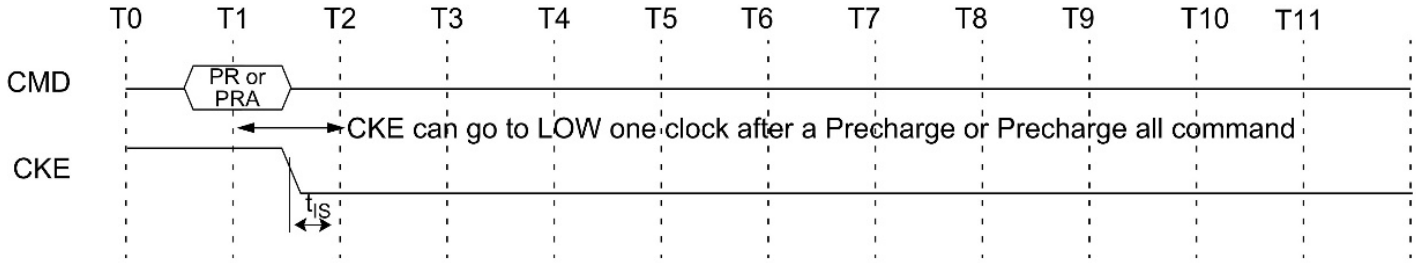
Refresh command to power-down entry



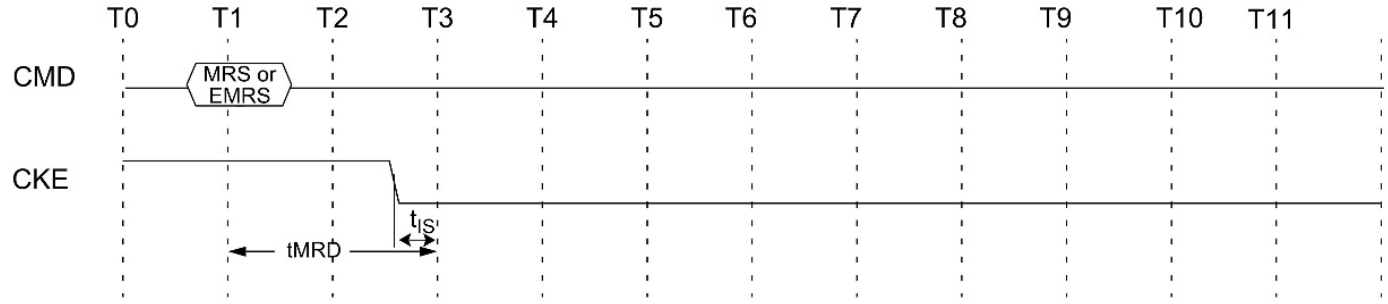
Active command to power-down entry



Precharge/precharge-all command to power-down entry

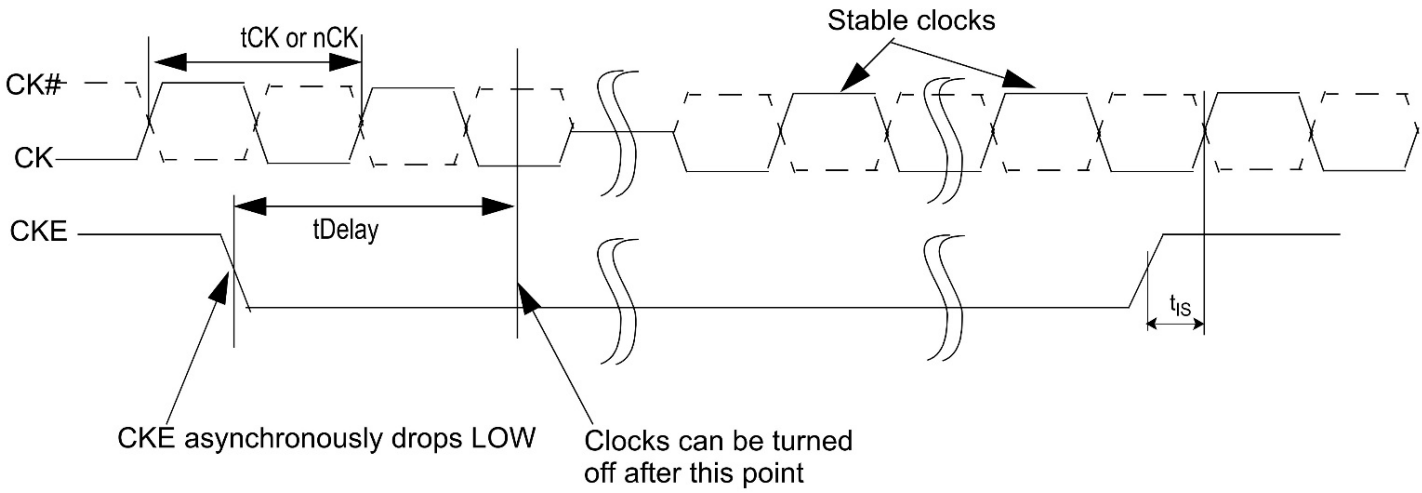


MRS/EMRS command to power-down entry



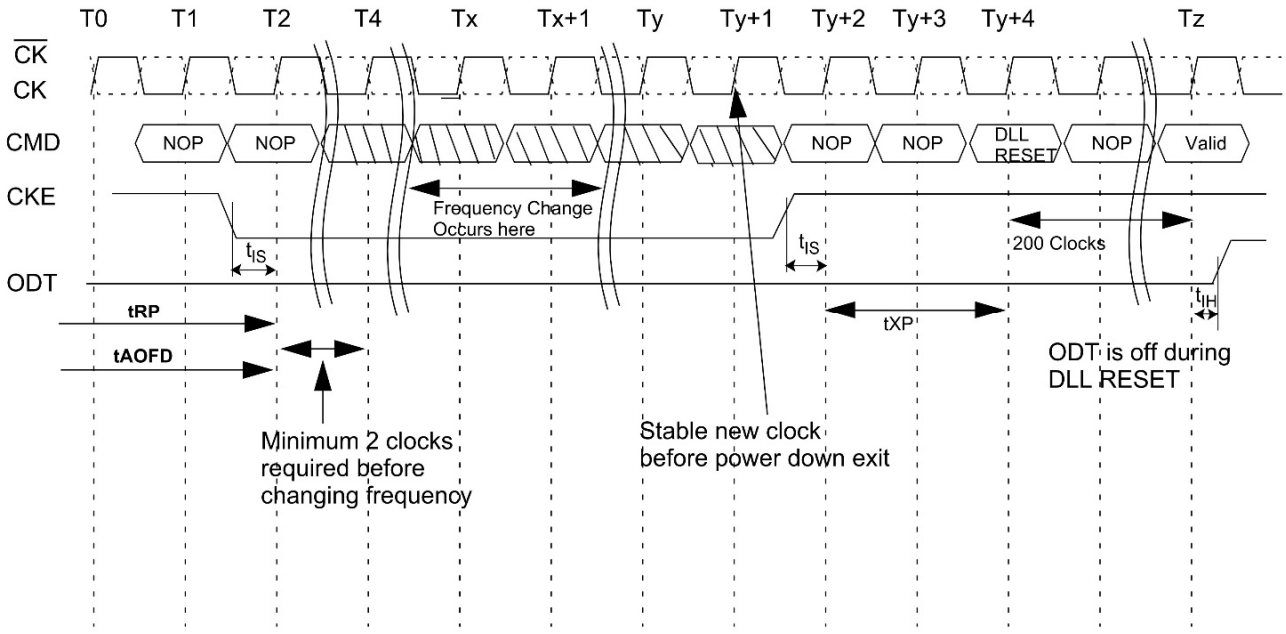
Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the initialization sequence. DRAM is ready for normal operation after the initialization sequence.



Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition:
DDR2 SRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via MRS command after precharge power down exit. Depending on new clock frequency an additional MRS or EMRS command may need to be issued to appropriately set the WR, CL etc.. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.



Terms and definitions

fCK,min: Minimum frequency supported by the DRAM (for all DDR2 speed bins, 1/tCK(avg),max = 125 MHz)
fCK,max: Maximum frequency supported by the DRAM (for DDR2-667, 1/tCK(avg),min = 333 MHz)
SSC band: If the system modulates the input clock frequency between fSSC,min and fSSC,max, this frequency band is referred to as SSC band
fSSC,nom: Mean frequency of fSSC,min and fSSC,max
Modulation frequency: Rate at which the frequency is modulated for SSC
Ex) 20 kHz modulation: Input clock frequency shifts gradually from fSSC,min to fSSC,max over 25 us (= 50 us / 2)

SSC (Spread Spectrum Clocking) Criteria

SSC is allowed only if fSSC,min is greater than or equal to fCK,min and fSSC,max is less than or equal to fCK,max. All input clock specs including, but not limited to, terr(nper) must be met at all times. Allowed modulation frequency is 20 kHz to 60 kHz.

Allowed SSC band

If the DRAM DLL is locked at fSSC,nom (by issuing a DLL reset and waiting 200 clock cycles) and then the SSC is turned on later, the system is allowed an SSC band of fSSC,nom +/- 1 %.
In all other cases, the system is allowed an SSC band of fSSC,nom +/- 0.5 %.
If the input clock frequency drifts out of this band, the output timings can no longer be guaranteed and DLL reset must be issued to regain the output timings assuming a different SSC band.

No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

Command truth table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BAx[9]	Axx[9] - A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1,8
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7,8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

Notes:

1) All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

2) Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

3) Burst reads or writes at BL = 4 cannot be terminated or interrupted.

4) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements.

5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

6) “X” means “H or L (but a defined logic level)”

7) Self refresh exit is asynchronous.

8) V_{REF} must be maintained during Self Refresh operation.

9) BAx and Axx refers to the MSBs of bank addresses and addresses, respectively, per device density.

Clock enable (CKE) truth table for synchronous transitions

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}, \overline{CAS}, \overline{WE}, \overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11,13,15
	L	H	DESELECT or NOP	Power Down Exit	4,8,11,13
Self Refresh	L	L	X	Maintain Self Refresh	11,15,16
	L	H	DESELECT or NOP	Self Refresh Exit	4,5,9,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4,8,10,11,13
	H	L	REFRESH	Self Refresh Entry	6,9,11,13
	H	H	Refer to the Command Truth Table		7

Notes:

1) CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

2) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.

3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

5) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.

6) Self Refresh mode can only be entered from the All Banks Idle state.

7) Must be a legal command as defined in the Command Truth Table.

8) Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

9) Valid commands for Self Refresh Exit are NOP and DESELECT only.

10) Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section Power-down and Self refresh operation for a detailed list of restrictions.

11) t_{CKE}min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CK} + t_{IH}$.

12) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

13) The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements.

14) CKE must be maintained HIGH while the SDRAM is in OCD calibration mode.

15) "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMR(1)).

16) V_{REF} must be maintained during Self Refresh operation.

DM truth table

Name (Functional)	DM	DQs	Notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:

1) Used to mask write data, provided coincident with corresponding data.

Absolute maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0 V ~ 2.3 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5 V ~ 2.3 V	V	1,3
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5 V ~ 2.3 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5 V ~ 2.3 V	V	1,4
T_{STG}	Storage Temperature	-55 to +100	ºC	1,2

Notes:

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

3) V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV, V_{REF} may be equal to or less than 300 mV.

4) Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

AC & DC operating conditions

Recommended DC operating conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	5
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1,5
V_{REF}	Input Reference Voltage	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	mV	2,3
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	4

Notes:

1) There is no specific device V_{DD} supply voltage requirement for SSTL_18 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

3) Peak to peak ac noise on V_{REF} may not exceed +/- 2% V_{REF}(dc).

4) V_{TT} of transmitting device must track V_{REF} of receiving device.

5) V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDQL} tied together.

Operating temperature condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 95	ºC	1,2
T_{OPER}	Operating Temperature	-40 to 95	ºC	1,2

Notes:

1) Operating Temperature is the case surface temperature on the center/top side of the DRAM.

2) The operation temperature range are the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operation specification may be required. During operation, the DRAM case temperature must be maintained between 0 – 85 ºC under all other specification parameter. However, in some applications, it is desirable to operate the DRAM up to 95 ºC case temperature. Therefore, two spec options may exist.

a) Supporting 0 – 85 ºC with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options.

b) This is an optional feature and not required. Supporting 0 – 85 ºC and being able to extend to 95 ºC with doubling auto-refresh commands in frequency to a 32 ms period (t_{REFI} = 3.9 us)

ODT DC electrical characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Units	Notes
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50Ω	Rtt3(eff)	40	50	60	Ω	1,2
Deviation of VM with respect to V_{DDQ}/2	ΔVM	-6		+6	%	1

Notes:

1) Test condition for Rtt measurements.

2) Optional for DDR2-400/533/667, mandatory for DDR2-800.

Measurement Definition for Rtt(eff): Apply V_{IH}(ac) and V_{IL}(ac) to test pin separately, then measure current I(V_{IH}(ac)) and I(V_{IL}(ac)) respectively. V_{IH}(ac), V_{IL}(ac) and V_{DDQ} values defined in SSTL_18

$$Rtt(eff) = \frac{\mathrm{VIHac} - \mathrm{VILac}}{\mathrm{I(VIHac)} - \mathrm{I(VILac)}}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\left(\frac{2 \times \mathrm{VM}}{VDDQ}\right) - 1\right) \times 100\%$$

Input DC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL}(dc)	DC input logic LOW	-0.3	V_{REF} - 0.125	V	

Input AC logic level

Symbol	Parameter	DDR2-800		Units	Notes
		Min.	Max.		
V_{IH}(ac)	AC input logic HIGH	V_{REF} + 0.2	V_{DDQ} + V_{peak}	V	1
V_{IL}(ac)	AC input logic LOW	V_{SSQ} - V_{peak}	V_{REF} - 0.2	V	1

Notes:

1) Refer to Overshoot/undershoot specifications for V_{peak} value: maximum peak amplitude allowed for overshoot and undershoot.

AC input test conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 x V_{DDQ}	V	1
VSWING(MAX)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2,3

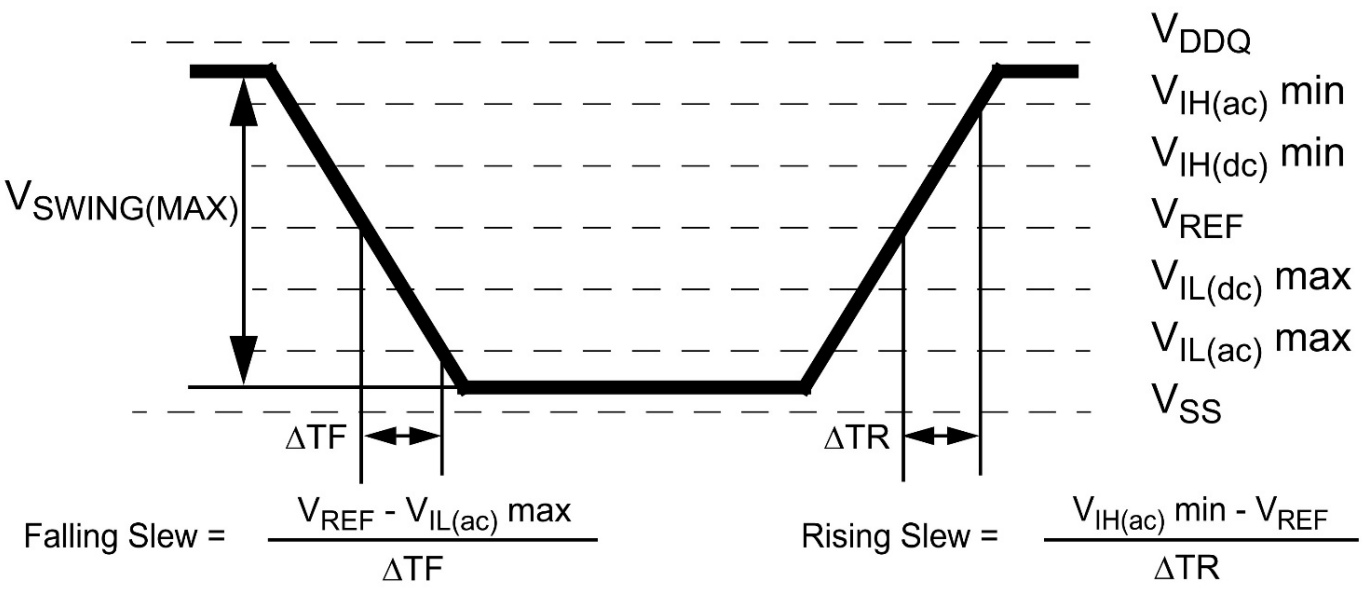
Notes:

1) Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(ac) level applied to the device under test.

2) The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(ac) min for rising edges and the range from V_{REF} to V_{IL}(ac) max for falling edges as shown in the below figure.

3) AC timings are referenced with input waveforms switching from V_{IL}(ac) to V_{IH}(ac) on the positive transitions and V_{IH}(ac) to V_{IL}(ac) on the negative transitions.

AC input test signal waveform



Differential input AC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{ID}(ac)$	AC differential input voltage	0.5	V_{DDQ}	V	1,3
$V_{IX}(ac)$	AC differential crosspoint voltage	0.5 x V_{DDQ} - 0.175	0.5 x V_{DDQ} + 0.175	V	2

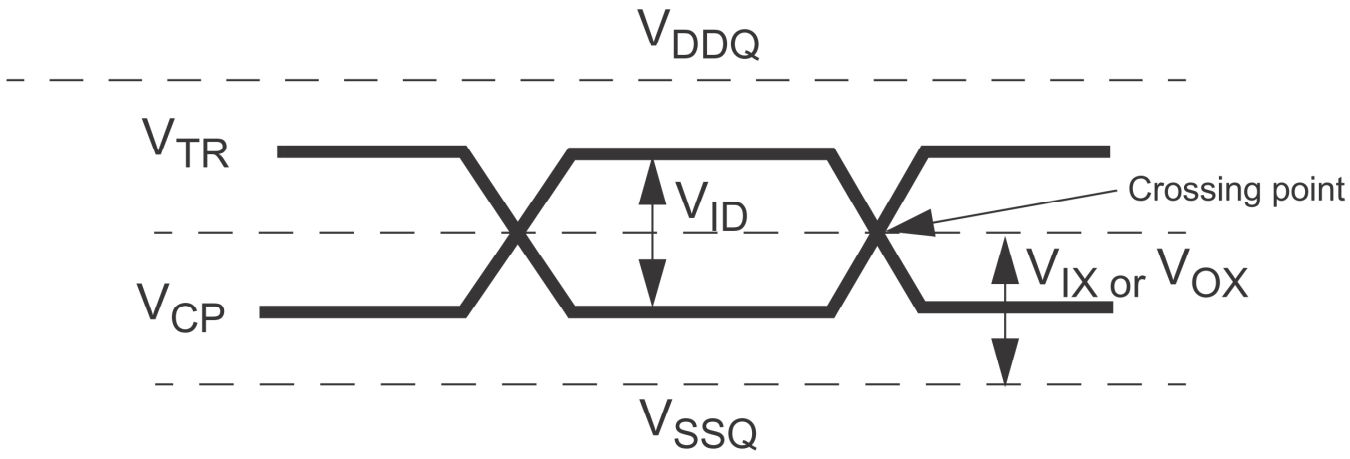
Notes:

1) $V_{ID}(ac)$ specifies the input differential voltage | $V_{TR} - V_{CP}$ | required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH}(ac) - V_{IL}(ac)$.

2) The typical value of $V_{IX}(ac)$ is expected to be about 0.5 x V_{DDQ} of the transmitting device and $V_{IX}(ac)$ is expected to track variations in V_{DDQ}. $V_{IX}(ac)$ indicates the voltage at which differential input signals must cross.

3) Refer to Overshoot/undershoot specifications for V_{peak} value: maximum peak amplitude allowed for overshoot and undershoot.

Differential signal levels



Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{OX}(ac)$	AC differential crosspoint voltage	0.5 x V_{DDQ} - 0.125	0.5 x V_{DDQ} + 0.125	V	1

Notes:

1) The typical value of $V_{OX}(ac)$ is expected to be about 0.5 x V_{DDQ} of the transmitting device and $V_{OX}(ac)$ is expected to track variations in V_{DDQ}. $V_{OX}(ac)$ indicates the voltage at which differential output signals must cross.

Overshoot/undershoot specification

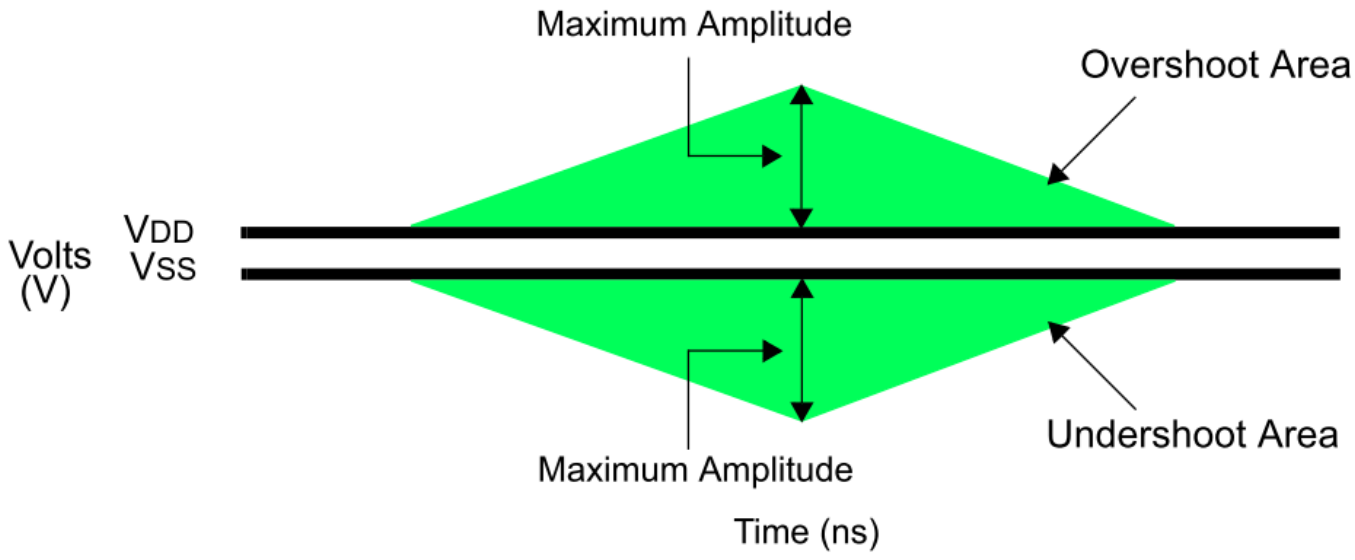
AC overshoot/undershoot specification for address and control pins: A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification
	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V
Maximum overshoot area above V_{DD}	0.66 V-ns
Maximum undershoot area below V_{SS}	0.66 V-ns

Notes:

1) The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Register vendor data sheets will specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets will also specify the maximum overshoot/undershoot that their DRAM can tolerate. This will allow the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register will induce in the specific RDIMM application.

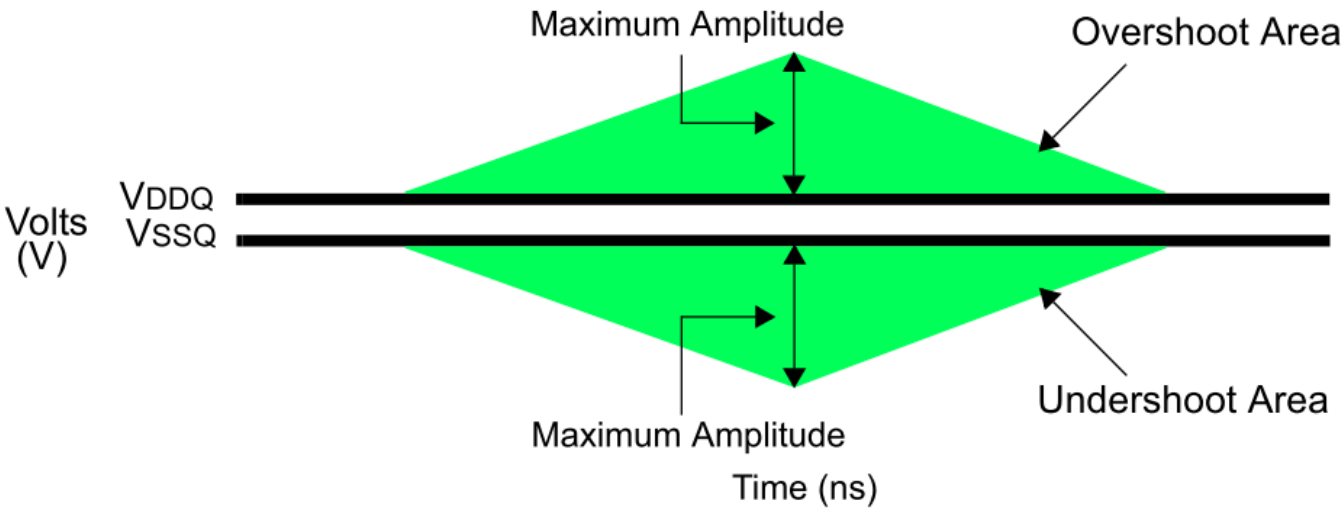
AC overshoot and undershoot definition for address and control pins



AC overshoot/undershoot specification for clock, data, strobe, and mask pins: DQ, (U/L/R)DQS, $\overline{(U/L/R)DQS}$, DM, CK, $\overline{CK}$

Parameter	Specification
	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5 V
Maximum peak amplitude allowed for undershoot area	0.5 V
Maximum overshoot area above V_{DDQ}	0.23 V-ns
Maximum undershoot area below V_{SSQ}	0.23 V-ns

AC overshoot and undershoot definition for clock, data, strobe and mask pins



Power and ground clamps are required on the following input only pins:

a) BA0-BAx
b) A0-Axx
c) $\overline{\text{RAS}}$
d) $\overline{\text{CAS}}$
e) $\overline{\text{WE}}$
f) $\overline{\text{CS}}$
g) ODT
h) CKE

V-I characteristics for input-only pins with clamps

Voltage cross Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Output buffer characteristics

Output AC test conditons

Symbol	Parameter	SSTL_18	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 x V_{DDQ}	V	1

Notes:

1) The V_{DDQ} of the device under test is referenced.

Output DC current drive

Symbol	Parameter	SSTL_18	Units	Notes
I_{OH}(dc)	Output Minimum Source DC Current	-13.4	mA	1,3,4
I_{OL}(dc)	Output Minimum Sink DC Current	13.4	mA	2,3,4

Notes:

1) V_{DDQ} = 1.7V; V_{OUT} = 1420mV. (V_{OUT} - V_{DDQ}) / I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.

2) V_{DDQ} = 1.7V; V_{OUT} = 280mV. V_{OUT} / I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.

3) The dc value of V_{REF} applied to the receiving device is set to V_{TT}.

4) The values of I_{OH}(dc) and I_{OL}(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

OCD default characteristics

Description	Parameter	Min.	Nom.	Max.	Units	Notes
Output impedance		See full strength default driver characteristics			Ω	1
Output impedance step size for OCD calibration		0		1.5	Ω	6
Pull-up and pull-down mismatch		0		4	Ω	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,7,8,9

Notes:

1) Absolute Specifications (T_{OPER}; V_{DD} = +1.8V +/- 0.1V, V_{DDQ} = +1.8V +/- 0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.

2) Impedance measurement condition for output source dc current: V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV; (V_{OUT}-V_{DDQ}) / I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT} / I_{OH} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.

3) Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

4) Slew rate measured from V_{IL}(ac) to V_{IH}(ac).

5) The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

6) This represents the step size when the OCD is near 18Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0Ω value (no calibration) can only be achieved if the OCD impedance is 18Ω +/- 0.75Ω under nominal conditions.

7) DRAM output slew rate specification applies to 400 MT/s. 533 MT/s & 667 MT/s speed bins.

8) Timing skew due to DRAM output slew rate mis-match between DQS/$\overline{\text{DQS}}$ and associated DQ'S is included in t_{DQSQ} and t_{QHS} specification.

9) DDR2 SDRAM output slew rate test load is defined in AC Timing specification Table.

DDR2 SDRAM default output driver V-I characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMR(1) bits A7-A9 = '111'. The driver characteristics evaluation conditions are:

a) Nominal Default 25ºC (Tcase), V_{DDQ} = 1.8V, typical progress

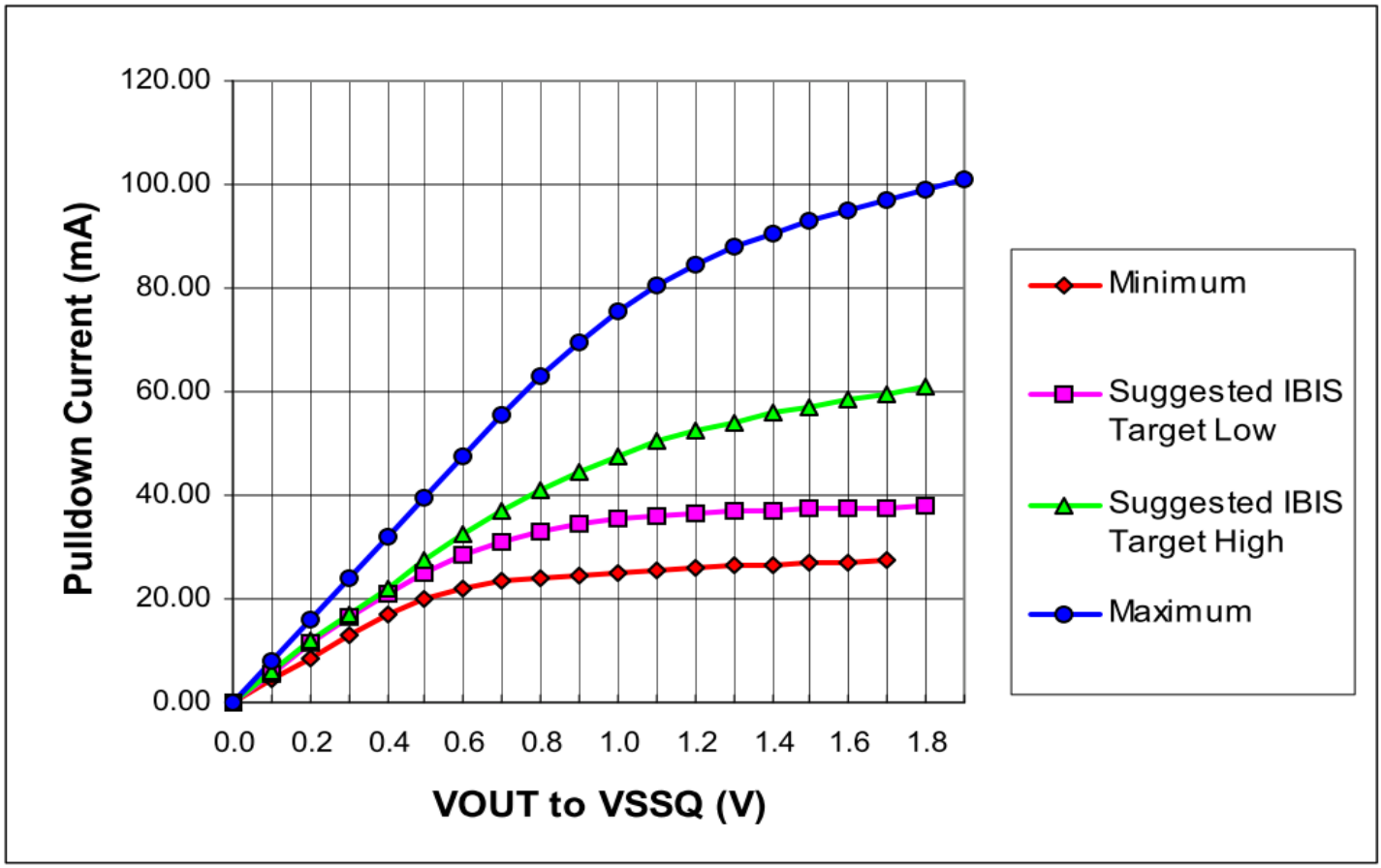
b) Minimum T_{OPER}(max), V_{DDQ} = 1.7V, slow-slow process

c) Maximum 0ºC (Tcase), V_{DDQ} = 1.9V, fast-fast process

Full strength default pulldown driver characteristics

	Pulldown Current (mA)			
Voltage (V)	**Minimum**	**Suggested IBIS Target Low**	**Suggested IBIS Target High**	**Maximum**
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8		37.90	60.90	99.05
1.9				101.05

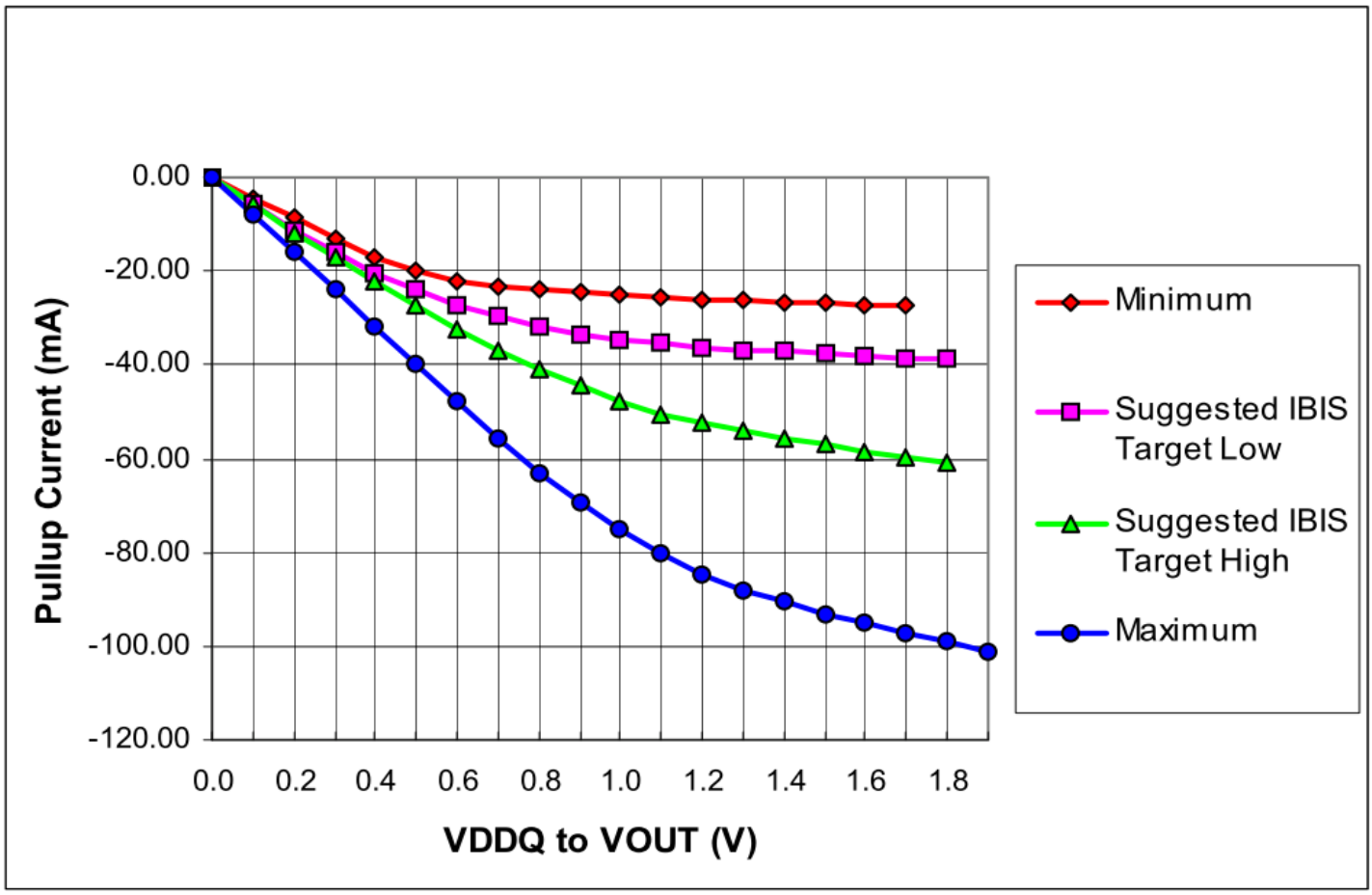
DDR2 default pulldown characteristics for full strength driver



Full strength default pullup driver characteristics

	Pulldown Current (mA)			
Voltage (V)	**Minimum**	**Nominal Default Low**	**Nominal Default High**	**Maximum**
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8		37.90	60.90	99.05
1.9				101.05

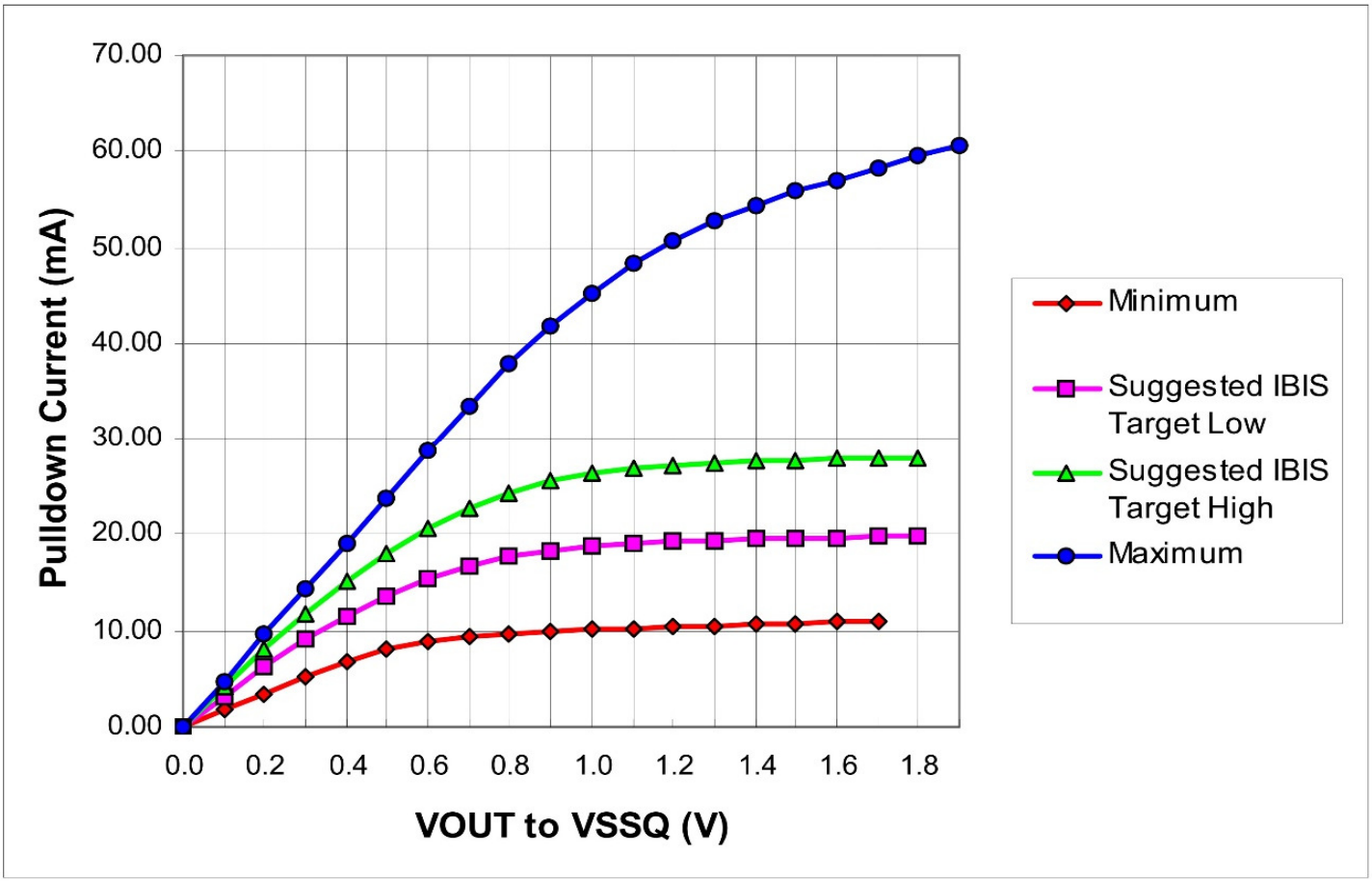
DDR2 default pullup characteristics for full strength output driver



Reduced strength default pulldown driver characteristics

	Pulldown Current (mA)			
Voltage (V)	**Minimum**	**Suggested IBIS Target Low**	**Suggested IBIS Target High**	**Maximum**
0.0	0.00	0.00	0.00	0.00
0.1	1.72	3.24	4.11	4.77
0.2	3.44	6.25	8.01	9.54
0.3	5.16	9.03	11.67	14.31
0.4	6.76	11.52	15.03	19.08
0.5	8.02	13.66	18.03	23.85
0.6	8.84	15.41	20.61	28.62
0.7	9.31	16.77	22.71	33.33
0.8	9.64	17.74	24.35	37.77
0.9	9.89	18.38	25.56	41.73
1.0	10.09	18.80	26.38	45.21
1.1	10.26	19.06	26.90	48.21
1.2	10.41	19.23	27.24	50.73
1.3	10.54	19.35	27.47	52.77
1.4	10.66	19.46	27.64	54.42
1.5	10.77	19.56	27.78	55.80
1.6	10.88	19.65	27.89	57.03
1.7	10.98	19.73	27.97	58.23
1.8		19.80	28.02	59.43
1.9				60.63

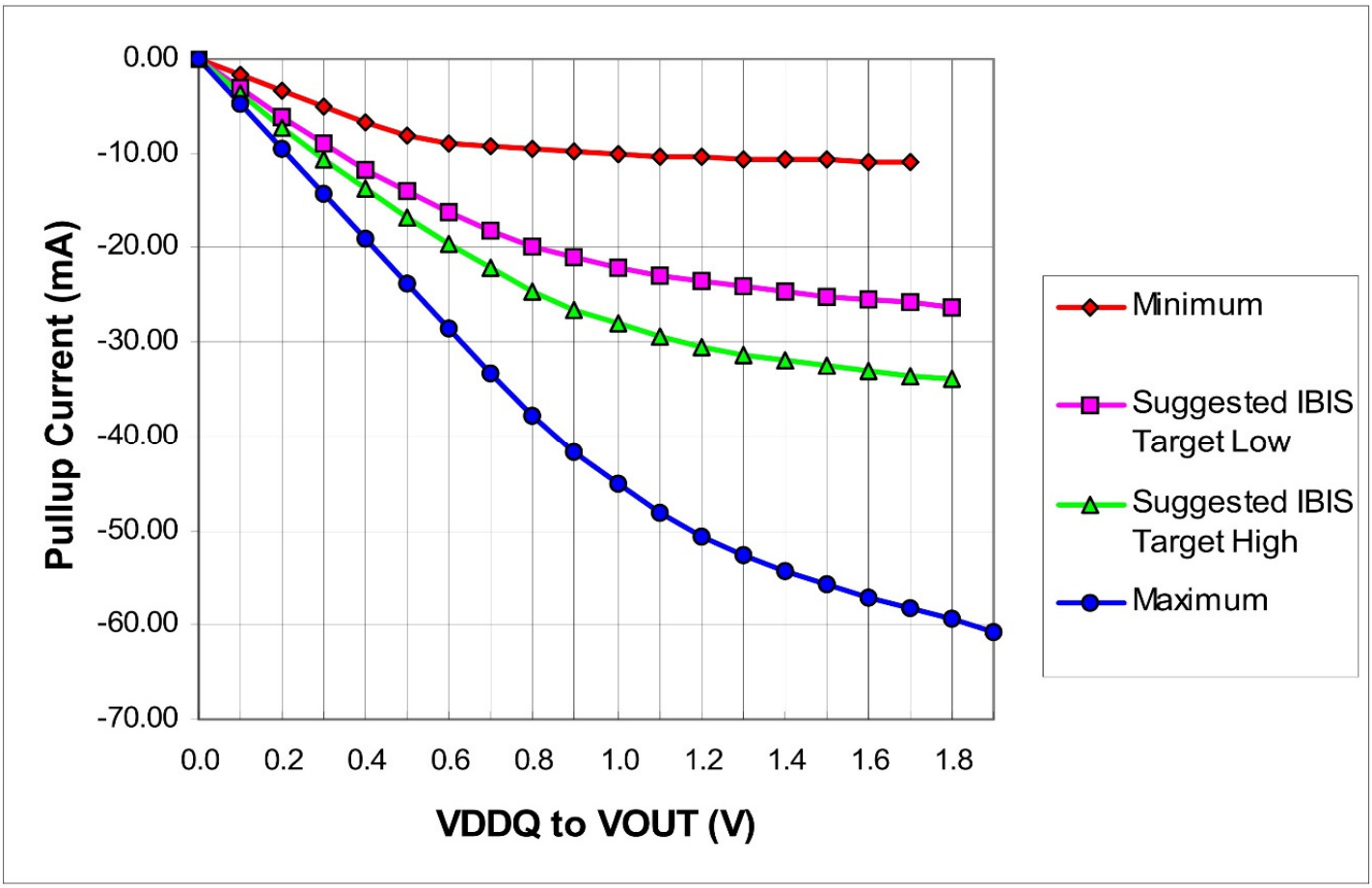
DDR2 default pulldown characteristics for reduced strength drive



Reduced strength default pullup driver characteristics

	Pulldown Current (mA)			
Voltage (V)	**Minimum**	**Suggested IBIS Target Low**	**Suggested IBIS Target High**	**Maximum**
0.0	0.00	0.000	0.00	0.00
0.1	-1.72	-3.200	-3.70	-4.77
0.2	-3.44	-6.200	-7.22	-9.54
0.3	-5.16	-9.040	-10.56	-14.31
0.4	-6.76	-11.690	-13.75	-19.08
0.5	-8.02	-14.110	-16.78	-23.85
0.6	-8.84	-16.270	-19.61	-28.62
0.7	-9.31	-18.160	-22.20	-33.33
0.8	-9.64	-19.770	-24.50	-37.77
0.9	-9.89	-21.100	-26.46	-41.73
1.0	-10.09	-22.150	-28.07	-45.21
1.1	-10.26	-22.960	-29.36	-48.21
1.2	-10.41	-23.610	-30.40	-50.73
1.3	-10.54	-24.160	-31.24	-52.77
1.4	-10.66	-24.640	-31.93	-54.42
1.5	-10.77	-25.070	-32.51	-55.80
1.6	-10.88	-25.470	-33.01	-57.03
1.7	-10.98	-25.850	-33.46	-58.23
1.8		-26.210	-33.89	-59.43
1.9				-60.63

DDR2 default pullup characteristics for reduced strength drive



DDR2 SDRAM calibrated output driver V-I characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in Off-chip driver (OCD) impedance adjustment. The data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18Ω. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5Ω step size with no calibration error at the exact nominal conditions only (I.e. perfect calibration procedure, 1.5Ω maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM Portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

a) Nominal 25ºC (Tcase), V_{DDQ} = 1.8V, typical process
b) Nominal Low and Nominal High 25ºC (Tcase), V_{DDQ} = 1.8V, any process
c) Nominal Minimum T_{OPER}(max), V_{DDQ} = 1.7V, any process
d) Nominal Maximum 0ºC (Tcase), V_{DDQ} = 1.9V, any process

Full strength calibrated pulldown driver characteristics

	Calibrated Pulldown Current (mA)				
Voltage (V)	**Nominal Minimum (21Ω)**	**Nominal Low (18.75Ω)**	**Nominal (18Ω)**	**Nominal High (17.25Ω)**	**Nominal Maximum (15Ω)**
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

Full strength calibrated pullup driver characteristics

	Calibrated Pullup Current (mA)				
Voltage (V)	**Nominal Minimum (21Ω)**	**Nominal Low (18.75Ω)**	**Nominal (18Ω)**	**Nominal High (17.25Ω)**	**Nominal Maximum (15Ω)**
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

I_{DD} Specification

(V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

	Parameter/Condition	I/O	-25 DDR2-800	Units	Notes
			Max		
I_{DD0}	Operating One Bank Active Precharge Current	x8	56	mA	1,2
I_{DD1}	Operating One Bank Active Read Precharge Current	x8	70	mA	1,2
I_{DD2P}	Precharge Power Down Current	x8	12	mA	1,2
I_{DD2N}	Precharge Standby Current	x8	37	mA	1,2
I_{DD2Q}	Precharge Quiet Standby Current	x8	36	mA	1,2
I_{DD3P}	Active Power Down Standby Current MRS(12)=0	x8	32	mA	1,2
	Active Power Down Standby Current MRS(12)=1	x8	32	mA	
I_{DD3N}	Active Standby Current	x8	58	mA	1,2
I_{DD4R}	Operating Current Burst Read	x8	130	mA	1,2
I_{DD4W}	Operating Current Burst Write	x8	132	mA	1,2
I_{DD5B}	Burst Auto-Refresh Current (t_{RFC} = t_{RFC}min)	x8	145	mA	1,2
I_{DD5D}	Distributed Auto-Refresh Current (t_{CK} = t_{CK}min)	x8	18	mA	1,2
I_{DD6}	Self-Refresh Current	x8	12	mA	1,2
I_{DD7}	Operating Current	x8	185	mA	1

Notes:

1) I_{DD} specifications are tested after the device is properly initialized.

2) input slew rate is specified by AC Parametric Test Condition.

3) IDD parameters are specified with ODT disabled.

4) Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS and $\overline{\text{UDQS}}$, I_{DD} values must be met with all combinations of EMRS bits 10 and 11.

5) For DDR2-667/800 testing, t_{CK} in the Conditions should be interpreted as t_{CK}(avg).

6) Definitions for I_{DD}

LOW = V_{in} <= V_{ILAC}(max)

HIGH = V_{in} >= V_{IHAC}(min)

STABLE = inputs stable at a HIGH or LOW level

FLOATING = inputs at V_{REF} = V_{DDQ}/2

SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

I_{DD} testing parameters

Speed	DDR2-800	Units
Bin(CL-t_{RCD}-t_{RP})	5-5-5	
CL(I_{DD})	5	t_{CK}
t_{RCD}(I_{DD})	12.5	ns
t_{RC}(I_{DD})	57.5	ns
t_{RRD}(I_{DD})-1KB	7.5	ns
t_{RRD}(I_{DD})-2KB	10	ns
t_{FAW}(I_{DD})-1KB	35	ns
t_{FAW}(I_{DD})-2KB	45	ns
t_{CK}(I_{DD})	2.5	ns
t_{RAS}min(I_{DD})	45	ns
t_{RAS}max(I_{DD})	70000	ns
t_{RP}(I_{DD})	12.5	ns
t_{RFC}(I_{DD})-2Gb	195	ns

Input/output capacitance

Parameter	Symbol	DDR2-800		Units
		Min.	Max.	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	X	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	X	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	X	0.5	pF

AC Characteristics

(V_{DDQ} = 1.8V ± 0.1V, V_{DD} = 1.8 ± 0.1V)

Parameter		Symbol	(DDR2-800) -25		Units	Notes
			Min.	Max.		
Row Cycle Time		t_{RC}	57.5	-	ns	
Auto Refresh Row Cycle Time		t_{RFC}	195	-	ns	11
Row Active Time		t_{RAS}	45	70K	ns	21
Row Address to Column Address Delay		t_{RCD}	12.5	-	ns	20
Row Active to Row Active Delay (1KB page size)		t_{RRD}	7.5	-	ns	
Row Active to Row Active Delay (2 KB page size)		t_{RRD}	10	-	ns	
Four Activate Window (1 KB page size)		t_{FAW}	35	-	ns	
Four Activate Window (2 KB page size)		t_{FAW}	45	-	ns	
Column Address to Column Address Delay		t_{CCD}	2	-	nCK	
Row Precharge Time		t_{RP}	12.5	-	ns	
Write Recovery Time		t_{WR}	15	-	ns	
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	WR + t_{nRP}	-	nCK	12
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	-	-	ns	2
	$\overline{CAS}$ Latency = 4		3.75	8	ns	2
	$\overline{CAS}$ Latency = 5		2.5	8	ns	2
	$\overline{CAS}$ Latency = 6		2.5	8	ns	
Average clock high pulse width		t_{CH}(avg)	0.48	0.52	t_{CK}(avg)	
Average clock low pulse width		t_{CL}(avg)	0.48	0.52	t_{CK}(avg)	
Data-Out edge to Clock edge Skew		t_{AC}	-0.40	0.40	ns	
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.35	0.35	ns	
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.20	ns	
Data-Out hold time from DQS		t_{QH}	t_{HP} - t_{QHS}	-	ns	
Data hold skew factor		t_{QHS}	-	0.30	ns	
Clock Half Period		t_{HP}	min(t_{CH}(abs),t_{CL}(abs))	-	ns	5
Input Setup Time (fast slew rate)		t_{IS}(base)	0.175	-	ns	15,17

Parameter	Symbol	(DDR2-800) -25		Units	Notes
		Min.	Max.		
Input Hold Time (fast slew rate)	t_{IH}(base)	0.250	-	ns	15,17
Input Pulse Width	t_{IPW}	0.60	-	t_{CK}(avg)	
Write DQS High Level Width	t_{DQSH}	0.35	-	t_{CK}(avg)	
Write DQS Low Level Width	t_{DQSL}	0.35	-	t_{CK}(avg)	
CLK to First Rising edge of DQS-In	t_{DQSS}	-0.25	0.25	t_{CK}(avg)	
Data-In Setup Time to DQS-In (DQ & DM)	t_{DS} (base)	0.05	-	ns	16,17, 18
Data-in Hold Time to DQS-In (DQ & DM)	t_{DH} (base)	0.125	-	ns	16,17, 18
DQS falling edge to CLK rising Setup Time	t_{DSS}	0.2	-	t_{CK}(avg)	
DQS falling edge from CLK rising Hold Time	t_{DSH}	0.2	-	t_{CK}(avg)	
DQ & DM Input Pulse Width	t_{DIPW}	0.35	-	t_{CK}(avg)	
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	t_{CK}(avg)	
Read DQS Postamble Time	t_{RPST}	0.4	0.6	t_{CK}(avg)	
Write DQS Preamble Time	t_{WPRE}	0.35	-	t_{CK}(avg)	
Write DQS Postamble Time	t_{WPST}	0.4	0.6	t_{CK}(avg)	10
Internal read to precharge command delay	t_{RTP}	7.5	-	ns	
Internal write to read command delay	t_{WTR}	7.5	-	ns	13
Data out high impedance time from CLK/$\overline{CLK}$	t_{HZ}	-	t_{AC}(max)	ns	7
DQS/$\overline{DQS}$ low impedance time from CLK/$\overline{CLK}$	$t_{LZ(DQS)}$	t_{AC}(min)	t_{AC}(max)	ns	
DQ low impedance time from CLK/$\overline{CLK}$	$t_{LZ(DQ)}$	2 * t_{AC}(min)	t_{AC}(max)	ns	7
Mode Register Set Delay	t_{MRD}	2	-	nCK	9
MRS command to ODT update delay	t_{MOD}	0	12	ns	
Exit Self Refresh to Non – Read Command	t_{XSNR}	t_{RFC} + 10	-	ns	19
Exit Self Refresh to Read Command	t_{XSRD}	200	-	nCK	
Exit Precharge Power Down to any non-Read Command	t_{XP}	2	-	nCK	14
Exit Active Power Down to Read Command	t_{XARD}	2	-	nCK	

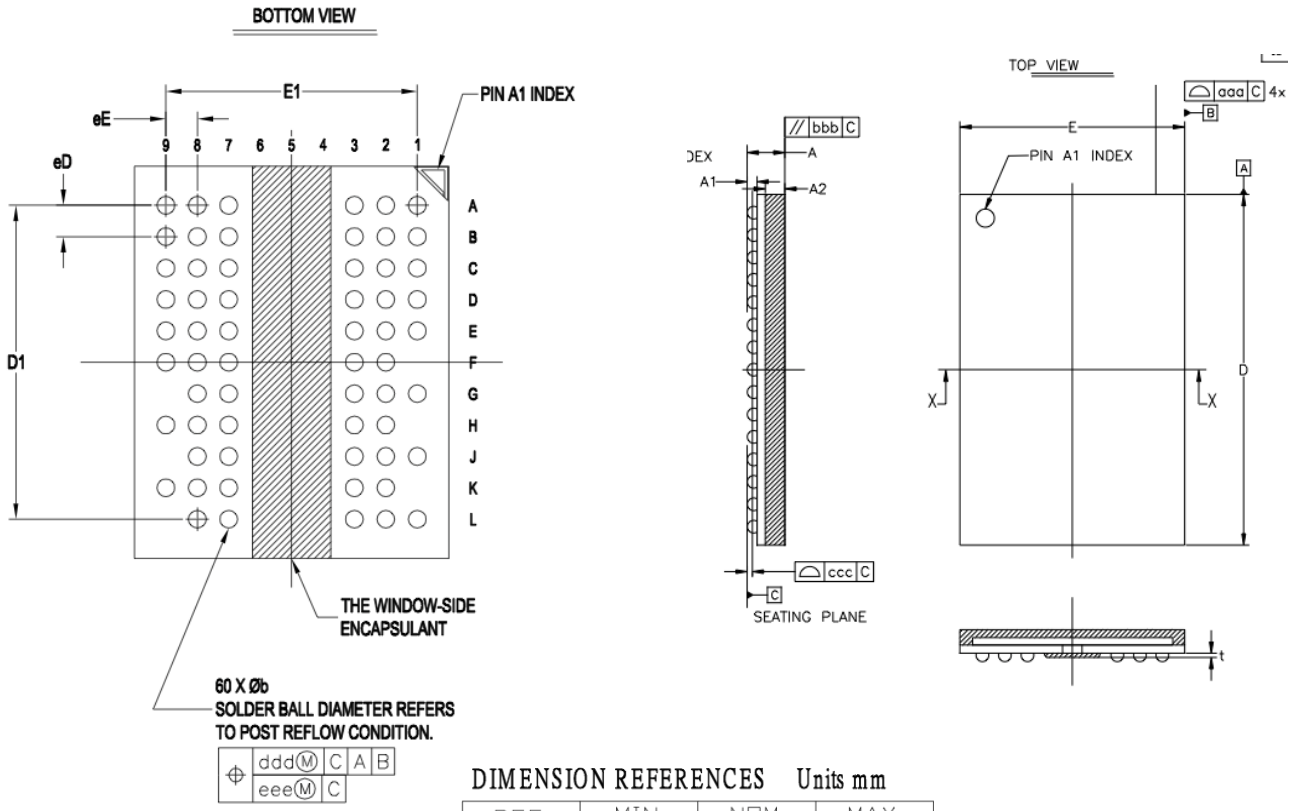
Parameter	Symbol	(DDR2-800) -25		Units	Notes
		Min.	Max.		
Exit Active Power Down to Read Command (Slow exit, Lower Power)	t_{XARDS}	8 - AL	-	nCK	
Minimum time clocks remains ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK}(avg) + t_{IH}$	-	ns	
CKE minimum high and low pulse width	t_{CKE}	3	-	nCK	
Average Periodic Refresh Interval, 0°C ≤ Tcase ≤ +85°C	t_{REFI}	-	7.8	us	18
Average Periodic Refresh Interval, +85°C < Tcase ≤ +95°C	t_{REFI}	-	3.9	us	
Period Jitter	$t_{JIT(PER)}$	-100	100	ps	
Duty Cycle Jitter	$t_{JIT(DUTY)}$	-100	100	ps	
Cycle to Cycle	$t_{JIT(CC)}$	-200	200	ps	
Cumulative error, 2 cycles	$t_{ERR(2PER)}$	-150	150	ps	
Cumulative error, 3 cycles	$t_{ERR(3PER)}$	-175	175	ps	
Cumulative error, 4 cycles	$t_{ERR(4PER)}$	-200	200	ps	
Cumulative error, 5 cycles	$t_{ERR(5PER)}$	-200	200	ps	
Cumulative error, 6-10 cycles	$t_{ERR(6-10PER)}$	-300	300	ps	
Cumulative error, 11-50cycles	$t_{ERR(11-50PER)}$	-450	450	ps	

Notes for Electrical Characteristics & AC Timing

1. Input slew rate is 1 V/ns and AC timings are guaranteed for linear signal transitions.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK / CK) is the point at which CK and $\overline{CK}$ cross: the DQS/$\overline{DQS}$ input reference level is the crosspoint when in differential strobe mode; the input reference level for signals other than CK/$\overline{CK}$, or DQS/$\overline{DQS}$ is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as LOW.
4. The output timing reference voltage level is V_{TT}.
5. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}.
6. For input frequency change during DRAM operation.
7. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8. These parameters guarantee device timing, but they are not necessarily tested on each device.
9. The specific requirement is that DQS and $\overline{DQS}$ be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}. When programmed in differential strobe mode, DQS is always the logic complement of DQS except when both are in high-Z.
10. The maximum limit for this parameter is not a device limit. The device operate with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
11. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device. (Note: t_{RFC} depends on DRAM density)
12. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
13. t_{WTR} is at least two clocks independent of operation frequency.
14. User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MRS, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MRS, A12 =”1”) a slow power-down exit timing t_{XARDS} has to be satisfied.
15. Timings are guaranteed with command / address input slew rate of 1.0 V/ns.
16. Timings are guaranteed with data / mask input slew rate of 1.0 V/ns.
17. Timings are guaranteed with CK/$\overline{CK}$ differential slew rate 2.0 V/ns, and DQS/$\overline{DQS}$ (and RDQS/$\overline{RDQS}$) differential slew rate 2.0 V/ns in differential strobe mode.
18. If refresh timing or t_{DS} / t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19. In all circumstances, t_{XSNR} can be satisfied using t_{XSNR} = t_{RFC} + 10 ns.
20. The t_{RCD} timing parameter is valid for both activate command to read or write command with and without Auto-Pre-charge. Therefore a separate parameter t_{RAP} for activate command to read or write command with Auto-Precharge is not necessary anymore.
21. t_{RAS}(max) is calculated from the maximum amount of time a DDR2 device can operate without a Refresh command which is equal to 9 * t_{REFI}

Package Diagram (x8)

60-Ball Fine Pitch Ball Grid Array Outline



DIMENSION REFERENCES Units mm

REF.	MIN.	NOM.	MAX.
A	---	1.10	1.20
A1	0.25	0.35	0.40
A2	0.50	0.53	0.56
b	0.40	0.45	0.50
D	9.90	10.00	10.10
E	7.90	8.00	8.10
D1		8.00 BSC	
E1		6.40 BSC	
eE		0.80 BSC	
eD		0.80 BSC	
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08
t	---	0.17	0.20

Revision History

Rev	History	Release Date	Remarks
1.0	Formal Release	Oct. 2022	