Data Sheet

ACPL-M75N, ACPL-074N, ACPL-W70N, ACPL-K73N

High-Speed 15-Mbaud Digital CMOS Optocouplers

Description

The Broadcom®ACPL-M75N, ACPL-074N, ACPL-W70N, and ACPL-K73N optocouplers utilize LED packaging and CMOS IC technologies to achieve excellent optical galvanic isolation at a data rate of up to 15 Mbaud.

An internal Faraday shield provides a guaranteed common-mode transient immunity specification of 30 kV/µs, minimum.

The basic building blocks of these optocouplers are a high-speed LED and a CMOS detector IC. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Features

- Superior optical isolation and insulation
- 3.3V and 5V CMOS compatibility
- Low power I_{DD}: 1.5 mA, maximum
- Low LED driving current I_F: 4 mA, minimum
- Data rate: 15 Mbaud, minimum
- Common-mode transient immunity: 30 kV/µs, minimum
- Operating temperature range: –40°C to +125°C
- Package selection: SO-5, SO-8, Stretched SO-6, and Stretched SO-8 packages
- Safety and regulatory approval:
  - IEC/EN 60747-5-5 Insulation Working Voltage:
    567 V_{PK} for ACPL-M75N, ACPL-074N
    1,140 V_{PK} for ACPL-W70N, ACPL-K73N
  - UL 1577 Isolation Voltage:
    3750 V_{RMS}/1 minute for ACPL-M75N, ACPL-074N
    5000 V_{RMS}/1 minute for ACPL-W70N, ACPL-K73N
  - CAN/CSA-C22.2 No. 62368-1

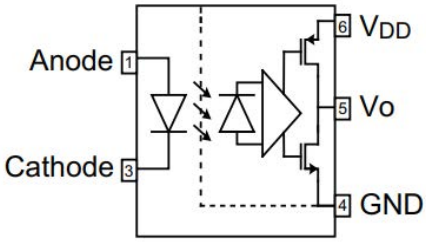
Applications

- Communication interfaces: RS-485, CANBus, and I^2C
- Microprocessor and microcontroller system interfaces
- Digital isolation for A/D and D/A converters

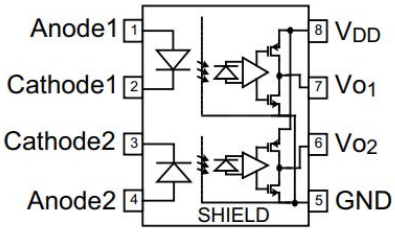
CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments. The components are not AEC-Q100 qualified and not recommended for automotive applications.

Functional Diagrams

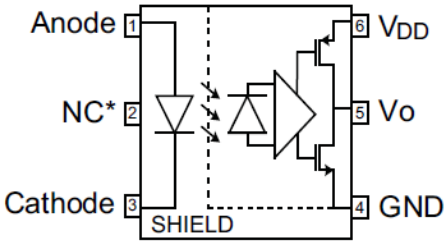
ACPL-M75N



ACPL-074N, ACPL-K73N



ACPL-W70N



NOTE: Connect a 0.1-µF bypass capacitor between pins VDD and GND.

Truth Table

LED	Output V_O
ON	LOW
OFF	HIGH

Recommended Reflow Soldering Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Use non-halide flux.

Ordering Information

The ACPL-M75N and ACPL-074N are UL recognized with an isolation voltage of 3750 V_{RMS} for 1 minute per UL1577.

The ACPL-W70N and ACPL-K73N are UL recognized with an isolation voltage of 5000 V_{RMS} for 1 minute per UL1577.

All devices are RoHS compliant.

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN 60747-5-5	Quantity
ACPL-M75N	-000E	SO-5	X	—	—	100 per tube
	-060E		X	—	X	100 per tube
	-500E		X	X	—	1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-074N	-000E	SO-8	X	—	—	100 per tube
	-060E		X	—	X	100 per tube
	-500E		X	X	—	1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-W70N	-000E	Stretched SO-6	X	—	—	100 per tube
	-060E		X	—	X	100 per tube
	-500E		X	X	—	1000 per reel
	-560E		X	X	X	1000 per reel
ACPL-K73N	-000E	Stretched SO-8	X	—	—	80 per tube
	-060E		X	—	X	80 per tube
	-500E		X	X	—	1000 per reel
	-560E		X	X	X	1000 per reel

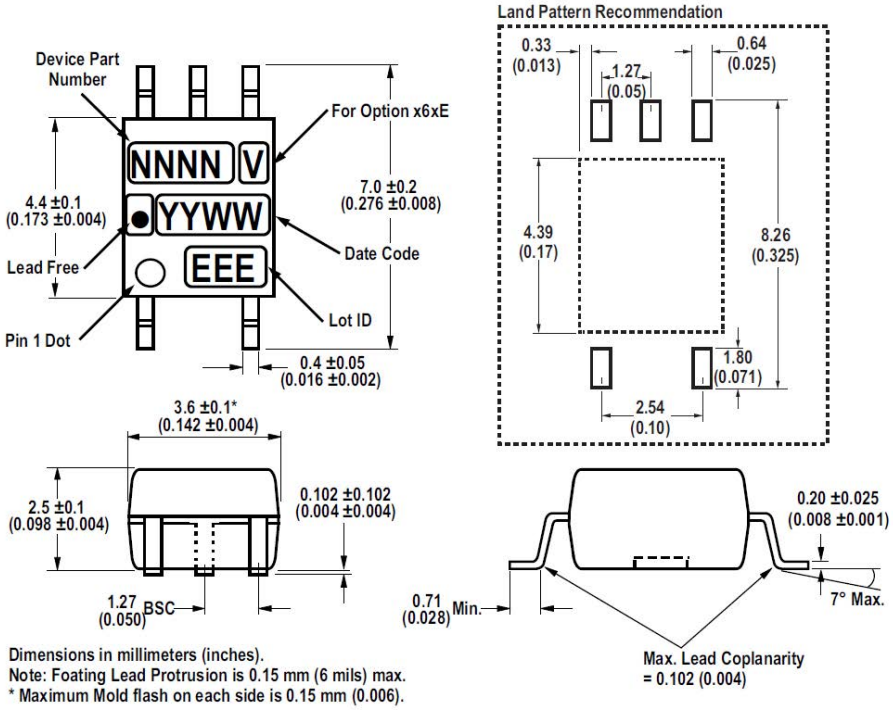
To order, choose a part number from the part number column and combine it with the desired option from the option column to form an order entry.

Example: Specify part number ACPL-M75N-560E to order an optocoupler with a surface-mount SO-5 package in tape and reel packaging with 1500 parts per reel, with IEC/EN 60747-5-5 safety approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

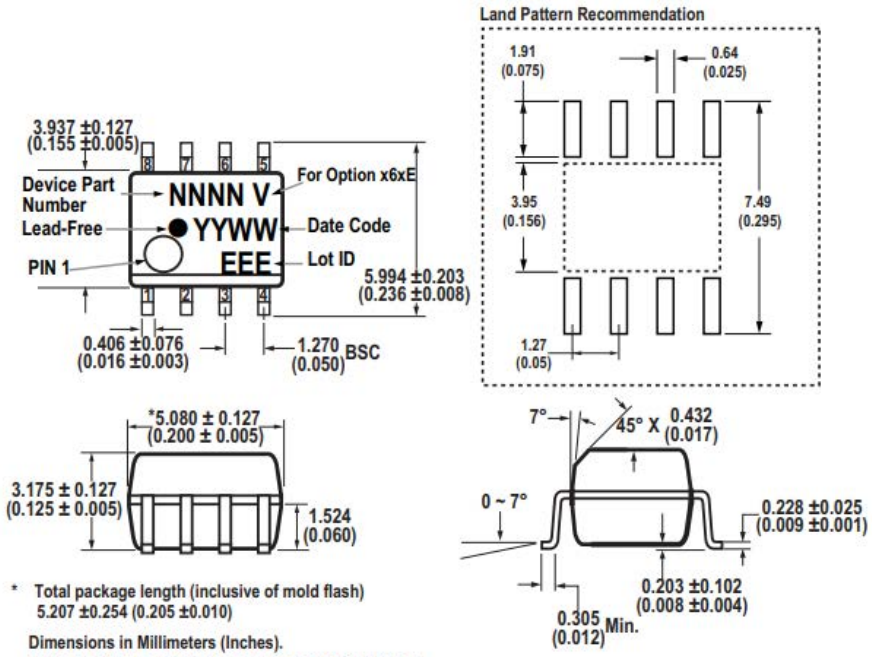
Package Outline Drawings

ACPL-M75N SO-5 Package



Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.
* Maximum Mold flash on each side is 0.15 mm (0.006).

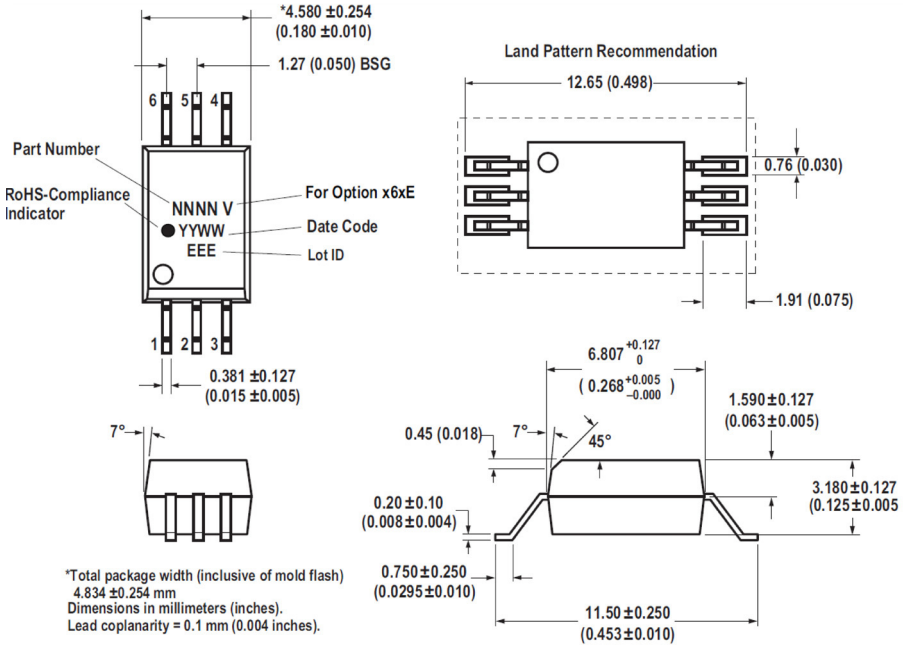
ACPL-074N SO-8 Package



* Total package length (inclusive of mold flash) 5.207 ±0.254 (0.205 ±0.010)

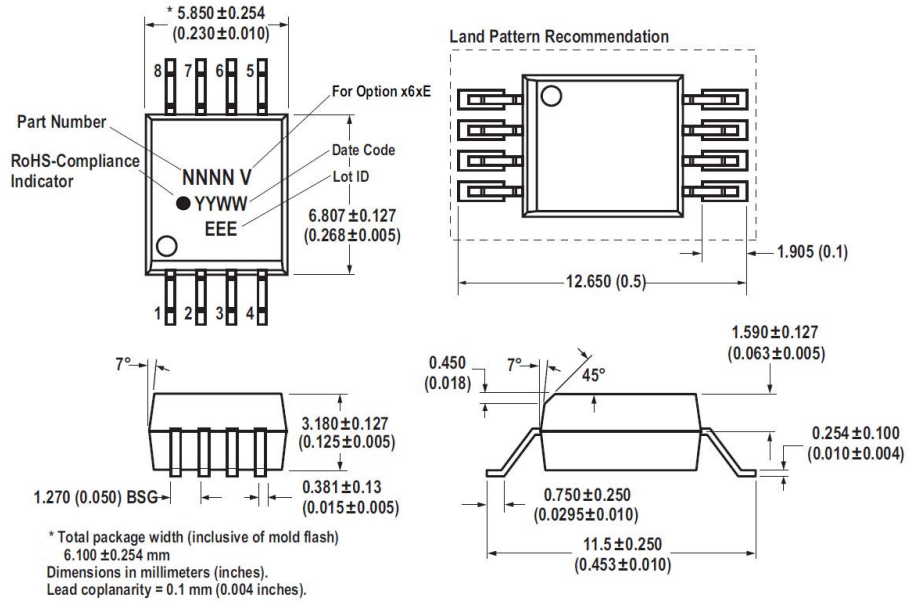
Dimensions in Millimeters (Inches).
Note: Floating lead protrusion is 0.15 mm (6 mils) max.
Lead coplanarity = 0.10 mm (0.004 inches) max.
Option number 500 not marked.

ACPL-W70N Stretched SO-6 Package



*Total package width (inclusive of mold flash)
4.834 ±0.254 mm
Dimensions in millimeters (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

ACPL-K73N Stretched SO-8 Package



* Total package width (inclusive of mold flash)
6.100 ±0.254 mm
Dimensions in millimeters (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Regulatory Information

IEC/EN 60747-5-5	Option 060, 560 only
UL	Approved under UL 1577, component recognition program, File E55361
CSA	Approved under CAN/CSA-C22.2 No. 62368-1

Insulation-Related and Safety-Related Specifications

Parameter	Symbol	ACPL-074N	ACPL-M75N	ACPL-W70N ACPL-K73N	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	4.9	5.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	4.8	5.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	≥175	≥175	V	VDE 0303-11/DIN EN 60112 (2010-05)
Isolation Group	—	IIIa	IIIa	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN 60747-5-5 Insulation-Related Characteristics (Option 060/560)

Parameter	Symbol	Characteristics		Unit
		ACPL-074N ACPL-M75N	ACPL-W70N ACPL-K73N	
Installation Classification per DIN VDE 0110/1.89, Table 1				
For Rated Mains Voltage ≤150 V_{RMS}	—	I-IV	I-IV	—
For Rated Mains Voltage ≤300 V_{RMS}	—	I-IV	I-IV	—
For Rated Mains Voltage ≤600 V_{RMS}	—	I-III	I-IV	—
For Rated Mains Voltage ≤1000 V_{RMS}	—	I-II	I-III	—
Climatic Classification	—	40/125/21	40/125/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	2	—
Maximum Working Insulation Voltage	V_{IORM}	567	1140	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	1063	2137	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, Test with t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	907	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	6000	8000	V_{PEAK}
Safety-Limiting Values: Maximum values allowed in the event of a failure				
Case Temperature	T_S	150	175	°C
Input Current	$I_{S, INPUT}$	150	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$\geq 10^9$	$\geq 10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section (IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Condition
Storage Temperature	T_S	–55	+125	°C	
Ambient Operating Temperature	T_A	–40	+125	°C	
IC Junction Temperature	T_J	—	+150	°C	
Supply Voltage	V_{DD}	0	6.5	V	
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V	
Average Forward Input Current (per channel)	I_F	—	20	mA	
Peak Transient Input Current (I_F at 1-µs pulse width, <10% duty cycle)	$I_{F(tran)}$	—	1	A	<1-µs pulse width, <300 pulses per second
			80	mA	<1-µs pulse width, <10% duty cycle
Input Power Dissipation	P_I	—	35	mW	
Output Power Dissipation (per channel)	P_O	—	30	mW	
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Recommended Reflow Soldering Profile.				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltage	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Forward Input Current	$I_{F(ON)}$	4	10	mA
Forward Off State Voltage	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended ambient operating temperature T_A = –40°C to +125°C, 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at V_{DD} = +5V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure
Input Forward Voltage	V_F	1.20	1.50	1.85	V	I_F = 6 mA	1
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.6	VDD – 0.2	—	V	I_{OH} = –3.2 mA, I_F = 0	4
Logic Low Output Voltage	V_{OL}	—	0.25	0.60	V	I_{OL} = 4 mA, I_F = 6 mA	3
Input Threshold Current	I_{TH}	—	0.7	3.5	mA		
Logic High Output Supply Current (per channel)	I_{DDH}	—	0.9	1.5	mA	I_F = 0	
Logic Low Output Supply Current (per channel)	I_{DDL}	—	1.0	1.5	mA	I_F = 6 mA	
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0V	
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C		

Switching Specifications (AC)

Over recommended ambient operating temperature T_A = –40°C to +125°C, 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at V_{DD} = +5V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	36	55	ns	I_F = 6 mA, CMOS Signal Level	5, 6, 7, 8, 9
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	30	55	ns		
Pulse Width Distortion[b]	| PWD |	—	6	25	ns		
Propagation Delay Skew[c]	t_{PSK}	—	—	25	ns		
Output Rise Time (10% to 90%)	t_R	—	6	—	ns		
Output Fall Time (90% to 10%)	t_F	—	5	—	ns		
Static Common-Mode Transient Immunity at Logic High Output[d]	CM_H	30	—	—	kV/µs	V_{CM} = 1000V, I_F = 6 mA, CMOS Signal Level, T_A = 25°C	10
Static Common-Mode Transient Immunity at Logic Low Output[e]	CM_L	30	—	—	kV/µs	V_{CM} = 1000V, I_F = 6 mA, CMOS Signal Level, T_A = 25°C	11

a. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common-mode voltage to assure that the output remains in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common-mode voltage to assure that the output remains in a low logic state.

Package Characteristics

All typical specifications are at T_A = +25°C.

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Unit	Test Conditions
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	ACPL-074N ACPL-M75N	3750	—	—	V_{RMS}	RH ≤50%, t = 1 minute, T_A = 25°C
		ACPL-W70N ACPL-K73N	5000	—	—		
Input-Output Resistance	R_{I-O}	—	—	10^{14}	—	Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}	—	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

a. In accordance with UL 1577, ACPL-M75N/074N are proof tested by applying an insulation test voltage ≥4500 V_{rms} for 1 second, and ACPL-W70N/K73N are proof tested by applying an insulation test voltage ≥6000 V_{rms} for 1 second; leakage detection current limit, I_{I-O} ≤5 µA.

Performance Plots

Figure 1: Typical Diode Input Forward Current Characteristic

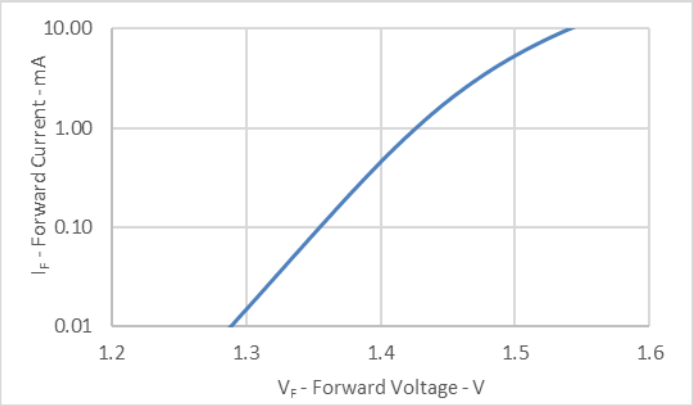


Figure 2: Typical Output Voltage vs. Input Forward Current

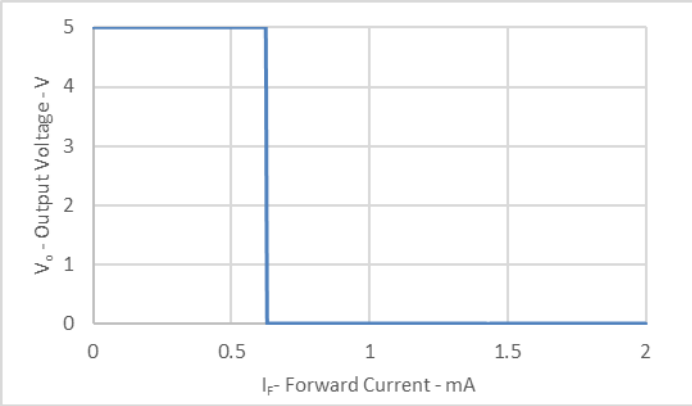


Figure 3: Typical Logic Low Output Voltage vs. Logic Low Output Current

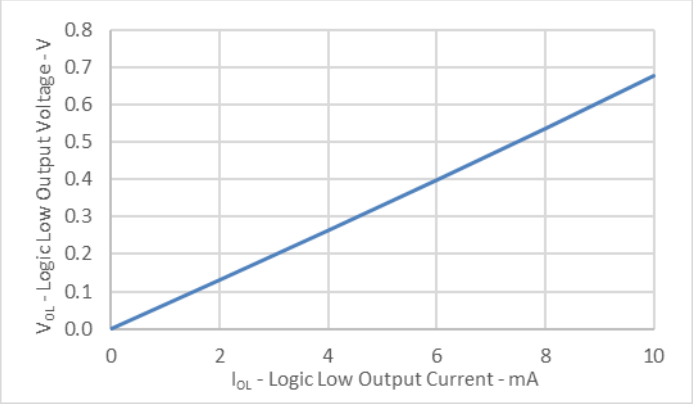


Figure 4: Typical Logic High Output Voltage vs. Logic High Output Current

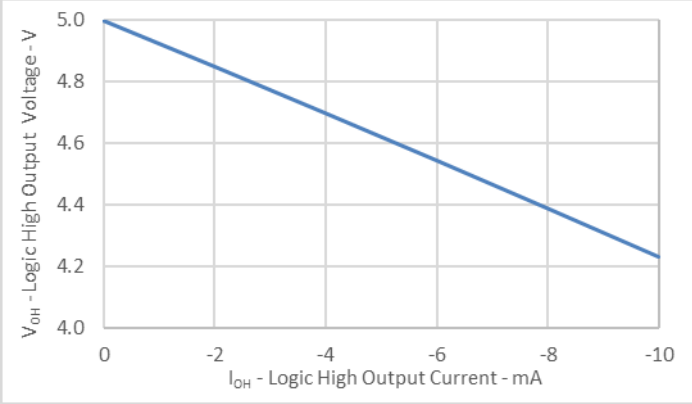


Figure 5: Typical Switching Speed vs. Temperature at 5V

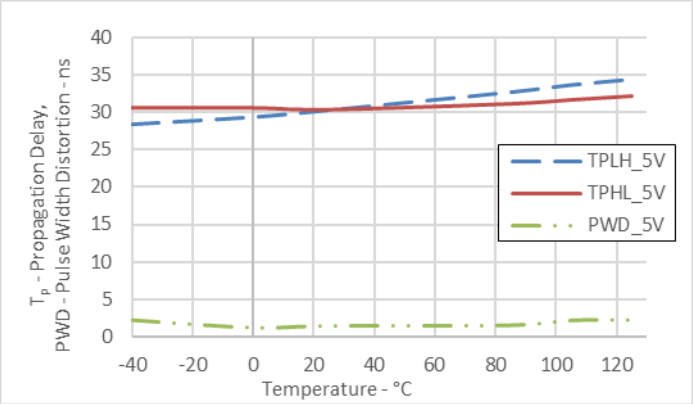


Figure 6: Typical Switching Speed vs. Temperature at 3V

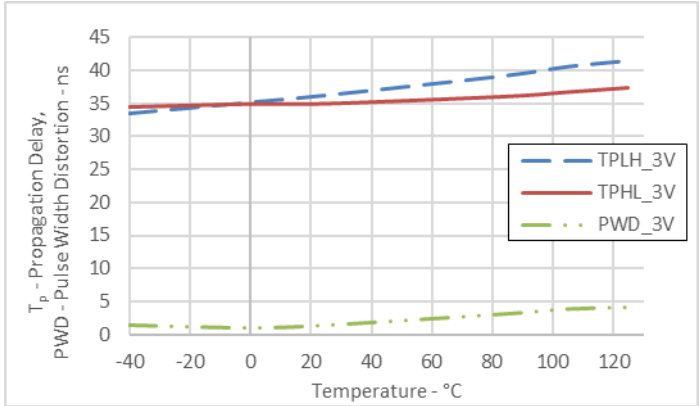


Figure 7: Typical Switching Speed vs. Forward Current at 5V

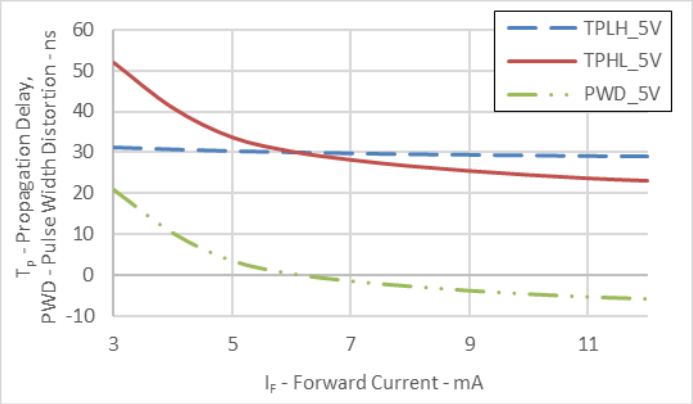
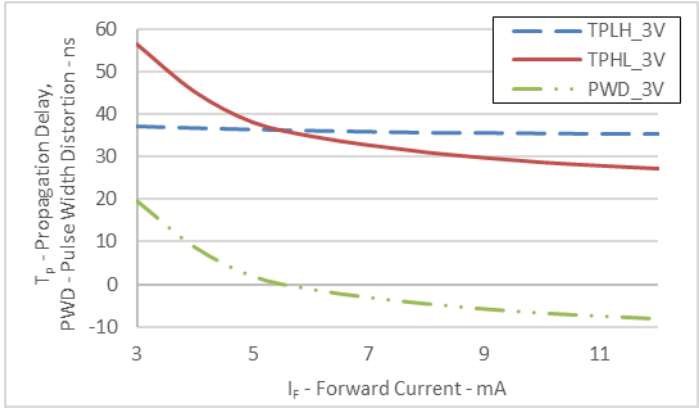
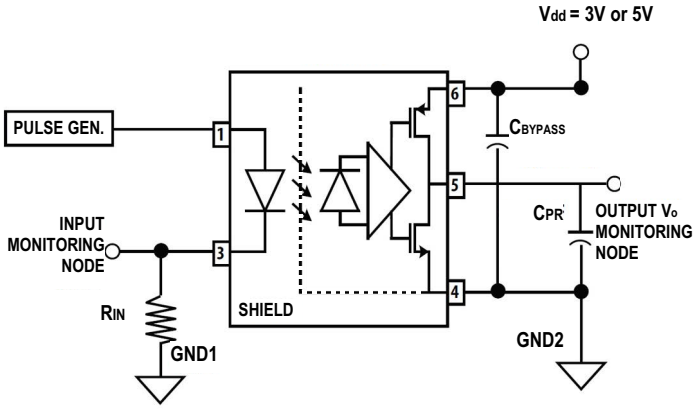


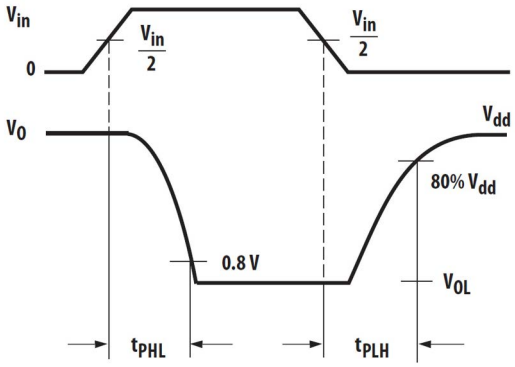
Figure 8: Typical Switching Speed vs. Forward Current at 3V



Test Circuit Diagrams

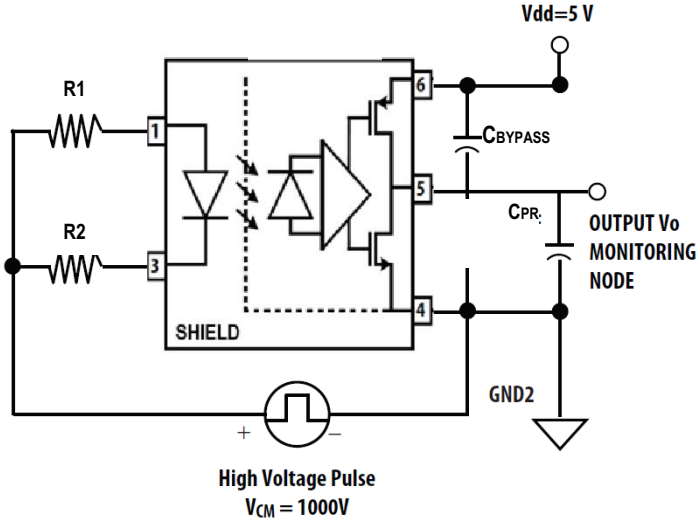
Figure 9: Switching Speed Test Circuit and Typical Waveform





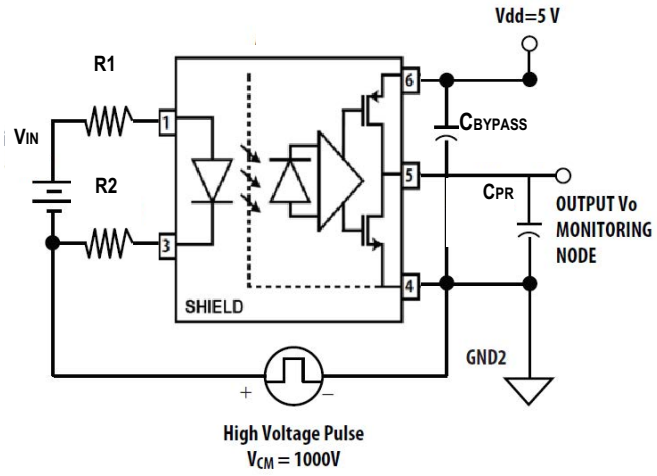
R_{IN}	560Ω
C_{PR}	Capacitance induced from probe and jig
C_{BYPASS}	0.1-µF bypass capacitor

Figure 10: CMR Test Circuit (for CM_H)



R_1	390Ω
R_2	180Ω
C_{PR}	Capacitance induced from probe and jig
C_{BYPASS}	0.1-µF bypass capacitor

Figure 11: CMR Test Circuit (for CM_L)



V_{IN}	5.0V
R_1	390Ω
R_2	180Ω
C_{PR}	Capacitance induced from probe and jig
C_{BYPASS}	0.1-µF bypass capacitor

NOTE: The provided test circuits are for single-channel devices, but the same circuit configuration can be applied to dual-channel devices using similar component values.

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