



# MT6319 4-Phase Buck Converter Product Brief

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**The full datasheet is available with an NDA**

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## Version History

Version	Date	Description
1.0	2023-09-18	Official release
1.1	2025-09-16	Updated the pin map and the pin descriptions. Categorized the functions using different colors. Updated Table 2-3. Pin voltage range Added a new part MT6319AAP and MT6319ABP: <ul style="list-style-type: none"><li>Added information in Table 1-1. Ordering options, Table 1-2. Part voltage table</li></ul>

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# 1 Overview

## 1.1 Features

- Four high-efficiency step-down DC/DC
  - Max. output current 5A per phase
  - Phases bundled up to a 4-phase converter
  - Programmable over-current protection
  - Programmable loop compensation for each phase configuration by eFuse
  - Auto CCM/PFM, force-CCM operation and automatic low power mode setting
  - Remote differential feedback voltage sensing
  - Vout range = 0.3~1.19375V with 6.25 mV per step, DVS through compatible interface or SRCLKEN pin
- SPMI or I2C-compatible interface which supports high-speed modes in 5G modem application field
- Selectable interface (SPMI/I2C) by eFuse
- Dedicated FAULTB pin to report fault alarm to main PMIC
- Chip enable pin for on/off control
- Output short circuit and input over-voltage protection
- Over-temperature protection
- Input under-voltage lockout (UVLO)
- 45-pin 2.35×3.44 mm WLCSP package

## 1.2 Applications

- Smart phones, eBooks and tablets, mobile phones and Ultrabooks
- Handsets, gaming devices, car infotainment
- TV and media players
- Industrial HMI, desktop POS, KIOSK, digital signage

## 1.3 General Description

The MT6319 is designed to meet the power management requirements of the latest applications processors in mobile phones and similar portable applications.

The device contains four step-down DC/DC converters, which are bundled together in 4-phase buck converter and can be configured into various phase configurations by eFuse to power any application requirement.

The device is fully controlled by SPMI interface or an I2C compatible serial interface.

The MT6319 focuses on high-efficiency, step-down conversion over a wide output current range. The step-down converter enters the low power mode at light load for maximum efficiency. The regulator supports remote differential voltage sensing to compensate  $I \cdot R$  drop between the regulator output and the load.

The protection features include short-circuit protection, output under voltage protection (power good function), input OVP, UVLO and temperature warning and shutdown functions.

Several fault flags are provided for status information of the IC.

During startup, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.

The MT6319 is available in a 45-pin WLCSP package. The operating temperature ranges from  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

## 1.4 Ordering Information

**Table 1-1. Ordering option**

Part Number	Package	Operational Temperature Range
MT6319LP/A	WLCSP 45L	$-30^{\circ}\text{C} \sim +85^{\circ}\text{C}$
MT6319AAP/A	WLCSP 45L	$-30^{\circ}\text{C} \sim +85^{\circ}\text{C}$
MT6319ABP/A	WLCSP 45L	$-30^{\circ}\text{C} \sim +85^{\circ}\text{C}$

## 1.5 Part Voltage Table

**Table 1-2. Part voltage table**

Top marking <sup>(1)</sup>	Default voltage (V)	I <sub>max</sub> <sup>(2)</sup> (mA)	Default on (Y/N)	Configuration	Lo	Application
MT6319LP/A	0.75	5,000*2	Y	VBUCK1	0.24 $\mu\text{H}$	CPUB
				VBUCK2	0.24 $\mu\text{H}$	
	1.125	5,000	Y	VBUCK3	0.24 $\mu\text{H}$	VDD2
	0.6	5,000	Y	VBUCK4	0.24 $\mu\text{H}$	VDDQ
MT6319AAP/A	0.75	5,000*2	Y	VBUCK1	0.24 $\mu\text{H}$	CPUB
				VBUCK2	0.24 $\mu\text{H}$	
	1.125	5,000	Y	VBUCK3	0.24 $\mu\text{H}$	VDD2
	0.6	5,000	Y	VBUCK4	0.47 $\mu\text{H}$	VDDQ
MT6319ABP/A	0.75	5,000*2	Y	VBUCK1	0.24 $\mu\text{H}$	CPUB
				VBUCK2	0.24 $\mu\text{H}$	
	1.05	5,000	Y	VBUCK3	0.24 $\mu\text{H}$	VDD2H
	0.50625	5,000	Y	VBUCK4	0.47 $\mu\text{H}$	VDDQ

(1) Note 1 The parts top marking (LP) interface is used by SPMI only.

(2) Note 2 I<sub>max</sub> for multi-phase configurations should consider the over-temperature protection possibility since they are hosted in a tiny package.

## 1.6 Pin Assignment and Description

The MT6319 pin information is distributed as below.

Section 1.6.1 The MT6319 pin map overview (Figure 1-1).

The function groups for the MT6319 pin map are categorized as follows.

	I
	O
	PWR
	GND
	I/O
	NC

Section 1.6.2 Lists all the detailed pin descriptions.

### 1.6.1 Pin Map

	1	2	3	4	5	6	
A	<a href="#">PVDD2</a>	<a href="#">VBUCK2</a>	<a href="#">PGND2</a>	<a href="#">PGND1</a>	<a href="#">VBUCK1</a>	<a href="#">PVDD1</a>	A
B	<a href="#">PVDD2</a>	<a href="#">VBUCK2</a>	<a href="#">PGND2</a>	<a href="#">PGND1</a>	<a href="#">VBUCK1</a>	<a href="#">PVDD1</a>	B
C	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">INT</a>	C
D	<a href="#">AV</a>	<a href="#">VFBN2</a>	<a href="#">VFBN2</a>	<a href="#">FAULTB</a>	<a href="#">VFBN1</a>	<a href="#">VFBN1</a>	D
E	<a href="#">DVDD18</a>	<a href="#">FSOURCE</a>	<a href="#">SRCLKEN</a>	<a href="#">WDTRSTB</a>	<a href="#">SCLK</a>	<a href="#">SDAT</a>	E
F	<a href="#">AG</a>	<a href="#">VFBN4</a>	<a href="#">VFBN4</a>	<a href="#">EN</a>	<a href="#">VFBN3</a>	<a href="#">VFBN3</a>	F
G	<a href="#">DVDD18_VIO</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">NC</a>	<a href="#">RSV1</a>	G
H	<a href="#">PVDD4</a>	<a href="#">VBUCK4</a>	<a href="#">PGND4</a>	<a href="#">PGND3</a>	<a href="#">VBUCK3</a>	<a href="#">PVDD3</a>	H
J	<a href="#">PVDD4</a>	<a href="#">VBUCK4</a>	<a href="#">PGND4</a>	<a href="#">PGND3</a>	<a href="#">VBUCK3</a>	<a href="#">PVDD3</a>	J
	1	2	3	4	5	6	

	I
	O
	PWR
	GND
	I/O
	NC

Figure 1-1. MT6319 WLCSP 45L (2.35×3.44 mm) pin assignment

## 1.6.2 Pin Descriptions

Table 1-3. MT6319 pin descriptions

Ball Name	Ball Location	I/O Type	Description
<b>BUCK</b>			
AV	D1	PWR	Analog input for buck, to be connected to VSYS
AG	F1	GND	Ground of analog
VBUCK1	A5, B5	O	Switching node for buck 1
VBUCK2	A2, B2	O	Switching node for buck 2
VBUCK3	H5, J5	O	Switching node for buck 3
VBUCK4	H2, J2	O	Switching node for buck 4
PVDD1	A6, B6	PWR	Power input for buck 1, to be connected to VSYS
PVDD2	A1, B1	PWR	Power input for buck 2, to be connected to VSYS
PVDD3	H6, J6	PWR	Power input for buck 3, to be connected to VSYS
PVDD4	H1, J1	PWR	Power input for buck 4, to be connected to VSYS
PGND1	A4, B4	GND	Ground of power 1
PGND2	A3, B3	GND	Ground of power 2
PGND3	H4, J4	GND	Ground of power 3
PGND4	H3, J3	GND	Ground of power 4
VFBP1	D6	I	BUCK1 positive feedback
VFBP2	D2	I	BUCK2 positive feedback
VFBP3	F6	I	BUCK3 positive feedback
VFBP4	F2	I	BUCK4 positive feedback
VFBN1	D5	I	BUCK1 negative ground feedback
VFBN2	D3	I	BUCK2 negative ground feedback
VFBN3	F5	I	BUCK3 negative ground feedback
VFBN4	F3	I	BUCK4 negative ground feedback
<b>Digital</b>			
DVDD18_VIO	G1	PWR	Power to SPMI I/O, to make slave/master use the same power
DVDD18	E1	PWR	Digital power 1.8V
SRCLKEN	E3	I	Sleep control input
WDRSTB	E4	I	Watchdog reset input
SCLK	E5	I/O	SPMI/I2C clock
SDAT	E6	I/O	SPMI/I2C data
INT	C6	O	Interrupt output
FSOURCE	E2	I	eFuse power for programming
<b>Interface</b>			
EN	F4	I	Chip enable pin
FAULTB	D4	O	Fault alarm signal
<b>Others</b>			
RSV1	G6	O	For analog test
NC	C1~C5, G2~G5	NC	NC

## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 2-1. Absolute maximum ratings**

Parameter	Condition	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery pin input <sup>(1)</sup>	Steady state	-0.5		6	V
	Transient (< 10 ms)	-0.5		6	V
Non-battery power pin <sup>(2)</sup>	Steady state	-0.5		5	V
Signal pin <sup>(3)</sup>	Steady state	-0.5		V <sub>xx</sub> + 0.5 <sup>(3)</sup>	V
ESD robustness	HBM	2,000			V

(1) Note 1 VSYS\_XXX/Vxxx (BUCK SW node)/VSYSSENS/BATADC -> battery input pin

(2) Note 2 Non-battery power input -> refer to Table 2-1 (PWR pin but not connected with battery)

(3) Note 3 V<sub>xx</sub> = Max. operation voltage (refer to Table 2-2)

### 2.2 Thermal Characteristics

**Table 2-2. Thermal Characteristics**

Parameter	Condition	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient ( $\Theta_{JA}$ )	In free air		43.9		°C/W

Note. The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-7 condition.

## 2.3 Pin Voltage Range

The table below lists the operating voltage ranges for all MT6319 I/O pins.

**Table 2-3. Pin voltage range**

Ball	Symbol	Voltage Range	Unit
A5, B5	VBUCK1	0~5	V
A2, B2	VBUCK2	0~5	V
H5, J5	VBUCK3	0~5	V
H2, J2	VBUCK4	0~5	V
A6, B6	PVDD1	0~5	V
A1, B1	PVDD2	0~5	V
H6, J6	PVDD3	0~5	V
H1, J1	PVDD4	0~5	V
D1	AV	0~5	V
G1	DVDD18_VIO	0~1.98	V
A4, B4	PGND1	0	V
A3, B3	PGND2	0	V
H4, J4	PGND3	0	V
H3, J3	PGND4	0	V
F1	AG	0	V
E1	DVDD18	0~1.98	V
D6	VFBP1	0~5	V
D5	VFBN1	0	V
D2	VFBP2	0~5	V
D3	VFBN2	0	V
F6	VFBP3	0~5	V
F5	VFBN3	0	V
F2	VFBP4	0~5	V
F3	VFBN4	0	V
F4	EN	0~5	V
E3	SRCLKEN	0~1.98	V
E4	WDTRSTB	0~1.98	V
E5	SCLK	0~1.98	V
E6	SDAT	0~1.98	V
C6	INT	0~1.98	V
D4	FAULTB	0~5	V
E2	FSOURCE	0~7.5	V
G6	RSV1	0~5	V

## 2.4 Recommended Operating Range

**Table 2-4. Operation condition**

Parameter	Condition	Min.	Typical	Max.	Unit
Operating temperature range		-30		85	°C

## 2.5 Electrical Characteristics

VBAT = 2.5~5V, minimum loads applied on all outputs, unless otherwise noted

Typical values are at TA = 25°C.

**Table 2-5. General electrical specifications**

Parameter	Condition	Min.	Typical	Max.	Unit
<b>Operation ground current</b>					
Standby (one buck on)	Low power mode Chip_EN = High Buck_EN = High		304.5	358	μA
Standby (all bucks off)	Low power mode Chip_EN = High Buck_EN = Low		13	17.5	μA
Off mode	Chip_EN = Low			1	μA
<b>Under voltage (UV)</b>					
Under voltage falling threshold			2.4		V
Under voltage rising threshold			2.65		V
<b>Over voltage lockout (OVLO)</b>					
Over voltage rising threshold		5.7	5.8	5.9	V
<b>EN</b>					
High voltage		1.41			V
Low voltage				0.9	V
<b>Control input voltage (SCLK, SDAT, SRCLKEN related)</b>					
Control input high		0.75*DVDD			V
Control input low				0.25*VIO	V
<b>Thermal shutdown</b>					
PMIC shutdown threshold			150		degree

## 3 MT6319 Packaging

### 3.1 Package Dimensions

Package: WLCSP 45L

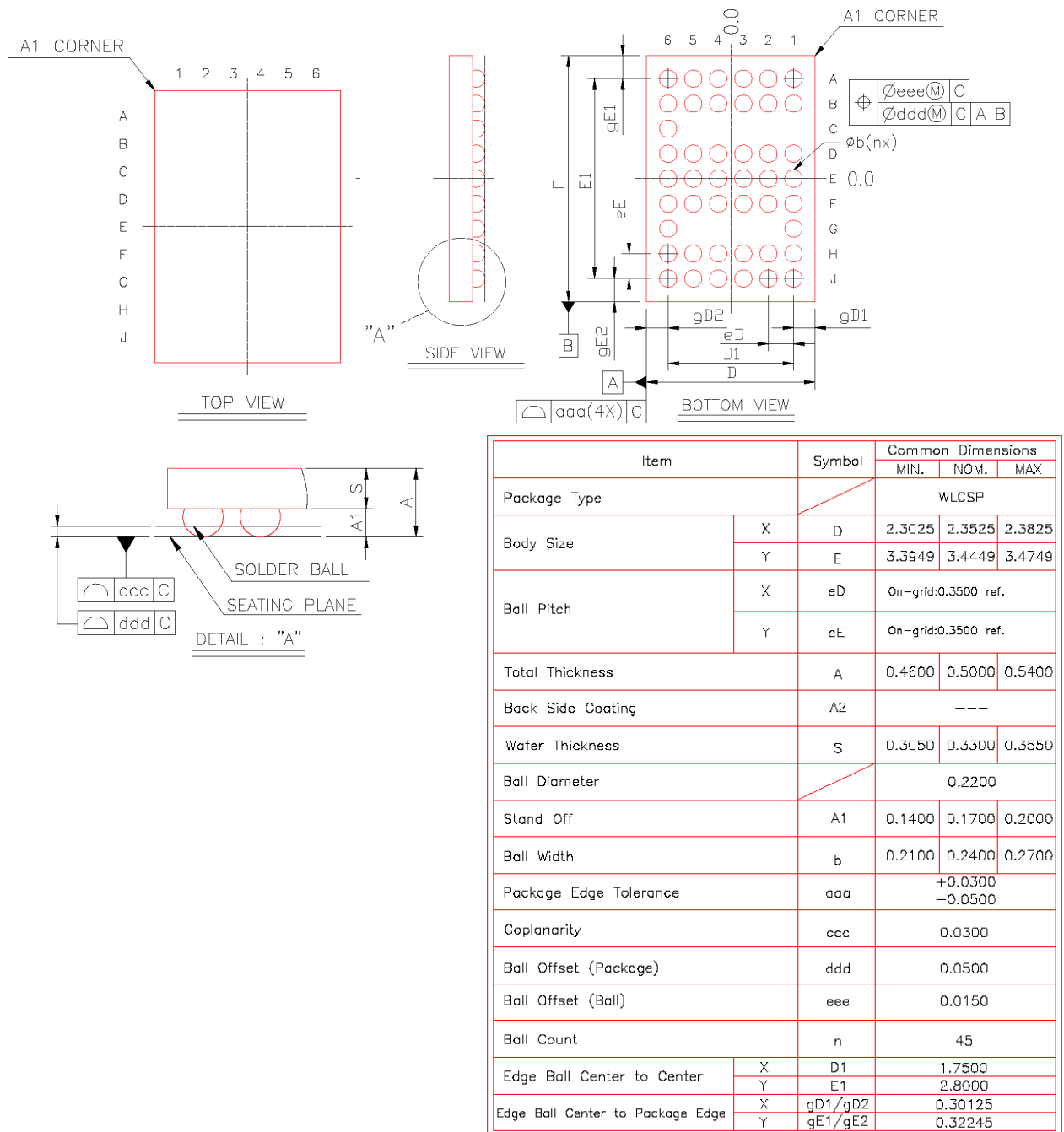


Figure 3-1. Package dimensions

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