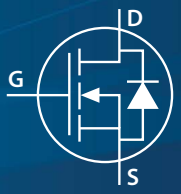
EPC2090 – Enhancement Mode Power Transistor

V_{DS}, 100 V

$R_{DS(on)}$, 5.2 mΩ max

I_D, 125 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised December 19, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

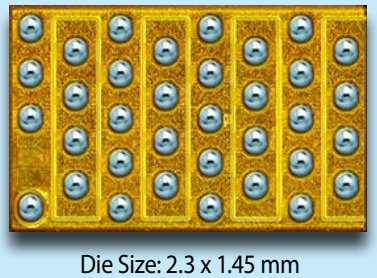
Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous ($T_J \le 125°C$)	46	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	125	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	1.07	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	2.9	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.045 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.004	0.045	mA
	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V, T_J = 90°C		0.02	0.17	
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	1.5	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.3	4	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	4	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4.2 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 16 A		3.8	5.2	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.



Die Size: 2.3 x 1.45 mm

EPC2090 eGaN® FETs are supplied in passivated die form with copper pillars.

Applications

- Copper Pillars for Package Integration
- DC-DC Converters
- Isolated DC-DC Converters
- Lidar
- Sync Rectification for AC-DC and DC-DC
- Point-of-Load Converters
- USB-C
- Class-D Audio
- LED Lighting
- eMobility

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		1046	1328	pF
C_{RSS}	Reverse Transfer Capacitance			2.9		
C_{OSS}	Output Capacitance			364	478	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		441		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			548		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 16 A		7.3	9.3	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 16 A		2.8		
Q_{GD}	Gate-to-Drain Charge			0.7		
$Q_{G(TH)}$	Gate Charge at Threshold			2.1		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		27	35	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

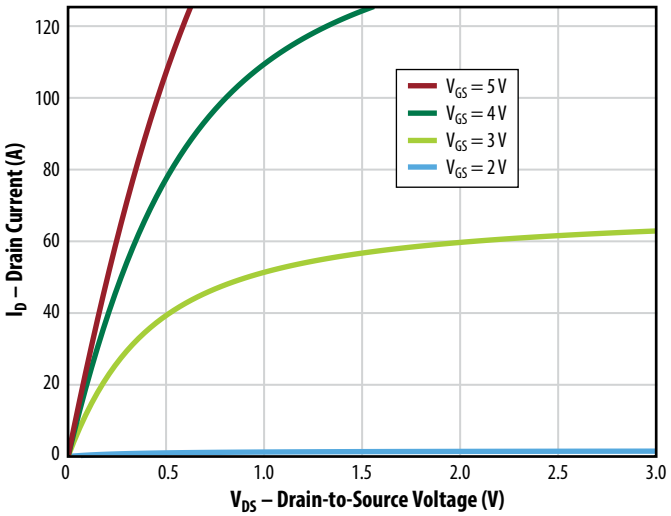


Figure 2: Typical Transfer Characteristics

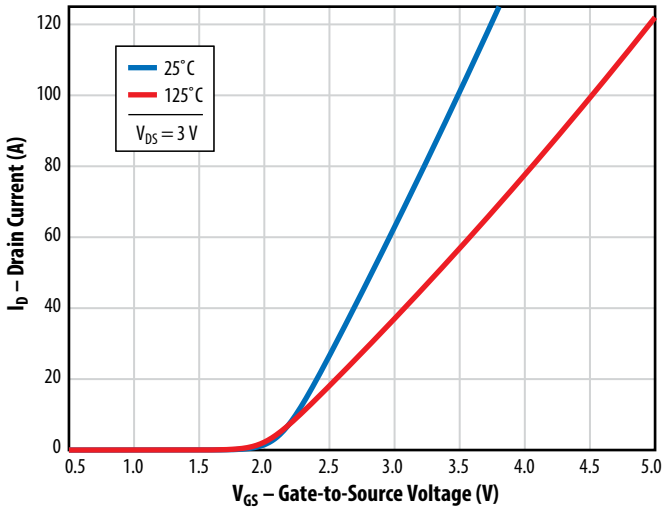


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

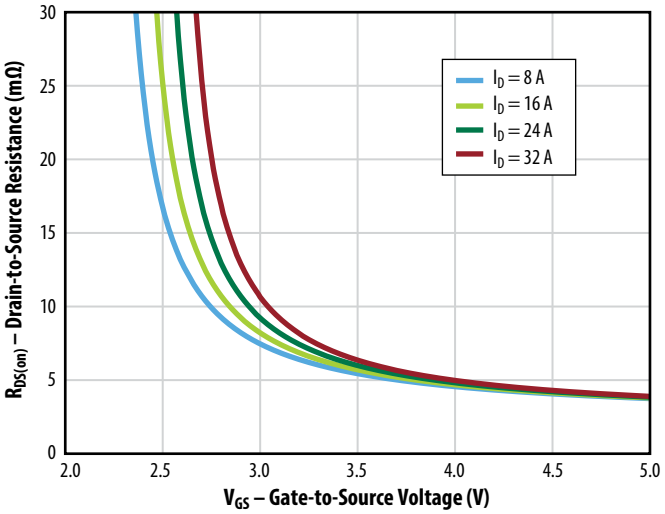


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

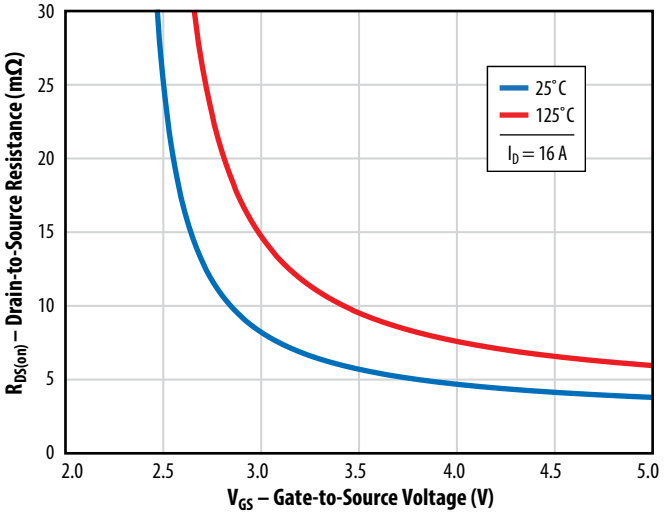


Figure 5a: Typical Capacitance (Linear Scale)

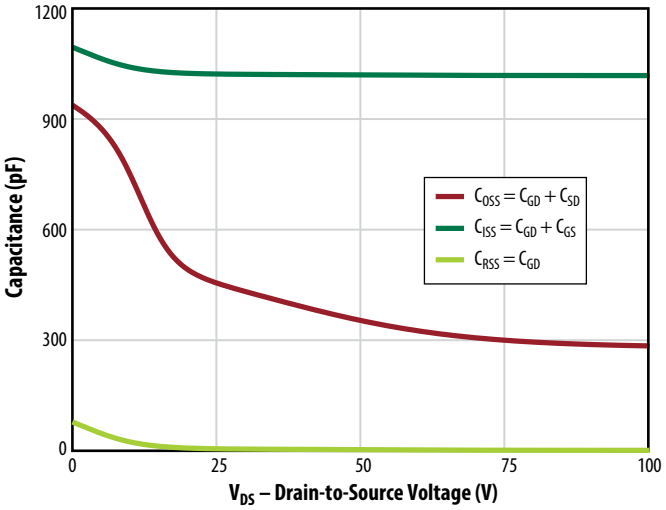


Figure 5b: Typical Capacitance (Log Scale)

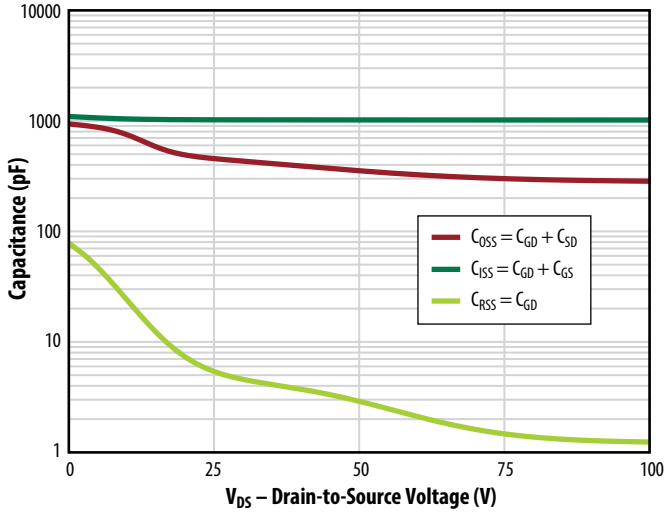


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

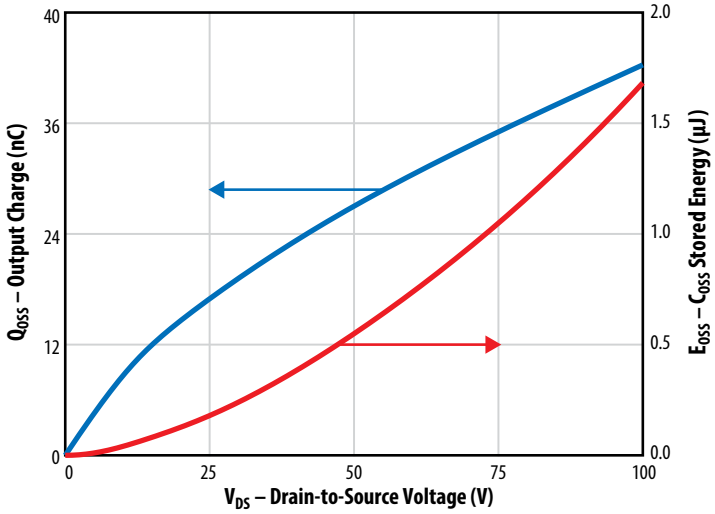


Figure 7: Typical Gate Charge

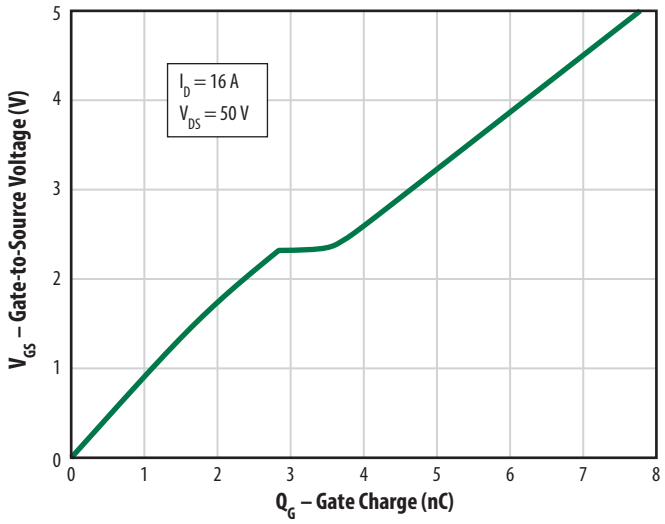


Figure 8: Reverse Drain-Source Characteristics

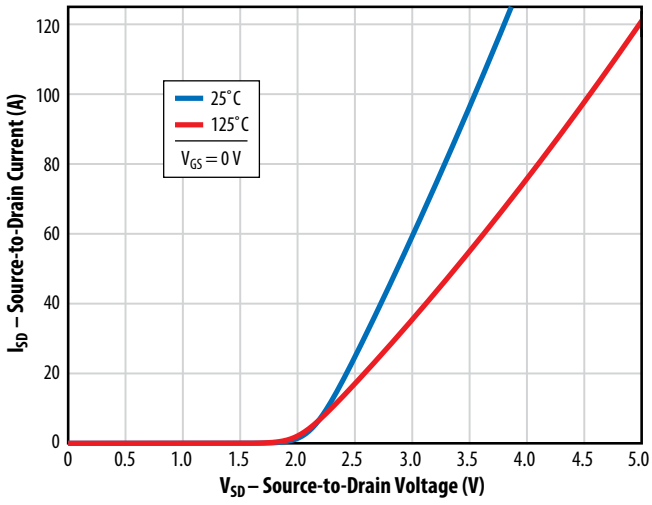
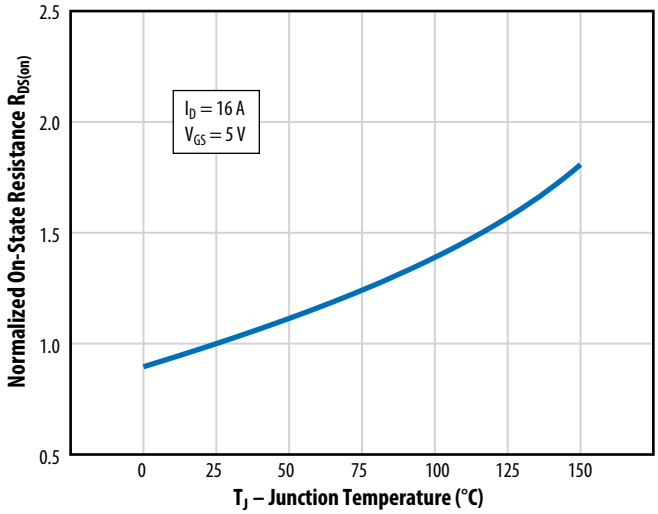


Figure 9: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Normalized Threshold Voltage vs. Temperature

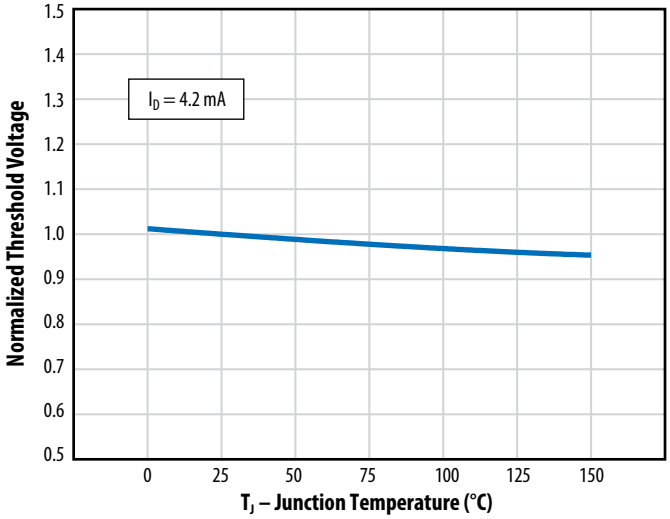
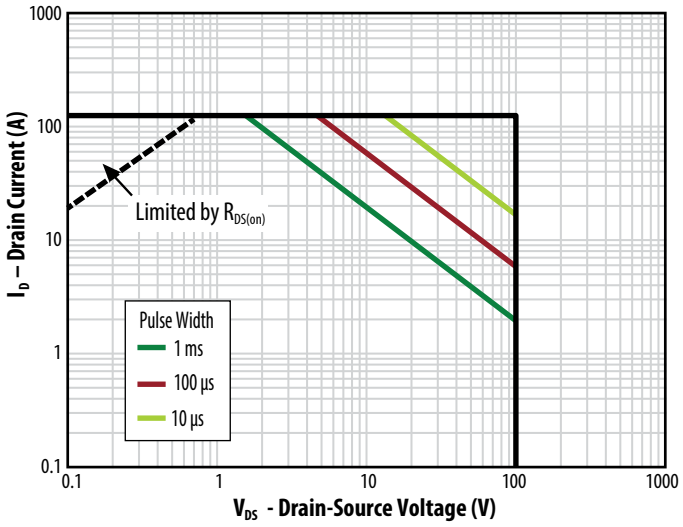
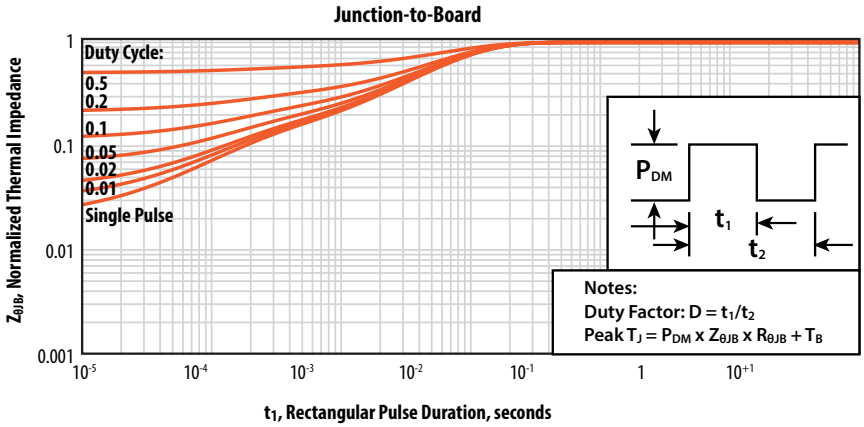


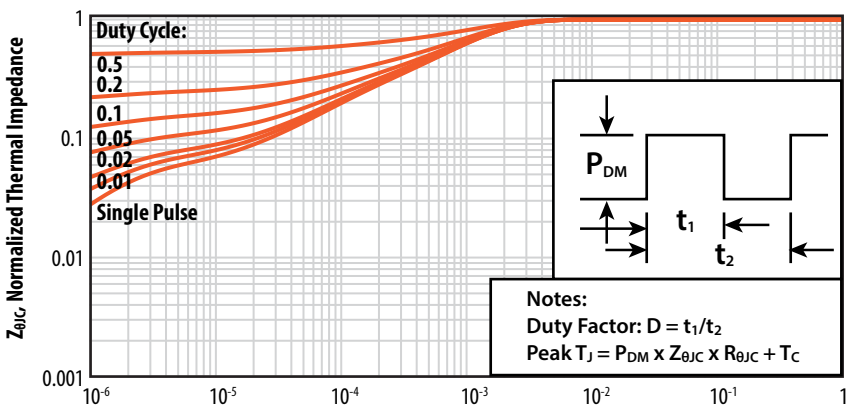
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

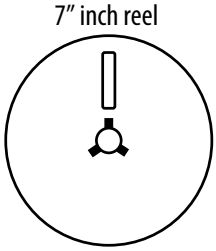
Figure 12: Transient Thermal Response Curves

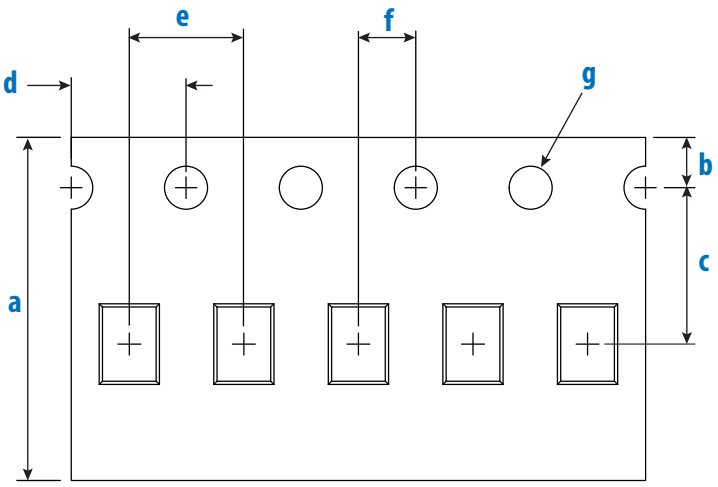


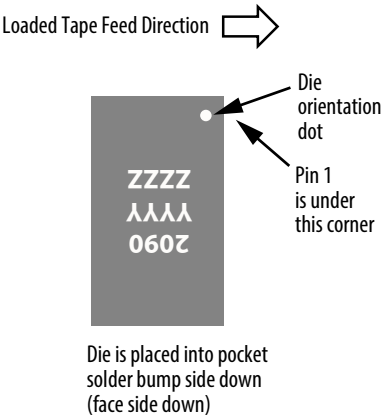


TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7″ reel





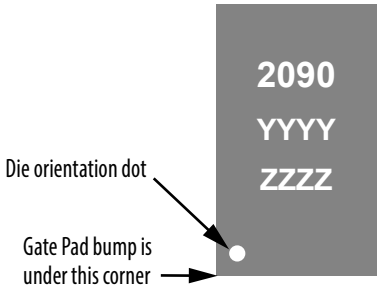


	Dimension (mm)		
EPC2204A (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

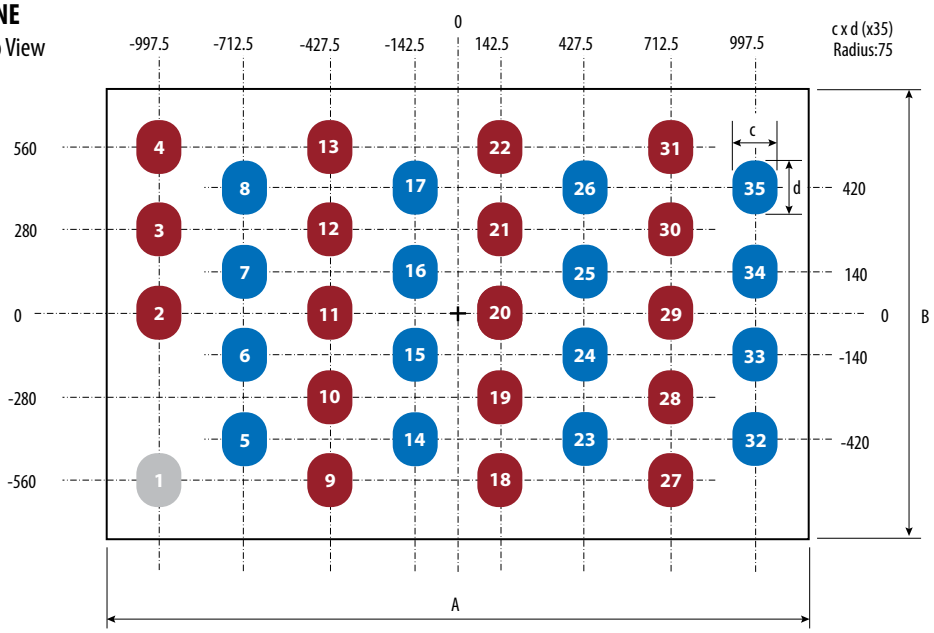
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2090	2090	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



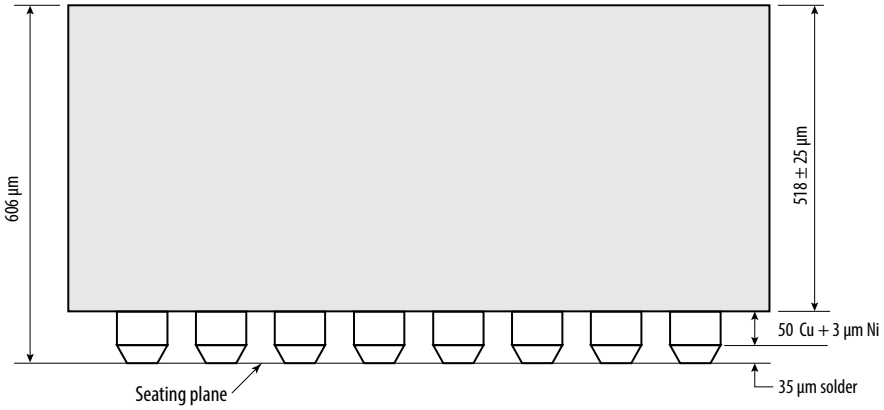
DIM	Micrometers		
	MIN	Nominal	MAX
A	2270	2300	2330
B	1420	1450	1480
c		150	
d		180	

Pad 1 is Gate;

Pads 2-4 ,9-13, 18-22, 27-31 are Source;

Pads 5-8, 14-17, 23-26, 32-35 are Drain

Side View



Note: solder cap height is post reflow

Additional resources available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)

Note: Cu pillar dies are not intended for mounting on a PCB, they are intended for use in a package. Terms of die usage: The die represented by this data sheet are intended for initial evaluation for integration to buyer defined package. EPC does not guarantee reliability in the buyer specific package. To ensure reliability, the die may need redesign to be optimized to buyers specific package. NRE may apply