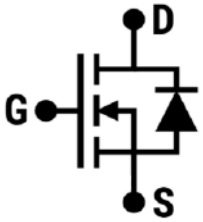
N3T080MP330
3300 V 80 mΩ Silicon Carbide MOSFET

V_{DS}	I_D	$R_{DS(on)}$	Package
3300 V	34 A	80 mΩ	Bare Die

Features
- State-of-the-art SiC MOSFET technology
- Reliable gate oxide process
- Ultra-low output capacitance
- Best-in-class figure-of-merits, [R_{on}*C_{oss}] and [R_{on}*C_{rss}]
- Stable switching characteristics up to 175 °C



Benefits
- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Enhanced system reliability
- Reduced total harmonic distortion

Applications
- Motor drives
- Solar PV inverters
- EV onboard chargers
- Server power supplies
- Energy storage systems
- EV fast charging stations
- Solid-state power controllers
- Uninterruptible power supplies

Maximum Ratings

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Voltage	$V_{(BR)DSS}$	T_C = 25 °C	3300	-	-	V	
Gate-Source Voltage	$V_{GS(max)}$		-10	-	25	V	
	$V_{GS,op}$	Recommended Operation	-	-5/+20	-		
Continuous Drain Current	I_D	V_{GS} = 20 V, T_C = 25 °C	-	-	34	A	Fig. 13
		V_{GS} = 20 V, T_C = 100 °C	-	-	24		
Pulsed Drain Current	$I_{D(pulse)}$	T_C = 25 °C	-	-	80	A	Fig. 12
Power Dissipation	P_{tot}	T_C = 25 °C	-	-	288	W	Fig. 14
Operating and Storage Temperature	T_J , T_{stg}		-55	-	175	°C	

Note: Based on TO-247-4L packaged die measurements

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Thermal and Bare Die Characteristics

Parameter	Symbol	Comment	Min.	Typ.	Max.	Unit	Note
Thermal Resistance, Junction to Case	R_{thJC}	Based on TO-247-4L packaged die measurements	-	0.32	0.52	°C/W	Fig. 11
Thermal Resistance, Junction to Ambient	R_{thJA}	Based on TO-247-4L packaged die measurements	-	-	40	°C/W	
Bare Die Thickness	w_{die}		335	360	385	µm	
Top Metal Thickness	w_{top}	Al/Cu metallization	-	5.0	-	µm	
Bottom Metal Thickness	w_{bottom}	Ag metallization	-	1.0	-	µm	

Electrical Characteristics (T_c = 25 °C unless otherwise specified)

STATIC CHARACTERISTICS

Note: Based on TO-247-4L packaged die measurements

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	3300	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 3300 V, V_{GS} = 0 V	-	1	100	µA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 10 mA	1.8	2.5	3	V	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = -10 / +25 V, V_{DS} = 0 V	-	-	±100	nA	
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 20 A	-	9.8	-	S	Fig. 8
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 20 A	-	79	90	mΩ	Fig. 1
		V_{GS} = 20 V, I_D = 20 A, T_C = 175 °C	-	252	-	mΩ	Fig. 3
		V_{GS} = 18 V, I_D = 20 A	-	81	-	mΩ	Fig. 1
		V_{GS} = 18 V, I_D = 20 A, T_C = 175 °C	-	253	-	mΩ	Fig. 3

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DYNAMIC CHARACTERISTICS

Note: Based on TO-247-4L packaged die measurements

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 1700 V, V_{AC} = 25 mV, f = 100 kHz	-	3830	-	pF	Fig. 10
Output Capacitance	C_{oss}		-	53.5	-		
Reverse Capacitance	C_{rss}		-	3.35	-		
Gate-Source Charge	Q_{GS}	V_{DS} = 1700 V, V_{GS} = -5 / +20 V, I_D = 20 A	-	30	-	nC	Fig. 15
Gate-Drain Charge	Q_{GD}		-	28	-		
Total Gate Charge	Q_G		-	168	-		
Internal Gate Resistance	$R_{G(int)}$	V_{AC} = 25 mV, f = 1 MHz	-	1.1	-	Ω	
Turn-On Switching Energy	E_{ON}	V_{DD} = 1700 V, I_D = 20 A, V_{GS} = -5 / +20 V, $R_{G(ext)}$ = 10 Ω, L = 500 µH	-	1283	-	µJ	Fig. 16
Turn-Off Switching Energy	E_{OFF}		-	217	-		Fig. 17
Total Switching Energy	E_{TOT}		-	1500	-		Fig. 18
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1700 V, I_D = 20 A, V_{GS} = -5 / +20 V, $R_{G(ext)}$ = 10 Ω, L = 500 µH Timing relative to V_{DS} Inductive Load	-	43	-	ns	Fig. 19
Rise Time	t_r		-	29	-		
Turn-Off Delay Time	$t_{d(off)}$		-	74	-		
Fall Time	t_f		-	22	-		

BODY DIODE CHARACTERISTICS

Note: Based on TO-247-4L packaged die measurements

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 20 A	-	4.8	-	V	Fig. 20
		V_{GS} = -5 V, I_{SD} = 20 A, T_J = 175 °C	-	4.1	-	V	Fig. 21
Continuous Diode Forward Current	I_S	V_{GS} = -5 V	-	44	-	A	
Reverse Recovery Time	t_{rr}	V_R= 1700 V, I_{SD} = 20 A, V_{GS} = -5 V, di_F/dt = 1000 A/µs	-	9	-	ns	
Reverse Recovery Charge	Q_{rr}		-	226	-	nC	
Peak Reverse Recovery Current	I_{RRM}		-	25	-	A	

Typical Performance

Note: Based on TO-247-4L packaged die measurements

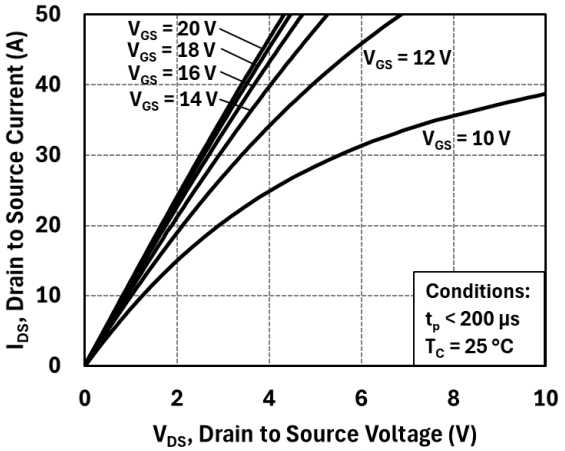


Figure 1: Output Characteristics at 25 °C

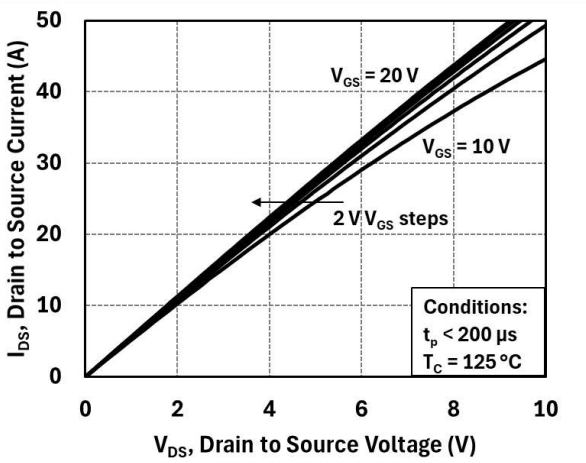


Figure 2: Output Characteristics at 125 °C

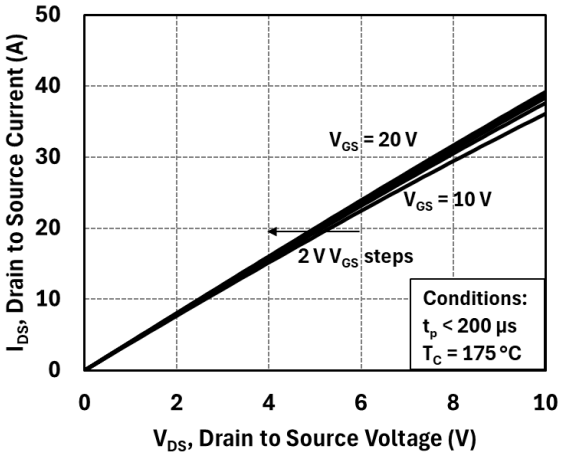


Figure 3: Output Characteristics at 175 °C

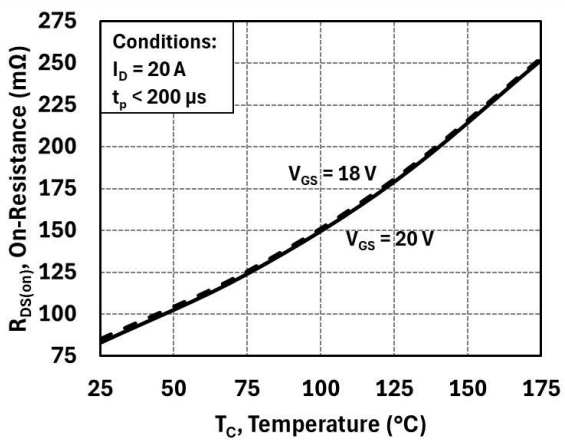


Figure 4: On-Resistance vs. Temperature

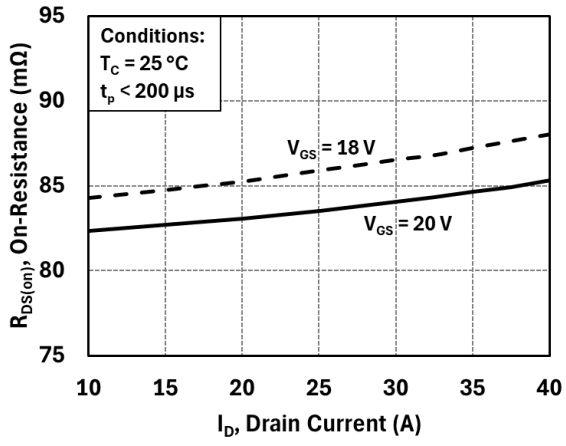


Figure 5: On-Resistance vs. Drain Current

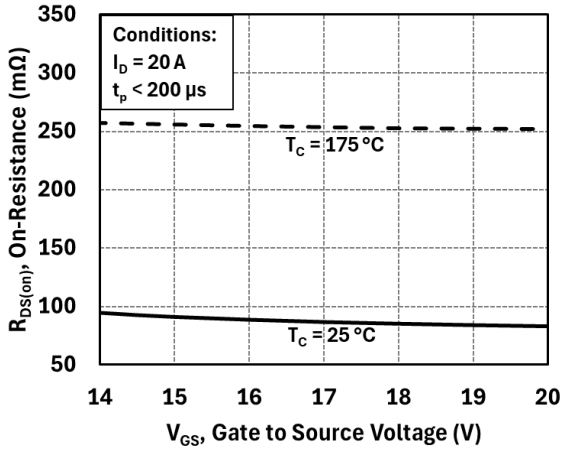


Figure 6: On-Resistance vs. Gate Voltage

Typical Performance

Note: Based on TO-247-4L packaged die measurements

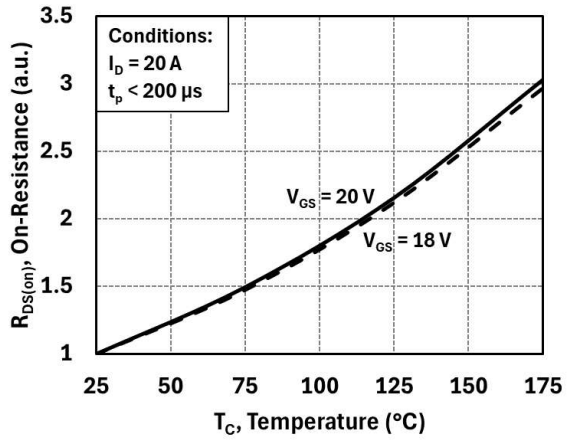


Figure 7: Normalized On-Resistance vs. Temperature

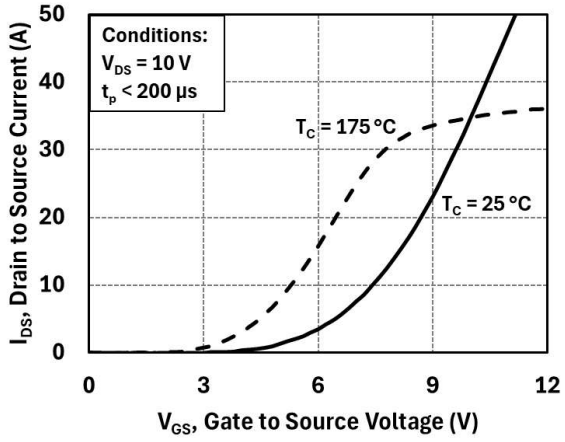


Figure 8: Transfer Characteristics

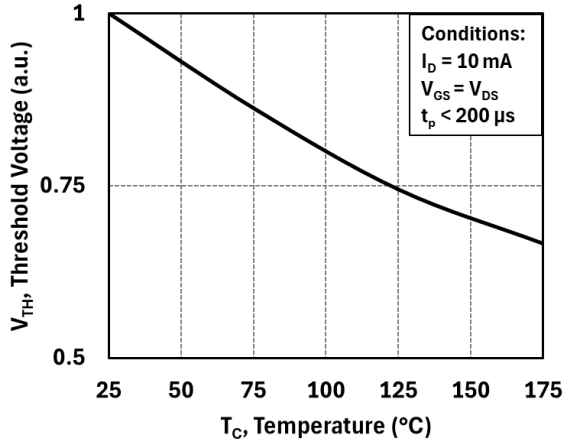


Figure 9: Threshold Voltage vs. Temperature

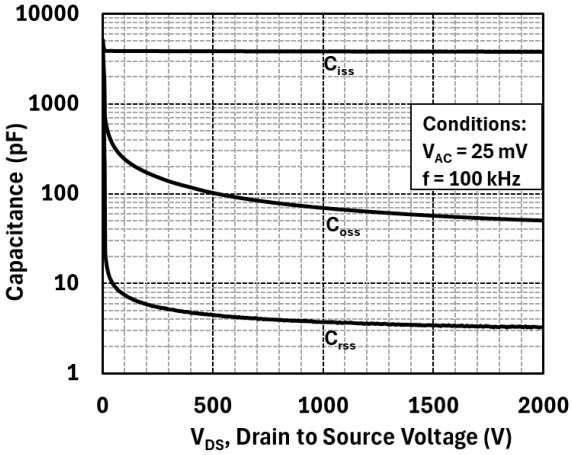


Figure 10: Capacitances vs. Drain-Source Voltage (0-1000 V)

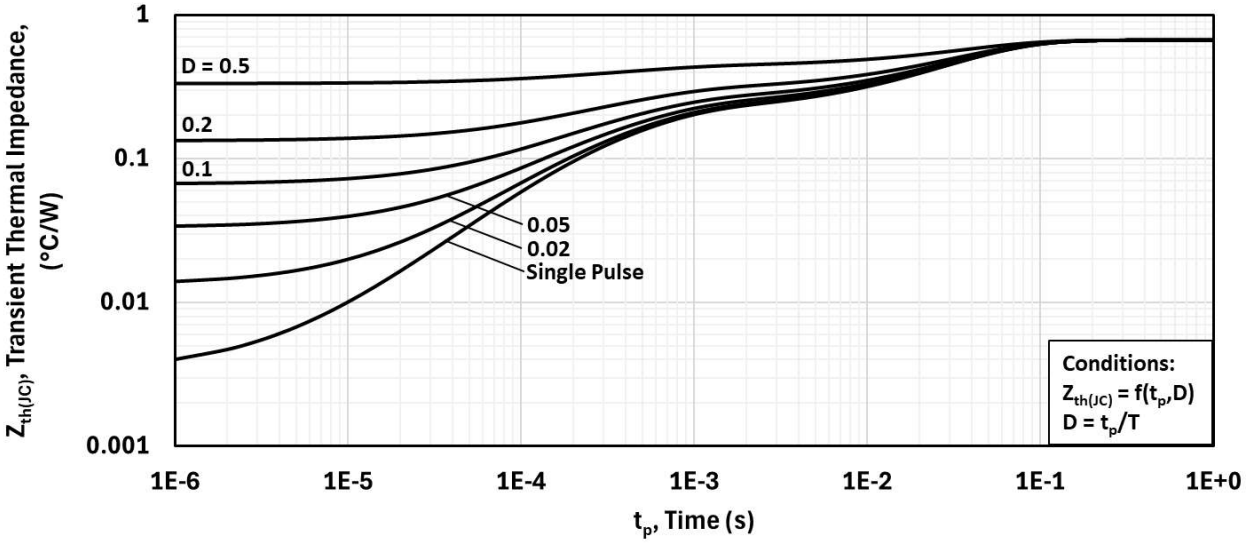


Figure 11: Transient Thermal Impedance

Typical Performance

Note: Based on TO-247-4L packaged die measurements

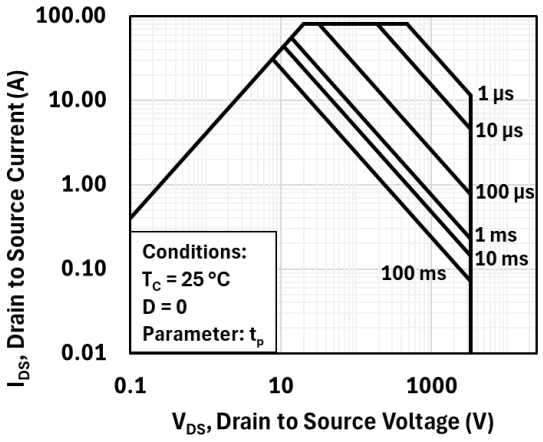


Figure 12: Safe Operating Area

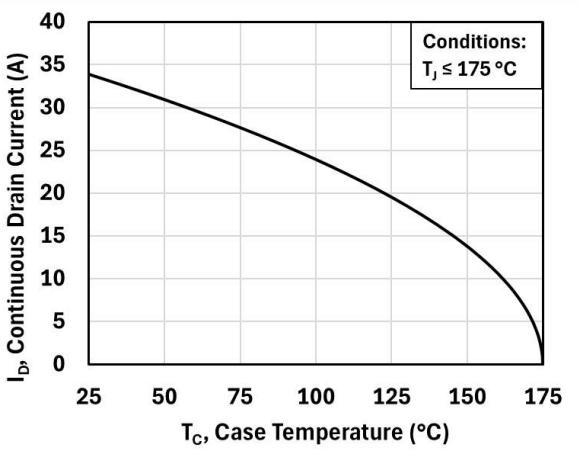


Figure 13: Current De-rating Curve

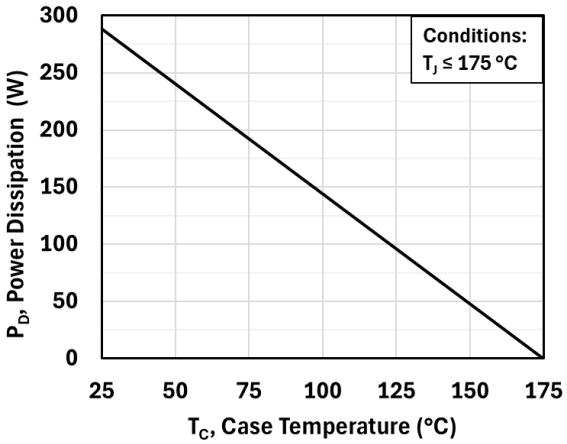


Figure 14: Power De-rating Curve

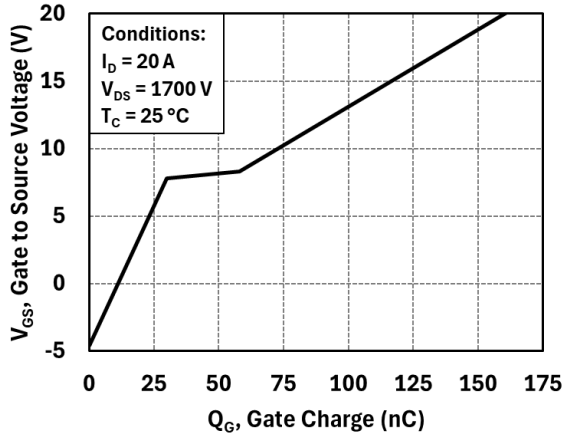


Figure 15: Gate Charge Characteristics

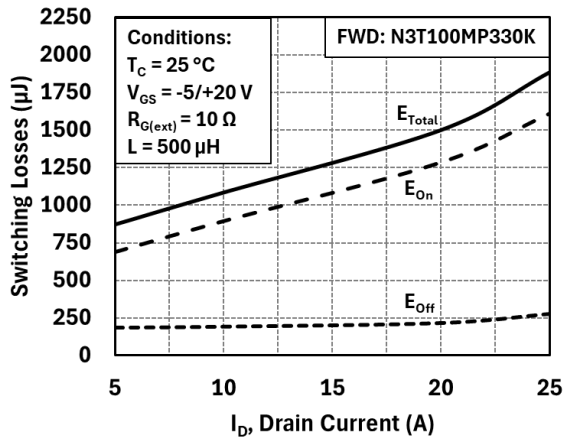


Figure 16: Inductive Switching Energy vs. Drain Current (V_{DD} = 1700 V)

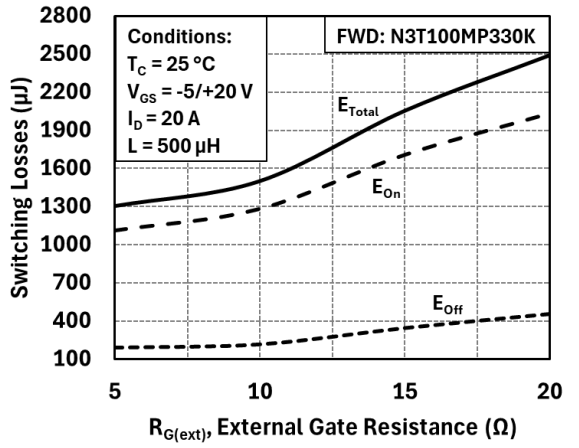


Figure 17: Inductive Switching Energy vs. $R_{G(ext)}$ (V_{DD} = 1700 V)

Typical Performance

Note: Based on TO-247-4L packaged die measurements

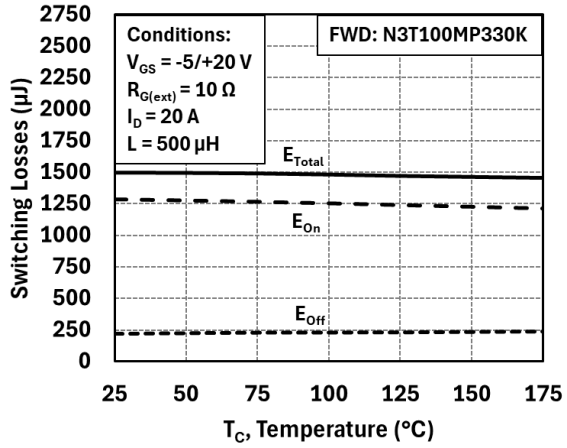


Figure 18: Inductive Switching Energy vs. Temperature (V_{DD} = 1700 V)

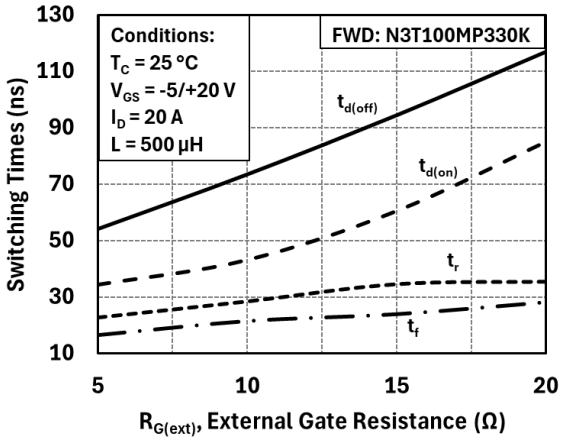


Figure 19: Switching Times vs. $R_{G(ext)}$ (V_{DD} = 1700 V)

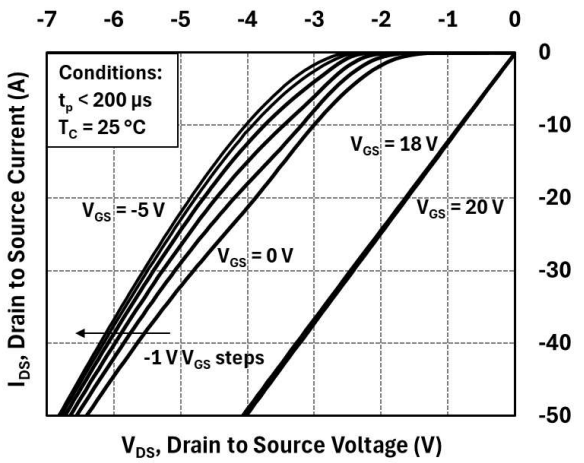


Figure 20: Body Diode Characteristics at 25 °C

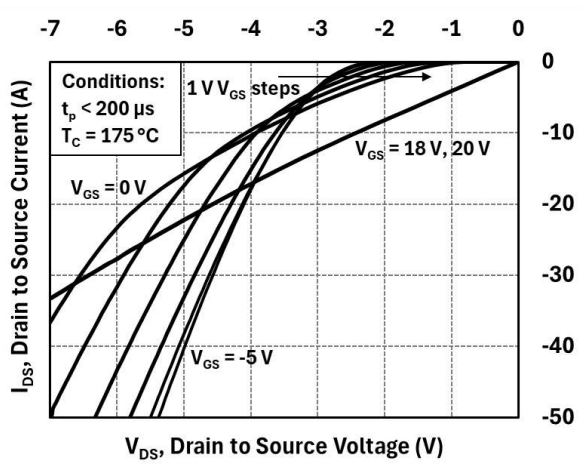


Figure 21: Body Diode Characteristics at 175 °C

Dynamic Testing Circuit Schematics

Note: Based on TO-247-4L packaged die measurements

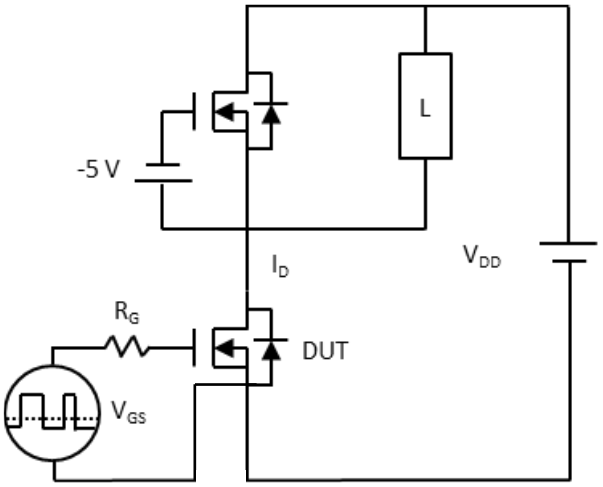


Figure 22: Inductive Load Switching Test Circuit

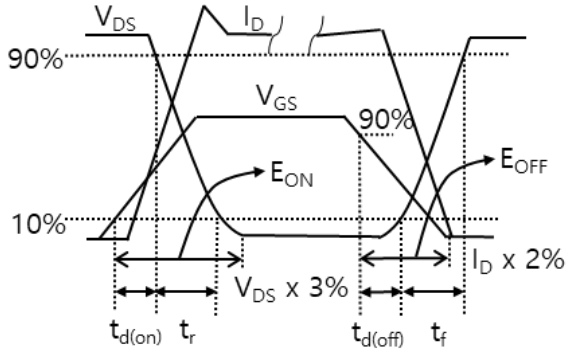


Figure 23: Inductive Load Switching Test Waveforms

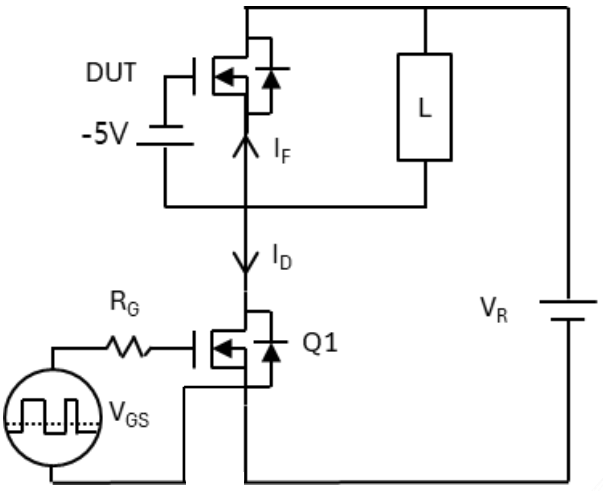


Figure 24: Reverse Recovery Test Circuit

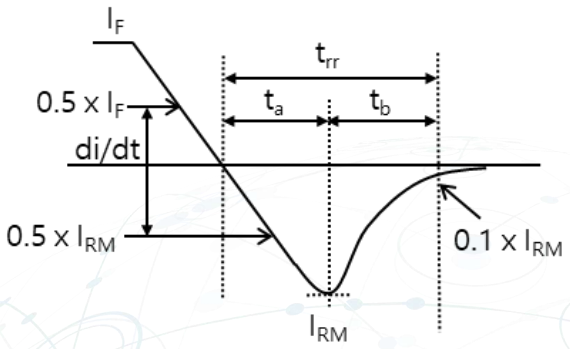


Figure 25: Body Diode Reverse Recovery Test Waveforms

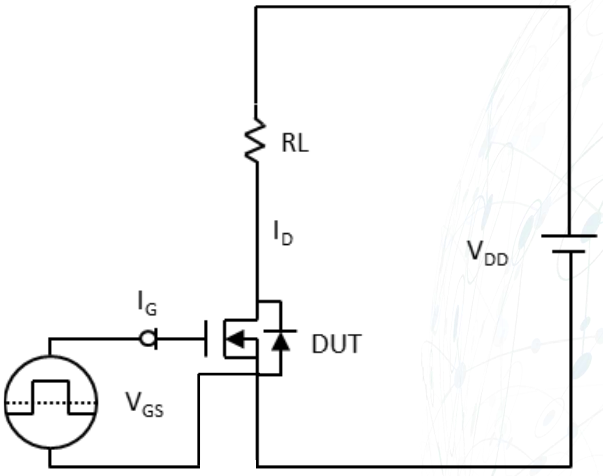


Figure 26: Gate Charge Test Circuit

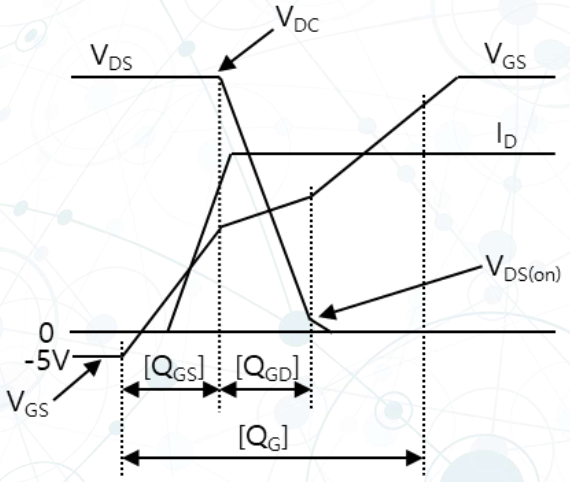
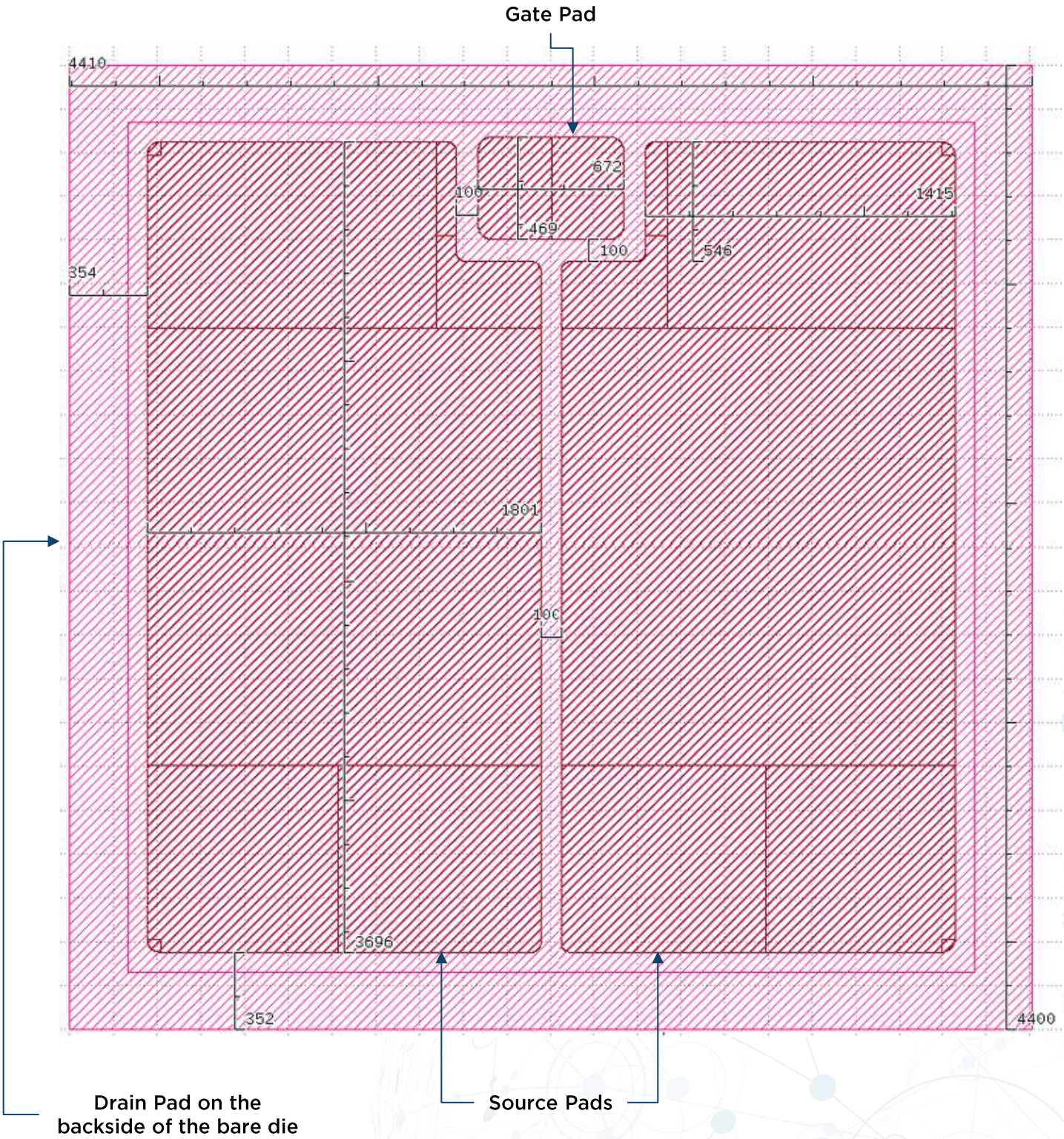


Figure 27: Gate Charge Test Waveforms

Bare Die Dimensions

Dimensions in µm



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