MM5140

DC to 8 GHz RF SP4T with Integrated Driver

POWERED BY ideal switch®

RoHS COMPLIANT

Product Overview

Description

The MM5140 is a high-power SP4T switch built on Menlo Micro's Ideal Switch® technology. This innovative technology enables highly reliable switches capable of greater than 25 W forward power. The MM5140 provides ultra-low insertion loss and superior linearity as an SP4T from DC to 8 GHz, with greater than 3 billion switching cycles. The MM5140 is an ideal solution for replacing large RF electromechanical relays, as well as RF/microwave solid-state switches in applications where linearity and insertion loss are critical parameters. The MM5140 features an integrated driver circuit with Serial Peripheral Interface (SPI) and General Purpose Input/Output (GPIO) interface control options and an integrated charge pump to drive the gate.

Features

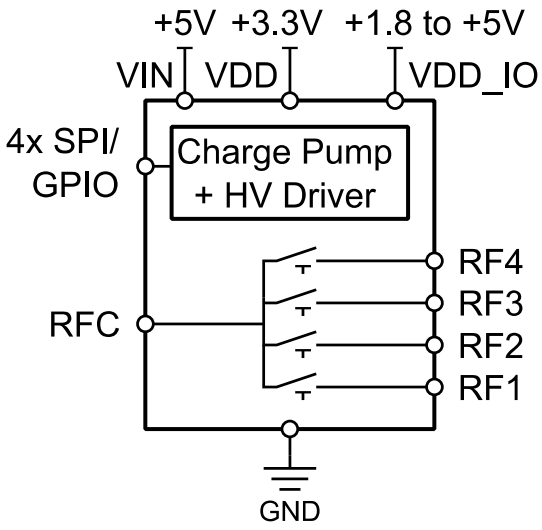
- DC to 8 GHz Frequency Range
- Integrated High-Voltage Driver
- 25 W (CW), 150 W (Pulsed) Max Power Handling
- Low On-State Insertion Loss: 0.5 dB @ 8.0 GHz
- High Linearity, 90 dBm IIP3
- > 25 dB Isolation @ 6.0 GHz
- Low Power Consumption <15 mW
- High Reliability > 3 billion Switching Operations
- 5.2 mm x 4.2 mm LGA Package

Applications

- Switched Filter Banks and Tunable Filters
- High Power RF Front-Ends
- Low-Loss Switch Matrices
- RF EM Relay Replacement
- Antenna Tuning
- Antenna Beam Steering
- Digital Step Attenuators

Markets

- Defense and Aerospace
- Test and Measurement
- Wireless Infrastructure



Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM5140 should be restricted to the limits indicated in the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM5140 is a Class 0 ESD device. When handling the MM5140, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1.

Power Sequencing

No specific power sequencing is required when using the internal charge pump.

When using an external high-voltage supply, see below.

Power-up Sequence

1. Connect Ground.
2. Apply VDD and VDD_IO – no sequencing restrictions between VDD and VDD_IO.
3. Apply VPP.
4. Apply input control signals.

Power-down Sequence

Reverse the power-up sequence.

Table 1. Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Unit
Open State Voltage Rating / Switch RF1-4 to RFC[2]	-150	150	V
Open State Voltage RF1-4, RFC to GND[2] [3]	-150	150	V
Hot Switching Voltage[4]	-0.5	0.5	V
Charge Pump Input (V_{IN})	-0.3	5.5	V
DC Supply Voltage (V_{DD})	-0.3	3.6	V
I/O Supply Voltage (V_{DD_IO})	-0.3	5.5	V
High Voltage Power Supply (V_{PP})	-0.3	105	V
Logic Input Levels	-0.5	V_{DD_IO}+0.3	V
DC Current Rating/Switch[5]	—	500	mA
CW Input Power @ 3 GHz[6]	—	25	W
Peak RF Power[7]	—	150	W
Storage Temperature Range[8]	-65	150	ºC
ESD Rating HBM RF1-4, RFC Pins	—	150	V
ESD Rating HBM Control and Power Pins[9]	—	2000	V
ESD Rating HBM VPP Pin	—	500	V
Mechanical Shock[10]	—	500	G
Vibration[11]	—	500	Hz

Notes:

1. All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition).
2. This also applies to ESD events. This is a Class 0 device.
3. RF pins must not be allowed to electrically float during switch operation. See section Floating Node Restrictions for details on avoiding floating nodes.
4. See section Hot Switch Restrictions for more information.
5. Total current of all channels combined.
6. For +85 ºC ambient test condition.
7. For a 10% duty cycle, 10 µs pulse width, +25 ºC ambient test condition.
8. See section Storage and Shelf Life for more information on shelf and floor life.
9. Control and power pins include: VIN, VDD, VDD_IO, FLT_MODE, FLTB, FLIP_BIT, CP_EN, MODE, and CTL1-4.
10. See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis. Data taken from MEMS die (MM5130) test results.
11. See JESD22-B103 for vibration test methodology at 3.1 G and 30min/cycle, 1 cycle/axis, 3 axis. Data taken from MEMS die (MM5130) test results.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Charge Pump Power Supply	V_{IN}	4.5	5.0	5.5	V
Low Voltage Digital Supply	V_{DD}	3.0	3.3	3.6	V
Logic Reference Level	V_{DD_IO}	1.71	—	5.25	V
High Voltage Power Supply	V_{PP}	87	89	91	V
CW RF Power[2]					
1 GHz		—	—	35	W
3 GHz		—	—	25	W
8 GHz		—	—	14	W
Ambient Temperature Range	T_A	-40	—	85	ºC
SPI Clock Frequency	f_{SCK}	—	—	33	MHz
Switch Cycle Frequency[3]		—	—	10	kHz

Notes:

1. When using an external high voltage supply.
2. For +85 ºC ambient test condition. See Thermal and Power Handling Considerations for more information.
3. Test condition is defined as full enable-disable cycles of one channel.

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted. Operating with all GND, AGND, DGND, and CPGND pins connected to system ground (0 V) and with input frequencies of greater than 10 MHz in a 50 Ω impedance system.

Table 3. RF Performance Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Operating Frequency Range		DC	—	8	GHz	
Insertion Loss		—	0.5	—	dB	
Input / Output Return Loss		—	14	—	dB	
Isolation (RF1-4 to RFC)		—	24	—	dB	
Third-Order Intercept Point	IP3	—	90	—	dBm	Measured at +25ºC.
Second Harmonic	H2	—	-125	—	dBc	Measured at 2.0 GHz fundamental frequency and 35 dBm input power. Measured at +25ºC.
Third Harmonic	H3	—	-145	—	dBc	Measured at 2.0 GHz fundamental frequency and 35 dBm input power. Measured at +25ºC.
Charge Pump Clock Feed Thru[1]		—	-132	—	dBm	Measured with 300 Hz resolution BW, 3 Hz video BW, 0dB internal attenuation, internal amplifier ON, single sweep. Measured at +25ºC.

Notes:

1. For applications that require low noise figure performance below 2 GHz, MM5230 with external MM101 driver is recommended.

Table 4. AC and DC Electrical Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Switching Time						RF switching time measured using a 100 MHz -10dBm signal, from 50% rising edge of last SPI CLK to settling to within 0.05 dB of final value.
Turn on	T_{ON}	—	14	—	µs	
Turn off	T_{OFF}	—	5	—	µs	
On/Off Operations (MM5140-01NDB)						Data taken from MEMS die (MM5130) reliability test results. Cold switched operations, measured at 10 kHz cycling rate, specified at ambient temperature.
@25 ºC		$3x10^9$	$30x10^9$	—	Cycle	
@85 ºC		—	$0.1x10^9$	—	Cycle	
Off-State RFx to RFC Leakage Current		—	40	150	nA	Measured with 75 V RFx to 0 V RFC.
On-State Resistance	R_{ON}	—	1.0	3	Ω	Measured with 0.5 A.
Off-State Capacitance (C_{IO})	C_{OFF}	—	2.5	—	fF	Measured at 1 MHz, 1 V_{RMS}.
Video Feedthrough		—	16	—	mV_{p-p}	Performed with 50 Ω terminations on all RF channels.

Table 5. Charge Pump and Driver Electrical Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
VIN Current (Dynamic)	I_{VIND}	—	1.5	2.5	mA	SPI mode, Charge pump on, all channels switching at 10 kHz.
VIN Quiescent Current	I_{VINQ}	—	1.25	2.0	mA	Charge pump on, all I/O and channels static.
VDD UVLO Rising Threshold	$UVLO_{RISE}$	2.77	—	2.95	V	
VDD UVLO Falling Threshold	$UVLO_{FALL}$	2.72	—	2.90	V	
Low Voltage Digital Current	I_{DD}	—	520	700	µA	SPI mode, all channels switching at 10 kHz.
Low Voltage Digital Quiescent Current	I_{DDQ}	—	470	550	µA	Charge pump On, All I/O & channels static.
Low Voltage Digital Sleep Mode Current	I_{DD_SLEEP}	—	<1	10	µA	Charge pump Off, SPI and inputs in static state.
I/O Logic Quiescent Current	$I_{DD\_IO\_Q}$	—	<10	50	µA	
Fault Indicator Open-Drain Output	FLTB	0	—	V_{DD_IO}	V	
Logic I/O Level High)	I/O_{VH}	0.7* V_{DD_IO}	—	V_{DD_IO}	V	
Logic I/O Level Low	I/O_{VL}	0	—	0.3* V_{DD_IO}	V	
MISO Load Capacitance	C_{MISO}	—	—	10	pF	Specification is for design guidance only. MISO load capacitance is SDI input capacitance pin and PCB trace capacitance from MISO to SDI.
MISO Max Source Current[1] @ V_{DD_IO}:	I_{MISOH}					Measured at V_{OUT} = 0.8 x V_{DD_IO}.
5.0 V		180	290	—	mA	
3.3 V		75	140	—	mA	
1.8 V		20	35	—	mA	

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
MISO Max Sink Current[1] @ V_{DD_IO}:	I_{MISOL}					Measured at V_{OUT} = 0.2 x VDD_IO.
5.0 V		140	260	—	mA	
3.3 V		65	140	—	mA	
1.8 V		20	40	—	mA	
SSB Pull-Up Resistor to V_{DD_IO}	R_{PU}	120	200	280	kΩ	SSB pull-up is only in SPI mode
I/O Pull-Down Resistors[2]	R_{PD}	120	200	280	kΩ	SSB pull-down is only in GPIO mode
VPP UVLO Rising Threshold	VPP_{EN}	75	79	81	V	
VPP UVLO Falling Threshold	VPP_{DIS}	74	78	80	V	
CP_EN pin toggle low time	T_{TOGGLE}	500	—	—	ns	Minimum time CP_EN must be held low to restart the IC from fault condition.
FLTB pin max sink current		65	140	—	mA	FLTB active low, measured with V_{DD_IO} = 3.3V.
Logic I/O Hysteresis (SCK only)	I/O_{HYS}	—	0.25	—	V	
Power-On-Reset	POR	—	1.25	2.5	ms	Time for logic input signals to be considered valid after application of V_{IN} and V_{DD}.
Start-Up Time	T_{ST}	—	20	33	ms	CP_EN=1 (CPEN bit=1) to V_{PP} rises to 90% of set value.

Notes:

1. MISO source current is pulled from VDD_IO. Max VDD_IO current draw is equal to $I_{DD\_IO\_Q}$ + VDD_IO / R_{SDI}, where R_{SDI} is the output impedance connected to MISO. In the case of daisy-chained MM5140 this is 46 µA.
2. The following I/O pins have internal pull-down resistors: SCK/CTL1, MOSI/CTL2, MISO/CTL3, SSB/CTL4 (GPIO mode only), CP_EN, FLIP_BIT, FLT_MODE. The MODE pin does not have an internal pull-up or pull-down resistor.

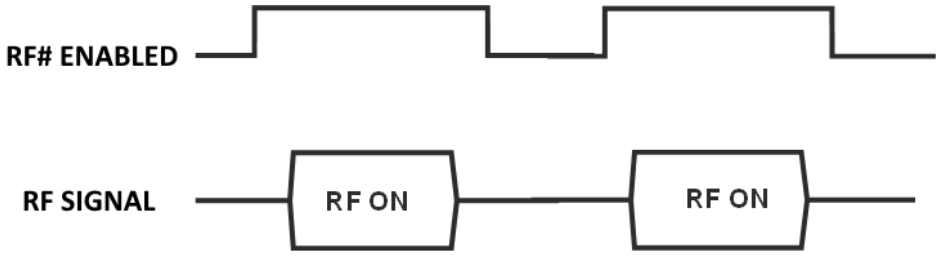
Table 6. Driver Interface AC Electrical Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
MOSI Valid to SCK Setup Time	t_{SU}	2	—	—	ns
MOSI Valid to SCK Hold Time	t_{HD}	5	—	—	ns
SCK High Time	t_{HI}	15.5	—	—	ns
SCK Low Time	t_{LO}	15.5	—	—	ns
SSB Pulse Width	t_{CSH}	15	—	—	ns
LSB SCK to SSB High	t_{CSHLD}	15	—	—	ns
SSB Low to SCK High	t_{CSSU}	15	—	—	ns
MISO Propagation Delay from SCK Falling Edge	t_{MISOH}	10	—	—	ns
MISO Output Valid after SSB Low	t_{CMISO}	20	—	—	ns
SSB Inactive to MISO High Impedance	t_{MISOZ}	—	—	10	ns

See the Programming section on page 22 for driver interface timing diagrams and details.

Hot Switch Restrictions

The MM5140 is not intended for hot switching applications and care should be taken to ensure that switching occurs at less than 0.5 V as illustrated below. Further, the voltage at the switch terminals must be within ±0.5 V relative to RF ground.



Floating Node Restrictions

RF pins must not be allowed to electrically float during switching operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples and recommended solutions are:

- Unconnected RF pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats RF pins, shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Functional Block Diagram

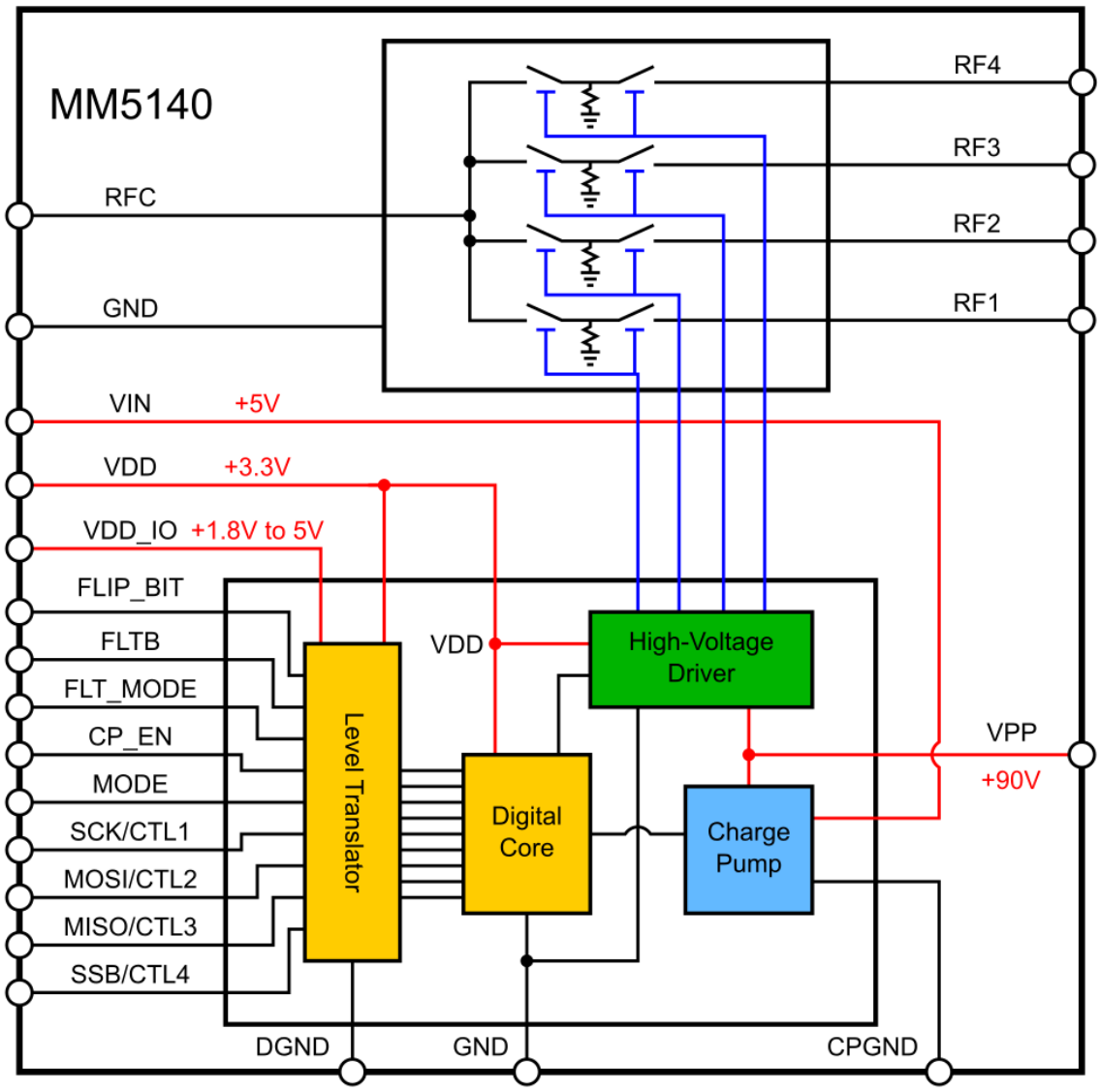


Figure 1. Functional Block Diagram

Package / Pinout Information

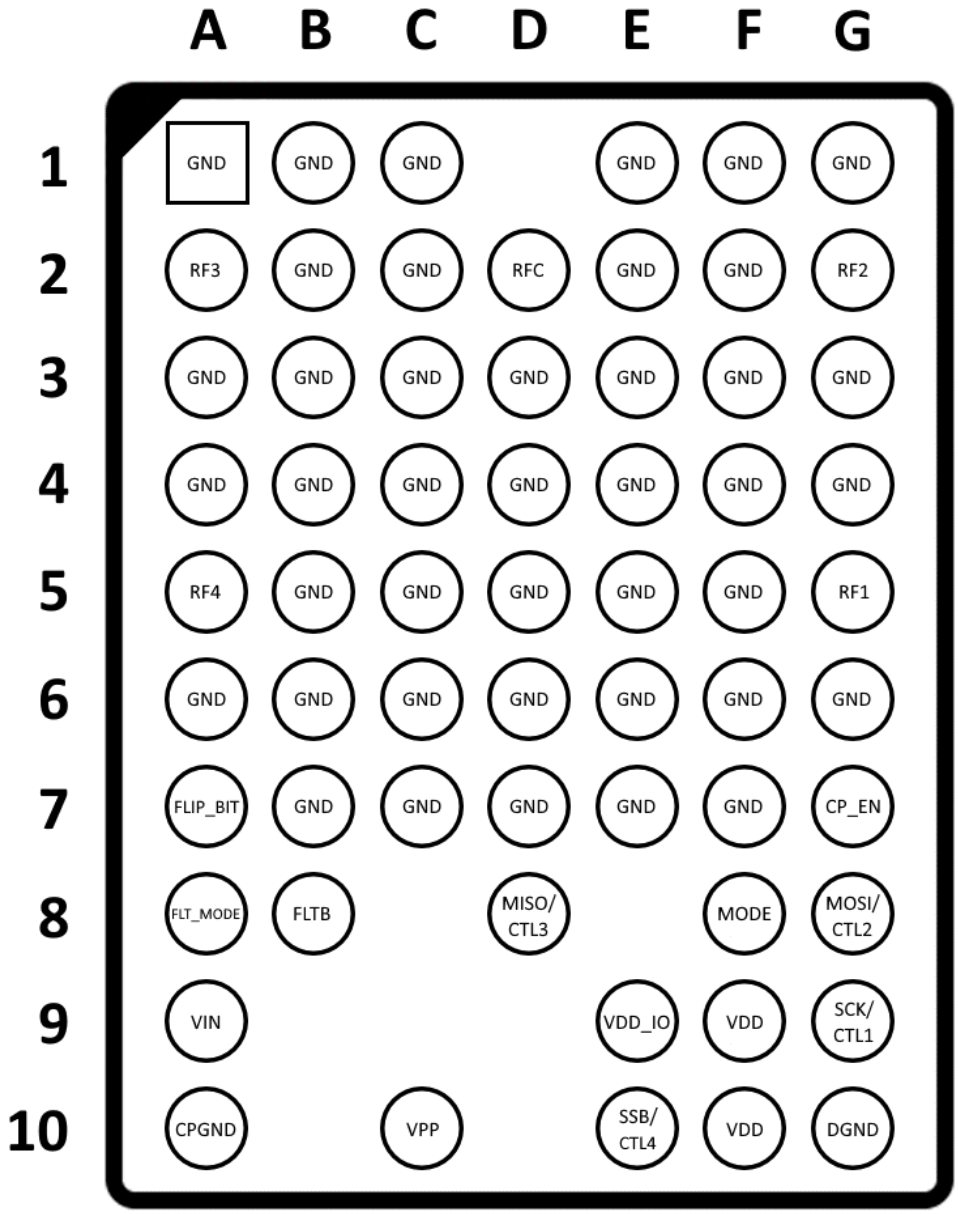


Figure 2. MM5140 5.2 mm x 4.2 mm LGA Package Pinout (Top View/As Mounted)

Table 7. Detailed Pin Description

Pin #	Pin Name	Description
A1, A3, A4, A6, B1-B7, C1-C7, D3-D7, E1-E7, F1-F7, G1, G3, G4, G6	GND	Connect to common ground. These pins are internally connected to the RF ground reference.
A2	RF3	RF channel 3 input/output.
A5	RF4	RF channel 4 input/output.
A7	FLIP_BIT	Connect to VDD_IO in SPI mode. In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and RF1-4. When FLIP_BIT is low, CTL1 enables RF1 when high, and so on for CTL2-4. When FLIP_BIT is high, refer to Table 8. This pin has an internal pull-down resistor.
A8	FLT_MODE	Pin is ignored in SPI mode. Fault Mode select in GPIO mode. Connect to VDD_IO to disable Fault Mode. This pin has an internal pull-down resistor.
A9	VIN	5 V nominal input to internal charge pump. Bypass with a low ESR 1 µF ceramic capacitor to CPGND.
A10	CPGND	Charge pump ground, should be connected to common ground.
B8	FLTB	Fault indicator in SPI and GPIO modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when fault is detected. Can be left open if not used. Pull-up voltage must be ≤ V_{DD_IO}.
C10	VPP	High-voltage output pin, 90 V nominal. Must connect with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor to GND.
D2	RFC	RF common input/output.
D8	MISO/CTL3	SPI data output in SPI mode; RF channel control in GPIO mode. This pin has an internal pull-down resistor.
E9	VDD_IO	For 3.3 V nominal logic I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8 V to +5.0 V). Bypass with a low ESR 1 µF ceramic capacitor if separate from VDD.

Pin #	Pin Name	Description
E10	SSB/CTL4	Chip select in SPI mode; RF channel control in GPIO mode. This pin has an internal pull-up resistor in SPI mode, and an internal pull-down resistor in GPIO mode.
F8	MODE[1]	Logic level input to switch inputs between SPI and GPIO modes. Connect to GND for SPI mode. Connect to VDD_IO for GPIO mode. This pin does NOT have an internal pull-up or pull-down resistor.
F9, F10	VDD	3.3 V nominal input to digital logic and internal level translators. Bypass with a low ESR 1 µF ceramic capacitor to GND.
G2	RF2	RF channel 2 input/output.
G5	RF1	RF channel 1 input/output.
G7	CP_EN	Pin is ignored in SPI mode. Charge pump enable pin in GPIO mode. Connect to VDD_IO to enable the charge pump. This pin has an internal pull-down resistor.
G8	MOSI/CTL2	SPI data input in SPI mode; RF channel control in GPIO mode. This pin has an internal pull-down resistor.
G9	SCK/CTL1	Clock input in SPI mode; RF channel control in GPIO mode. This pin has an internal pull-down resistor.
G10	DGND	Digital ground, should be connected to common ground.

Notes:

1. MODE should be tied to GND or VDD_IO if the use case is SPI or GPIO control, respectively.

Thermal and Power Handling Considerations

Under low-power operating conditions, the MM5140 case temperature mimics the environment temperature. However, during high power operation, the case will heat up due to power dissipation within the device. It is important to keep the device case temperature below 150 ºC for continued reliable operation of the internal controller. Based on an environmental hot temperature of 85 ºC, then a 65 ºC rise is allowable due to power dissipation. This results in a power dissipation limit of 0.8 W within the device. The operating power limit at a given frequency can then be calculated based on the insertion loss of the internal MEMS switch (MM5130).

Considering an insertion loss of -0.14 dB at 3 GHz:

Power Handling = Max. Power Dissipation / (1-10^(Insertion Loss/10))

= 0.8/0.032

= 25.0 W

As most self-heating within the package comes from the MM5130 insertion loss, we use this to set a limit on the power handling. The MM5130 insertion loss can also be approximated by a third order polynomial:

Insertion Loss (dB) = -1.1E-04*f3 + 1.2E-03*f2 – 0.024*f – 0.076

where f is frequency in GHz. See Figure 3 for the power derating curve in an 85 ºC environment.

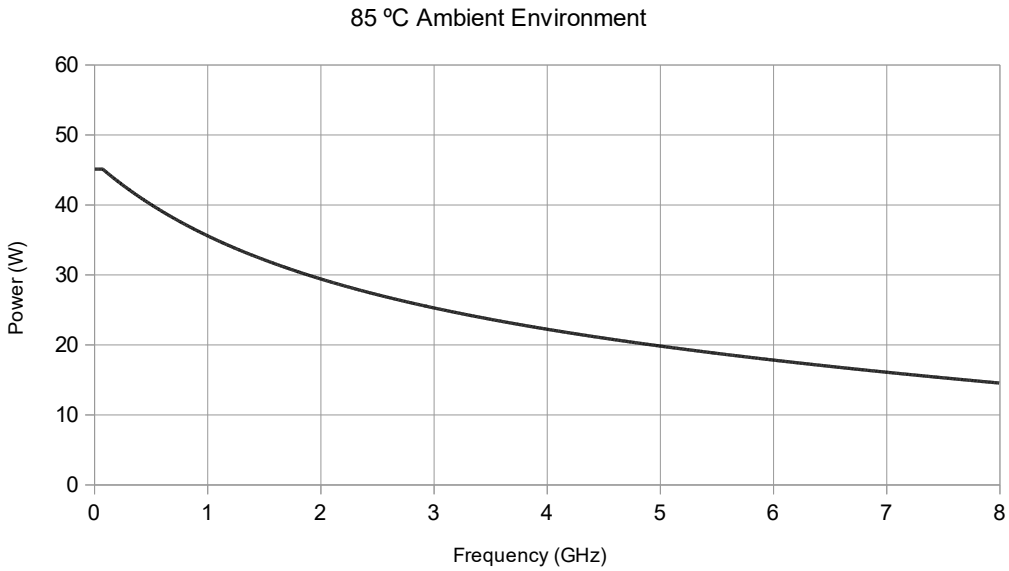


Figure 3. Maximum Power Handling vs. Frequency (1 of 2)

Below 10 MHz; the maximum power handling is shown in Figure 4.

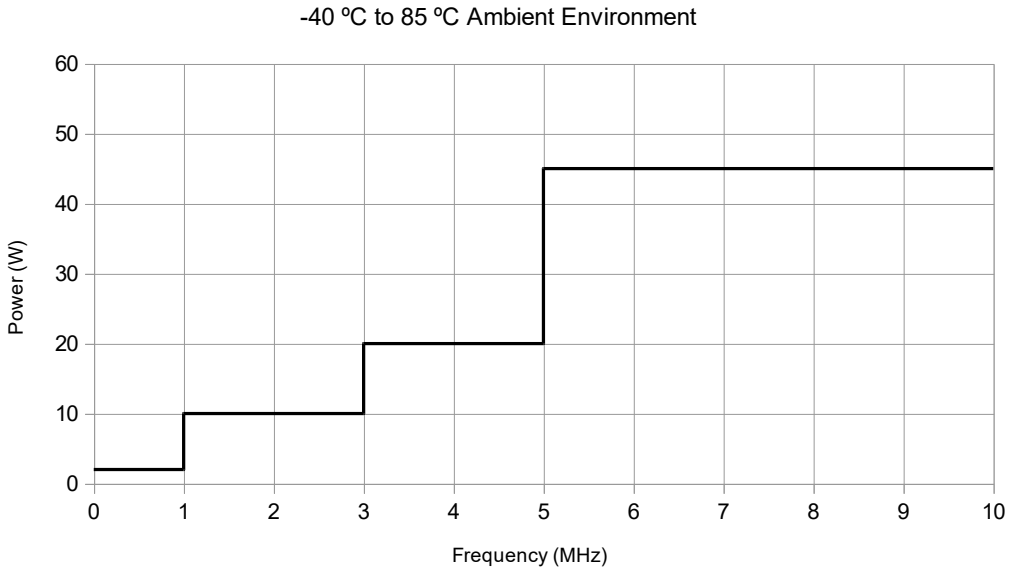


Figure 4. Maximum Power Handling vs. Frequency (2 of 2)

RF Performance

Typical device performance measured on MM5140 evaluation board, de-embedded.

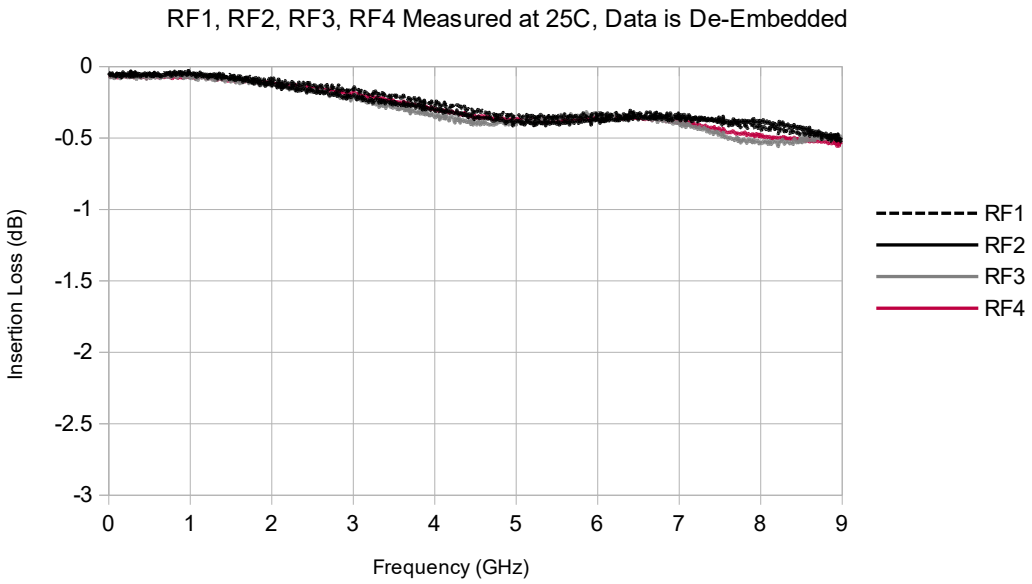


Figure 5. Insertion Loss / S21

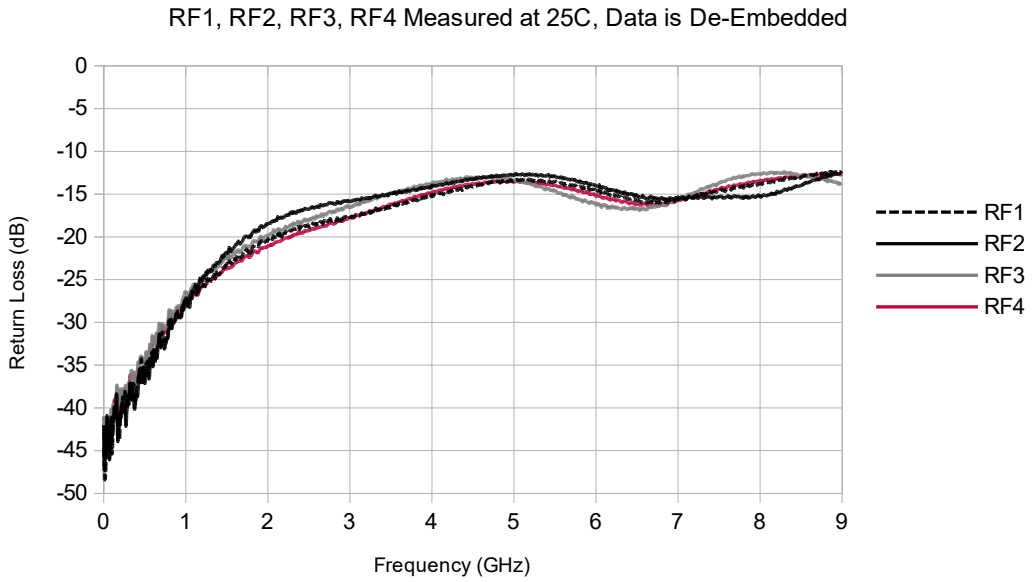


Figure 6. Return Loss / S11

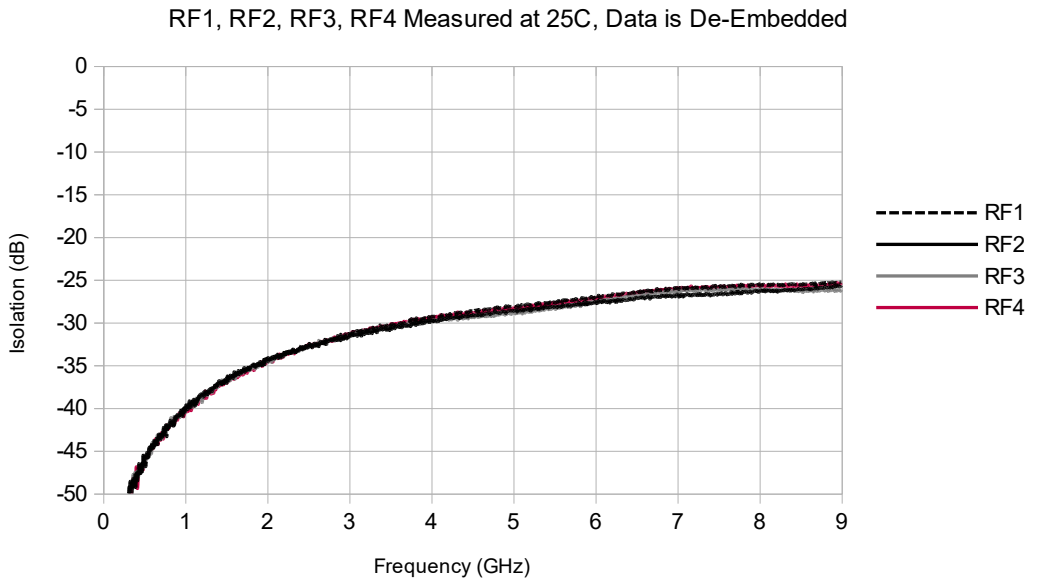


Figure 7. Off-State Isolation / S21

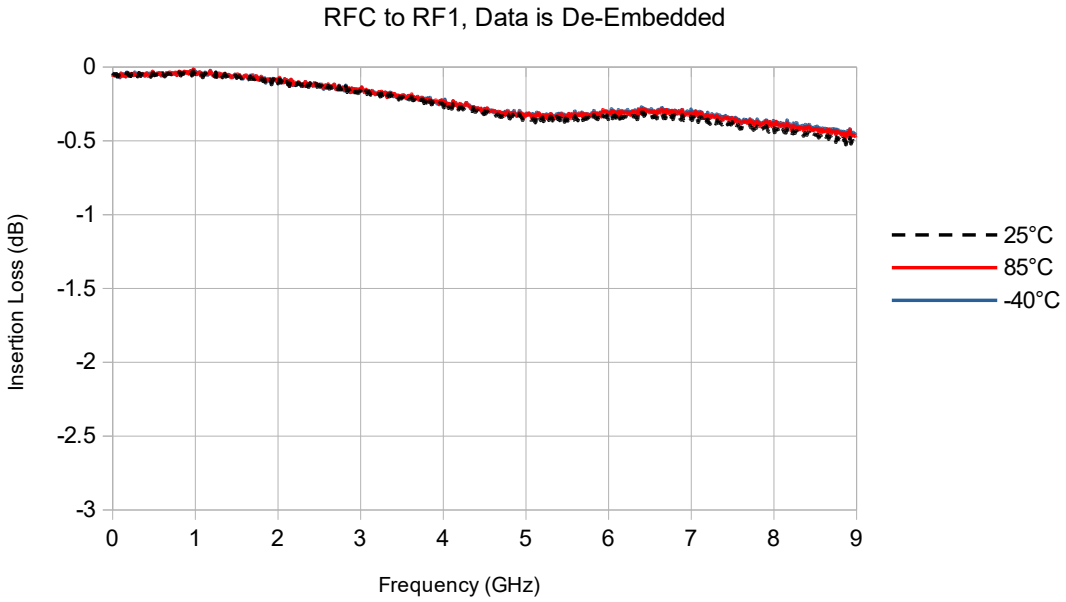


Figure 8. Insertion Loss / S21 vs. Temperature

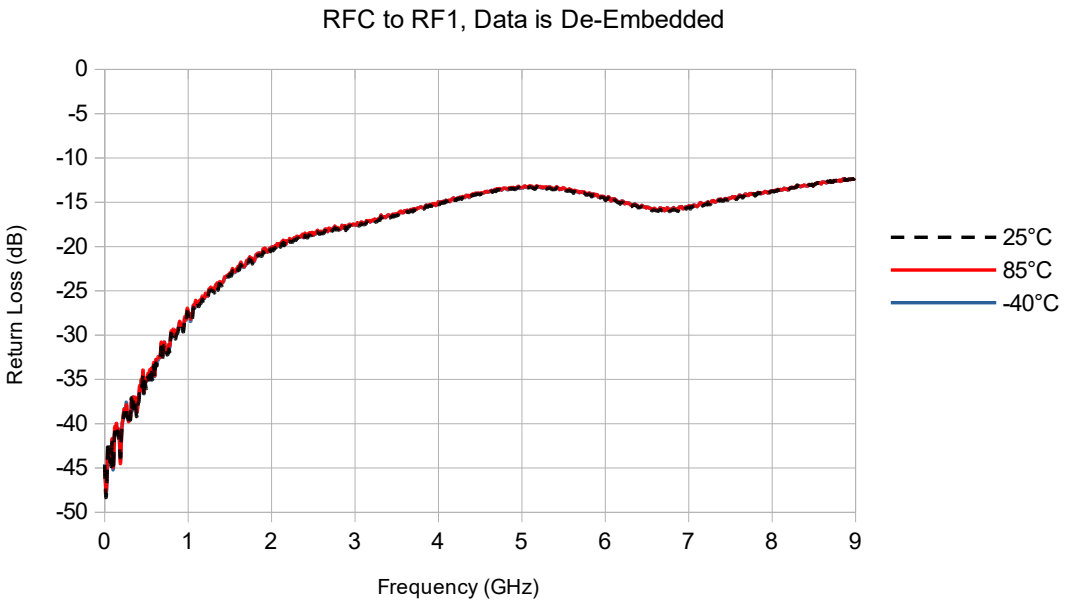


Figure 9. Return Loss / S11 vs. Temperature

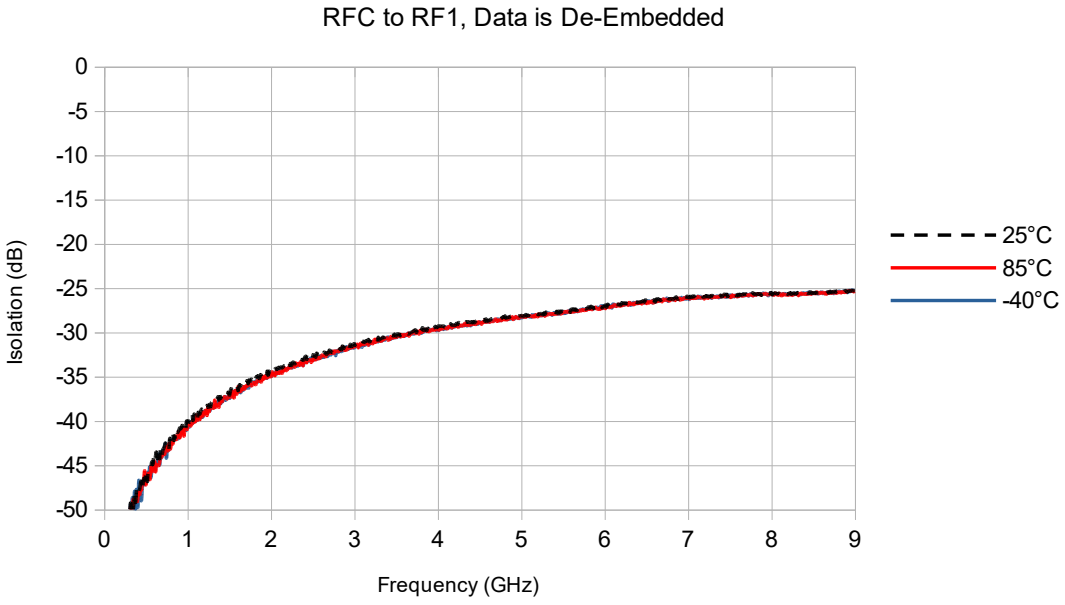


Figure 10. Off-State Isolation / S21 vs. Temperature

On / Off Switching Time

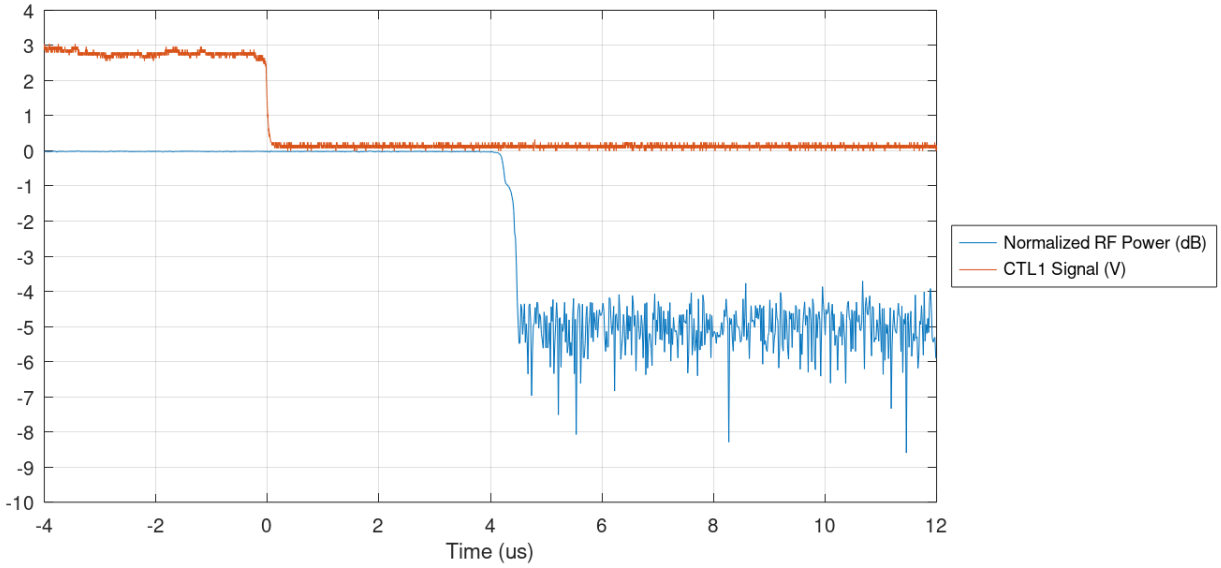


Figure 11. RF Off Switching Time (GPIO Mode)

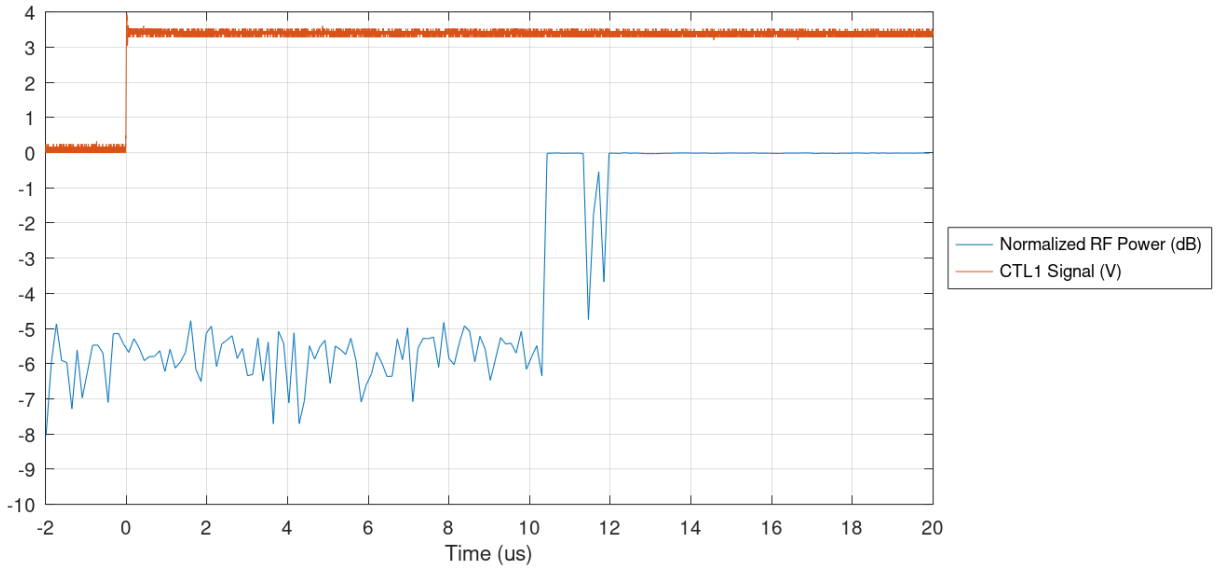


Figure 12. RF On Switching Time (GPIO Mode)

Switch Reliability

Switch Hold-Down duration predictions and actuation cycling reliability test results are plotted below. Hold Down median failure is predicted to be >68000 days (>186 years) @ 50ºC and >1800 days (>4.9 years) @ 85ºC. Failure criteria is 20% change in pull in voltage and is based on creep model extrapolation of 1000 hours Hold Down test data.

Cycling median failure is greater than 30 billion cycles @ 25ºC and 320 million cycles @ 85ºC.

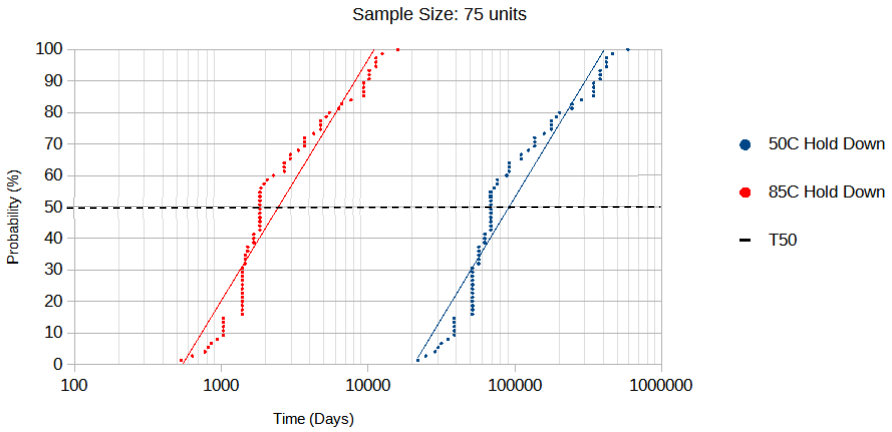


Figure 13. Hold Down: Days to Failure

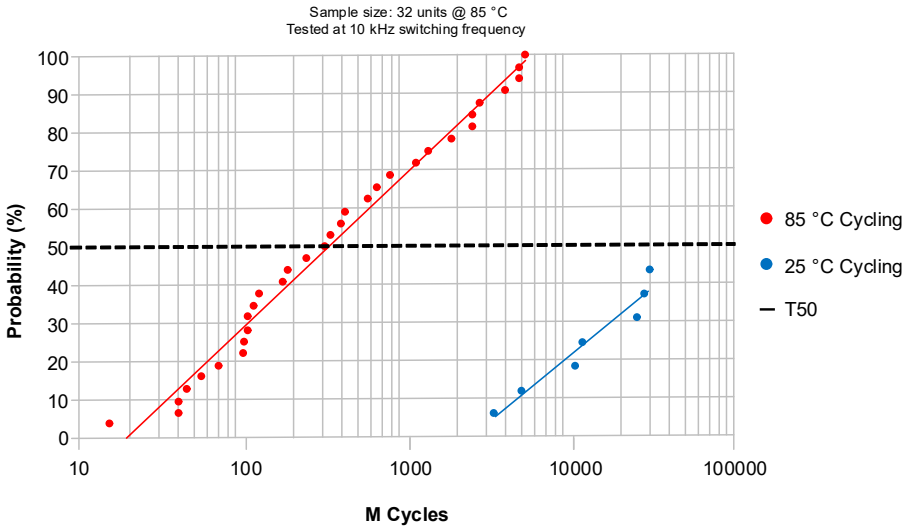


Figure 14. Cycling: M Cycles to Failure[1]

Notes:

2. Failure definition is stuck closed failure.

Programming

Communication Interface

The driver interface has two modes of operation: SPI and GPIO, selected by the MODE input pin.

All the SPI pins except the SSB and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float.

The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is CTL4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

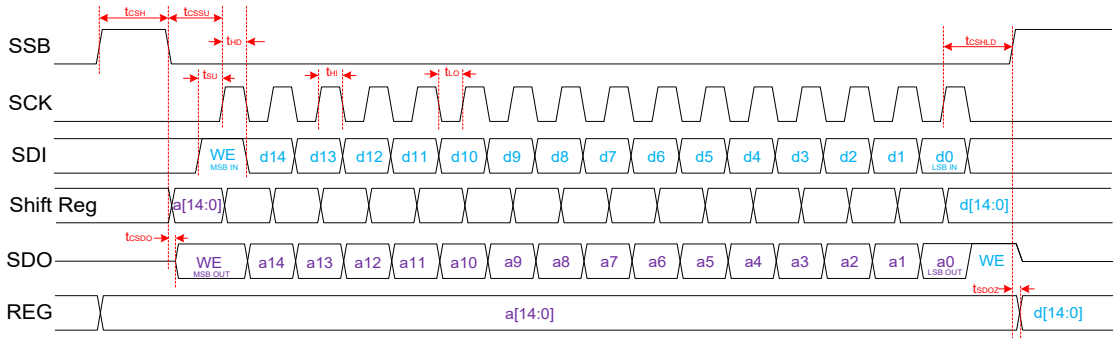


Figure 15. SPI Timing Diagram

SPI Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. In Daisy Chain Operation, see Figure 18, Figure 19, and Figure 20.

The SPI works at any frequency up to a maximum of 33 MHz and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

SPI Interface Mode

SPI timing diagrams are provided in Figure 15 through Figure 20. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data (DN) to

the Target, while the Target passes its previous (DN-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

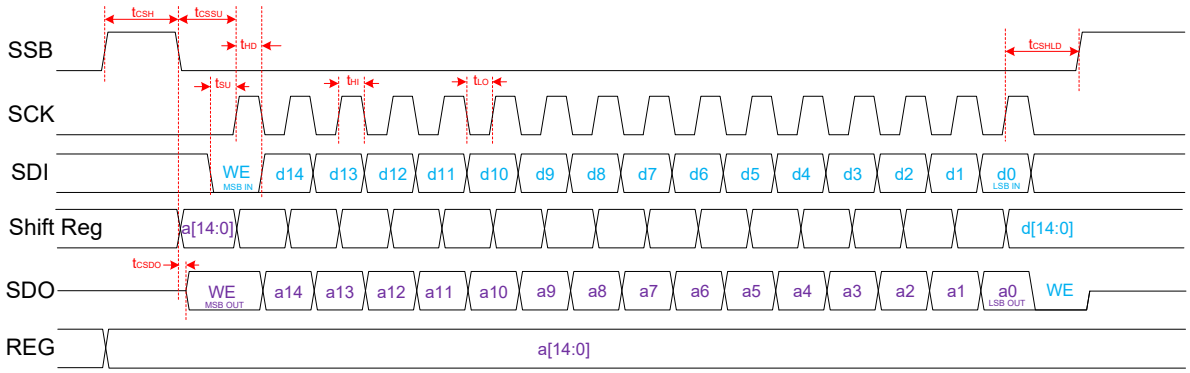


Figure 16. SPI Read Only (1 IC, No Daisy Chain)

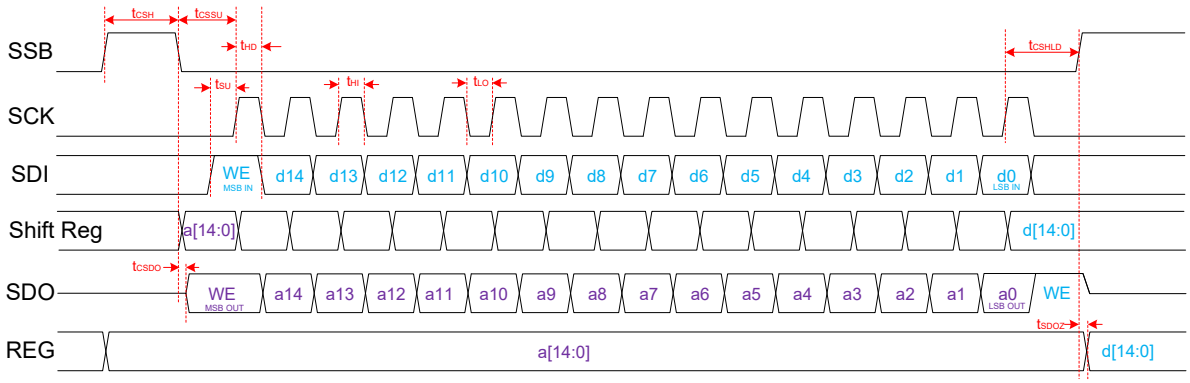


Figure 17. SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the MISO pin while clocking the SCK pin.

Register STATE holds the state of the 4 switches and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high. Register CONTROL holds four control bits (CPEN, VPPCOMP, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high.

In SPI mode, the CP_EN and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead. The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	0	0	RF4	RF3	RF2	RF1
bit 7							bit 0

bit 7: **Low**
Set this bit low.
bit 6: **Low**
Set this bit low.
bit 5: **Low**
Set this bit low.
bit 4: **Low**
Set this bit low.
bit 3: **RF4**
1 = RFC to RF4 is enabled
0 = RFC to RF4 is disabled
bit 2: **RF3**
1 = RFC to RF3 is enabled
0 = RFC to RF3 is disabled
bit 1: **RF2**
1 = RFC to RF2 is enabled
0 = RFC to RF2 is disabled
bit 0: **RF1**
1 = RFC to RF1 is enabled
0 = RFC to RF1 is disabled

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit 7							bit 0

bit 7: **WR_EN**

1 = Enable write mode

0 = Disable Write mode (read only)

bit 6: **FSTAT** (see Note 1 below)

1 = VPP OR VDD Fault status = faulted

0 = VPP OR VDD Fault status = NOT faulted

bit 5: **SLEEP**

1 = SLEEP mode active (all analog circuits disabled)

0 = SLEEP mode inactive (all analog circuits enabled)

bit 4: **FLTMODE**

1 = Fault Mode Disabled (shutdown Disabled)

0 = Fault Mode Enabled (shutdown Enabled)

bit 3: **VPPCOMP**

1 = VPP under-voltage comparator is disabled

0 = VPP under-voltage comparator is active

bit 2: **Do Not Care**

This bit can be set to either state without effecting performance.

bit 1: **CPEN**

1 = Charge Pump is enabled

0 = Charge Pump is disabled

bit 0: **Do Not Care**

This bit can be set to either state without effecting performance.

Notes:

3. After this bit is set high, it must be written to 0 to clear the fault. If fault mode is enabled, CPEN must be toggled to restart the charge pump. See Fault Conditions for more information.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the MISO of one chip to the MOSI of the next chip in the chain, as shown in Figure 18. SPI timing diagrams with daisy-chained devices are provided in Figure 19 and Figure 20.

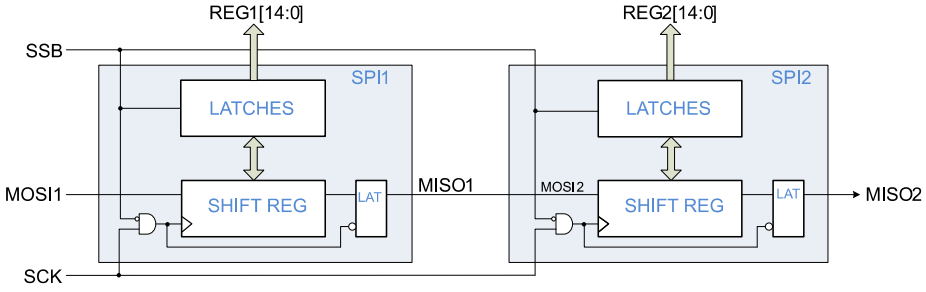


Figure 18. SPI with Two ICs Daisy-chained

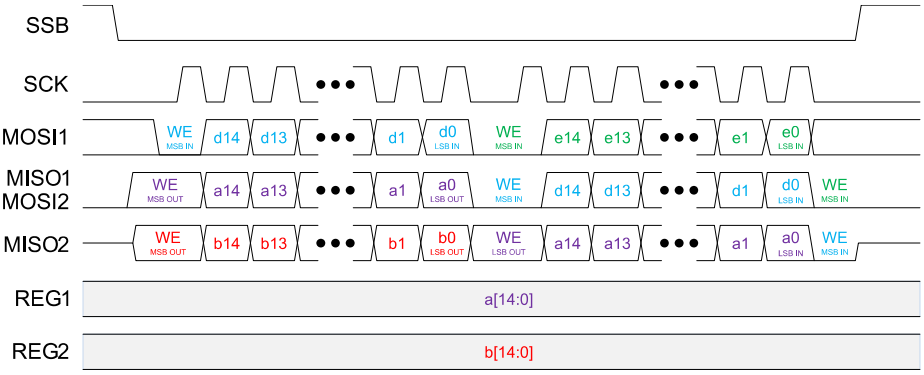


Figure 19. SPI Read Only (Two ICs Daisy-chained)

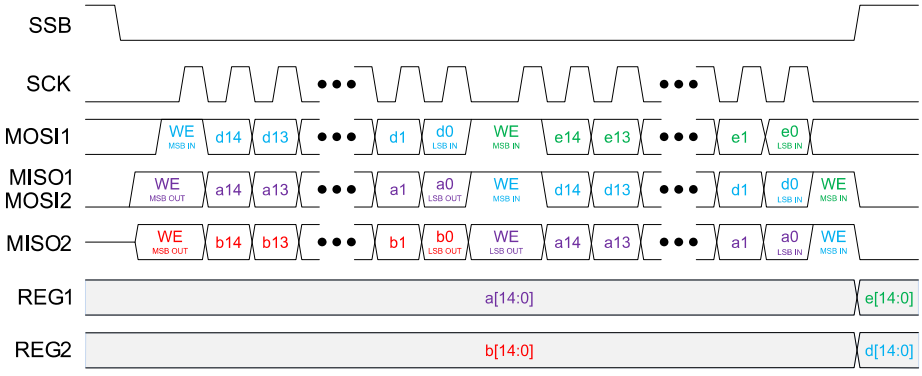


Figure 20. SPI Read & Write (Two ICs Daisy-chained)

GPIO Communication

MODE = 1 activates the GPIO (General Purpose Input Output or Parallel Mode) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs.

Table 8. Switch State Table in GPIO Mode

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
0	1	0	0	0	0	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	**ON**
2	1	0	0	1	0	OFF	OFF	**ON**	OFF
3	1	0	0	1	1	OFF	**ON**	OFF	OFF
4	1	0	1	0	0	**ON**	OFF	OFF	OFF
5	1	0	1	0	1	OFF	OFF	OFF	OFF
6	1	0	1	1	0	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	OFF	OFF	OFF
8	1	1	0	0	0	OFF	OFF	OFF	OFF
9	1	1	0	0	1	**ON**	OFF	OFF	**ON**
10	1	1	0	1	0	OFF	**ON**	**ON**	OFF
11	1	1	0	1	1	**ON**	OFF	**ON**	OFF
12	1	1	1	0	0	**ON**	OFF	**ON**	OFF
13	1	1	1	0	1	**ON**	OFF	**ON**	OFF
14	1	1	1	1	0	OFF	**ON**	OFF	**ON**
15	1	1	1	1	1	OFF	OFF	OFF	OFF
16	0	0	0	0	0	OFF	OFF	OFF	OFF
17	0	0	0	0	1	OFF	OFF	OFF	**ON**
18	0	0	0	1	0	OFF	OFF	**ON**	OFF
19	0	0	0	1	1	OFF	OFF	**ON**	**ON**
20	0	0	1	0	0	OFF	**ON**	OFF	OFF
21	0	0	1	0	1	OFF	**ON**	OFF	**ON**
22	0	0	1	1	0	OFF	**ON**	**ON**	OFF

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
23	0	0	1	1	1	OFF	**ON**	**ON**	**ON**
24	0	1	0	0	0	**ON**	OFF	OFF	OFF
25	0	1	0	0	1	**ON**	OFF	OFF	**ON**
26	0	1	0	1	0	**ON**	OFF	**ON**	OFF
27	0	1	0	1	1	**ON**	OFF	**ON**	**ON**
28	0	1	1	0	0	**ON**	**ON**	OFF	OFF
29	0	1	1	0	1	**ON**	**ON**	OFF	**ON**
30	0	1	1	1	0	**ON**	**ON**	**ON**	OFF
31	0	1	1	1	1	**ON**	**ON**	**ON**	**ON**

Fault Conditions

There are two comparators that can signal a fault condition - VDD under voltage fault and VPP under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO.

Note: The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP_EN pin is set low.

The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than $UVLO_{RISE}$ and VPP goes higher than V_{EN}). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below $UVLO_{FALL}$ or VPP goes below VPP_{DIS}, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared – the FSTAT bit remains latched high until it is cleared via a SPI write.

If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the outputs are all set low and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to re-start the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

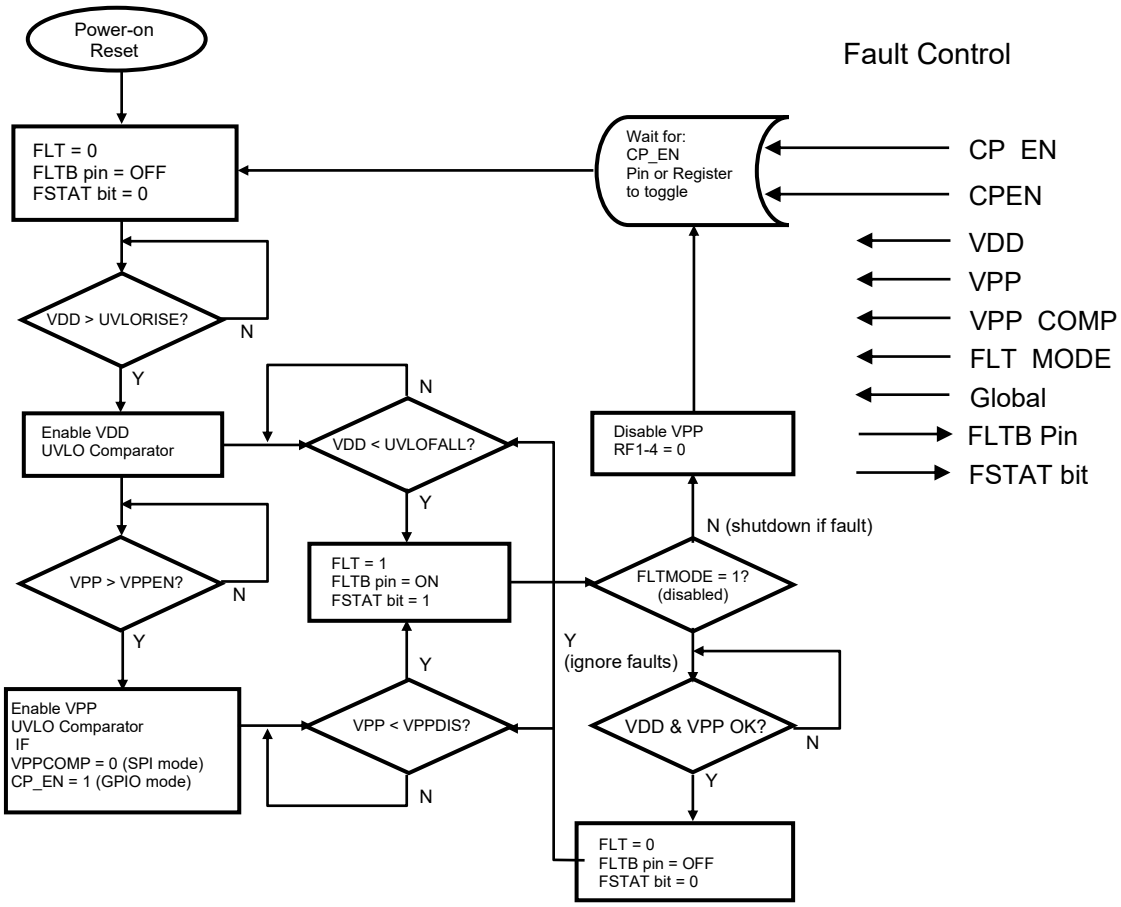


Figure 21. Flowchart for Fault

Notes:

1. The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2. VDD_IO is not monitored unless it is connected to VDD.
3. VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP_EN pin is low In GPIO mode.

External Circuitry

The MM5140's internal driver requires external circuitry to operate its charge pump. The diagram below shows the suggested bypass capacitors that have been used with good results. Menlo Micro recommends selecting components with equal or better performance.

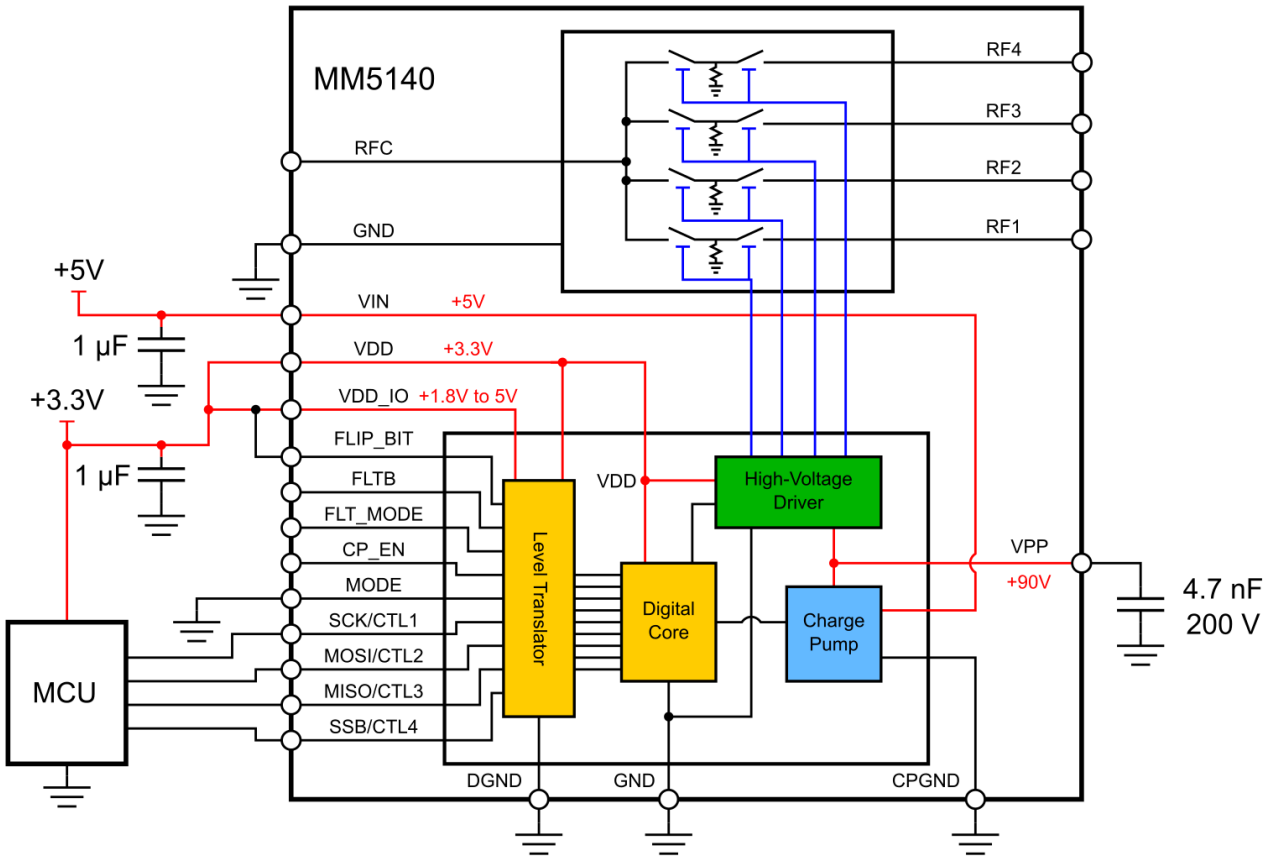
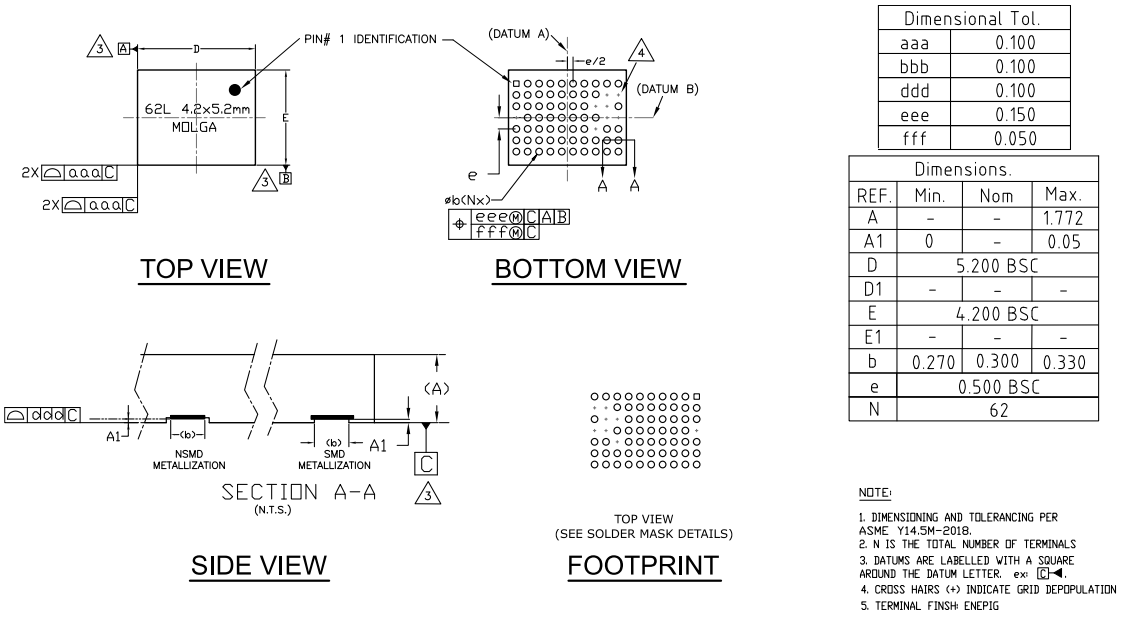


Figure 22. MM5140 Application Diagram

Package Drawing

62 Pin LGA Package

Dimensions are given in millimeters.



Dimensional Tol.	
aaa	0.100
bbb	0.100
ddd	0.100
eee	0.150
fff	0.050

Dimensions.			
REF.	Min.	Nom	Max.
A	-	-	1.772
A1	0	-	0.05
D	5.200 BSC		
D1	-	-	-
E	4.200 BSC		
E1	-	-	-
b	0.270	0.300	0.330
e	0.500 BSC		
N	62		

NOTE:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
2. N IS THE TOTAL NUMBER OF TERMINALS
3. DATUMS ARE LABELLED WITH A SQUARE AROUND THE DATUM LETTER. ex: C
4. CROSS HAIRS (+) INDICATE GRID DEPOPULATION
5. TERMINAL FINSH: ENEPIG

Figure 23. Package Drawing

The pin array is located symmetrically on the package body as specified in JEDEC Design Guide 4.25B for JEDEC LGA. An exception to JEDEC LGA guidelines is made for the letter axis and number axis. See Figure 2.

Solder Mask Details

Dimensions are given in millimeters.

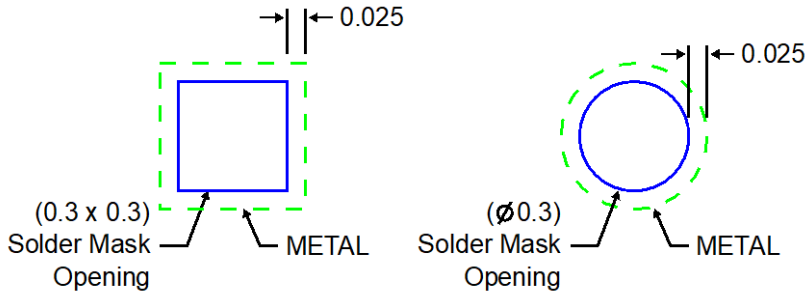


Figure 24. Solder Mask Details

Recommended PCB Layout and SMT Parameters

- Use solder mask defined pads to allow a solid grounding plane under the part. See Figure 24 for recommended solder mask opening.
- Place ground vias under package near RF pins.
- Minimize the distance between decoupling capacitors and supply pins. The ground pin of the VIN decoupling capacitor should be close to the CPGND pin of MM5120.
- Use Type 5 solder paste.

Figure 25 below shows an example layout. This example uses a Rogers 4350b core with a thickness of 254 microns. 50Ω coplanar waveguide transmission lines are used to route the RF, with a trace thickness of 383 microns, and ground spacing of 152 microns.

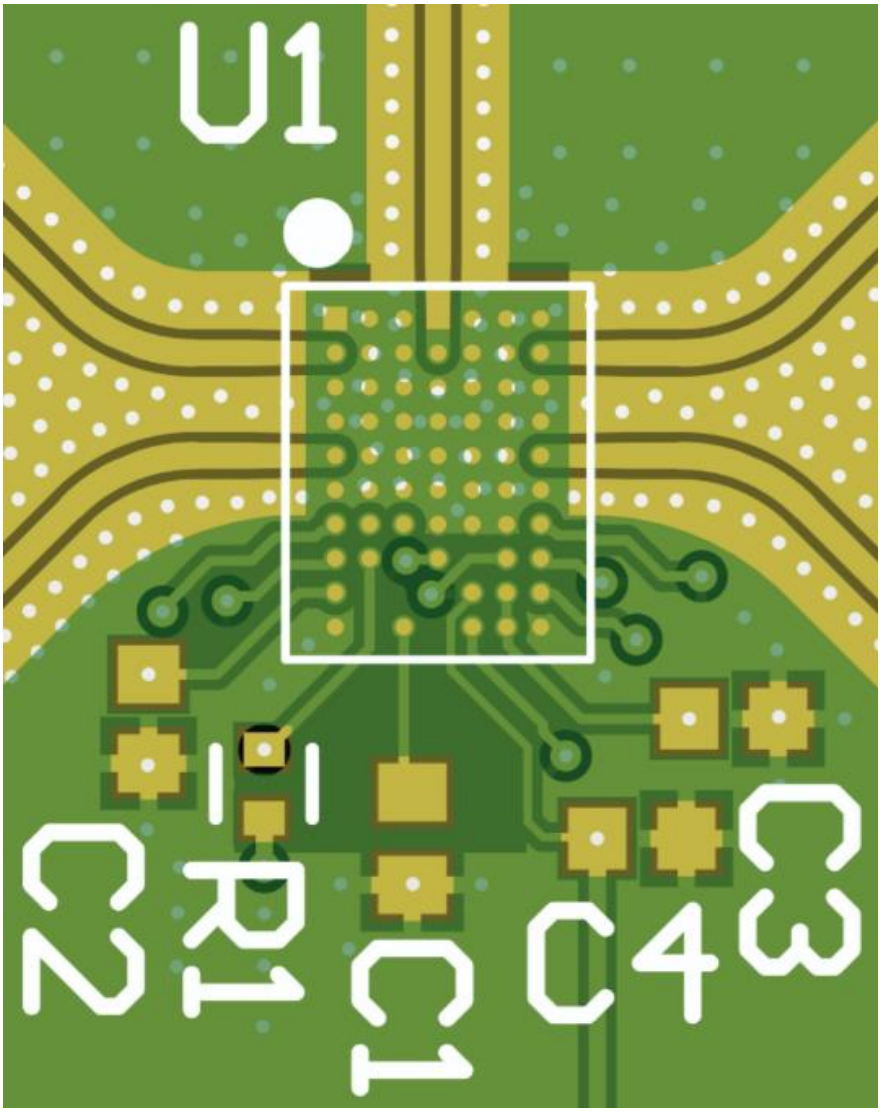


Figure 25. Example PCB Layout

Recommended Solder Reflow Profile

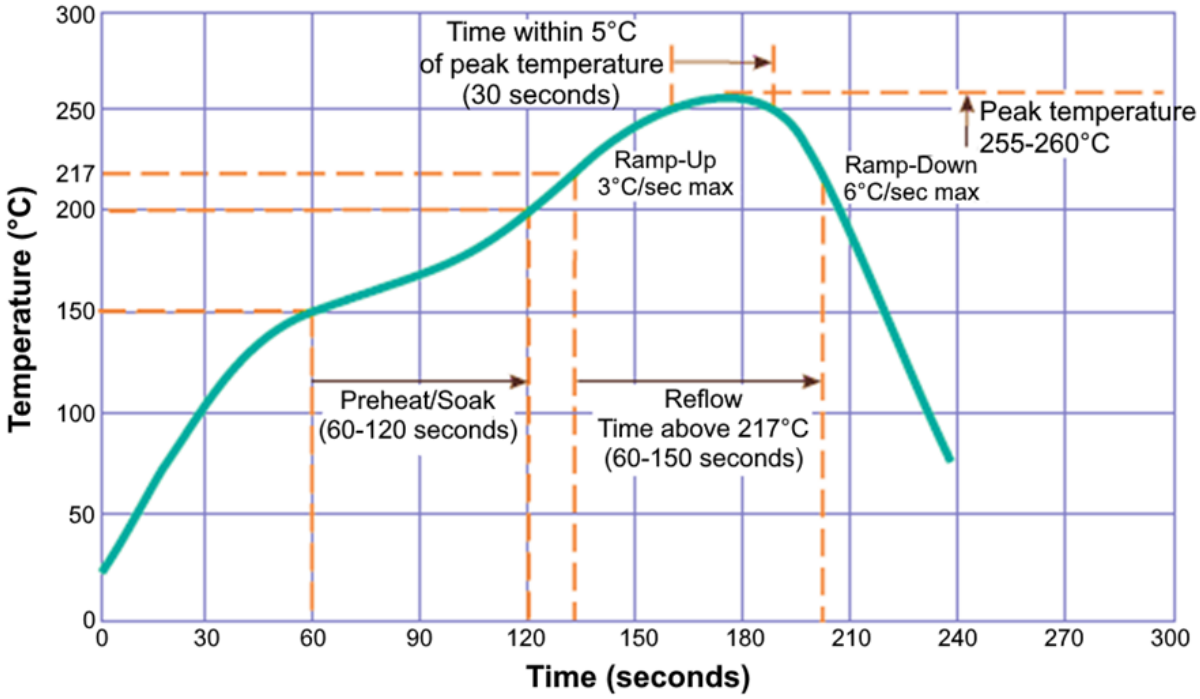


Figure 26. Recommended Reflow Profile

A ROHS compliant Solder Alloy used is SAC alloy: 96.5% Sn, 3.0%Ag, 0.5%Cu. These are the nominal percentages of the components. This alloy is designed to replace SnPb solders to eliminate Lead (Pb) from the process, requiring a higher reflow temperature. Moisture resistance performance may be impacted if not using the Pb-Free reflow conditions.

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.[1]

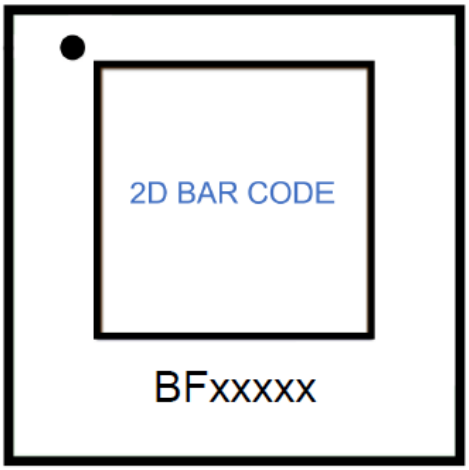
Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags the following is recommended:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less.

[1] Parts labeled prior to July 13th, 2023 may be labeled as MSL 4 rating based on rating at the time of manufacturing/packaging.

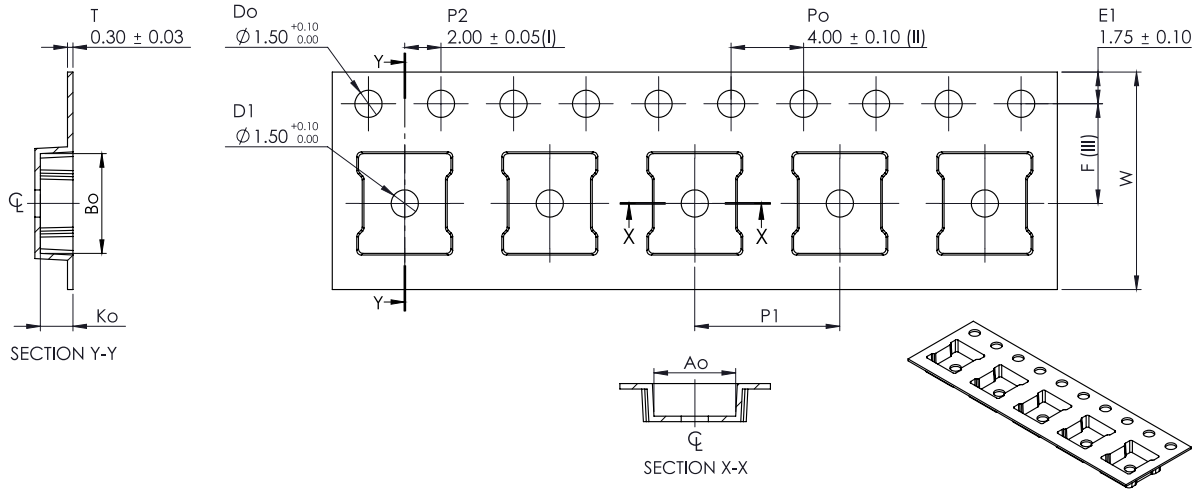
Package Marking Information



Dot ● = Pin 1 Indicator
Line 1 = 2D Bar Code
Line 2 = Human-readable product code

Figure 27. Package Marking Drawing

Package Materials Information



Ao	4.50	+/- 0.10
Bo	5.50	+/- 0.10
Ko	1.80	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+0.30 / -0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes, No measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 28. Tape and Reel Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package Description	Temp Range	Device Marking[1]
MM5140-01NDB	DC-8GHz - SP4T - 5mm x 4mm LGA, Industrial Temp	-40°C to +85°C	BFxxxxx
MM5140-01NDB-TR	DC-8GHz - SP4T - 5mm x 4mm LGA, Industrial Temp, Tape and Reel (Qty 250)	-40°C to +85°C	BFxxxxx
MM5140EVK1	Evaluation board for MM5140 DC-8GHz - SP4T - 5mm x 4mm LGA		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is a placeholder for a 5-digit numerical code.

Legacy Product	New Product Name	
Name	**Bulk**	**Tape and Reel[1]**
MM5140-01C	**MM5140-01NDB**	**MM5140-01NDB-TR**

Notes:

1. 250pcs standard tape and reel increment.

Important Information

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Please contact Menlo Micro for the latest specifications, additional product information, test and evaluation boards, product samples, worldwide sales and distribution locations:

Internet: www.menlomicro.com
E-mail: sales@menlomicro.com

For product technical questions and application information: support@menlomicro.com.

