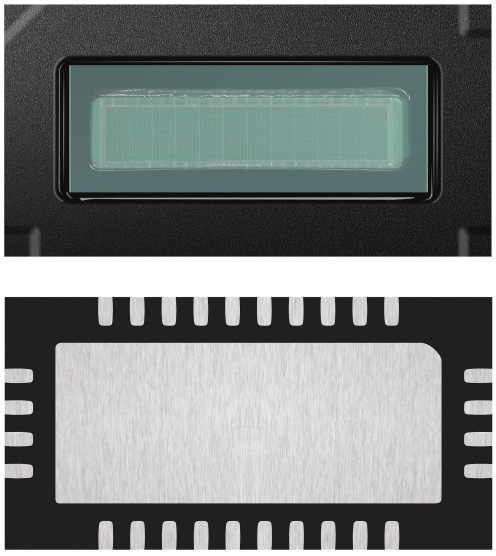
RDM-Series 1 x 12 SiPM Array

ArrayRDM-0112A20-QFN-TR (1)

The ArrayRDM-0112A20-QFN-TR(1) is a monolithic 1 × 12 array of Silicon Photomultiplier (SiPM) pixels based on the market-leading RDM process. The RDM process has been specifically developed to create products that give high PDE at the NIR wavelengths used for LiDAR and 3D ranging applications. For details of Automotive Qualification, please contact **onsemi**.

Table 1. KEY SENSOR AND PACKAGE SPECIFICATIONS

Parameter	Value	Comments
Silicon Process	RDM	
Number of Pixels	12	
Array Configuration	1 × 12	Monolithic silicon array
Pixel Size	1.12 × 0.47 mm	
Pixel Pitch	0.49 mm	
Microcell Size	20 μm	
Number of Microcells per Pixel	806	
Package Size	5.2 × 10.0 × 1.85 mm	W × L × H (see case outline on page 8 for more details)
Output Type	Analog	Standard output per pixel



The ArrayRDM-0112A20-QFN-TR Product
Case 485FZ

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 6 of this data sheet.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit	Comment
Maximum Overvoltage (Vov)	9	V	All temperatures
Maximum Current	20	mA	For entire array (12 channels) at recommended Vov
Maximum Storage Temperature	125	°C	
Functional Operating Temperature Range	−40 to 105	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: Vop = Vbr + Vov. Vbr is temperature dependent. Vop is also temperature dependent.

Table 3. ELECTRICAL SPECIFICATIONS

Parameter	−40°C		21°C		105°C		Unit
	Min	Max	Min	Max	Min	Max	
Breakdown Voltage (Vbr)	19.5	20.5	21.0	22.0	23.0	33.0	V

NOTES: Vbr is defined as the intercept between the below-breakdown leakage current and the linear fit to the square root of the dark current above breakdown.
Vbr is temperature dependent. At 105°C the Vbr range within a lot will be 1 V. Refer to per lot data for exact range.
Vop = Vbr + Vov. Vop is also temperature dependent.

Table 4. BIASING SPECIFICATIONS

Parameter	Value	Unit	Comment
Recommended Overvoltage (Vov)	8	V	Vov across full operating temperature range
Maximum Overvoltage (Vov)	9	V	All temperatures

NOTE: Operating bias voltage (Vop) = Vbr + Vov

Table 5. CALCULATED ELECTRICAL PARAMETERS

Parameter	Typical Value	Unit	Comment
Terminal Capacitance	20	pF	Per SiPM channel
Saturation Current (continuous)	2.8	mA	Per SiPM channel
Saturation Current (pulse)	6.2	mA	Per SiPM channel

NOTES: Terminal capacitance is calculated from Gain of a typical device at recommended Vov.
Saturation current is calculated from Gain and recovery time of a typical device at recommended Vov.

Table 6. PACKAGE SPECIFICATIONS

Parameter	Value	Unit	Comment
ESD − HBM	500	V	Class 1B
ESD − CDM	500	V	Class C2A
θ_{JC}	4	°C/W	Junction-to-Case thermal resistance is simulated with a heat sink at 25°C mounted on bottom of the package
θ_{JA}	58	°C/W	Junction-to-Ambient thermal resistance is simulated with a 1S0P test PCB according to JESD51-7 standard
MSL	4		All variants

Table 7. TYPICAL SIPM PERFORMANCE SPECIFICATIONS

Parameter	Typical value at Vop		Unit
	Vop = 29.0 V	Vop = 30.0 V	
PDE @ 905 nm	15.6	16.8	%
Crosstalk	22	27	%
Thermal DCR per pixel	0.12	0.13	Mcps
Total DCR per pixel	0.13	0.14	Mcps
Delayed Crosstalk	7	9	%
1PE Level (via reference circuit)	47	54	mV
Gain	1.1×10^6	1.2×10^6	
Rise Time (20%−80%)	190	188	ps
Recovery Time (90%−10%)	49	51	ns

NOTE: Table shows typical performance parameters at 21°C.

90% − 10% Recovery Time Parameter

The recovery time indicates the time taken for the microcells to recover to fully biased state. Recovery time is measured by applying a low power 905 nm 50 ps laser pulse at the SiPM and measuring the resulting pulse shape on the standard output. The 90% to 10 % recovery time is the time interval between the signal crossing the 90% threshold and the 10% threshold, relative to the peak amplitude. Note that recovery time will depend on a number of factors including the circuit. The circuit used for this measurement is pictured in Figure 1. Typical pulse shapes for both the standard and fast output, also using this circuit, are shown in Figure 2.

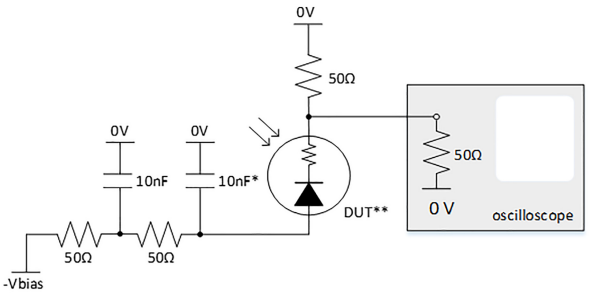


Figure 1. The Circuit used for Recovery Time Parameter Measurement

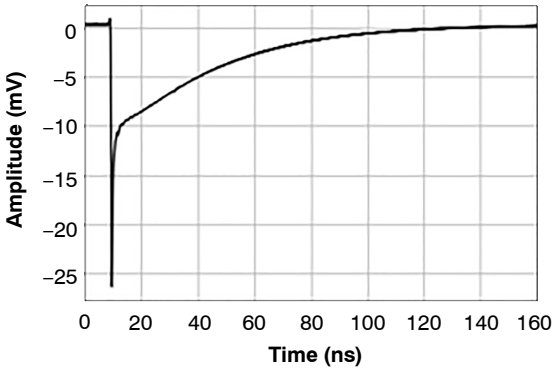


Figure 2. Pulse Shape

1PE Measurement Details

The single photoelectron pulse height is characterized by measuring the amplified 1PE signal using the measurement circuit in Figure 3. The measured values include the gain due to the amplifiers, which is ~100X.

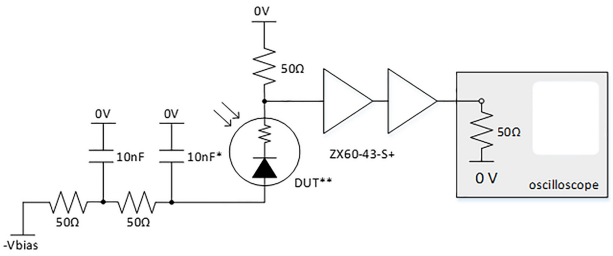


Figure 3. Measurement Circuit for Single Photoelectron Measurement Gain is ~ 100x

* Additional decoupling not shown.
** Single SiPM channel shown only.

PIN ASSIGNMENT

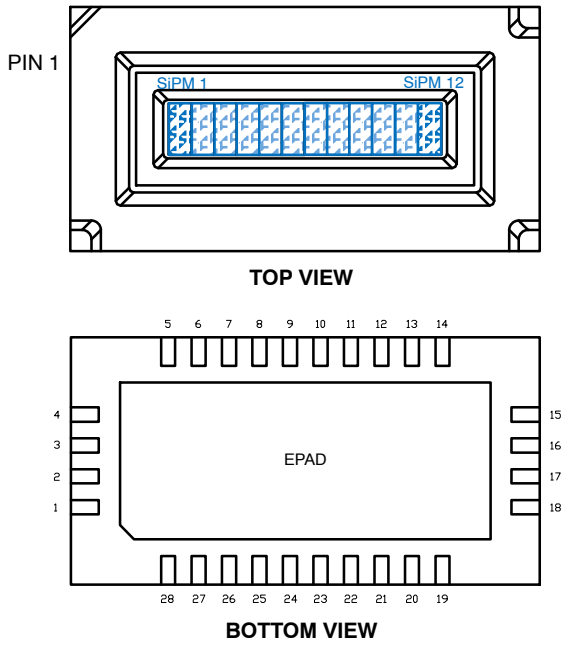


Figure 4. Device and Pin Numbering

Pin #	Pin Name	Pin Function
1	Cathode 1	SiPM 1 standard output
28	Cathode 2	SiPM 2 standard output
27	Cathode 3	SiPM 3 standard output
26	Cathode 4	SiPM 4 standard output
25	Cathode 5	SiPM 5 standard output
24	Cathode 6	SiPM 6 standard output
23	Cathode 7	SiPM 7 standard output
22	Cathode 8	SiPM 8 standard output
21	Cathode 9	SiPM 9 standard output
20	Cathode 10	SiPM 10 standard output
19	Cathode 11	SiPM 11 standard output
18	Cathode 12	SiPM 12 standard output
EPAD	Anode	Common Anode
2–17	NC	No Connect

APPLICATION ADVICE

The ArrayRDM-0112A20-QFN-TR(1) is formed of a linear array of 12 SiPM pixels. The QFN package provides a connection to each pixel cathode (for access to the individual signals) and a common anode. The common anode allows the provision of a single bias supply for all 12 pixels. The recommended test connections and biasing are as per the evaluation board that is detailed in the following section.

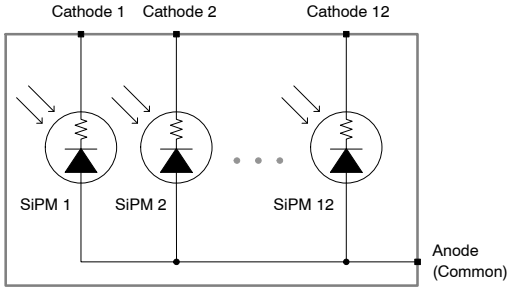


Figure 5. Array Schematic Showing Pixel Connections

TYPICAL SIPM PERFORMANCE PLOTS

Below plots show the SiPM performance characteristics for a typical device at room temperature. For detailed characterization information please contact **onsemi**.

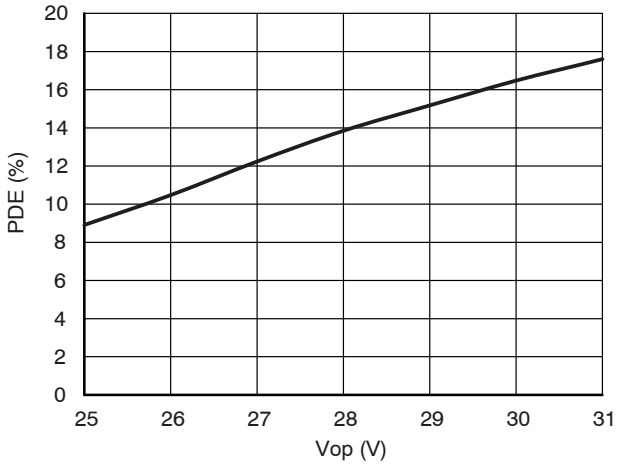


Figure 6. PDE at 905 nm vs. Bias Voltage

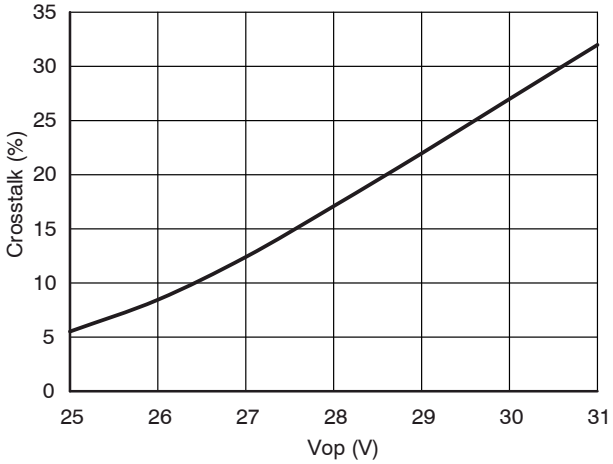


Figure 7. Crosstalk vs. Bias Voltage

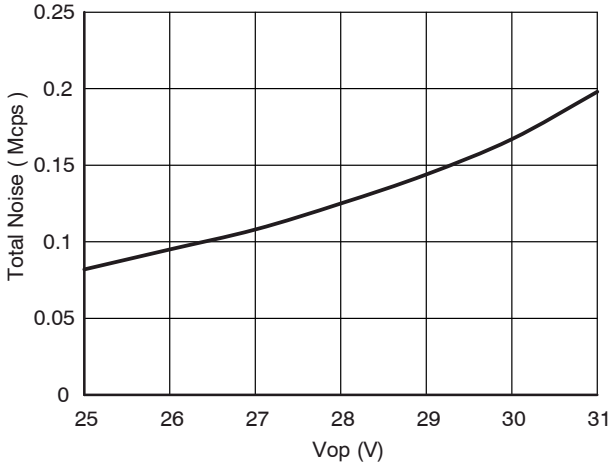


Figure 8. Total Noise (DCR per Channel) vs. Bias Voltage

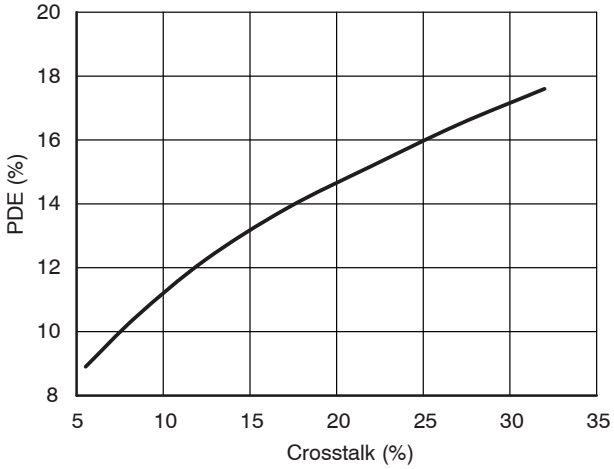


Figure 9. PDE at 905 nm vs. Crosstalk

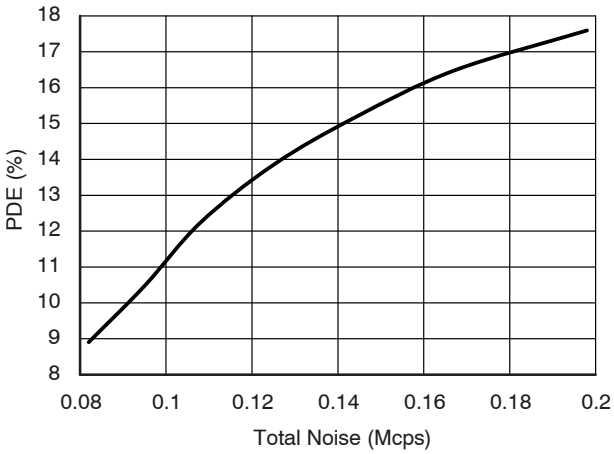


Figure 10. PDE at 905 nm vs. Total Noise (DCR per Channel)

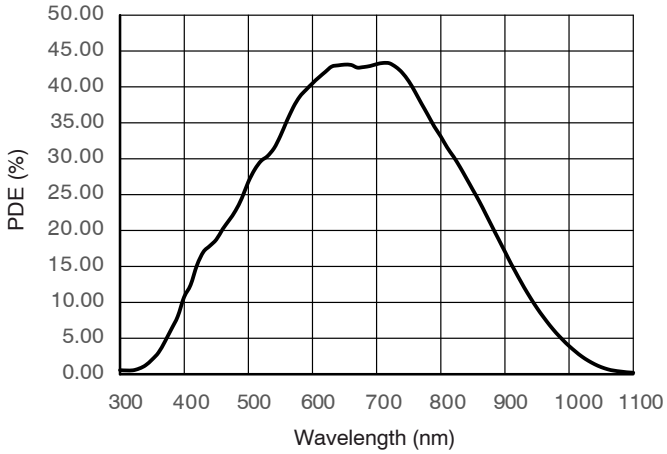


Figure 11. PDE vs Wavelength (21°C, Vop=29.5V)

EVALUATION BOARD

The ArrayRDM-0112A20-GEVB evaluation board consists of:

- ArrayRDM-0112A20-QFN SiPM array
- 12 U.FL connectors for access to each pixel cathode for signal readout
- An SMA connector for applying the bias to the common anode
- Bias filtering circuit
- Decoupling capacitors (12 x 10 nF and 4 x 100 nF decoupling capacitors from anode to ground – not shown)

This product allows users to quickly and easily set up an evaluation of the array product.

Note that a negative bias supply should be suppled via the SMA connector (J13) and the U.FL connectors (J1 to J12) should be 50 Ω terminated.

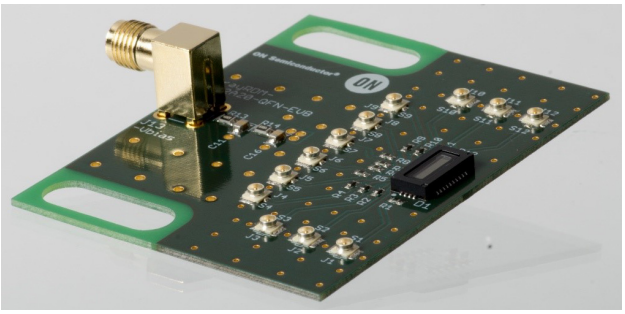


Figure 12. ArrayRDM-0112A20-GEVB Top Side View Showing the 1x12 Sensor

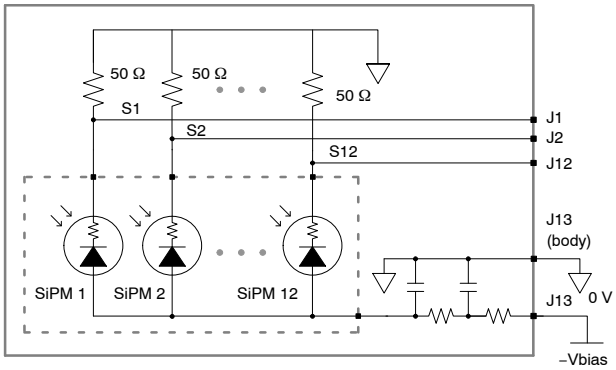


Figure 13. ArrayRDM-0112A20-GEVB Board Schematic

Connector	Style
J1–J12	U.FL Receptacle (Hirose U.FL-R-SMT)
J13	SMA Jack (F)

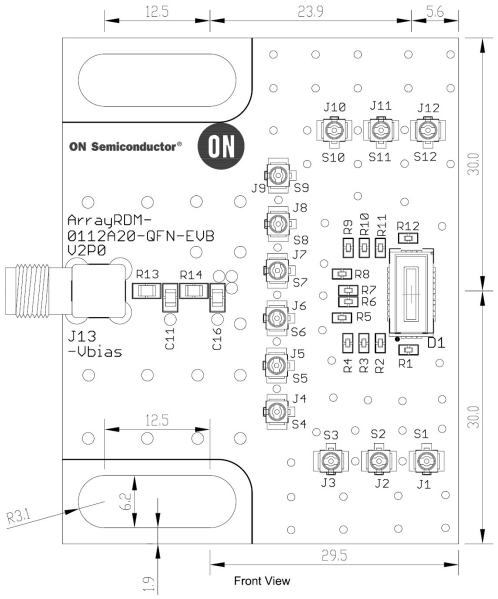
ORDERING INFORMATION

Table 8. ORDERING INFORMATION

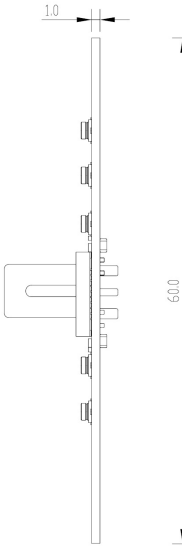
Part Number	Product Description	Shipping Format
ArrayRDM-0112A20-QFN-TR	Monolithic 1 × 12 array of NIR sensitive SiPM pixels formed using the RDM process. Individual cathode connection per pixel and a common anode available via the 28-pin QFN package.	Tape and Reel
ArrayRDM-0112A20-QFN-TR1		Cut Tape
ArrayRDM-0112A20-QFN-TR-E	Prototype sample	Cut Tape
ArrayRDM-0112A20-GEVB	Evaluation board consisting of an ArrayRDM-0112A20-QFN mounted onto PCB. A U.FL connector gives access to each pixel cathode and fast output. The bias is supplied via an SMA connector to the common anode.	ESD Package

NOTE: For sample information please contact **onsemi**.

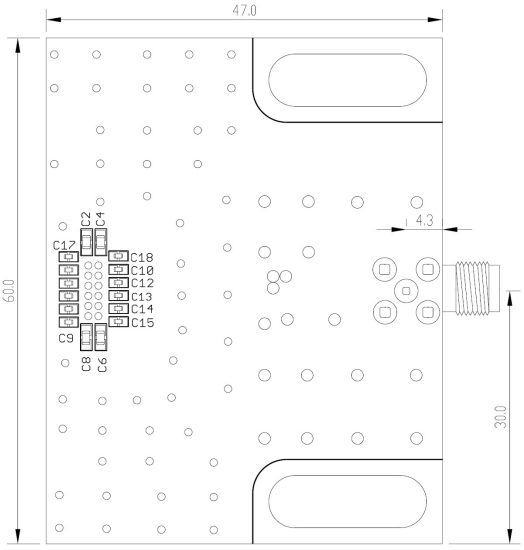
EVALUATION BOARD DRAWING



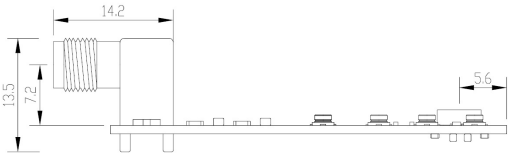
Front View



Side View

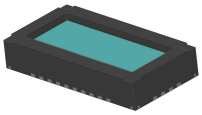


Back View



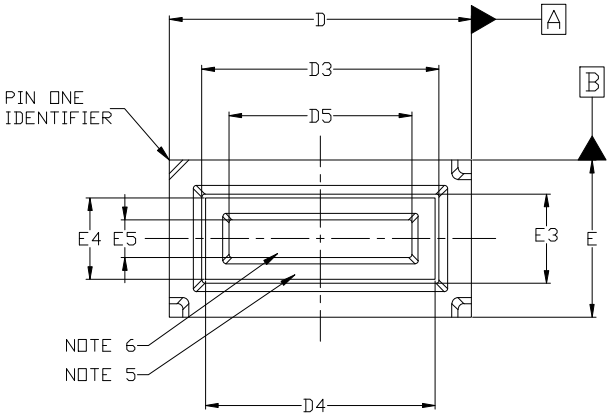
Side View

Connector	Signal Name	Description
J1	S1	Standard output 1
J2	S2	Standard output 2
J3	S3	Standard output 3
J4	S4	Standard output 4
J5	S5	Standard output 5
J6	S6	Standard output 6
J7	S7	Standard output 7
J8	S8	Standard output 8
J9	S9	Standard output 9
J10	S10	Standard output 10
J11	S11	Standard output 11
J12	S12	Standard output 12
J13	-Vbias	Negative Bias supply

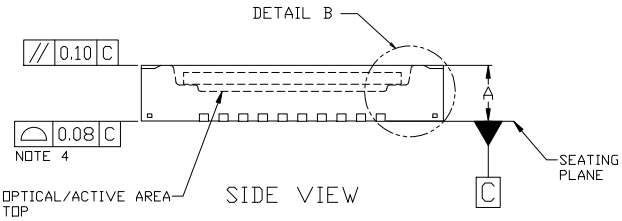


QFN28 10.00x5.20x1.85, 0.65P
CASE 485FZ
ISSUE F

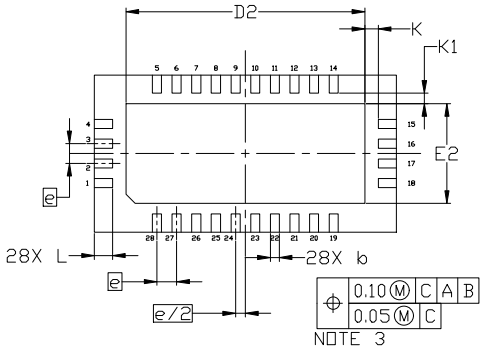
DATE 14 JUL 2023



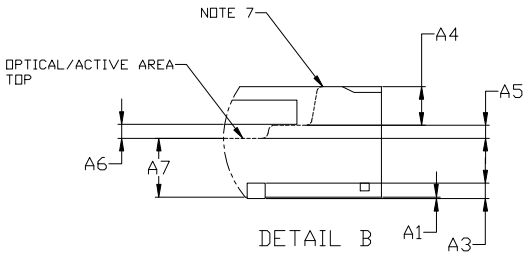
TOP VIEW



SIDE VIEW



BOTTOM VIEW

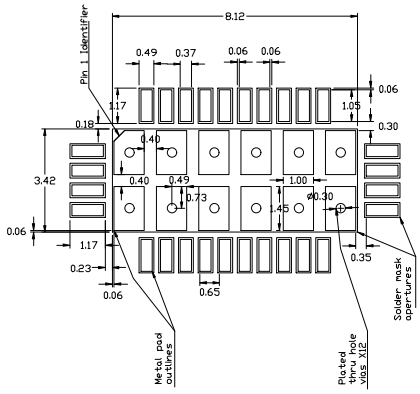


DETAIL B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. GLASS LID AREA, 0.4mm THICKNESS. DEFINED BY D4 & E4.
6. OPTICAL/ACTIVE AREA IS CENTERED.
   ALIGNMENT TO PACKAGE CENTER: +/- 0.05 mm
   ROTATION ALLOWED: +/- 0.5°
7. MOLD INNER CAVITY RADIUS AT 0.1mm AT 10° DRAFT ANGLE.
8. DIMENSION A6 MEASURES THE BOTTOM OF THE GLASS TO TOP OF DIE.
9. DIMENSION A7 MEASURES THE BOTTOM OF THE PACKAGE TO TOP OF DIE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.75	1.85	1.95
A1	0.00	---	0.05
A3	0.254 REF		
A4	0.594 REF		
A5	0.256 REF		
A6	0.270 REF		
A7	0.971	1.014	1.052
b	0.25	0.30	0.35
D	9.90	10.00	10.10
D2	7.80	7.90	8.00
D3	7.57 REF		

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
D4	7.32 REF		
D5	6.40 REF		
E	5.10	5.20	5.30
E2	3.20	3.30	3.40
E3	2.67 REF		
E4	2.42 REF		
E5	1.50 REF		
e	0.65 BSC		
K	0.45 REF		
K1	0.35 REF		
L	0.55	0.60	0.65



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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