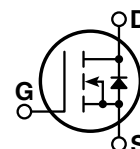
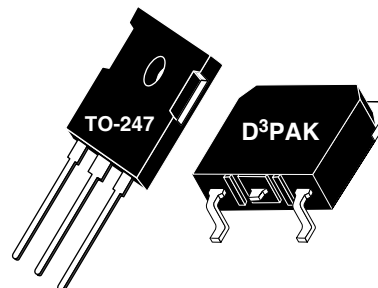


POWER MOS V®

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **TO-247 or Surface Mount**
- **Lower Leakage**
- **Surface Mount D³PAK Package**
- **100% Avalanche Tested**

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT1201R6BVR/SVR	UNIT
V_{DSS}	Drain-Source Voltage	1200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	8	Amps
I_{DM}	Pulsed Drain Current ^①	32	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	280	Watts
	Linear Derating Factor	2.24	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	8	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1200			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	10			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			1.600	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			25	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			250	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT1201R6BVR/SVR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		3050	3660	pF
C_{oss}	Output Capacitance			255	360	
C_{rss}	Reverse Transfer Capacitance			125	190	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$		155	230	nC
Q_{gs}	Gate-Source Charge			15	23	
Q_{gd}	Gate-Drain ("Miller") Charge			78	115	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6\Omega$		12	24	ns
t_r	Rise Time			10	20	
$t_{d(off)}$	Turn-off Delay Time			50	75	
t_f	Fall Time			15	30	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			8	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			32	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V$, $I_S = -I_{D[Cont.]}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D[Cont.]}$, $di_S/dt = 100A/\mu s$)		500		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -I_{D[Cont.]}$, $di_S/dt = 100A/\mu s$)		7		μC

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.45	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

③ See MIL-STD-750 Method 3471

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

④ Starting $T_J = +25^\circ C$, $L = 37.81mH$, $R_G = 25\Omega$, Peak $I_L = 8A$

APT Reserves the right to change, without notice, the specifications and information contained herein.

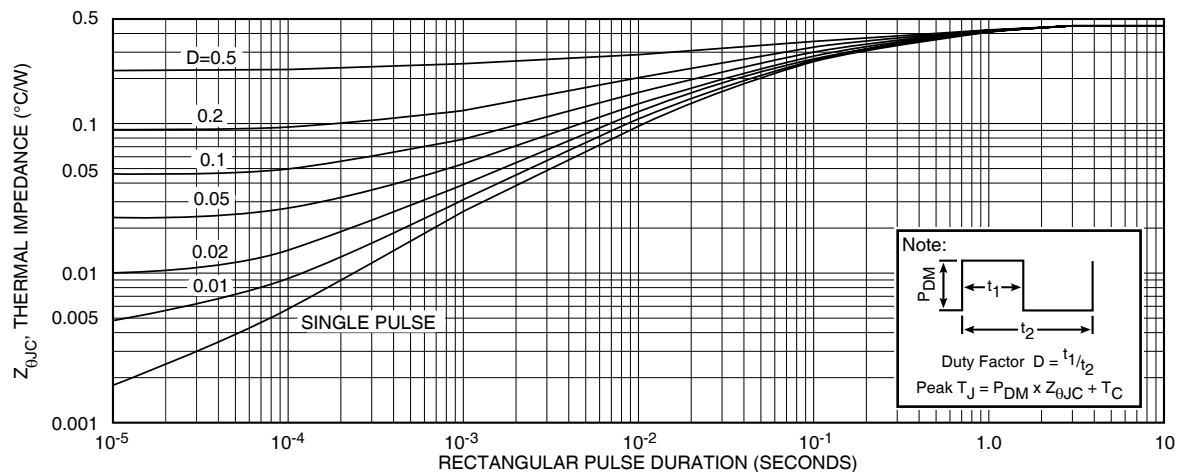


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

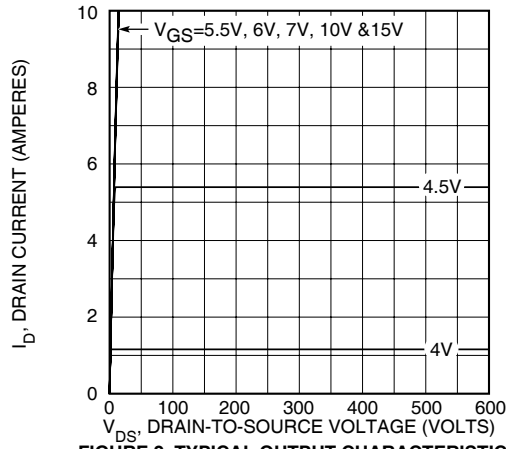


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

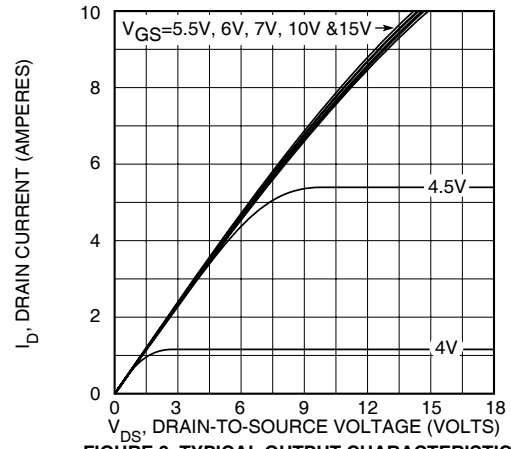


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

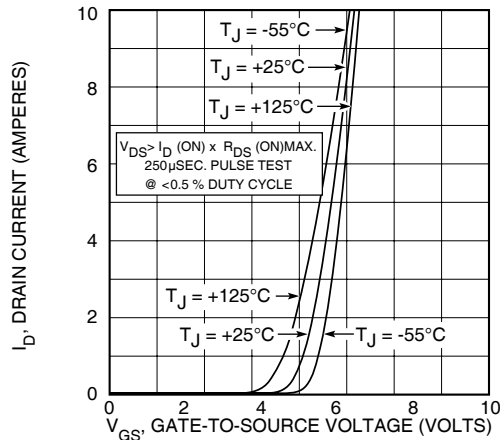


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

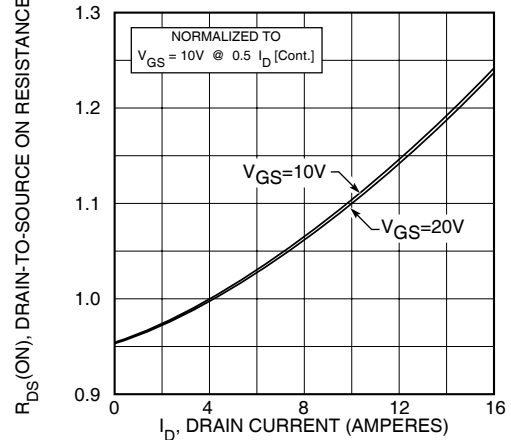


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

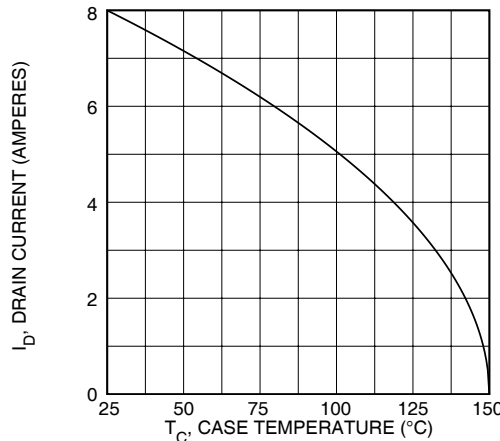


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

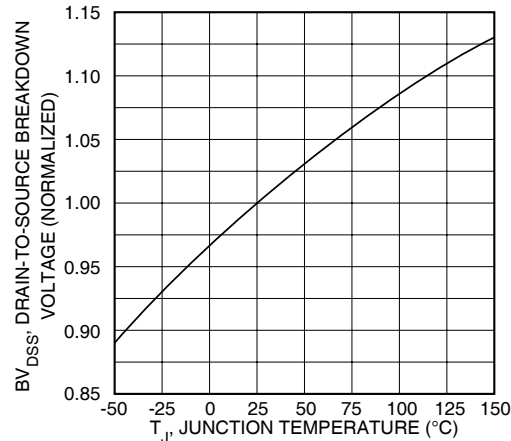


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

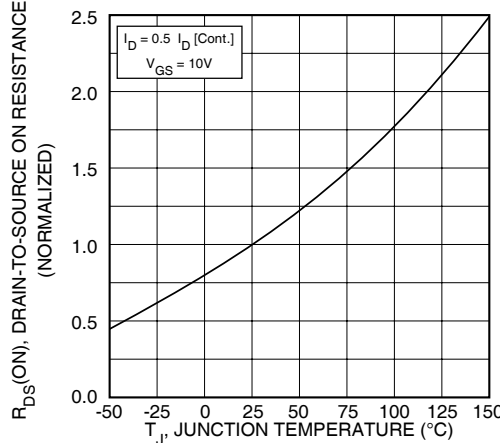


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

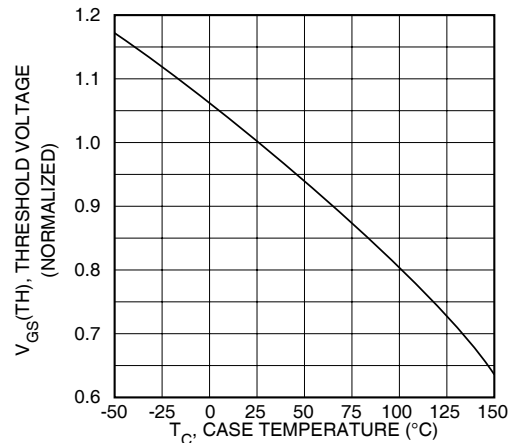


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

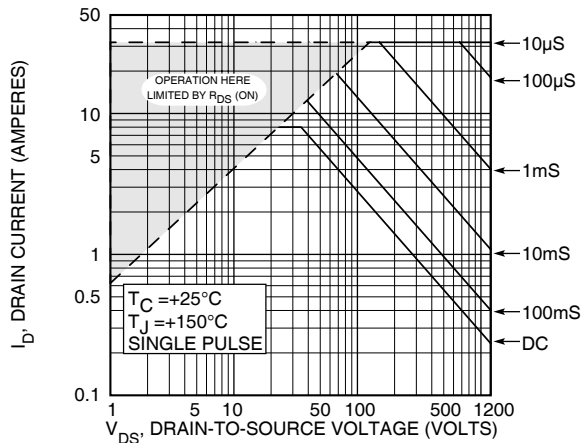


FIGURE 10, MAXIMUM SAFE OPERATING AREA

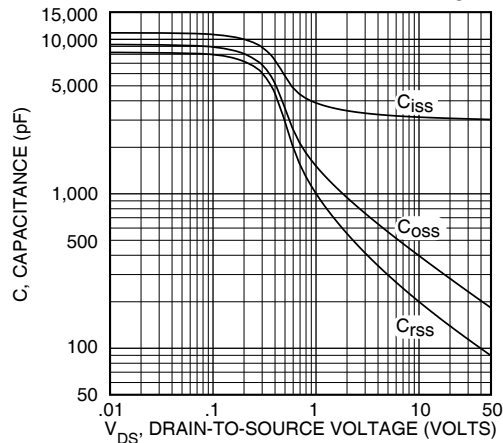


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

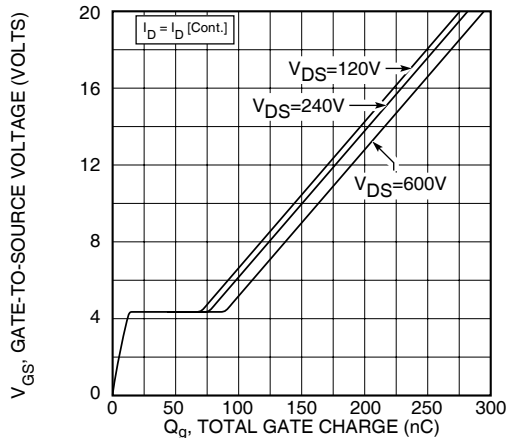


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

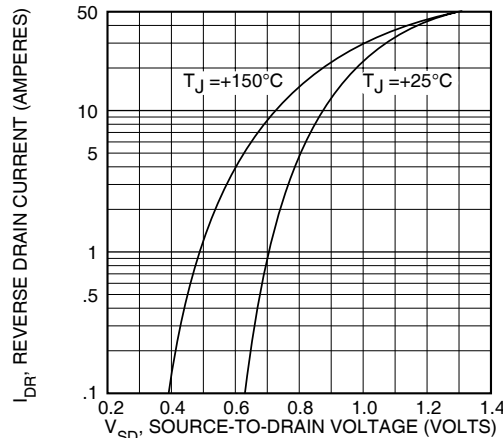
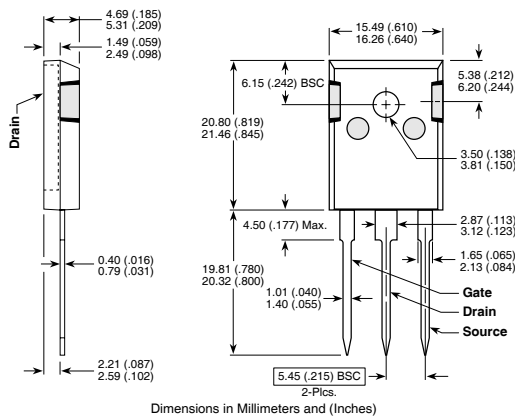


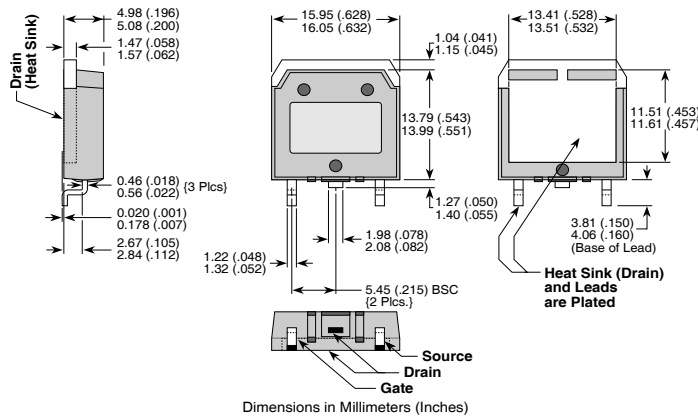
FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline



Dimensions in Millimeters and (Inches)

D³PAK Package Outline



Dimensions in Millimeters (Inches)

APT's devices are covered by one or more of the following U.S. patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058