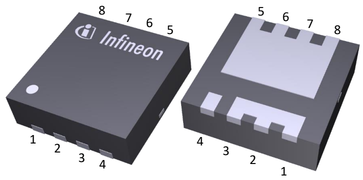
MOSFET

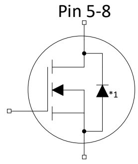
OptiMOS™ 7 Power-Transistor, 40 V

PG-TSDSON-8 FL



Features

- N-channel, normal level
- Enhanced SOA
- Drives optimized
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.55	mΩ
I_D	177	A
Q_{OSS}	47	nC
$Q_G(0V..10V)$	37	nC
$Q_{rr}(100A/\mu s)$	24	nC

Part number	Package	Marking	Related links
ISZ015N04NM7V	PG-TSDSON-8	15N04NM7	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	177	A	V_{GS}=10 V, T_C=25 °C
				125		V_{GS}=10 V, T_C=100 °C
				132		V_{GS}=15 V, T_C=100 °C
				32		V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	708	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	68	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	94	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3) See Diagram 3 for more detailed information

4) See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5)]	R_{thJA}	-	-	50	°C/W	-

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.35	2.75	3.15	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.19	1.40	mΩ	V_{GS}=15 V, I_D=50 A
			1.35	1.55		V_{GS}=10 V, I_D=50 A
Gate resistance	R_G	-	0.8	-	Ω	-
Transconductance	g_{fs}	-	100	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6)]	C_{iss}	-	2400	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance [6)]	C_{oss}		1300			
Reverse transfer capacitance [6)]	C_{rss}		30			
Turn-on delay time	$t_{d(on)}$	-	8.2	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		2.6			
Turn-off delay time	$t_{d(off)}$		13			
Fall time	t_f		4.5			

6) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		6.7	-	nC	
Gate to drain charge	Q_{gd}		8.2	-	nC	
Switching charge	Q_{sw}		14	-	nC	
Gate charge total [8)]	Q_g		37	46	nC	
Gate plateau voltage	$V_{plateau}$		5.1	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	34	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	47	-	nC	V_{DS}=20 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

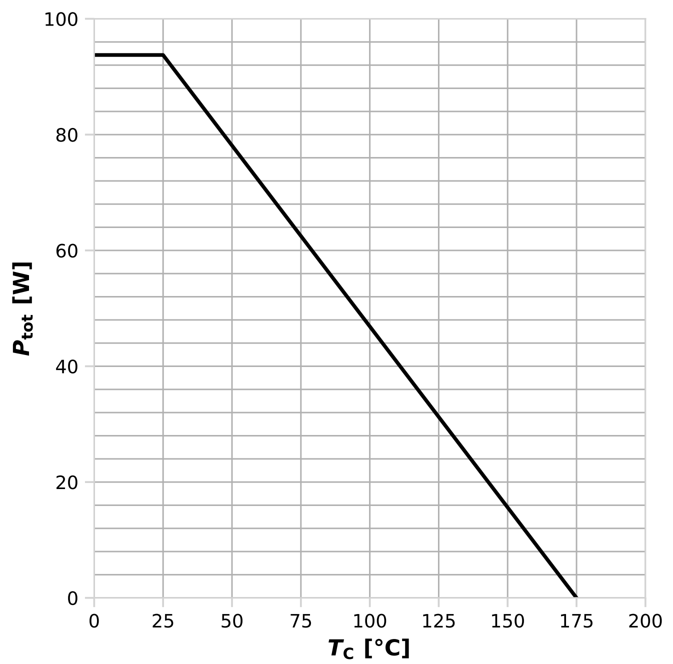
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	94	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			708		
Diode forward voltage	V_{SD}	-	0.83	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	34	-	ns	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		24		nC	

9) Defined by design. Not subject to production test.

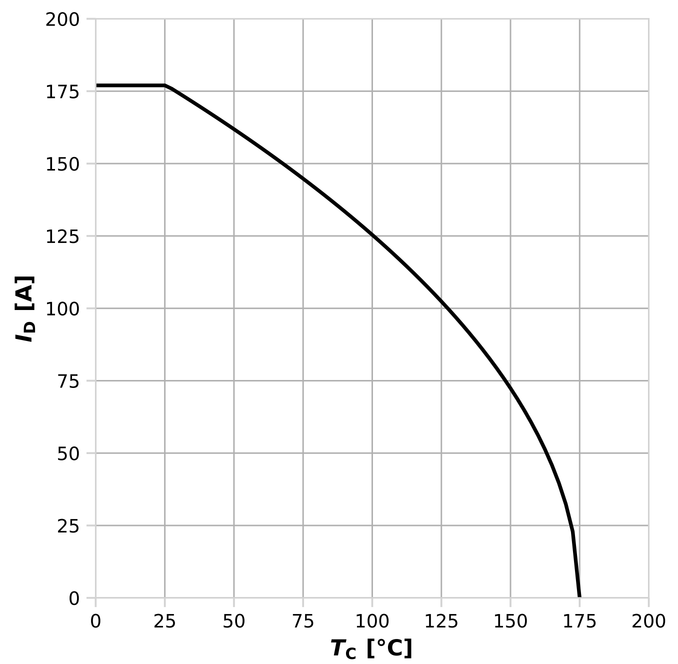
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



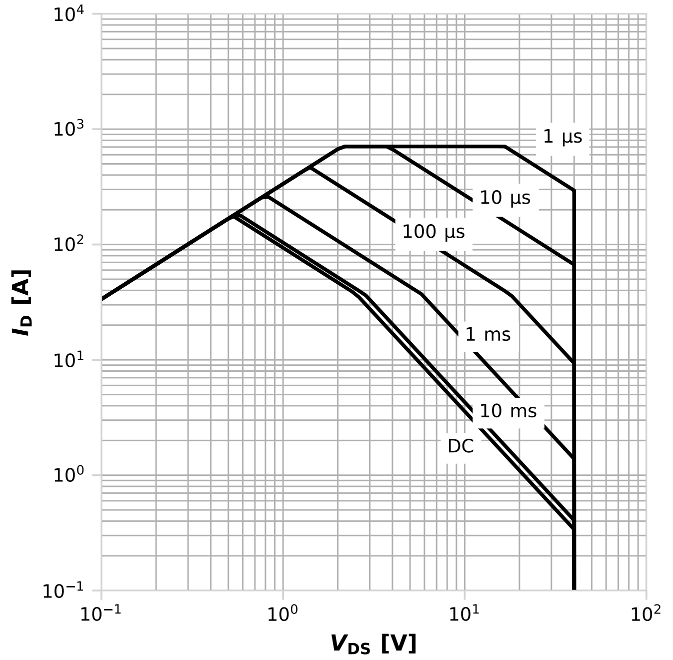
P_{tot}=f(T_C)

Diagram 2: Drain current



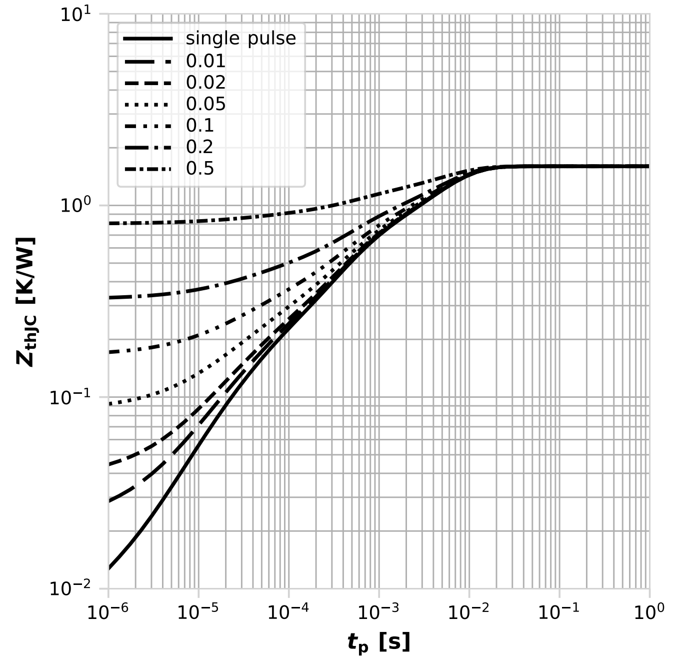
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



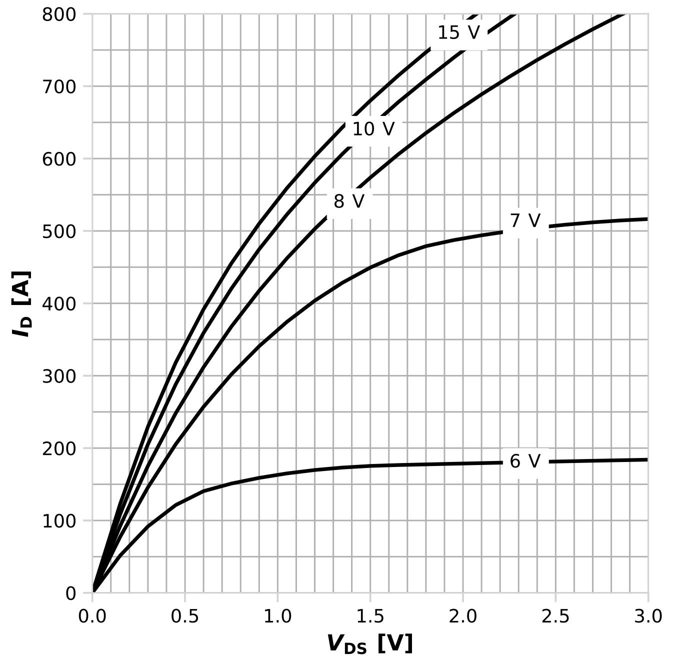
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



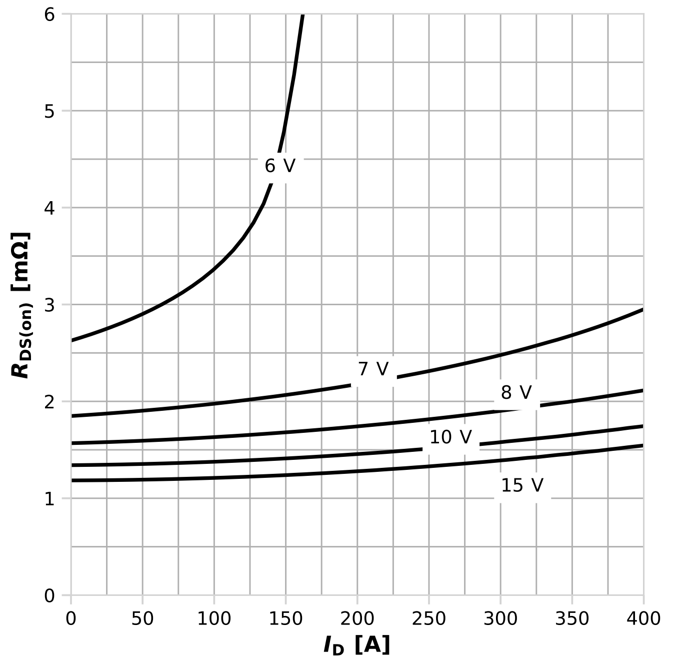
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



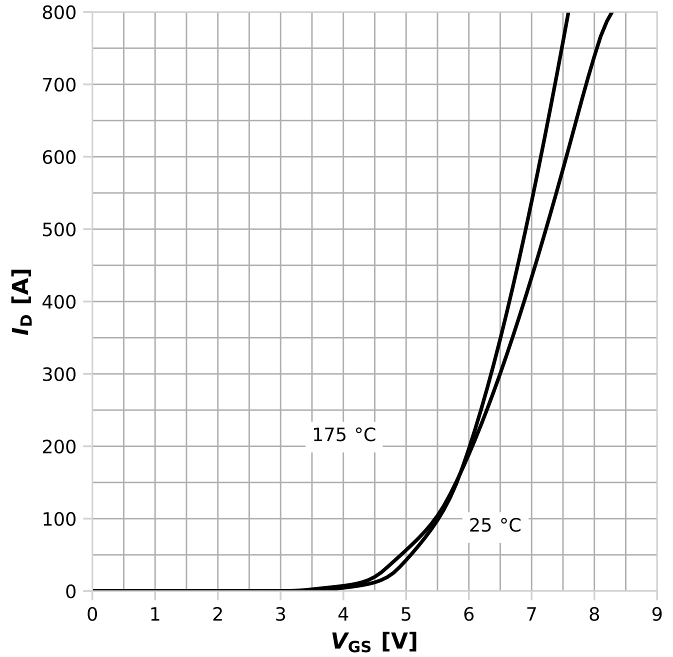
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



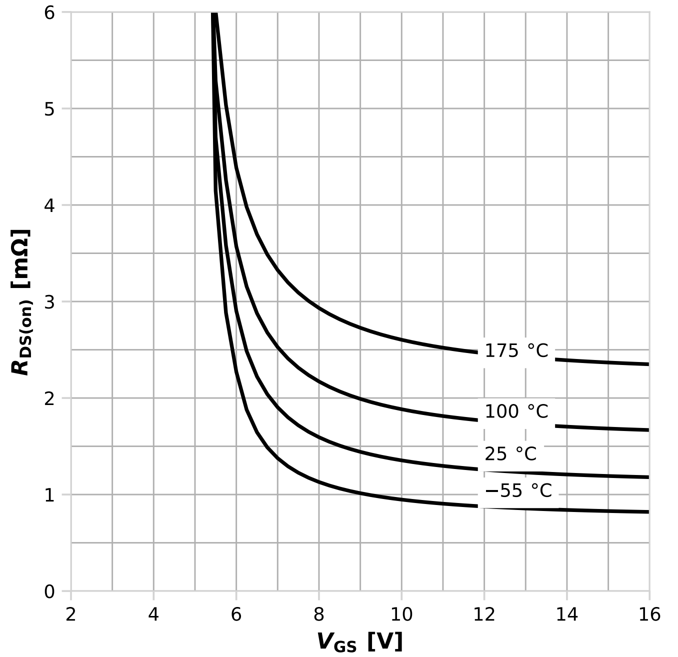
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



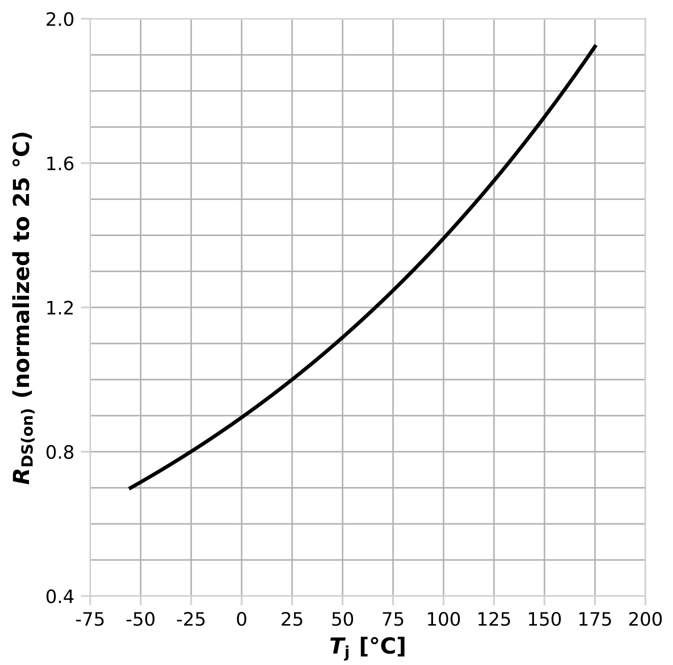
I_D=f(V_{GS}), $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



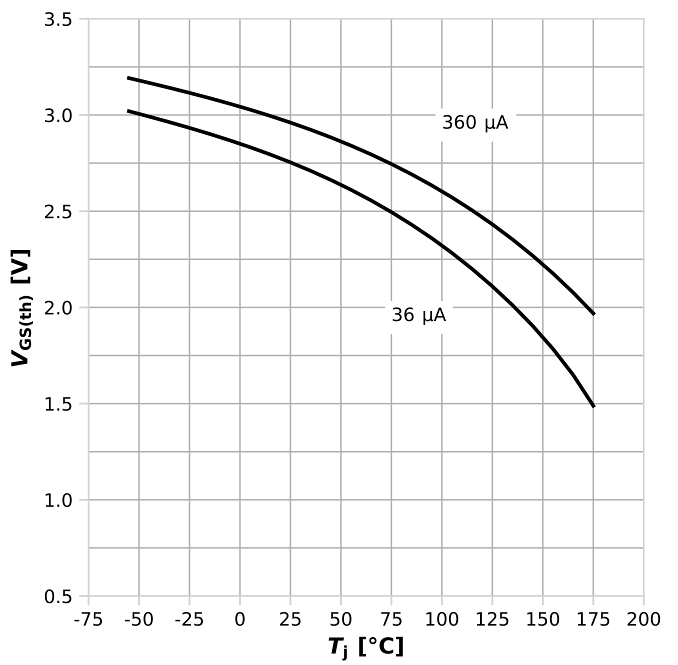
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



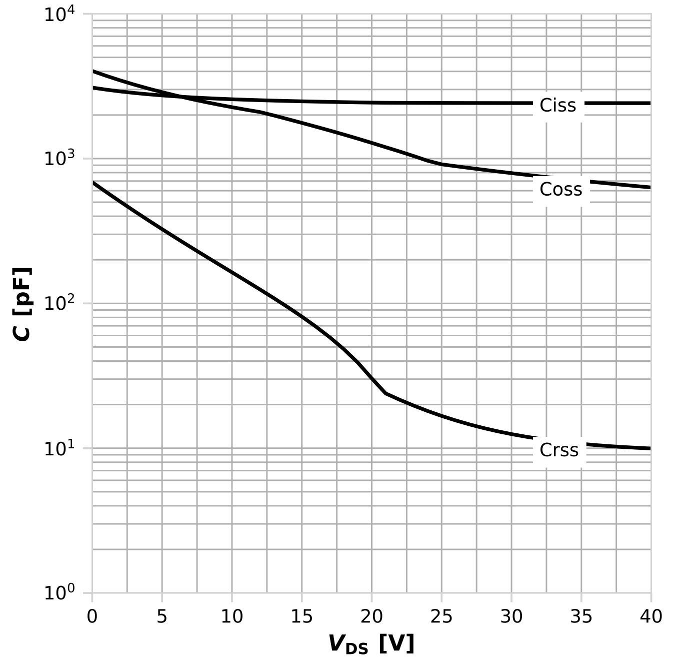
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



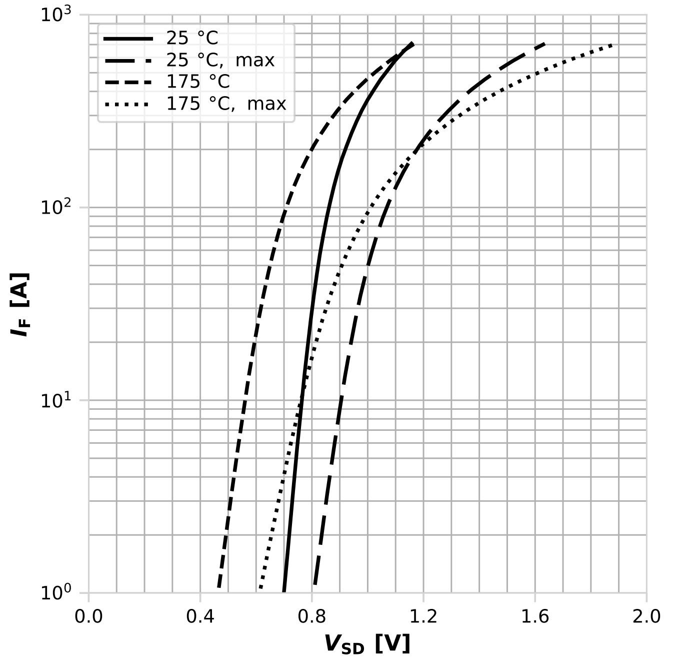
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

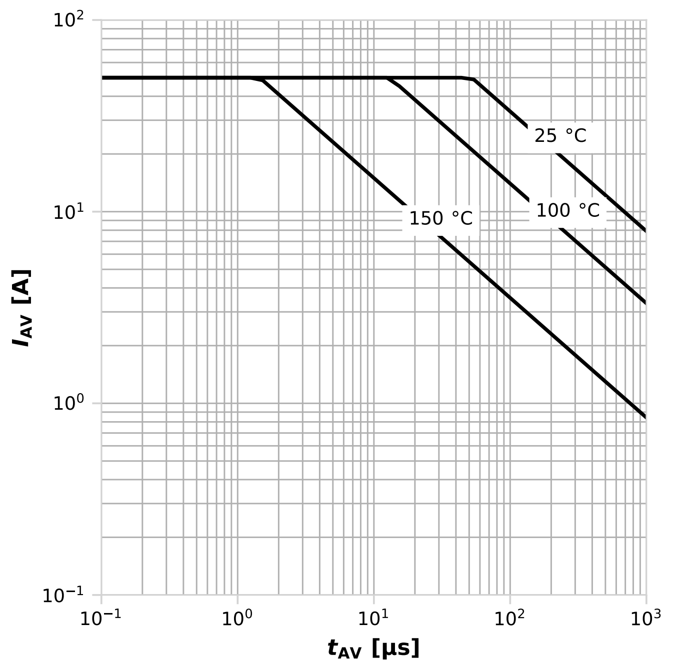
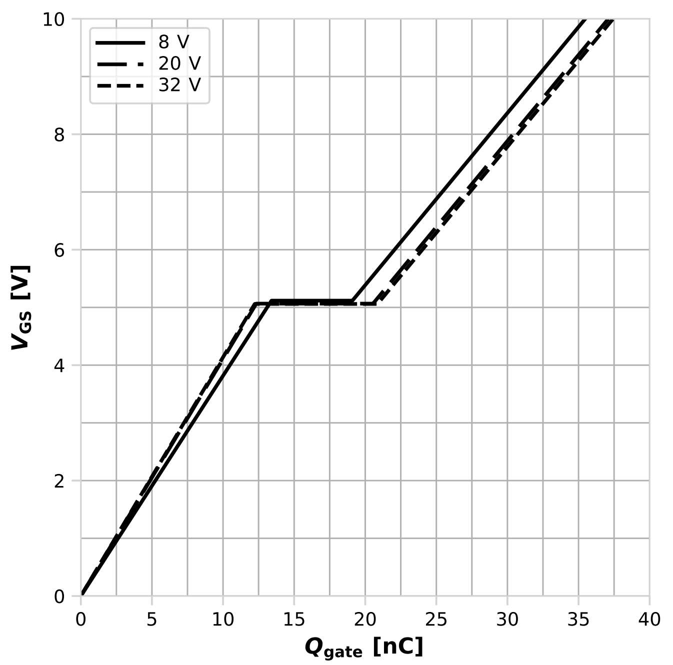
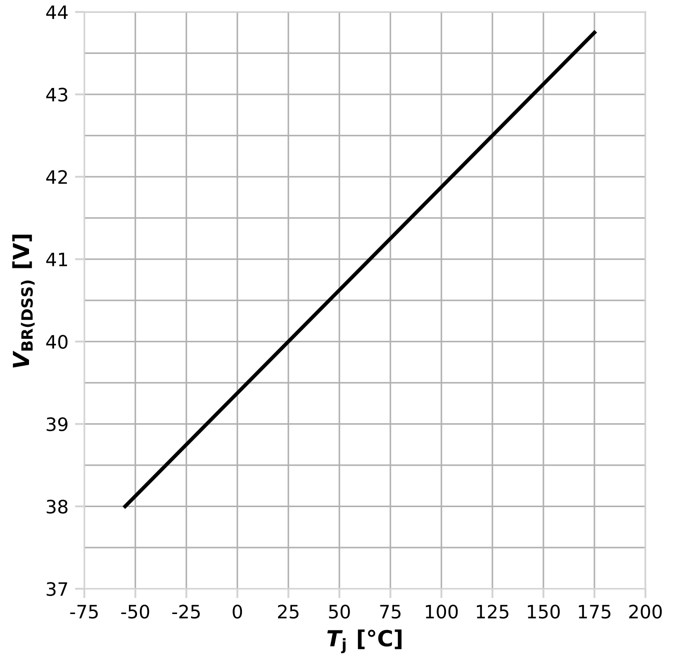
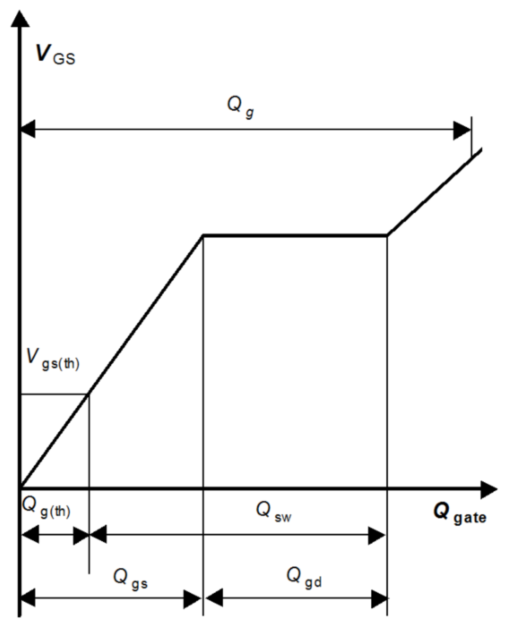
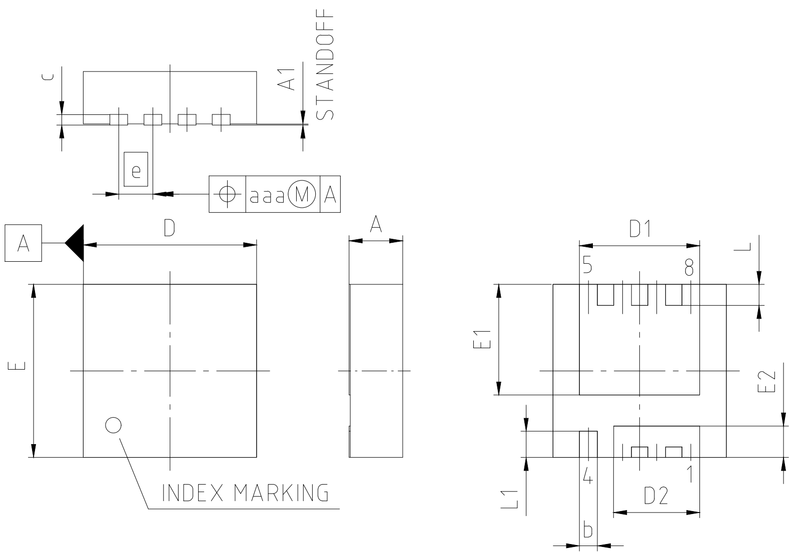
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	0.10	0.30
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.50	0.70
e	0.65	
L	0.30	0.50
L1	0.40	0.60
aaa	0.06	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSDSON-8, dimensions in mm

Revision history

ISZ015N04NM7V

Revision 2025-04-22, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-04-22	Release of final version

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