PI7C9X3G0000GPEVB

for

PI7C9X3G606GP
PI7C9X3G808GP
PI7C9X3G816GP
PI7C9X3G1224GP
PI7C9X3G1632GP

PCI EXPRESS GEN 3 PACKET SWITCH FAMILY
Evaluation Board
User's Manual

Version 0.1
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A Product Line of
Diodes Incorporated

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Table of Contents

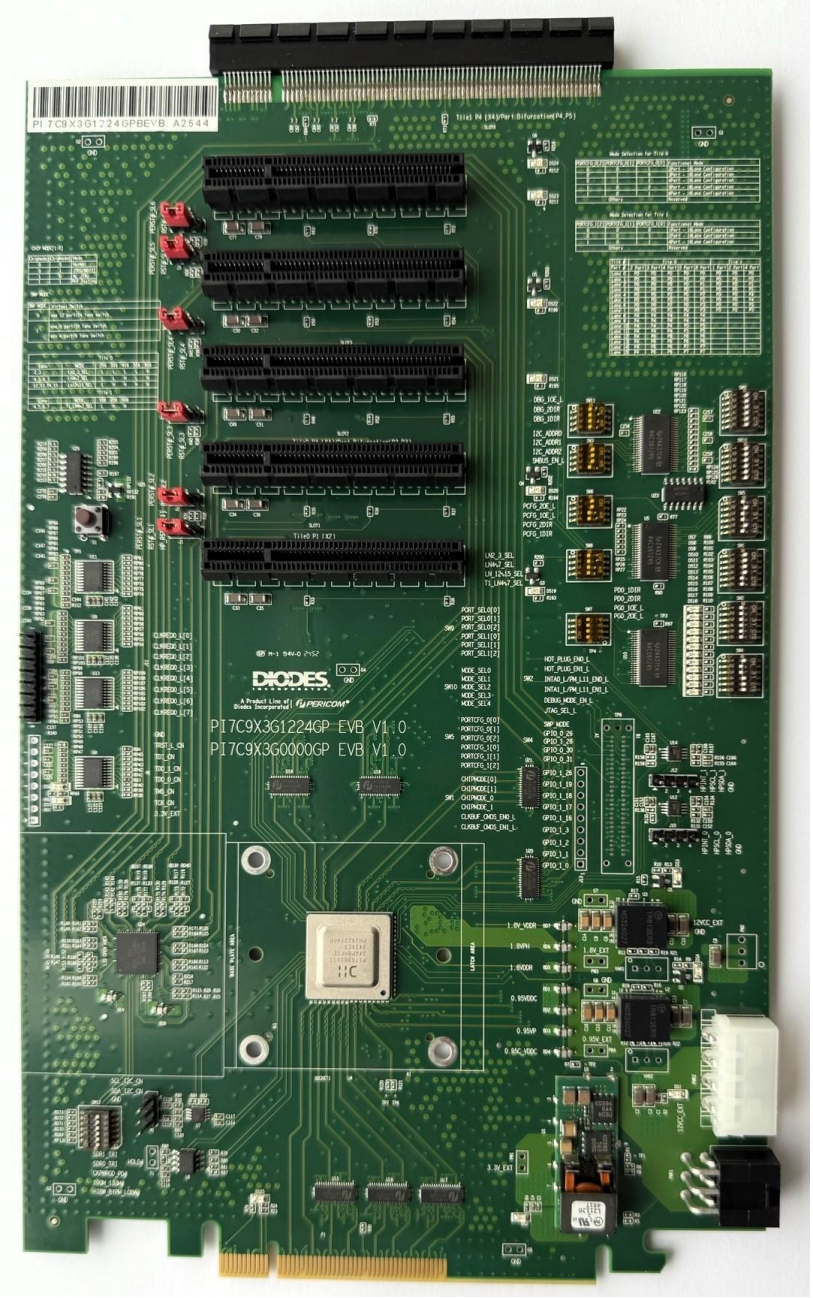
Tables

Figures

REVISION HISTORY

Date	Revision Number	Description
02/14/2025	0.1	PI7C9X3G0000GP EVB User's Manual

1 Packing List

Item	Unit	Illustration
Base board	1	

2 General Information

The DIODES™ PI7C9X3G0000GP EVB Board is for user to evaluate PI7C9X3G0000GP family include PI7C9X3G606GP, PI7C9X3G808GP, PI7C9X3G816GP, PI7C9X3G1224GP and PI7C9X3G1632GP that built on the PI7C9X3G1224GP, an 12Port-24Lane PCI Express GEN 3 Switch IC. The architecture of the PCIe packet switch allows flexible port configuration by allocating variable lane width for each port. A basic cell of the switch architecture is called a tile, which consists of 8 ports and 16 lanes for Tile 0, 4 ports and 8 lanes for Tile 1. The PI7C9X3G1224GP (the PCIe3 Packet Switch IC) is built with 2 tiles connected by internal signal paths. Each tile can be configured to have different port types such as upstream port and downstream ports to support various port configurations for fan-out application in single switch or dual-switch partition modes. Besides fan-out, there are some designated ports that can be programmed as Cross-Domain End-Point (CDEP) ports to allow multiple hosts connected to the switch for fail-over or multiple-host computation and communication applications. Inside the packet switch, multiple DMA channels are embedded to facilitate data communication more efficiently among hosts.

In addition, the PI7C9X3G0000GP Family offers some extra benefits such as "maintaining high signal integrity in stress channel", "advanced power management mechanism", "enhanced reliability, availability and serviceability (RAS)" and "Surprised Hot Plug with LED Enclosure Management".

2.1 PI7C9X3G0000GP Family Features

- PI7C9X3G000GP Family include product number of:
  - PI7C9X3G606GP (6-port/ 6-lane)
  - PI7C9X3G808GP (8-port/ 8-lane)
  - PI7C9X3G816GP (8-port/ 16-lane)
  - PI7C9X3G1224GP (12-port/ 24-lane)
  - PI7C9X3G1632GP (16-port/ 32-lane)
- Port and Lane Configurations for 6-16 ports/ 6-32 Lanes PCI Express GEN3 packet switch
  - Configurable Upstream port number up to 2
  - Configurable Upstream Lane widths of x1, x2, x4, x8 or x16
  - Configurable Downstream port number up to 15
  - Configurable Downstream Lane widths of x1, x2, x4, x8 or x16
- Reference Clock Management
  - Integrated PCIe Gen3 clock buffer for all downstream ports
  - Support three reference clock structures (Common, SRNS and SRIS)
  - Handle SSC Isolation up to three ports
  - Provide two clock application modes (Base and CDSR)
- Power Management
  - Support 7 power states (P0/P0s/P1/P1.1/P1.2/P2/P1.2PG)
  - Start-up power management scheme
    - "Empty" Hot-Plug ports put in P2 state
  - Continuous power management scheme
    - Support ASPM L1 Sub-state (P1.1/P1.2)
- PHY and MAC Layers
  - PHY initial settings optionally programmable through JTAG, EEPROM, and SMBus/I^2C
  - Adaptive Continuous Time Linear Equalizer and 5-tap Decision Feedback Equalizer for RX
  - Adaptive and programmable 3-tap TX equalization
  - RX Polarity Inversion and Lane Reversal
- Data Link Layer
  - Programmable ACK latency timer to respond ACK based upon traffic condition

- Configurable Flow Control Credit to balance bandwidth utilization and buffer usage
- Transaction Layer
  - Packet forwarding options including Cut-Through and Store & Forward
  - Support up to 512-Byte Max Payload Size
  - Low packet forwarding latency < 150ns (typical case)
  - Access Control Service (ACS) for peer-to-peer traffic
  - Address Translation (AT) packet for SR-IOV application
  - Support Atomic operation
  - Support Multicast
  - Provide Performance Visibility for ingress/egress packet types and packet counts
- Multi-Host Application
  - Support up to 3 Cross-Domain End-Point (CDEP) ports for Host-to-Host Communications
  - Support Fail-over using CDEP port
  - Provide up to 8 physical or 16 virtual DMA channels enabling communications among Hosts and EPs
  - Switch bifurcated up to 2 individual packet switches to allow 2 hosts operating independently
- Reliability, Availability and Serviceability
  - Enhanced Advanced Error Reporting
  - End-to-End Data Protection with ECC
  - Error Handling Mechanism
  - Support Surprise Hot Removal
  - Support Downstream Port Containment (DPC)
  - Support Hot Plug for Upstream and Downstream port
  - Provide Serial and Parallel Hot Plug Types
  - Support LED Management
  - Thermal Sensor reporting operational temperature instantly
  - IEEE 1149.1 and 1149.6 JTAG interface support
- Advanced Diagnostic Tools
  - PHY Eye™
  - MAC Viewer™ (including embedded LA)
  - PCIBUDDY™
  - On-Line PRBS loopback test
  - On-Line Compliance pattern test
- Side-band Management Interface
  - I2C/SMBUS/JTAG
  - SPI EEPROM
- Standard Compliance
  - Compliant with PCI Express Base Specification Revision 3.1
  - Compliant with PCI Express CEM Specification Revision 3.0
  - Compliant with Advanced Configuration Power Interface (ACPI) Specification
  - Compliant with System Management (SM) Bus, Version 2.0
- Power
  - Two power rails (0.95V and 1.8V)
  - Power consumption: Refer to Datasheet
  - Totally Lead-Free & Fully RoHS Compliant
  - Halogen and Antimony Free. "Green" Device
  - For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Package
  - 144 FCCSP 10 x 10mm (3G606GP)

- 196 FCBGA 15 x 15mm (3G808GP)
- 324 FCBGA 19 x 19mm (3G816GP/ 3G1224GP)
- 676 FCBGA 27 x 27mm (3G1632GP)

- Operating Ambient Temperature
  - Support Industrial Temperature Range -40° to 85°C (Note 5)

2.2 PI7C9X3G0000GP EVB Board Features

- PERICOM PI7C9X3G1224GP PCI Express switch IC in a 324-ball Plastic BGA package
- Based on PCI Express Card Electromechanical (CEM) Specification CEM 3.0 and PCI Express External Cabling Specification 1.0
- Tile0 supports up to 5 different port configurations
- Tile1 supports up to 3 different port configurations
- T0P2/P3(SLOT2),T0P4/P5(SLOT3),T0P6/P7(SLOT4),T1P0/P1(SLOT5),T1P4/P5(SLOT6) each share one PCIE slot and with PCIE to M.2 Adapter implementation x2 link(516/816_408mode)
- In system programmable Serial EEPROM
- Provides the I2C/MSBUS interface
- DIP switches for configuration
- Manual push-button PERST# capability
- Up to twelve LEDs for visual inspection of link speed and status for each port

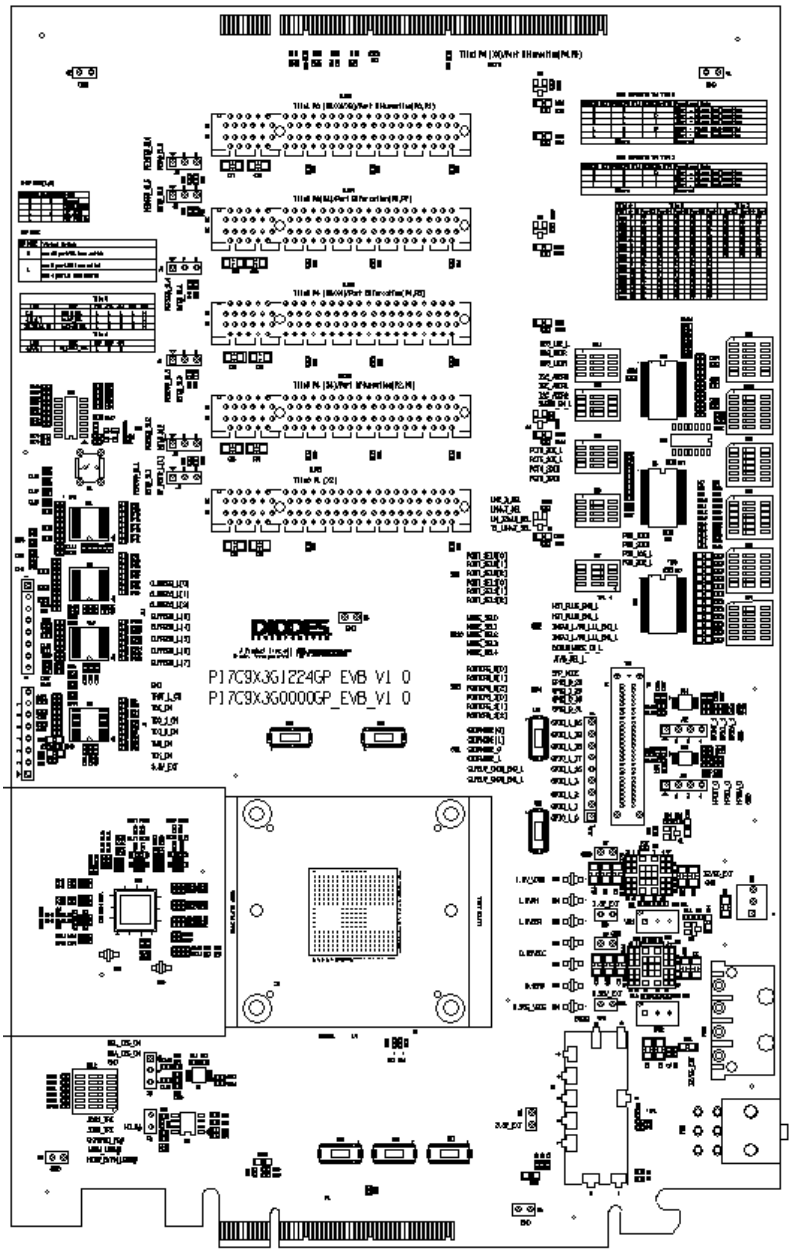


Figure 2-1 PI7C9X3G0000GP EVB Front View

3 Hardware Architecture and Interfaces

The PI7C9X3G0000GP EVB Board is designed around the PI7C9X3G1224GP, a 12-port 24-lane GEN 3 switch IC, and based on the PCI Express CEM 3.0 Specification. The EVB Board offers a 2/4/8-lane upstream port, five x8 PCI Express slot, and one x16 PCI Express slot. The EVB Board includes two tiles. Tile 0 can be configured into 2 Ports, 3 Ports, 4 Ports and 8 Ports across 16 lanes, and Tile 1 can be configured into 1 Port, 2 Ports and 4 Ports across 8 lanes, by employing PORTCFG_x[2:0] pins, where x= 0 and 1. (see Table 3-1/ Table 3-2 for details) and to connect to its upstream PC through Golden finger. It also provides visual indications for power, link speed, port

status, and port number.

Table 3-1 Mode Selection for Tile 0

PORTCFG_0[2]	PORTCFG_0[1]	PORTCFG_0[0]	Functional Mode
0	0	1	2Port-16Lane Configuration
0	1	0	3Port-16Lane Configuration
0	1	1	4Port-16Lane Configuration
1	0	0	5Port-16Lane Configuration
1	0	1	8Port-16Lane Configuration
Others			Reserved

Table 3-2 Mode Selection for Tile 1

PORTCFG_0[2]	PORTCFG_0[1]	PORTCFG_0[0]	Functional Mode
0	0	0	1Port-8Lane Configuration
0	0	1	2Port-8Lane Configuration
1	0	1	4Port-8Lane Configuration
Others			Reserved

3.1 Power Distribution Circuits

To support the power of the EVB Board and the power of the PCI Express add-in cards plug into up to each connector, an external ATX power supply is required. Refer to Figure 3-1, the EVB Board has two different ATX power connectors for power connections. These include one 4-pin Peripheral Power Connectors, and one 6-pin +12V Power Connector.

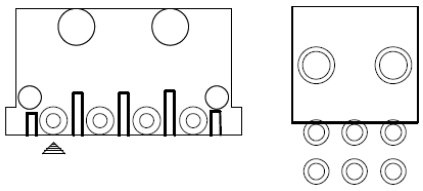
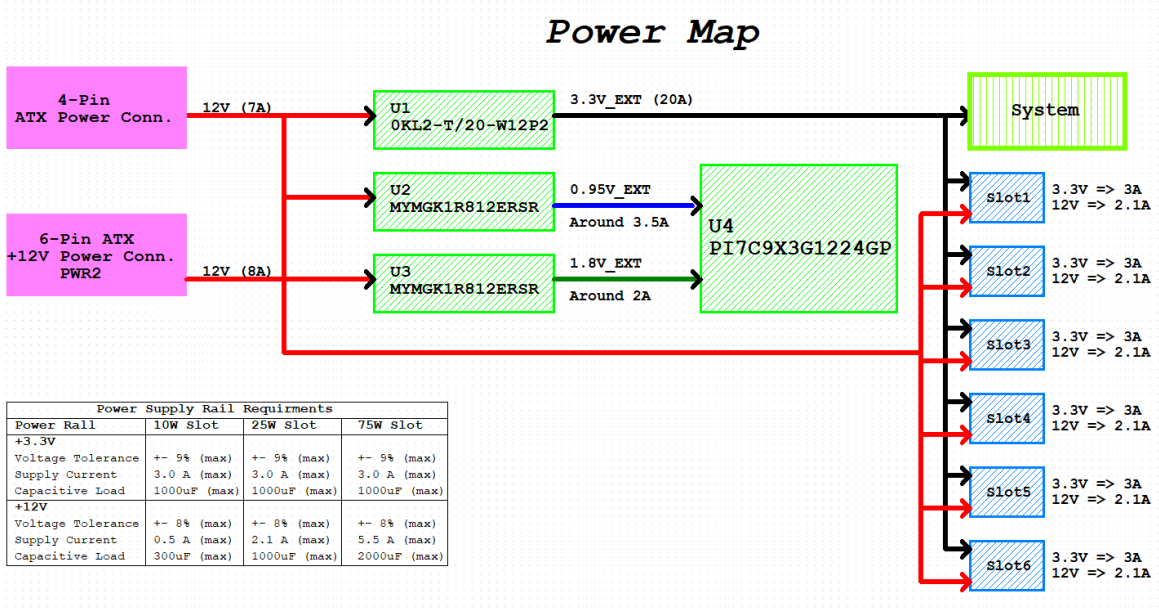


Figure 3-1 Power Connectors

The 6-pin +12V Power Connector should be connected and one 4-pin ATX Peripheral Power Connectors should be connected depending on the power consumption requirements of the PCI Express add-in cards plugging into the PCI Express slots of the EVB Board.



Power Supply Rail Requirments			
Power Rail	10W Slot	25W Slot	75W Slot
+3.3V			
Voltage Tolerance	+- 9% (max)	+- 9% (max)	+- 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000uF (max)	1000uF (max)	1000uF (max)
+12V			
Voltage Tolerance	+- 8% (max)	+- 8% (max)	+- 8% (max)
Supply Current	0.5 A (max)	2.1 A (max)	5.5 A (max)
Capacitive Load	300uF (max)	1000uF (max)	2000uF (max)

Figure 3-2 EVB Board Power Distribution Circuits

Refer to Figure 3-2, 6 PCI Express slots get 3.3 volt and 12 volt power from both 4-pin Power Connectors, and 6-pin +12V Power Connector. PI7C9X3G0000GPEVB also gets their power from the both Power Connectors. Different DC/DC converter uses 12V input generates 3.3V_EXT, 1.8V_EXT, and 0.95V_EXT to the on-board circuit.

4 On-Board LED Indicators, Connectors, Switches, and Jumpers

4.1 LED Indicators

The EVB provides several LEDs for power indicators, Hot-Plug output indicators, link speed/status, port numbers and link width of each port. All LED indicators and their associated functions are described in the Table 4-1 below.

Table 4-1 LED Indicator Descriptions

Indicator Type	Locations	LED Functions
Power LEDs/red color	DS1	On：12VCC_EXT is applied to the EVB from the ATX power supply
	DS2	On：3.3V_EXT is applied to the EVB from the ATX power supply
	DS3	On：1.8V_EXT is applied to the EVB from the ATX power supply
	DS4	On：0.95V_EXT is applied to the EVB from the ATX power supply
	DS25(Green)	On：3.3VAUX is applied to the EVB from the P1(Golden finger)
Port Link Status and Speed LEDs / Green color	DS7	Used to indicate the link status for Tile0 P0 LED off：link down or no connected or no configured LED on：link up with GEN 3 speed (8Gbps) LED blinking：link up with GEN 1 speed (2.5Gbps) LED blinking fast：link up with GEN 2 speed (5Gbps)
	DS8	Used to indicate the link status for Tile0 P1
	DS9	Used to indicate the link status for Tile0 P2
	DS10	Used to indicate the link status for Tile0 P3
	DS11	Used to indicate the link status for Tile0 P4
	DS12	Used to indicate the link status for Tile0 P5
	DS13	Used to indicate the link status for Tile0 P6
	DS14	Used to indicate the link status for Tile0 P7
	DS15	Used to indicate the link status for Tile1 P0
	DS16	Used to indicate the link status for Tile1 P1
	DS17	Used to indicate the link status for Tile1 P4
	DS18	Used to indicate the link status for Tile1 P5
Fatal Error LED	DS5/DS6	When Advanced Error happens
SLOT LEDs /blue color	DS19~DS24	On: slot is configure by PORTCFG_x[2:0]

4.2 Connector Ports

The EVB provides six downstream PCI Express ports to enable connections for PCIE end devices.

Table 4-2 Connector Port

Connector	Function
P1	X8 (216-Mode, 316-Mode, and 516 Mode) upstream PCI Express Tile0 Port 0 X4 (416-Mode) upstream PCI Express Tile0 Port 0 X2 (816-Mode) upstream PCI Express Tile0 Port 0 Connects to the Root Complex.
SLOT1	X2 (816-Mode) downstream PCI Express Tile0 Port 1 Connects to a PCI Express end device
SLOT2	X4 (316-mode and 416-Mode) downstream PCI Express Tile0 Port 2 X2 (816-Mode) downstream PCI Express Tile0 Port 2 and Port3 Connects to a PCI Express end device

Connector	Function
SLOT3	X8 (216-Mode) downstream PCI Express Tile0 Port 4 X4 (316-Mode and 416-Mode) downstream PCI Express Tile0 Port 4 X2 (516-Mode and 816-Mode) downstream PCI Express Tile0 Port 4 and Port5 Connects to a PCI Express end device
SLOT4	X4 (316-Mode and 416-Mode) downstream Tile0 PCI Express Port 6 X2 (816-Mode) downstream PCI Express Tile0 Port 6 and Port7 Connects to a PCI Express end device
SLOT5	X8 (108-Mode) downstream PCI Express Tile1 Port 0 X4 (208-Mode) downstream PCI Express Tile1 Port 0 X2 (408-Mode) downstream PCI Express Tile1 Port 0 and Port1 Connects to a PCI Express end device
SLOT6	X4 (208-Mode) downstream PCI Express Tile1 Port 4 X2 (408-Mode) downstream PCI Express Tile1 Port 4 and Port5 Connects to a PCI Express end device

4.3 DIP Switches

The PI7C9X3G0000GP EVB Board contains several DIP switches for various functions. Refer to Figure 4-1, the dip switches are distributed in three areas.

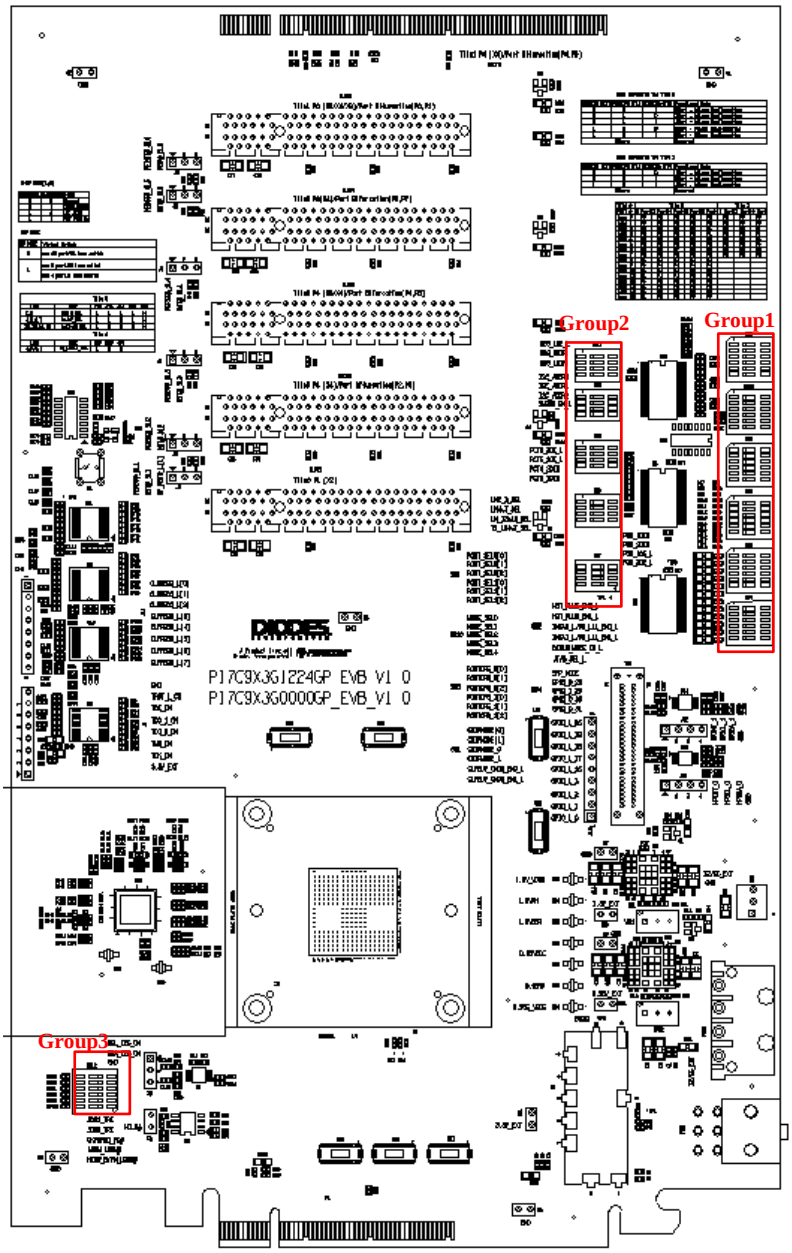
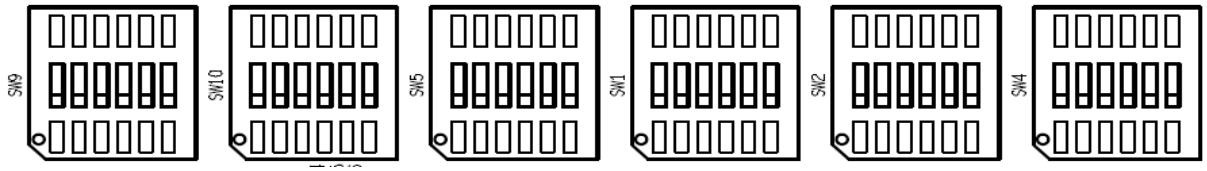


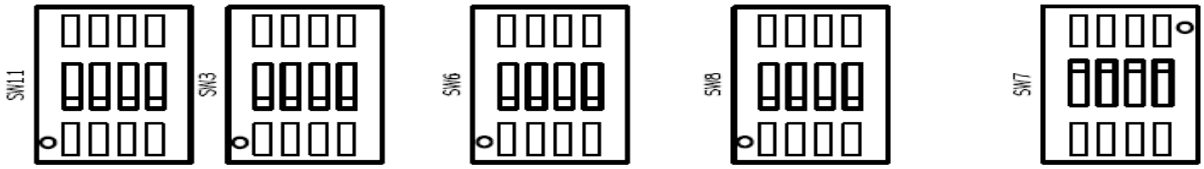
Figure 4-1 DIP Switches Area

4.3.1 *Dip Switch*

Group1



Group2



Group3

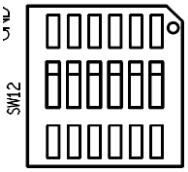


Figure 4-2 DIP Switches

Table 4-3 describes the functions of each switch.

Table 4-3 Functional Descriptions of Dip Switches

<table>
<tr><th>Name</th><th>Function</th><th>Setting</th></tr>
<tr><td>SW1</td><td>CHIPMODE[1:0]
CKMODE_0
CKMODE_1
CLKBUF_CMOS_EN0_L
CLKBUF_CMOS_EN1_L</td><td>Default：on, on, on, on, off, off (000011)
1. CHIPMODE[0]：Chip Operational Mode
2. CHIPMODE[1]：Chip Operational Mode
<table>
<tr><th>CHIP_MODE[1:0]</th><th>Operational Mode</th></tr>
<tr><td>00</td><td>Normal</td></tr>
<tr><td>01</td><td>IDDQ/MBIST</td></tr>
<tr><td>10</td><td>AC JTAG</td></tr>
<tr><td>11</td><td>PHY Testing</td></tr>
</table>
3. CKMODE_0：Clock Operational Mode
4. CKMODE_1：Clock Operational Mode
<table>
<tr><th>CKMODE_x</th><th>Operational Mode</th></tr>
<tr><td>0</td><td>BASE</td></tr>
<tr><td>1</td><td>CDSR</td></tr>
</table>
5. CLKBUF_CMOS_EN0_L：Internal Reference Clock Input Select
6. CLKBUF_CMOS_EN1_L：Internal Reference Clock Input Select
<table>
<tr><th>CLKBUF_CMOS_ENx_L</th><th>Operational Mode</th></tr>
<tr><td>0</td><td>CMOS</td></tr>
<tr><td>1</td><td>HCSL</td></tr>
</table>
Note：Default set Normal mode / BASE mode / HCSL mode</td></tr>
</table>

<table>
<tr><td>SW2</td><td>HOT_PLUG_EN0_L
HOT_PLUG_EN1_L
INTA0_L / PM_L11_EN0_L
INTA1_L
Debug_Mode_EN_L
JTAG_SEL_L</td><td>Default：off, off, off, off, off, off (111111)
1. HOT_PLUG_EN0_L：Hot Plug Function Enable (Active LOW)
2. HOT_PLUG_EN1_L：Hot Plug Function Enable (Active LOW)
3. INTA0_L / PM_L11_EN0_L：PM L1.1 Function Enable for Tile 0 (Active LOW)
4. INTA1_L：Interrupt Output Enable
5. Debug_Mode_EN_L：Debug Mode Enable (Active LOW)
6. JTAG_SEL_L：JTAG Selection (Active LOW)</td></tr>
<tr><td>SW3</td><td>I2C_ADDR[2:0]
SMBUS_EN_L</td><td>Default：on, on, on, off (0001)
1. I2C_ADDR[0]：SMBUS/I2C Slave Address
2. I2C_ADDR[1]：SMBUS/I2C Slave Address
3. I2C_ADDR[2]：SMBUS/I2C Slave Address
4. SMBUS_EN_L：System Manage Bus Enable (Active LOW)</td></tr>
<tr><td>SW4</td><td>SWP_MODE
CKBUFPD0_L
CKBUFPD1_L
PHY_SRAM_BYPASS
SURPRISE_HP_0</td><td>Default：on, off , off , on , off , (01101)
1. SWP_MODE：Switch Partition Mode
<table>
<tr><th>SWP_MODE</th><th>Virtual Switch</th></tr>
<tr><td>0</td><td>one 12 port/24 lane switch</td></tr>
<tr><td>1</td><td>one 8 port/16 lane switch
one 4 port/8 lane switch</td></tr>
</table>
2. CKBUFPD0_L：Integrated Reference Clock Buffer Power Down Signals
3. CKBUFPD1_L：Integrated Reference Clock Buffer Power Down Signals
4. PHY_SRAM_BYPASS：Bypass PHY SRAM
5. SURPRISE_HP_0：Surprise Hot Plug Function for Tile 0</td></tr>
<tr><td>SW5</td><td>PORTCFG_0[2:0]
PORTCFG_1[2:0]</td><td>Default：off, on, off ,off ,on, off (101101)
1. PORTCFG_0[0]：Port Configuration
2. PORTCFG_0[1]：Port Configuration
3. PORTCFG_0[2]：Port Configuration
4. PORTCFG_1[0]：Port Configuration
5. PORTCFG_1[1]：Port Configuration
6. PORTCFG_1[2]：Port Configuration
Mode Selection for Tile 0
<table>
<tr><th>PORTCFG_0[2]</th><th>PORTCFG_0[1]</th><th>PORTCFG_0[0]</th><th>Functional Mode</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2Port-16Lane Configuration</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3Port-16Lane Configuration</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4Port-16Lane Configuration</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5Port-16Lane Configuration</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>8Port-16Lane Configuration</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table>
Mode Selection for Tile 1
<table>
<tr><th>PORTCFG_0[2]</th><th>PORTCFG_0[1]</th><th>PORTCFG_0[0]</th><th>Functional Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1Port-8Lane Configuration</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2Port-8Lane Configuration</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4Port-8Lane Configuration</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>SW6</td><td>PCFG_2OE_L
PCFG_1OE_L
PCFG_2DIR
PCFG_1DIR</td><td>Default：off, off, off ,off (1111)
1. PCFG_2OE_L：Reserved
2. PCFG_1OE_L：Reserved
3. PCFG_2DIR：Reserved
4. PCFG_1DIR：Reserved</td></tr>
</table>

<table>
<tr><td>SW7</td><td>PG1_2OE_L
PG0_1OE_L
PG1_2DIR
PG0_1DIR</td><td>Default：on, on, on ,on (0000)
1. PG1_2OE_L：Reserved
2. PG0_1OE_L：Reserved
3. PG1_2DIR：Reserved
4. PG0_1DIR：Reserved</td></tr>
<tr><td>SW8</td><td>Ln2_3_SEL
Ln4~7_SEL
Ln12~15_SEL
T1 Ln4~7_SEL</td><td>Default：off, off, off ,off (1111)
1. Ln2_3_SEL：Set Signal Switch for different modes
2. Ln4~7_SEL：Set Signal Switch for different modes
3. Ln12~15_SEL：Set Signal Switch for different modes
4. T1 Ln4~7_SEL：Set Signal Switch for different modes
Mode Selection for Tile 0
<table>
<tr><th>Lane</th><th>Mode</th><th>216</th><th>316</th><th>416</th><th>516</th><th>816</th></tr>
<tr><td>2,3</td><td>Ln2_3_SEL</td><td>on</td><td>on</td><td>on</td><td>on</td><td>off</td></tr>
<tr><td>4,5
6,7</td><td>Ln4~7_SEL</td><td>on</td><td>on</td><td>off</td><td>on</td><td>off</td></tr>
<tr><td>12,13
14,15</td><td>Ln12~15_SEL</td><td>on</td><td>off</td><td>off</td><td>off</td><td>off</td></tr>
</table>
Mode Selection for Tile 1
<table>
<tr><th>Lane</th><th>Mode</th><th>108</th><th>208</th><th>408</th><th>NA</th><th>NA</th></tr>
<tr><td>4,5
6,7</td><td>T1 Ln4~7_SEL</td><td>on</td><td>off</td><td>off</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>SW9</td><td>PORT_SEL0[2:0]
PORT_SEL1[2:0]</td><td>Default：on, on, on ,on ,on, on (000000)
1. PORT_SEL0[0]：Reserved
2. PORT_SEL0[1]：Reserved
3. PORT_SEL0[2]：Reserved
4. PORT_SEL1[0]：Reserved
5. PORT_SEL1[1]：Reserved
6. PORT_SEL1[2]：Reserved
Note：For developer debug</td></tr>
<tr><td>SW10</td><td>MODE_SEL[4:0]</td><td>Default：on, on, on ,on ,on, on (000000)
1. MODE_SEL0：Reserved
2. MODE_SEL1：Reserved
3. MODE_SEL2：Reserved
4. MODE_SEL3：Reserved
5. MODE_SEL4：Reserved
6. NC
Note：For developer debug</td></tr>
<tr><td>SW11</td><td>DBG_2OE_L
DBG_1OE_L
DBG_2DIR
DBG_1DIR</td><td>Default：off, off, off ,off (1111)
1. DBG_2OE_L：Reserved
2. DBG_1OE_L：Reserved
3. DBG_2DIR：Reserved
4. DBG_1DIR：Reserved</td></tr>
<tr><td>SW12</td><td>HIBW_BYPM_LOBW#
100M_133M#
CKPWRGD_PD#
SADR0_tri
SADR1_tri</td><td>Default：off, off, off, off, off, off (111111)
1. HIBW_BYPM_LOBW#：Reserved
2. HIBW_BYPM_LOBW#：Reserved
3. 100M_133M#：Reserved
4. CKPWRGD_PD#：Reserved
5. SADR0_tri：Reserved
6. SADR1_tri：Reserved</td></tr>
</table>

4.4 Push-Button Switches

4.4.1 *Manual Reset# (S1)*

The EVB Board provides a manual switch (S1) for manual PERST# capability. Note that manual PERST# will only apply warm reset to the PI7C9X3G1224GP (the PCIe3 Packet Switch IC).

4.5 Power Connectors and Headers

4.5.1 *ATX Peripheral Power Connectors*

The EVB Board has two Power Connectors.

Table 4-4 4-pin Power Connectors

Pin #	Signal Name
1	5V
2	GND
3	GND
4	12V

4.5.2 *6-pin +12V Power Connector*

Table 4-5 Signal Names of PWR2

Pin #	Signal Name	Pin #	Signal Name
1	+12VDC	5	COM
2	+12VDC	6	S
3	+12VDC	7	COM

4.5.3 *JTAG Header (J9)*

The 1x8 header provides a direct connection to the PI7C9X3G1224GP (the PCIe3 Packet Switch IC). JTAG interface. The 8-pin connector is designed to allow a direct interface to 3rd party JTAG controllers, such as the Corelis USB-1149.1/E controller. The pin assignment for the JTAG header is listed at Table 4-6.

Table 4-6 Pin assignment JTAG

Pin #	Signal Name	Pin #	Signal Name
1	3.3V_EXT	2	TCK
3	TMS	4	TDO_0
5	TDO_1	6	TDI
7	TRST_L	8	GND

4.5.4 *I2C /SMBus Header (J8)*

The 1x3 header provides a direct connection to the PI7C9X3G1224GP (the PCIe3 Packet Switch IC). I2C interface. The pin assignment for I2C/SMBUS Header is listed at Table 4-7.

Table 4-7 Signal Names for I2C/SMBUS Header

Pin #	Signal Name	Pin #	Signal Name
1	SCL_I2C	2	SDA_I2C
3	GND		

4.5.5 *Serial Hot Plug I2C Header (J10, J12)*

The 1x4 header provides a direct connection to the PI7C9X3G1224GP (the PCIe3 Packet Switch IC). Serial Hot Plug I2C interface. Must be used with SHP test adapter to verify SHP. The pin assignment for SHP I2C Header is listed at Table 4-78.

Table 4-8 Signal Names for SHP I2C Header

Pin #	Signal Name	Pin #	Signal Name
1	HPINT_0	2	HPSCL_0
3	HPSDA_0	4	GND

4.5.6 *PM_L11 CLKREQ Header (J11)*

The 1x8 header provides a direct connection to the PI7C9X3G1224GP (the PCIe3 Packet Switch IC). PM_L11 CLKREQ interface. When PM_L11_EN0_L = 0, the corresponding Port CLKREQ must be connected to the CLKREQ of the EP supporting PM_L11 at the back. The pin assignment for PM_L11 CLKREQ Header is listed at Table 4-79.

Table 4-9 Signal Names for PM_L11 CLKREQ Header

Pin #	Signal Name	Pin #	Signal Name
1	CLKREQ0_L[0]	2	CLKREQ0_L[1]
3	CLKREQ0_L[2]	4	CLKREQ0_L[3]
5	CLKREQ0_L[4]	6	CLKREQ0_L[5]
7	CLKREQ0_L[6]	8	CLKREQ0_L[7]