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MAX20781

High Bandwidth Smart Power-Stage IC with Integrated Current and Temperature Sensors

Product Highlights

- Space-Optimized Solution
  - Monolithic, Smart Power Stage
  - Small Footprint: 24mm^2
- 96.1% Peak Efficiency
  - 400kHz, 12V V_{IN}, 1.8V V_{OUT}
- Telemetry & Fault Reporting through Controller IC PMBus
  - Accurate Temperature Monitoring and Reporting
  - Accurate Per-Phase Current Reporting
  - Fault_ID Indicates Type of Fault
- Advanced Self-Protection Features*
  - Supply and Boost UVLO Protection
  - Input Supply OVLO Protection
  - Boost Refresh
  - VX Short and Overtemperature Shutdown
  - VX Open and Short Detection at Power-Up
  - Fast Overcurrent Protection
  - Open/Short Pin Detection During Startup

**Protection features vary with different part variants*

Key Applications

- High-Current Multiphase-Voltage Regulators

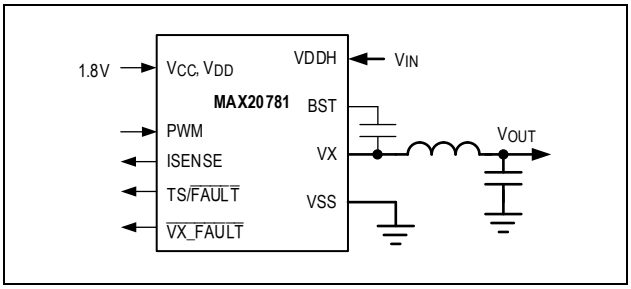
  The MAX20781 is a feature-rich smart power-stage IC designed to work with Maxim's controllers to implement a high-density multiphase voltage regulator. Multiple smart power-stage ICs plus a controller provide a compact synchronous buck converter that includes accurate individual phase current and temperature reporting through PMBus™.

  Parallel connection of smart power-stage ICs double the total current for a single output, delivering over 1kA. Exposed top side package with active cooling enables up to 50A continuous current per phase.

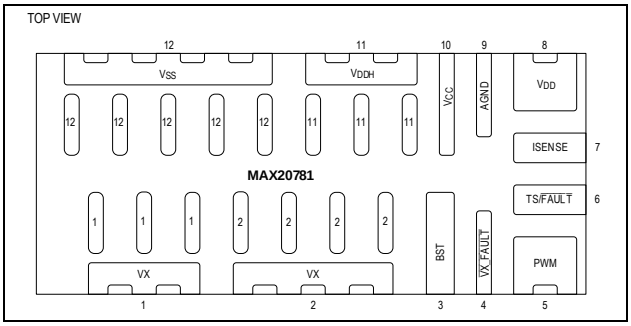
  High current-sense bandwidth enables high frequency operations with a minimum on-time of 100ns, ideal for 12V to sub-1V voltage conversion in GPUs, AI and Machine Learning ASICs.

PMBus is a trademark of SMIF, Inc.

Simplified Application Diagram



Pin Description



Electrical and Thermal Ratings

DESCRIPTON	CURRENT RATING* (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating**	86	4.5 to 16	0.25 to 2.3
Thermal Rating T_A = 55°C, 200LFM	52	12	1.8
	60	12	1.0

**T_J = 125°C. For specific operating conditions, see SOA curves in the Typical Operating Characteristics section.*

***Maximum-Phase DC current limited by POCP and FASTPOCP_R typical values*

***Ordering Information* appears at end of data sheet.**

PRELIMINARY

19-101304; Rev 0; 11/21

Absolute Maximum Ratings

V_{DDH} to V_{SS} (Note 1) .....-0.3V to +23V

VX to V_{SS} (DC) .....-0.3V to +23V

VX to V_{SS} (AC) (Notes 1, 2) .....-10V to +25V

V_{DDH} to VX (DC) .....-0.3V to +23V

V_{DDH} to VX (AC) (Notes 1, 2) .....-10V to +25V

BST to V_{SS} (DC) .....-0.3V to +25.5V

BST to V_{SS} (AC) (Note 2).....-7V to +27.5V

BST to V_{CC} .....-0.3V to +23V

BST to VX Differential .....-0.3V to +2.5V

V_{DD}, V_{CC} to AGND.....-0.3V to +2.5V

PWM, ISENSE, TS/FAULT to AGND ..... -0.3V to V_{DD} + 0.3V

VX_FAULT to AGND.....-0.3V to +23V

V_{SS} to AGND.....-0.3V to +0.3V

Peak VX Current (Note 3) .....-70A to +130A

Junction Temperature (T_J) .....+150ºC

Storage Temperature Range .....-65ºC to +150ºC

Peak Reflow Temperature Lead-Free .....+260ºC

Note 1: Input HF capacitors placed not more than 40 mils away from the VDDH pin required to keep inductive voltage spikes within Absolute Maximum limits.

Note 2: AC is limited to 2ns per cycle.

Note 3: Per-phase current capability. POCP and FASTPOCP_R limit the application below the peak VX current rating.

Note 4: Applicable only to the MAX16600 EV kit in free space with no airflow.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 FC2QFN	
Package Code	F123A7F+1
Outline Number	21-100261
Land Pattern Number	90-100099
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	8°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	0.25°C/W

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Continuous Smart Power-Stage Thermal Design Current (TDC)

T_A = 55°C, T_J = 105°C, 400kHz, V_{DDH} = 12V, no heatsink

	V_{OUT} = 1.8V, 0.6mΩ LL (A)			**V_{OUT} = 1.0V, NO LL (A)**		
AIRFLOW	**NUMBER OF PHASES**			**NUMBER OF PHASES**		
	8	6	4	8	6	4
0LFM	16	20	24	18	22	26
200LFM	21	26	28	22	27	31
300LFM	24	28	31	25	29	34
400LFM	26	30	33	28	33	36

T_A = 55°C, T_J = 105°C, 400kHz, V_{DDH} = 12V, with heatsink (36-006032-00)

	V_{OUT} = 1.8V, 0.6mΩ LL (A)			**V_{OUT} = 1.0V, NO LL (A)**		
AIRFLOW	**NUMBER OF PHASES**			**NUMBER OF PHASES**		
	8	6	4	8	6	4
0LFM	18	23	30	20	25	31
200LFM	30	32	44	30	35	47
300LFM	32	36	45	33	39	48
400LFM	37	40	50	38	43	56

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Electrical Characteristics

(See Typical Multiphase Application Circuit, V_{DDH} = +12V, V_{DD} = V_{CC} = +1.8V, T_A = T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
SUPPLY VOLTAGES, SUPPLY CURRENT							
Input Supply Voltage Range	V_{DDH}			4.5		16	V
1.8V Supply Voltage	V_{DD}, V_{CC}			1.71		1.98	V
Input Supply Current	I_{VDDH}	Shutdown (PWM = 0, TS/FAULT = 0, ISENSE = 0), T_A = +32ºC			1.3	10	µA
		Inactive, no switching (PWM = Hi-Z), T_A = +32ºC			65	500	mA
1.8V Supply Current	I_{VCC} + I_{VDD}	Shutdown (PWM = 0, TS/FAULT = 0, ISENSE = 0), T_A = +32ºC			3	6	µA
		Inactive, no switching (PWM = Hi-Z), T_A = +32ºC			3	6.5	mA
		Load = 0, duty cycle = 15%, f_{SW} = 600kHz, T_A = +32ºC			44		
IRECON SPECIFICATIONS							
Current-Sense Gain	A_{I_5}	ISENSE / I_{VX}, duty cycle ≤ 20% (MAX20781A, MAX20781B)	-35A < I_{VX} < 35A (Note 5)	4.8	5	5.2	µA/A
			35A < I_{VX} < FASTPOCP_R (Note 6)	4.77	5	5.23	

(See Typical Multiphase Application Circuit, V_{DDH} = +12V, V_{DD} = V_{CC} = +1.8V, T_A = T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	A_{I_10}	ISENSE / I_{VX}, duty cycle ≤ 20% (MAX20781C, MAX20781D)	-35A < I_{VX} < 35A (Note 5)	9.6	10	10.4	
			35A < I_{VX} < FASTPOCP_R (Note 6)	9.55	10	10.45	
Current-Sense Offset		Duty cycle ≤ 20%, no load	A_I = 5µA/A (MAX20781A, MAX20781B)	-2.5	0	+2.5	µA
			A_I = 10µA/A (MAX20781C, MAX20781D)	-5	0	+5	
I_{RECON} Bandwidth		Load = 0A, R_{SENSE} = 287Ω			11		MHz
		Load = 85A, R_{SENSE} = 287Ω			19		
TEMPERATURE SENSOR							
Temperature-Sensor Dynamic Range	T_{RANGE}	(Note 7)		-40		125	°C
Temperature Sensor Gain	A_{TEMP}	T_J = 0°C to +125°C (Note 7)		3.058	3.196	3.334	mV/°C
Temperature Sensor Voltage	$V_{TS/FAULT}$ @0°C	T_J = 0°C (Note 7)		790	805	820	mV
	$V_{TS/FAULT}$ @125ºC	T_J = +125ºC (Note 7)		1190	1205	1224	mV
Temperature Sensor Bandwidth					144		kHz
PROTECTION FEATURES							
VDDH OVLO Threshold	V_{DDH_OVLO}	Rising V_{DDH}		17.35	17.8	18.15	V
VDDH UVLO Threshold	V_{DDH_UVLO}	Rising V_{DDH}, 200mV hysteresis		4	4.17	4.31	V
V_{DD} Undervoltage Lockout	V_{DD_UVLO}	Rising V_{DD}, 60mV hysteresis				1.7	V
		Falling V_{DD}		1.47	1.52	1.57	
V_{DD} Power on Reset	V_{DD_POR}	Falling V_{DD}, 110mV hysteresis			1		
BST Undervoltage Lockout (Rising)	V_{BST_UVLOR}	Rising V_{BST}, 60mV hysteresis, 200ns deglitch		1.47	1.56	1.62	V
BST Undervoltage Lockout (Falling)	V_{BST_UVLOF}	Falling V_{BST}, 50ns deglitch			1.217		V
Positive Current Limit (Rising)	FPOCP_R	Non-Latched Peak Current Limit		82	88	93	A
Positive Current Limit (Falling)	POCP	HS on inhibit level (valley)		75	84	92	A
Peak Negative-OCP Clamp Level	NOCP					-40	A
FASTOCP_R Propagation Delay	td_{FPOCP_R}	(Note 7, 8)			15		ns
Overtemperature Protection/Shutdown	T_{SHDN}	Rising threshold			160		°C
HS VX Short Threshold	$V_{HSVXSHT\_TH}$	HS on and VX shorted to V_{SS}			V_{DDH} - 0.67		V
LS VX Short	$V_{LSVXSHT\_TH}$	LS on and VX shorted to V_{DDH} (VX rising)			0.2 x V_{CC}		V
VX short response time	t_{VXSHRT}	VX short to FET off (Note 7)			12		ns

PRELIMINARY

(See Typical Multiphase Application Circuit, V_{DDH} = +12V, V_{DD} = V_{CC} = +1.8V, T_A = T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = T_J = +32°C. All devices 100% tested at T_A = T_J = +32°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VX Short Power-up threshold	V_{LSVXPU_TH}	Power up check	25	34	45	mV
VX to V_{SS} Short at Power Up - Isource	I_{VXPU}	VX=0V (Note 7)		128		mA
VX to V_{SS} Short Power Up Timeout	t_{VXSHT_TO}	From start of power up sequence	1.02	1.2	1.38	ms
VX Short Fault Detect to VX_FAULT Low	t_{VXFLTB_LOW}	(Note 7)		25		ns
VX_FAULT **PIN**						
VX_FAULT Output Low Voltage	V_{VXFLTB_VOL}	Output Logic Low (I=1mA)			90	mV
VX_FAULT leakage	$I_{VX\_FLTB\_LK}$	VX_FAULT = 12V, T_A = 32ºC			1	µA
VX_FAULT input threshold, rising	V_{VXFLTB_THR}	Rising threshold, enables VX-to-V_{SS} fault detection.		664		mV
VX_FAULT input threshold, falling	V_{VXFLTB_THF}	Falling threshold, disables VX-to-V_{SS} fault detection during I_{DDO}		527		mV
VX_FAULT Output Voltage Levels	V_{VXFLTB_VOH}	Output high, Isink = 1mA		V_{DD} - 0.4		V
	V_{VXFLTB_VOL}	Output low, Isource = 1mA		0.4		
TS/FAULT **PIN**						
TS/FAULT Digital Thresholds	V_{TSFLTB_IH}		V_{DD} - 0.1			V
	V_{TSFB_IL}				0.06	
	V_{TSFLTB_OH}	Output logic-high, (I = 1mA)	V_{DD} - 0.33			
	V_{TSFLTB_OL}	Output logic-low, (I = 10mA)			0.12	
Fault Detect to TS/FAULT Low Delay	t_{TSFLTB_LOW}			535		ns
PWM PIN						
PWM Input Levels	V_{PWM_H}	Input logic-high	V_{DD} - 0.23			V
	V_{PWM_L}	Input logic-low			0.24 x V_{DD}	
	V_{PWM_MID}	PWM input midlevel for VX three-state control		0.68		
PWM Midlevel Hold Time	$t_{PWM\_MID\_HOLD}$	VX_ low to Hi-Z transition		50		ns
PWM Input Current	I_{PWM_H}	Input current, PWM high		260		µA
	I_{PWM_L}	Input current, PWM low		-430		
VX PIN						
Minimum VX On-Time	$t_{VX\_MIN\_PT}$	Power-train minimum on-time.		34		ns
ISENSE PINS						
ISENSE Input Levels	V_{ISNS_H}	Input logic high	0.81			V
	V_{ISNS_L}	Input logic low			0.43	

Note 5: Replica current tested in application. Actual current sense gain tolerance validated in application.

Note 6: Guaranteed by design to ±4σ about the mean.

Note 7: Guaranteed by design. Not production tested.

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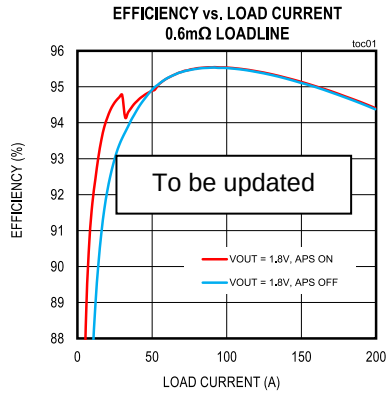
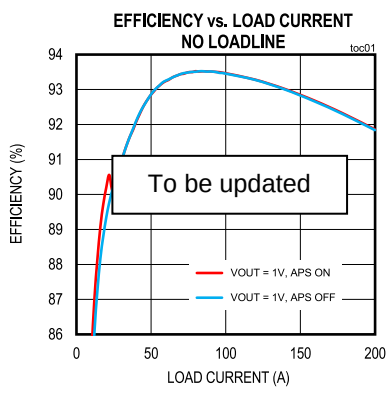
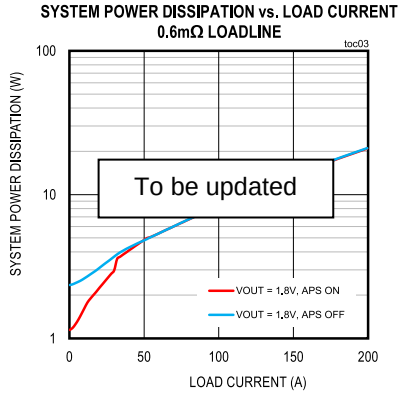
Note 8: Delay is from the time threshold is crossed to when the FET turns off. V_{DD} = V_{CC} = 1.8V, V_{DDH} = 12V, inductor = 50nH.

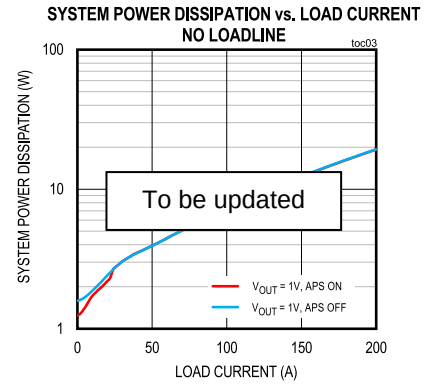
Typical Operating Characteristics

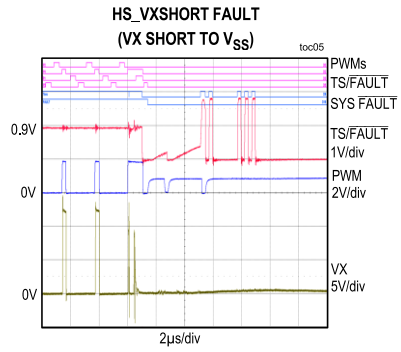
(V_{DDH} = 12V, T_A = +25°C, f_{SW} = 400kHz, 6-phase configuration, inductor = CLH1110-6, unless otherwise noted.)

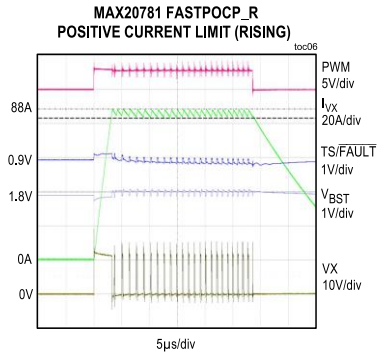


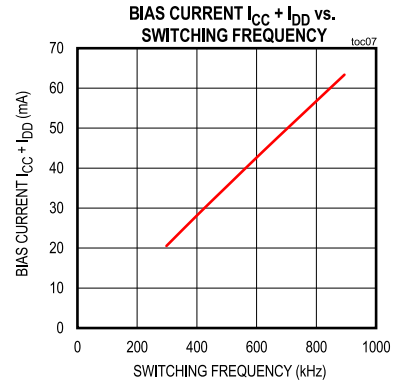


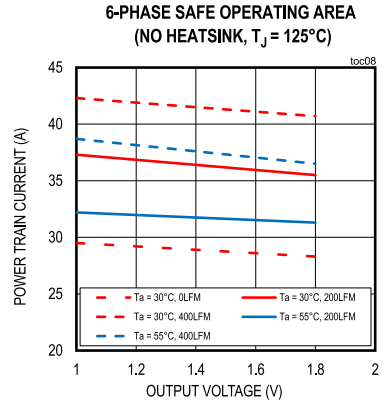












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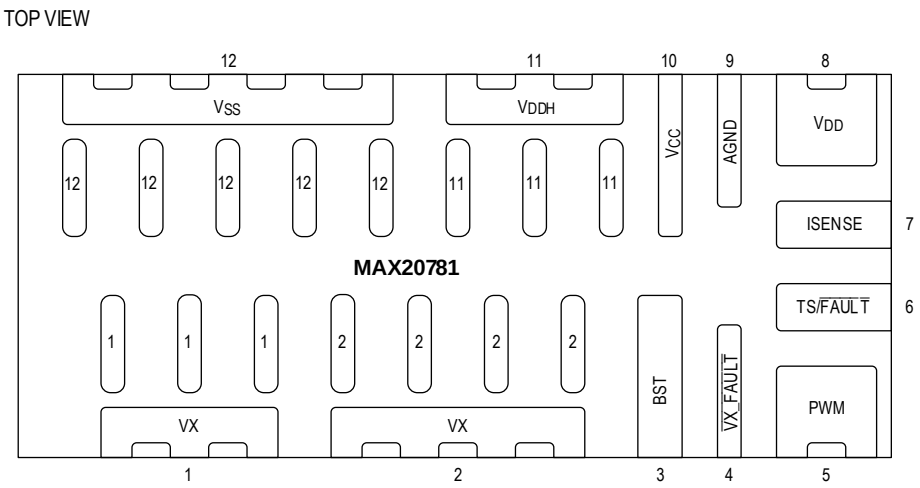
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1–2	VX	Switching Node. Connect to the switching node of the output inductor.
3	BST	Boost Supply Input. Connect a 0.68µF ceramic capacitor placed on the same side and 40 mils or closer to the IC between BST and VX.
4	VX_FAULT	VX_Fault Dual Function Pin. VX_FAULT is used to enable/disable the VX-to-V_{SS} short detection at startup, and to indicate when a VX-short fault occurs if the feature is enabled. VX_FAULT during I_{DDQ}: • High: Enable VX-to-V_{SS} short detection • Low: Disable VX-to-V_{SS} short detection • Latched: Latch is reset when entering I_{DDQ}. VX_FAULT during operation: • Open-drain output. Use this signal to disconnect the V_{DDH} input supply from the IC to prevent exothermic events.
5	PWM	PWM Input. Connect to the appropriate PWM output of the controller. PWM Logic Levels: • High: High-Side (HS) FET on, Low-Side (LS) FET off • Mid: Diode emulation mode; both FETs are off when the current reaches zero • Low: LS FET on, HS FET off
6	TS/FAULT	Smart Power-Stage Temperature and Fault Output. This dual-function pin is used to report the junction temperature and to communicate a fault condition to the controller. See the *Fault Detection and Fault_ID* and *Fault_ID Protocol* sections for the fault communication description. The junction temperature is calculated as shown below: $T_J = (V_{TS/FAULT} - V_{TS/FAULT}, 0°C)/A_{TEMP}$ $= (V_{TS/FAULT} - 805mV)/(3.196mV/°C)$ Connect TS/FAULT to the appropriate TSENSE input of the controller.
7	ISENSE	Current-Sense Output. Connect to the appropriate ISENSE input pin of the controller. The ISENSE current is an attenuated replica of the VX current:

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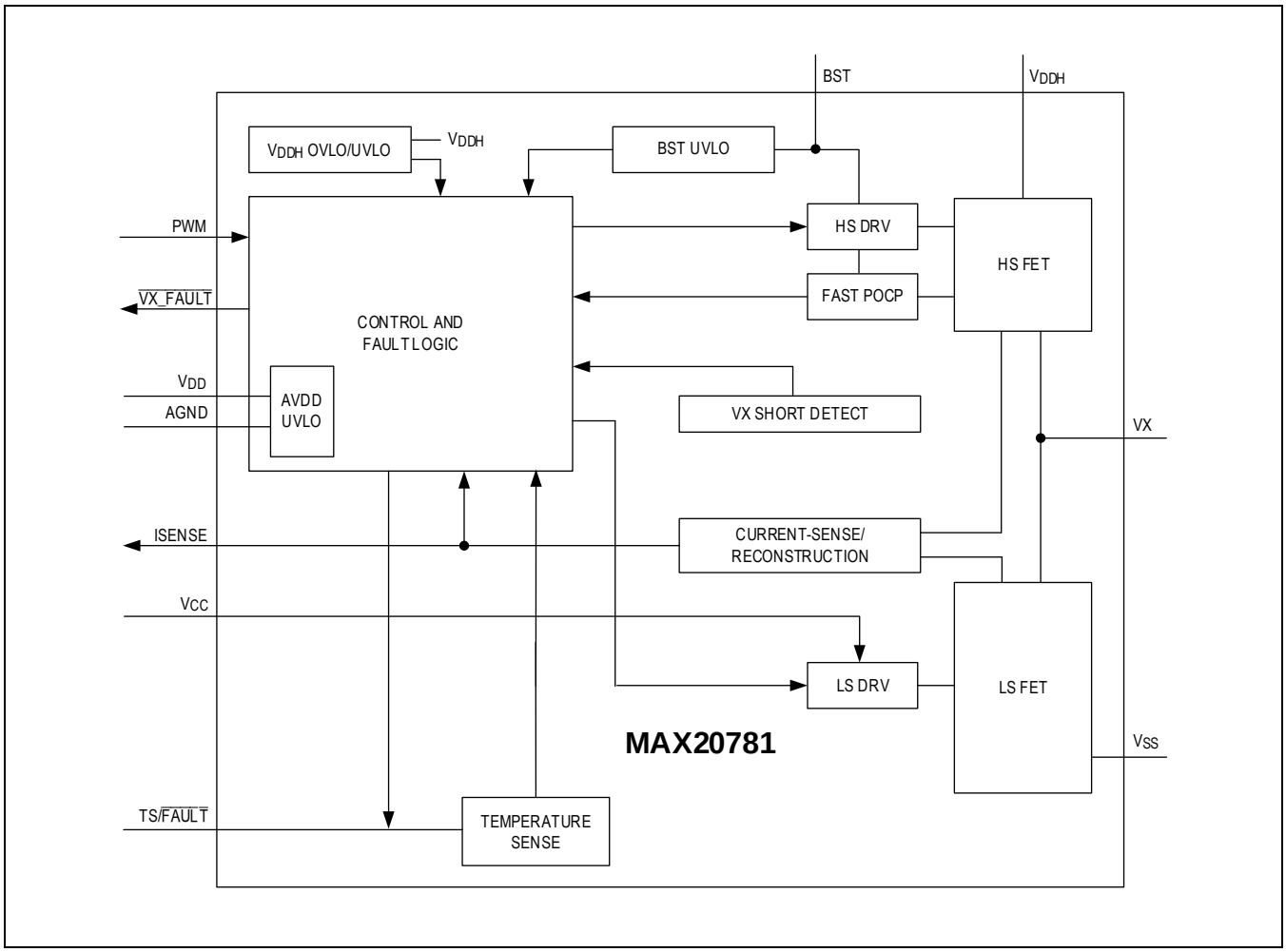
		ISENSE = I_{VX} x A_I See the *Electrical Characteristics* table for the Current Sense Gain (A_I) and Current Sense Offset.
8	V_{DD}	Analog Supply Input. Connect to the bias supply provided by the Master Controller or an external 1.8V bias supply through a 5Ω resistor. Connect a 0.47µF ceramic capacitor in close proximity to the IC's V_{DD} and AGND pins. See Table 1 for decoupling requirements.
9	AGND	Analog Ground. Connect to the ground plane using single via placed in close proximity to the IC.
10	V_{CC}	Gate Drive Supply. Connect to the bias supply provided by the Master Controller or an external 1.8V bias supply. Place a 1µF ceramic capacitor close to the V_{CC} pin. See Table 1 for decoupling requirements.
11	V_{DDH}	Drain of High-Side Power FET. Connect to the 12V input supply. See Table 1 for decoupling requirements.
12	V_{SS}	Power Ground. Connect to the return path of the output load.

Functional Diagrams



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Detailed Description

The MAX20781 smart power stage ICs provide the control logic, drivers, monitoring circuits, and power semiconductors for a synchronous buck converter. Precision measurement circuitry enables fault protection, status monitoring, and accurate lossless current sensing.

Power-Switch Control and Drivers

The smart power stage ICs operate in conjunction with a Maxim controller IC. The controller configures the voltage regulator through pin strapping and the number of populated phases. The smart power stage IC's switching is controlled by the proprietary command signals on the PWM signals. The PWM control signal has three defined states: high, low, and tri-state. The tri-state signal is used for phase shedding and DCM modes.

Bias Supply Pins

An external boost capacitor (0.68µF) is required to supply the voltage for the high-side switch driver. V_{DD} and V_{CC} are brought out separately to allow separate decoupling to improve noise immunity on the V_{DD} rail. The V_{DD} pin requires a 0.1µF decoupling capacitor. The V_{CC} pin requires 1µF decoupling capacitor. A 5Ω filter resistor is required between the V_{DD} and V_{CC} pins of each smart power stage IC. Table 1 shows the typical decoupling cap requirement.

Table 1. Typical Boost, Filtering, and Decoupling-Capacitor Requirements

DESCRIPTION	VALUE	TYPE	PACKAGE	QUANTITY
V_{DD} Capacitor	0.47µF, 6.3V	X7R, +125°C	0402	1
V_{CC} Capacitor	1µF, 6.3V	X7R, +125°C	0402	1
Boost Capacitor	0.68µF, 6.3V	X7R, +125°C	0402	1
V_{DD} Filter Resistor	4.7Ω	1/16W 1%	0402	1
V_{DDH} HF Capacitor	4.7nF, 50V	X7R, +125°C	0603	1
V_{DDH} MF Capacitor	10µF, 25V	X7R, +125°C	0603	2
V_{DDH} Bulk Capacitor	10µF, 25V	X5R	0805	2
V_{DDH} Bulk Capacitor	10µF, 25V	X5R	1206	2

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Current-Sense Output

The integrated lossless current sense (or "current reconstruction") produces a precise ratiometric current-sense signal for both positive and negative currents, which is sent to the controller as an analog current signal. This current-sense technology provides accurate current information over load and temperature that is not affected by tolerances of passive elements such as the output inductor, resistors, and capacitors.

Phase Configuration

The ability for the controller to dynamically disable and re-enable a phase is an integral part of the Maxim con-troller/power stage architecture. The controller sets the phase control signal to three state to disable a phase; the same state is used to control DCM operation. When using a coupled-inductor mode, a proprietary mode can be set by the controller, communicated to the smart power stage through PWM to minimize losses due to coupled currents in inactive phases.

Low Power I_{DDQ} State

The IC enters a low-power I_{DDQ} state when all the following three signals are held low: TS/FAULT, PWM and ISENSE. The controller forces this state when the regulator is in the OFF state. The smart power stage exits the I_{DDQ} state when any one of the required inputs is not held low.

Fault Protection

The IC features independent fault-monitoring and protection features. TS/FAULT is pulled low when a fault occurs. The Fault_ID is subsequently communicated to the controller over the TS/FAULT line to indicate the type of fault.

Overcurrent Protection

The IC incorporates instantaneous overcurrent fault protection using a lossless peak current sense and a reconstructed valley current. This overcurrent protection is separate from the system overcurrent protection and is intended to operate only in extreme fault conditions to protect the IC and other components. The system overcurrent protection of the controller should be set with sufficient margin below the individual smart power stage's threshold to ensure correct system operation.

For current-sourcing operation, the reconstructed valley current limit prevents the high-side FET from turning on until the current is below the POCP level, while the lossless peak current sense turns off the high-side FET if the instantaneous current exceeds the FASTPOCP_R overcurrent-protection value (see the *Electrical Characteristics* table). The FASTPOCP_R threshold is set to ensure that the maximum allowable peak current is not exceeded when using the recommended inductors. The sourcing current limiting is not considered a hard fault condition or the smart power stage; therefore, TS/FAULT is not asserted. The maximum achievable DC current per phase is given by Equation 1.

Equation 1:

$$Maximum\ VX\ DC\ Phase\ Current = \frac{I_{FASTOCP\_R} + I_{POCP}}{2}$$

In applications where the inductor ripple is lower than the difference between FASTOCP_R and POCP, the ripple current must be considered when calculating the maximum average current per phase, as shown in Equation 2. Note that the clamping is based on a fast current sense independent of the ISENSE signal. Limits shown for FASTPOCP_R and POCP in the *Electrical Characteristics* table reflect expected variations in application conditions and external component characteristics.

Equation 2:

$$Maximum\ VX\ DC\ Phase\ Current = I_{POCP} + \frac{I_{RIPPLE}}{2}$$

Note that the controller (i.e., system) overcurrent protection should be set lower than the corresponding smart power stages' maximum operating current.

For current-sinking protection, if the negative overcurrent-protection threshold is reached, the LS FET is turned off, the smart power stage limits the phase current, as shown in Equation 3, and TS/FAULT is not asserted.

Equation 3:

$$Maximum\ VX\ Negative\ DC\ Phase\ Current = I_{NOCP} + \frac{I_{RIPPLE}}{2}$$

V_{DD} and V_{BST} Undervoltage Lockout

The IC includes undervoltage-lockout circuits for V_{DD} and BST. For power-sequencing guidelines and operation with separate bias rails for controller and smart power stages, refer to the appropriate controller data sheet.

The IC features two BST_UVLO circuits: a fast one with 50ns deglitch and 1.217V typical threshold, and a slower one with 200ns deglitch and a higher 1.56V typical threshold. The fast BST_UVLO is active once the power-stage exits the I_{DDQ} state (PWM going high the first time). The slower BST_UVLO circuit is not active during the initial system power-on state (before regulation is enabled). The slower BST_UVLO (1.56V) is active approximately 18µs after the four BST charging cycles of the initial startup sequence. If any of these UVLO circuits is tripped during operation, the MAX20781 stops switching and a fault signal (TS/FAULT pulled LOW) is sent to the controller.

V_{DDH} Undervoltage and Overvoltage Lockout

The IC includes protection circuits that shut down the smart power stage and assert TS/FAULT if either V_{DDH} is above or below the correct operating range. If either of these circuits is tripped during operation, the smart power stage stops switching and a fault signal (TS/FAULT pulled LOW) is sent to the controller.

Temperature Sensing and Overtemperature Protection

Each IC incorporates an accurate die temperature sensor. The temperature-sense signal is sent to the controller as an analog signal through the TS/FAULT pin. The actual temperature of each smart power-stage device is then made available through the controller's SMBus or PMBus interface. The junction temperature is calculated as shown in Equation 4:

Equation 4:

$$T_J = \frac{V_{TS/FAULT} - V_{TS/FAULT},\ 0^o\ C}{A_{TEMP}}$$

where $V_{TS/FAULT}$ is the measured voltage on the TS/FAULT pin, and $V_{TS/FAULT}$, 0°C and A_{TEMP} are taken from the *Electrical Characteristics* table.

The MAX20781 also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the controller through the TS/FAULT pin.

VX Short Protection During Operation

The IC includes VX short detection to detect a local short circuit from the VX node to either V_{DDH} or V_{SS} during operation. If such a fault is detected, the smart power stage shuts down and communicates the fault to the controller through the TS/FAULT pin. The VX_FAULT signal is also pulled low. This high-voltage open-drain VX_FAULT signal can be used to directly disconnect an input power switch to immediately cut off the supply to V_{DDH} and prevent exothermic events.

Fault Detection and Fault_ID

If a fault is detected, the smart power stage sends a signal to the controller by pulling the TS/FAULT pin to ground. Under normal conditions, the voltage on this pin is an accurate analog representation of the power-stage temperature. If a fault is detected, this pin is asserted LOW to indicate that a fault condition was detected by a smart power-stage IC. Table 2 shows the faults that result in asserting this signal. For a latching fault, the fault must be cleared and the V_{DD} power cycled to re-enable the IC.

If a nonlatching fault is detected by the smart power stage, it pulls TS/FAULT low and stops switching. The smart power stage resumes switching and deasserts TS/FAULT around 37µs after the fault condition is removed. Refer to the controller data sheet for controller response to TS/ FAULT asserted LOW by the smart power-stage device.

Table 2. Fault-Detection and Protection Circuits

FAULT NAME	FAULT DESCRIPTION	FAULT RESPONSE	TS/FAULT	FAULT_ID	RESET BY(1)
BST_UVLO	Boost Supply Undervoltage Lockout	Shutdown	Asserted	2	I_{DDQ}
VDD_UVLO	VDD Undervoltage Lockout	Shutdown	Asserted	1	I_{DDQ}
VDDH_UVLO	Input Supply Undervoltage Lockout	Shutdown	Asserted	1	I_{DDQ}
VDDH_OVLO	Input Supply Overvoltage Lockout	Shutdown	Asserted	6	I_{DDQ}
POCP (Sourcing)	Positive Overcurrent: Valley positive current limit that inhibits HS FET turn on	Cycle-by-Cycle Clamp	Not asserted	N/A	N/A
NOCP (Sinking)	Negative Overcurrent: Peak negative current threshold that disables the LS FET	Cycle-by-Cycle Clamp	Not asserted	N/A	N/A
FASTPOCP_R	Fast Positive OCP Rising: Peak positive VX current limit	Cycle-by-Cycle Clamp	Not asserted	N/A	N/A
HS_VXSHORT	HS on and VX to VSS Short	Shutdown	Asserted	3(2)	Cycle Bias Supply
LS_VXSHORT	LS on and VDDH to VX Short	Shutdown	Asserted	4(2)	Cycle Bias Supply
OTP	Overtemperature Protection	Shutdown	Asserted	5	I_{DDQ}
Seal Ring	Seal Ring Continuity Broken	Shutdown	Asserted	5	I_{DDQ}

1. *Reset required after fault is cleared.*
2. *Not reported for power-up short detection.*

Fault_ID Protocol

Power-stage fault communication with the controller is done over the TS/FAULT line. When a fault is detected, the power-stage signals the fault by pulsing TS/FAULT line low then releasing it. The controller responds by stopping the PWM operation. The TS/FAULT line now takes on the fault communication function to indicate the ID of the fault that occurred.

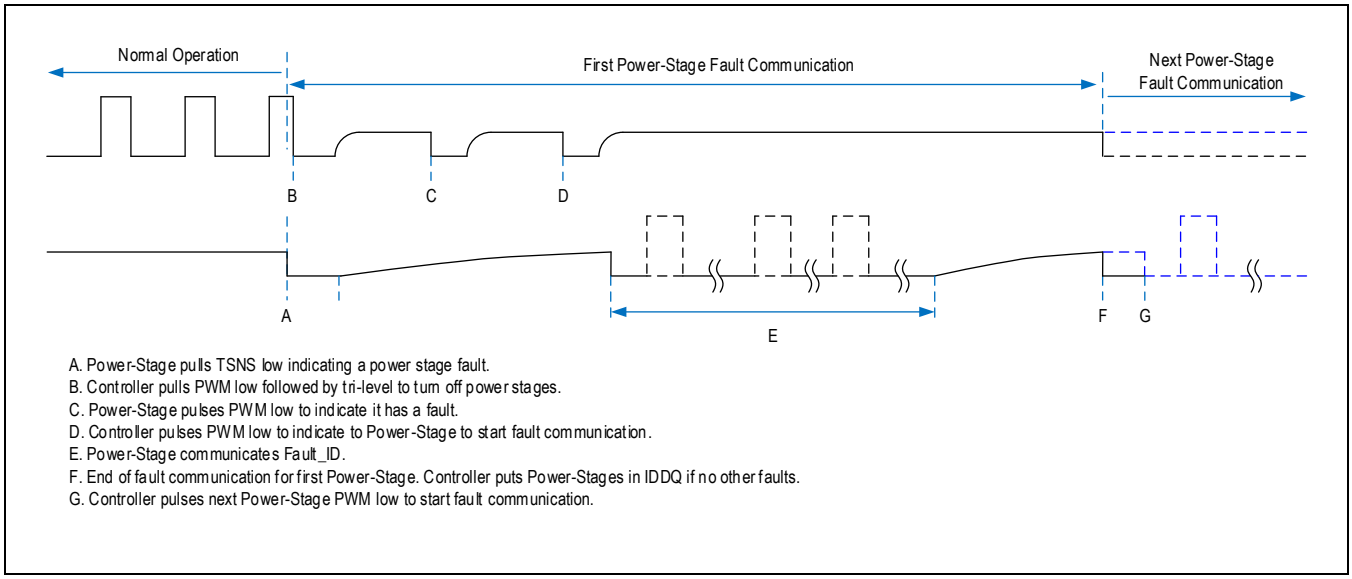


Figure 1. Fault_ID: Fault Communication Protocol.

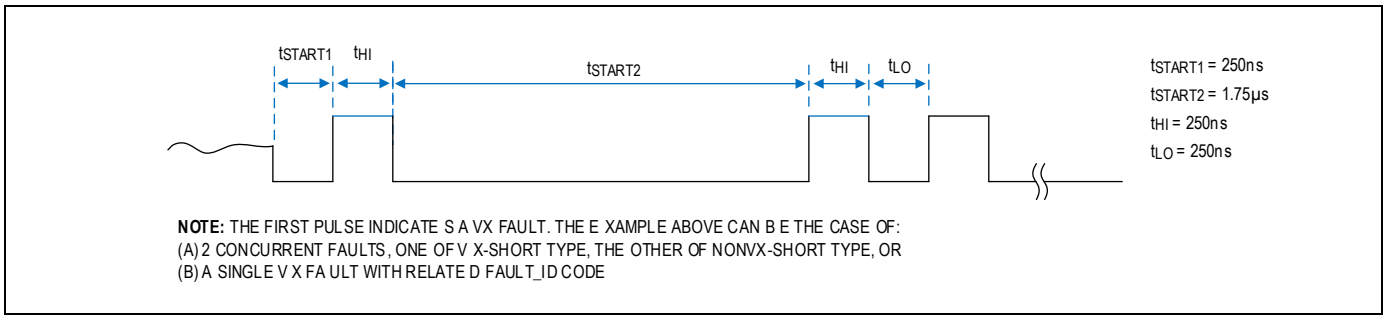


Figure 2. Fault_ID: Latching Fault with VXSHORT.

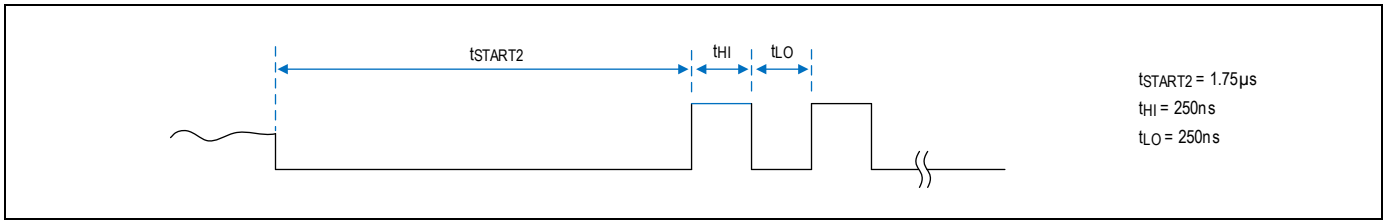


Figure 3. Fault_ID: Latching Fault without VXSHORT.

PRELIMINARY

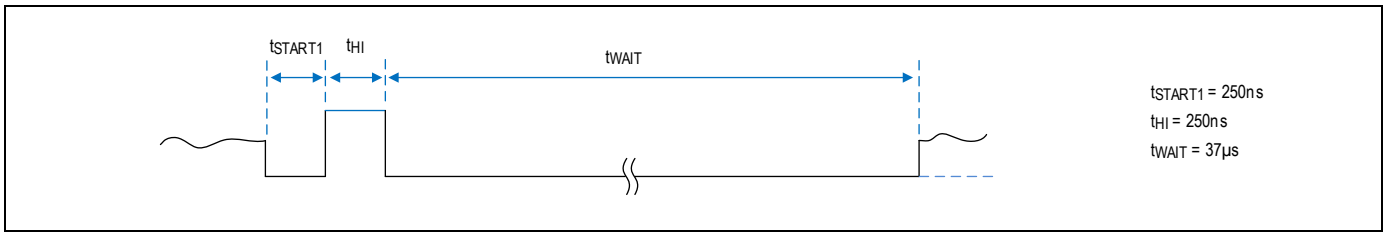


Figure 4. Fault_ID: Nonlatching Fault.

Pin Open/Short Detection

The IC features open/short pin detection that helps detect manufacturing or assembly issues before starting operation. V_{DDH} to VX short detection is done on initial power-up while still in the I_{DDQ} state. This provides protection even before the controller is ready. Other open/short pin detection start when exiting the I_{DDQ} state. Table 3 shows the pin detection details. Additional detection is performed by the controller IC after exiting the I_{DDQ} state.

Table 3. Pin Open/Short Detection

PIN NAME	FAULT-DETECTION TYPE
V_{CC}	Open Short to GND
V_{DD}	Protected by V_{DD_UVLO}
BST	Open Short to VX
ISENSE	Open Short to GND Short to V_{DD}
PWM	Open (detected by controller) Short to GND (detected by controller)
VX	V_{DDH} to VX short (requires V_{DD} to be present) VX open VX–V_{SS} short

PRELIMINARY

Applications Information

Bias Power Sequence

The bias supply for the controller and power-stage may come from different sources and have different power on sequence. It is strongly recommended that both controller and power-stage bias supplies are in regulation before the controller startup is initiated (controller enable pin is set high). Failure to observe proper power sequencing may result in power on failure and electrical stress to the IC.

Thermal Path and PCB Design

The smart power-stage IC has an exposed pad on the top-side of the package that is designed as an additional thermal path. This pad is electrically connected to AGND/V_{SS}, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results in low junction-to-ambient thermal impedance; hence, a lower junction temperature. This method provides an additional thermal path to the heat flow from the die to the PCB to ambient and also reduces the temperature of the PCB. Thermal performance is presented for various thermal conditions and airflow rates in the SOA plots (see the *Typical Operating Characteristics* section).

PCB Layout Guidelines

PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input and BST capacitors and output inductor, which should be placed close to the IC. The VX traces include large voltage swings (greater than 12V) with dV/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but also are shielded with a ground plane immediately beneath.

High-frequency capacitors are chosen based on their impedance vs. frequency characteristics. The right capacitor should have low impedance at the VX ringing frequency. Place these on the same side as the IC, 40 mils or closer to the V_{DDH} pin, and not more than 60 mils away. Typical mid-frequency and bulk capacitors provide the required decoupling at mid and low frequencies. These are placed after the HF capacitors, or on the opposite side of the PCB.

BST capacitors should be placed on the same side of IC as well, 40 mils or closer to the BST and VX pins, and not more than 60 mils away.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Contact Maxim to obtain MAX20781 layout guidelines for optimal design.

VX Voltage Spike and Derating

Parasitic inductance in the switching power path causes voltage spikes on VX during a low-to-high transition. Close placement of HF capacitors to the IC pins with adequate routing and vias keep the parasitic inductance low. Contact Maxim to obtain FC2QFN layout guidelines for optimal design.

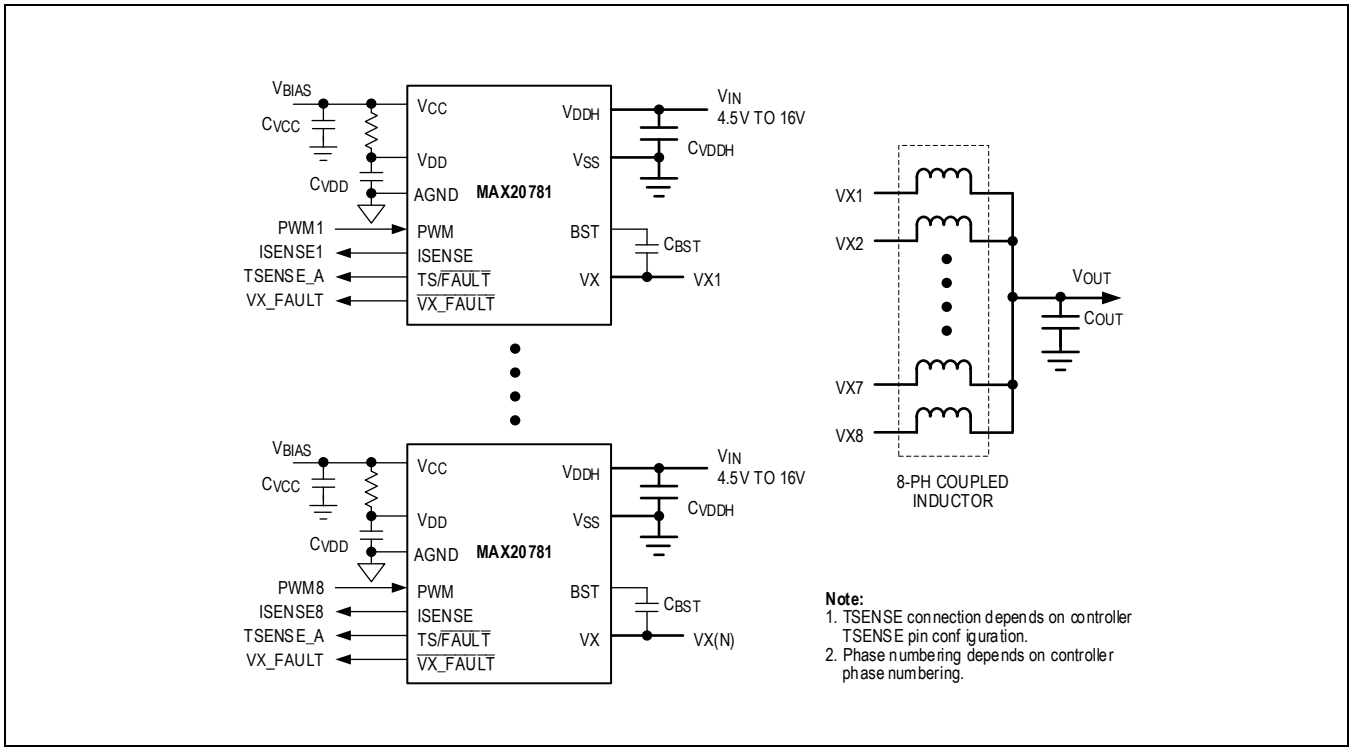
Equation 5:

$$EVS_{SPIKE} = VX(Abs\ Max) \times (Peak\ VX\ Current) \times 25ns$$

where VX(Abs Max) and I(Peak VX Current) are from the *Absolute Maximum Ratings* section

Following recommended component selection, placement, and board layout, the voltage spike duration is typically only a few nanoseconds. There is still at least 80% derating if the voltage spike duration is as long as 20ns.

Typical Multiphase Application Circuit



Function/Feature Differences

PART NUMBER	FUNCTION/FEATURE
MAX20781A	5µA/A irecon gain
MAX20781B	5µA/A irecon gain, Fast VX Transition
MAX20781C	10µA/A irecon gain
MAX20781D	10µA/A irecon gain, Fast VX Transition

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FUNCTION/FEATURE
MAX20781AAFC+*	-40°C to +125°C	12 FC2QFN	5µA/A irecon gain
MAX20781AAFC+T*	-40°C to +125°C	12 FC2QFN	5µA/A irecon gain
MAX20781BAFC+	-40°C to +125°C	12 FC2QFN	5µA/A irecon gain, Fast VX Transition
MAX20781BAFC+T	-40°C to +125°C	12 FC2QFN	5µA/A irecon gain, Fast VX Transition
MAX20781CAFC+*	-40°C to +125°C	12 FC2QFN	10µA/A irecon gain
MAX20781CAFC+T*	-40°C to +125°C	12 FC2QFN	10µA/A irecon gain
MAX20781DAFC+*	-40°C to +125°C	12 FC2QFN	10µA/A irecon gain, Fast VX Transition
MAX20781DAFC+T*	-40°C to +125°C	12 FC2QFN	10µA/A irecon gain, Fast VX Transition

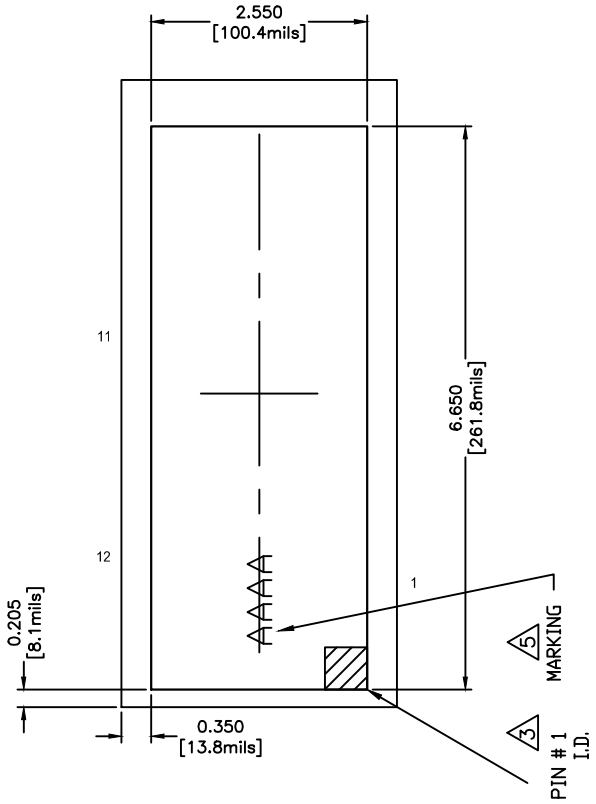
+Denotes a lead(Pb)-free/RoHS-compliant package.
** Future Product.*
+T = Tape and reel.

PRELIMINARY

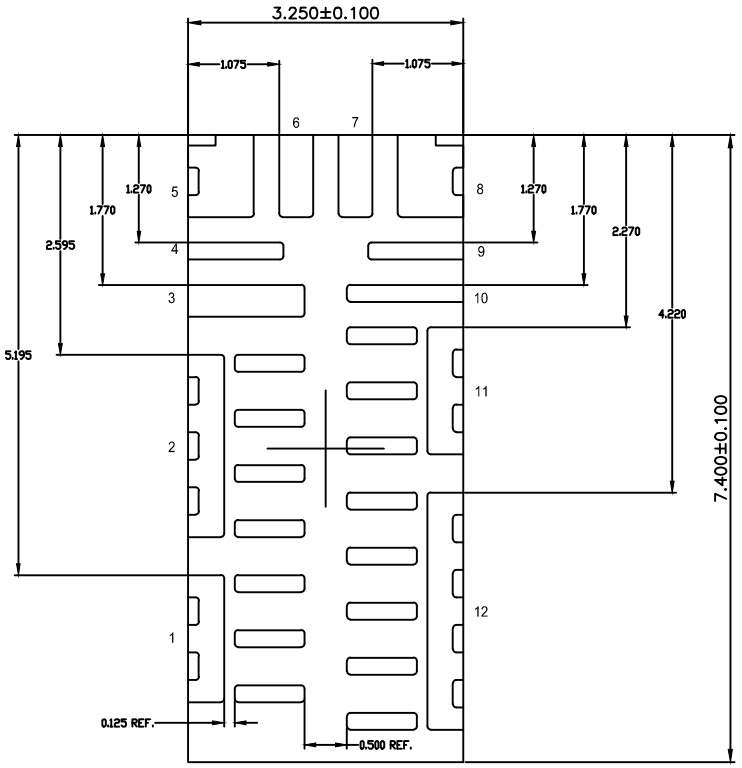
Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Initial release	—

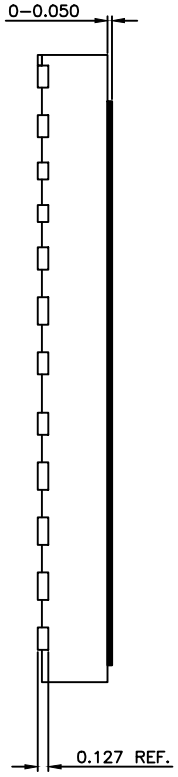
PRELIMINARY



TOP VIEW



BOTTOM VIEW



SIDE VIEW

POD FRONT VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
4. COPLANARITY APPLIES TO TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATIONS.
5. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
6. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
7. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODES.
8. PKG CODE: F123A7F+1

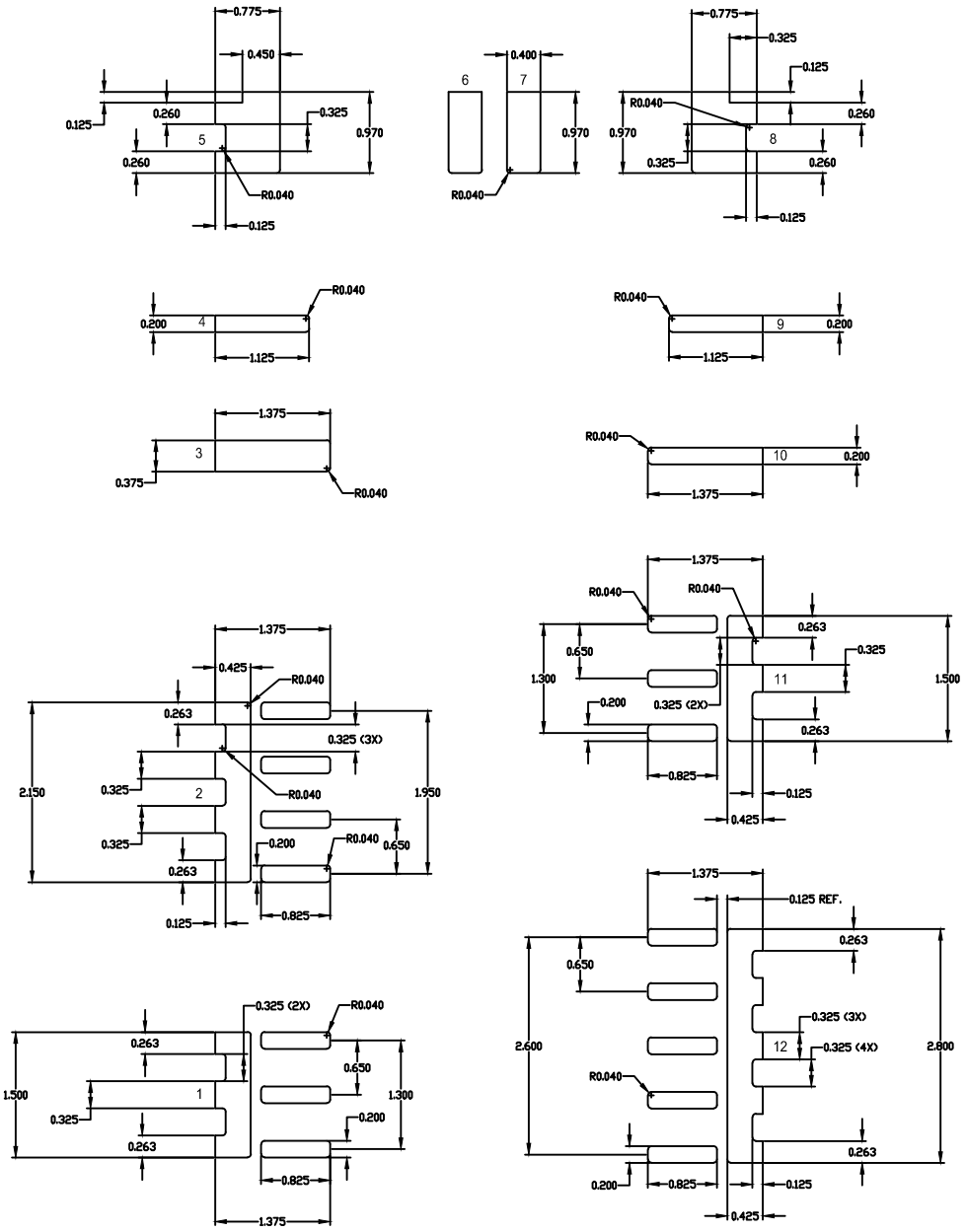
-DRAWING NOT TO SCALE-

ANALOG DEVICES

TITLE:
PACKAGE OUTLINE, 12L FC2QFN
3.25x7.40 mm FC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
CHILL GD	21-100261	C	1/2

PAD DETAILS



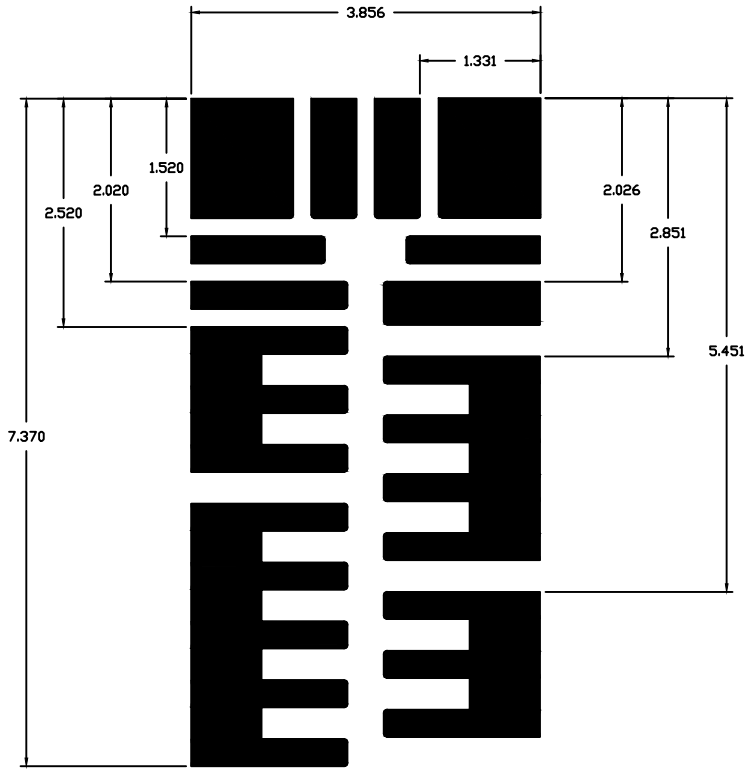
—DRAWING NOT TO SCALE—

ANALOG DEVICES

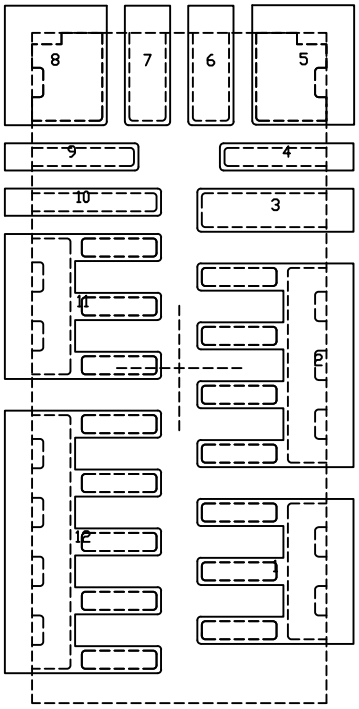
TITLE:
PACKAGE OUTLINE, 12L FC2QFN
3.25x7.40 mm FC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
CHILL GO	21-100261	C	2/2

RECOMMENDED LAND PATTERN



PACKAGE OVERLAY



NOTES:

1. REFERENCE PKG. OUTLINE: 21-100261, 21-100363
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE ONLY.
5. ALL DIMENSIONS IN MM.
6. REFER TO APPLICATION NOTES 5963 FOR SMT STENCIL DESIGN RECOMMENDATIONS

–DRAWING NOT TO SCALE–

PKG. CODES
[F123A7F-1]
[M123A7H-1]

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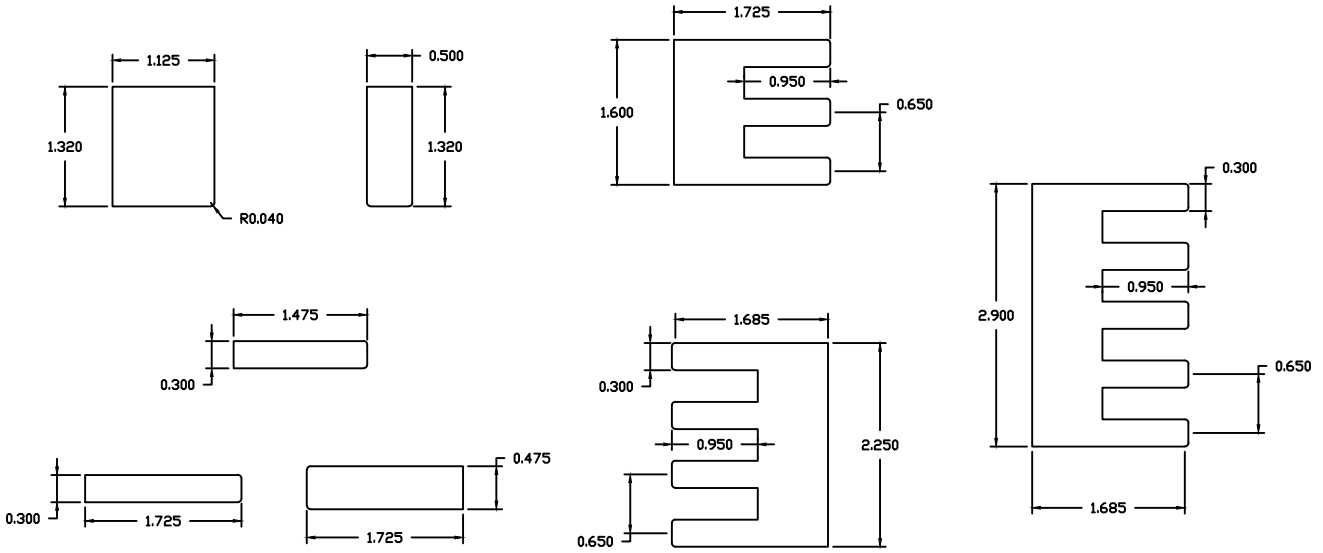
This document is subject to change without notice.
Contact technical support at http://www.maxim-ic.com/support for further questions.

TITLE:
PACKAGE LAND PATTERN,
FC2QFN, FD_mPLP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-100099	D	1/2

DETAILED DIMENSIONS



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TITLE:
PACKAGE LAND PATTERN,
FC2QFN, FD_mPLP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-100099	D	2/2