2N7002K-EVL

60V N-CHANNEL ENHANCEMENT MODE MOSFET - ESD PROTECTED

VENKEL LTD.

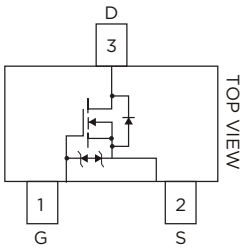
PART NUMBER	PACKAGE	VOLTAGE	CURRENT	CIRCUIT CONFIGURATION
2N7002K-□VL E = 7" Embossed T&R (3,000) U = 13" Embossed T&R (12,000)	SOT-23	60V	300mA	PIN 1: GATE; PIN 2: SOURCE; PIN 3: DRAIN

FEATURES:

- $R_{DS(ON)}$, V_{GS}@10V, I_{DS}@500mA=3Ω
- $R_{DS(ON)}$, V_{GS}@4.5V ,I_{DS}@200mA=4Ω
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- ESD Protected 2KV HBM

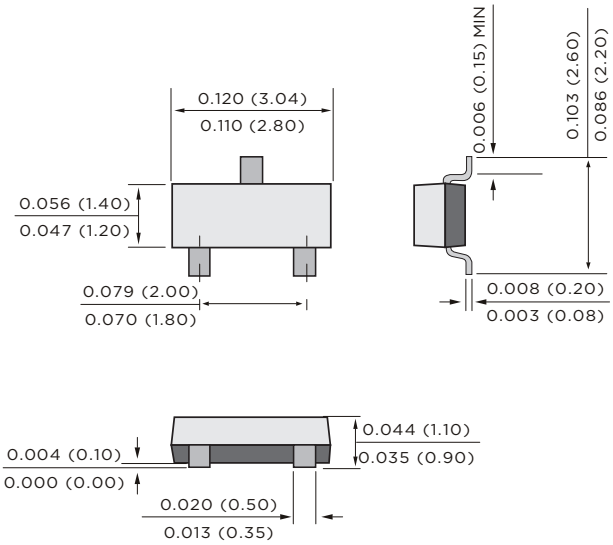
MECHANICAL DATA:

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750,Method 2026
- Approx. Weight: 0.0003 ounce, 0.0084 gram
- Marking: K72



SOT-23

Units: inch (mm)



MAXIMUM RATINGS & THERMAL CHARACTERISTICS

T_A=25˚C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	300	mA
Pulsed Drain Current (Note 1)		I_{DM}	2000	mA
Maximum Power Dissipation	T_A=25˚C T_A=75˚C	P_D	350 210	mW
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to +150	˚C
Junction to Ambient Thermal Resistance (PCB mounted) (Note 2)		$R_{\theta JA}$	357	˚C/W

NOTES:

1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, t≤10 sec
3. Pulse width ≤300us, Duty cycle≤2%

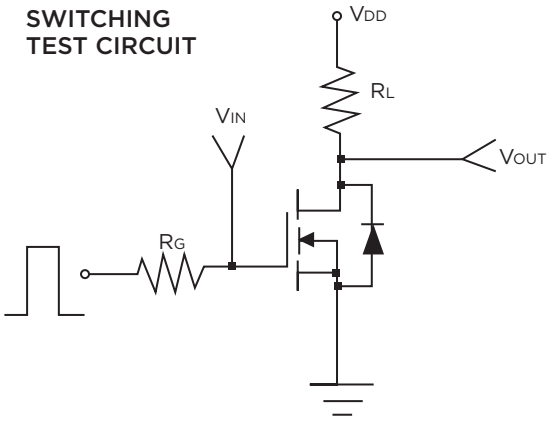
ENVIRONMENTAL INFORMATION

RoHS Status	10 of 10 Compliant
REACH Status	Compliant
Halogen Status	Halogen Free
Conflict Mineral Status	Conflict Mineral Free
Moisture Sensitivity Level (MSL)	1

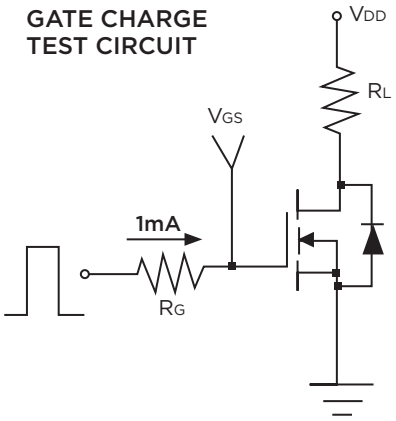
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
STATIC						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=0uA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=200mA	-	-	4.0	Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=500mA	-	-	3.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
Gate Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±10	uA
Forward Transconductance	G_{fS}	V_{DS}=15V, I_D=250mA	100	-	-	mS
DYNAMIC						
Total Gate Charge	Q_g	V_{DS}=15V, I_D=200mA V_{GS}=5V	-	-	0.8	nC
Turn-on Time	t_{on}	V_{DD}=30V, R_L=150Ω I_D=200mA, V_{GEN}=10V R_G=10Ω	-	-	20	ns
Turn-off Time	t_{off}		-	-	40	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V f=1.0MHz	-	-	35	pF
Output Capacitance	C_{oss}		-	-	10	
Reverse Transfer Capacitance	C_{rss}		-	-	5	
SOURCE DRAIN DIODE						
Diode Forward Voltage	V_{SD}	I_S=200mA, V_{GS}=0V	-	0.82	1.3	V
Continuous Diode Forward Voltage	I_S	-	-	-	300	mA
Pulse Diode Forward Voltage	I_{SM}	-	-	-	2000	mA

SWITCHING TEST CIRCUIT



GATE CHARGE TEST CIRCUIT



GRAPHS

Fig.1 Output Characteristic

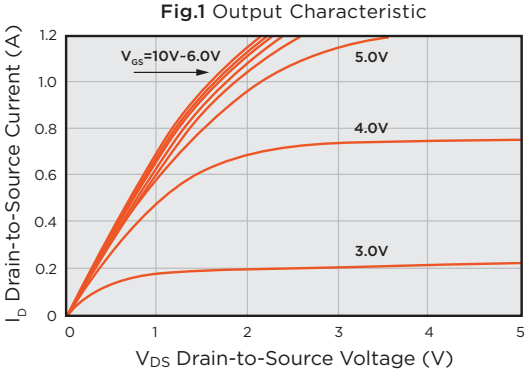


Fig.2 Transfer Characteristic

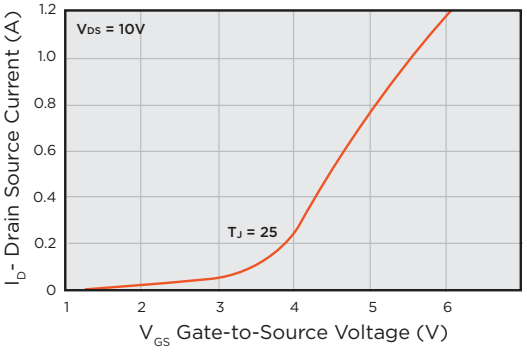


Fig.3 On-Resistance vs. Drain Current

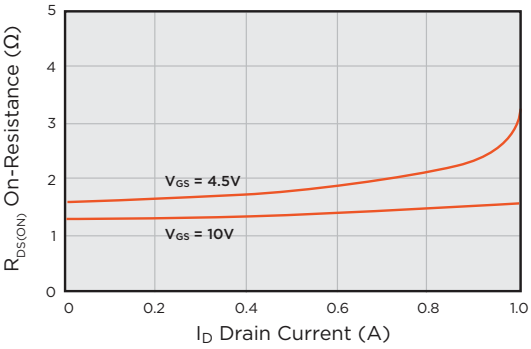


Fig.4 On Resistance vs. Gate to Source Voltage

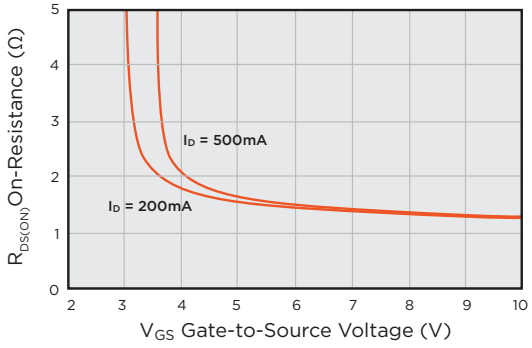


Fig.5 On-Resistance vs. Junction Temperature

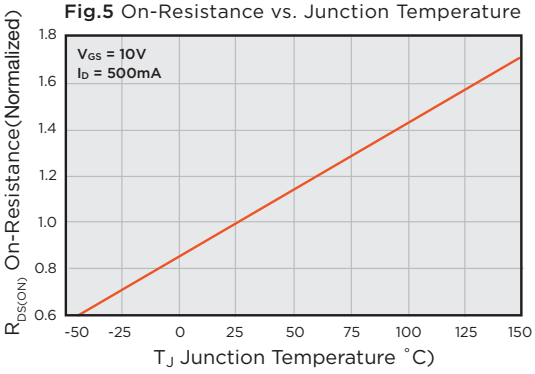


Fig.6 Gate Charge Waveform

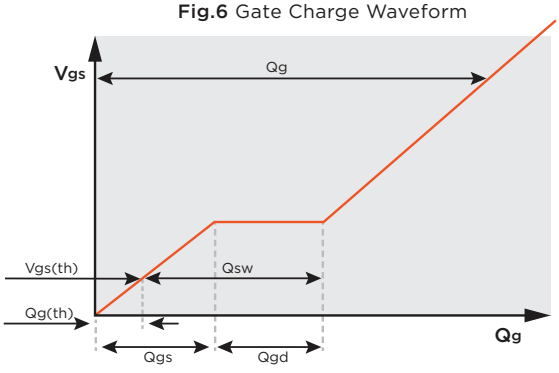


Fig.7 Gate Charge

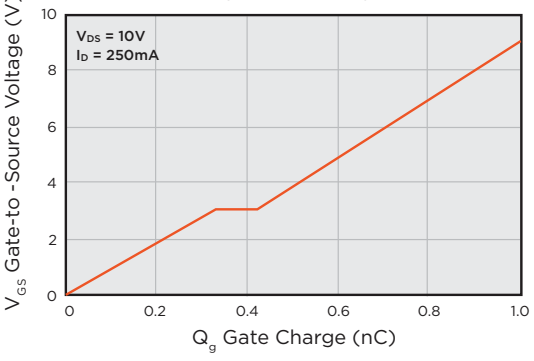
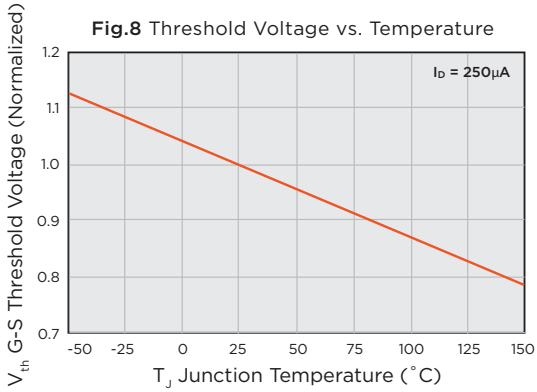


Fig.8 Threshold Voltage vs. Temperature



GRAPHS

Fig.9 Breakdown Voltage vs. Junction Temperature

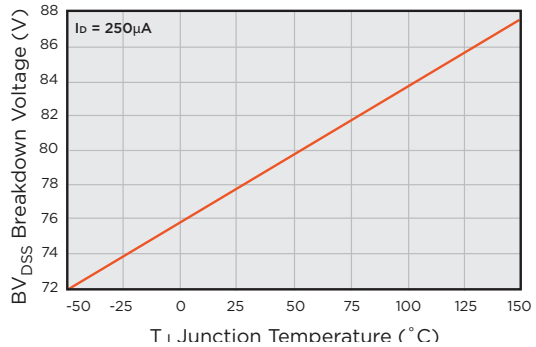


Fig.10 Source-Drain Diode Forward Voltage

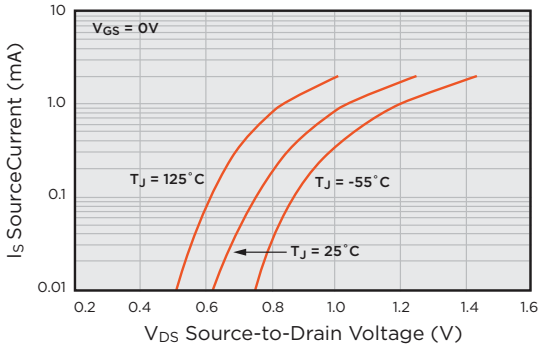
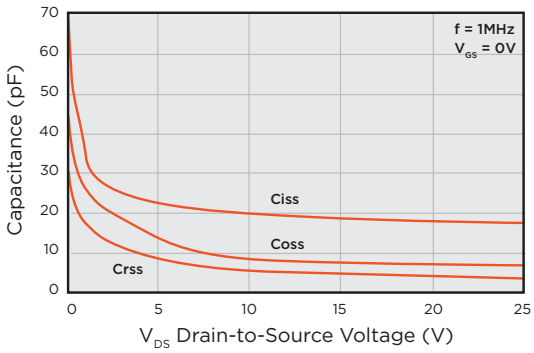


Fig.11 Capacitance vs. Drain to Source Voltage



MOUNTING PAD LAYOUT

Units: inch (mm)