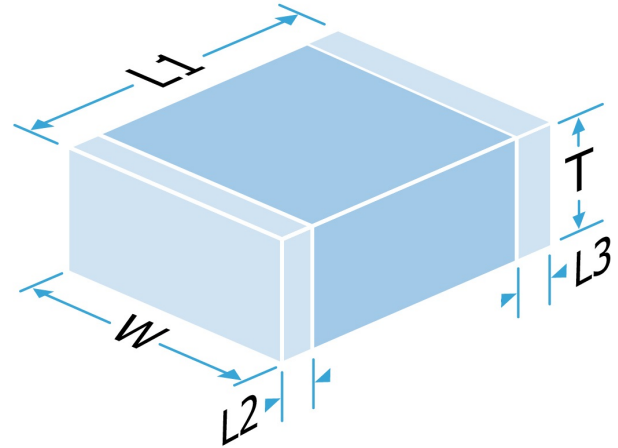


# Multilayer Ceramic Chip Capacitor

**Part Number:** 040220500103KXTFM2

**Description:** 0402 50Vdc 10nF  $\pm 10\%$  X7R - Non Mag (CTI  $\geq 600$ )

A range of X7R MLC capacitors with a guaranteed non-magnetic / relative permeability of 1.000 and having a customised design to achieve a lower ESR and improved Q factor than normal X7R MLCC's. Ideal for critical applications such as NMR / MRI and where PIM could potentially be an issue if nickel was present. These MLCC's can be used where an improved performance is required, such as blocking caps.



## Mechanical Specification

|  |   |
|--|---|
| Size Code                                  | 0402  |
| Length (L1) in mm (")                      | $1.0 \pm 0.10$ ( $0.04 \pm 0.004$ )                         |
| Width (W) in mm (")                        | $0.52 \pm 0.12$ ( $0.02 \pm 0.005$ )                        |
| Thickness (T) in mm (")                    | 0.64 Max ( $0.025$ Max)                                     |
| Minimum Termination Band (L2,L3) in mm (") | 0.10 ( $0.004$ )  |
| Maximum Termination Band (L2,L3) in mm (") | 0.40 ( $0.016$ )  |
| Termination Material                       | Copper Barrier, Sn Plated Solder (Non-Mag., RoHS compliant) |
| Solderability                              | IEC-60068-2-58  |
| Packaging                                  | 7" Reel Horizontal Orientation, 10000 per reel              |

## General Electrical Specification

|   |   |
|---|---|
| Rated Voltage   | 50Vdc   |
| Nominal Capacitance Value   | 10nF  |
| Capacitance Tolerance   | $\pm 10\%$  |
| Tangent of Loss Angle (Tan $\delta$ )                                     | $\leq 0.025$  |
| Capacitance and Tan $\delta$ Test Conditions                              | 1.0Vrms @ 1kHz  |
| Voltage Proof   | 125Vdc  |
| (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH) |   |
| Min Insulation Resistance (IR)  | 100.00GOhm @ 50Vdc                                      |
| Dielectric Classification   | X7R - Non Mag (CTI $\geq 600$ )                         |
| Rated Temperature Range   | $-55^{\circ}\text{C} / +125^{\circ}\text{C}$            |
| Maximum Capacitance Change over Temperature Range                         | No DC Voltage $\pm 15\%$<br>Rated DC Voltage -          |
| Climatic Category (IEC)   | 55/125/56   |
| Ageing Characteristic   | <2% per decade (nominal capacitance is 1000 hour value) |

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Date: Wednesday, July 02, 2025

20250702 130712022UTC

# Multilayer Ceramic Chip Capacitor

**Part Number:** 040220500103KXTFM2

**Description:** 0402 50Vdc 10nF  $\pm 10\%$  X7R - Non Mag (CTI  $\geq 600$ )

## Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

247 compliant

California Proposition 65

No exposure risk

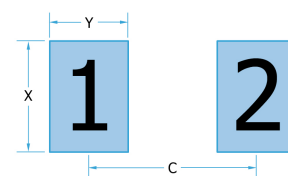
## Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

### IPC-7351 pad design

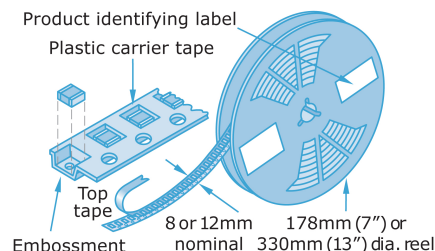
|   | 0402   |        |
|---|--------|--------|
| C | 0.90mm | 0.035" |
| Y | 0.65mm | 0.026" |
| X | 0.64mm | 0.025" |



## Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



## Soldering

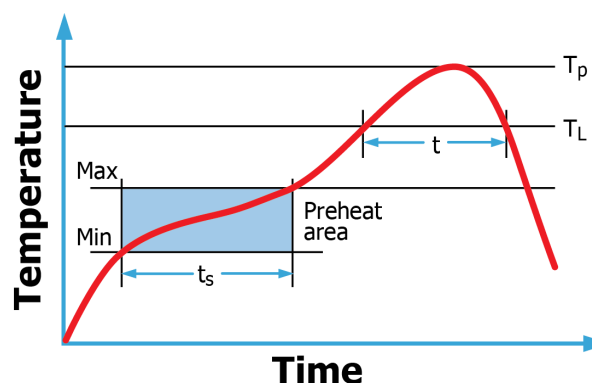
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness  $> 1.0\text{mm}$ . Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



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# Multilayer Ceramic Chip Capacitor

**Part Number:** 040220500103KXTFM2

**Description:** 0402 50Vdc 10nF  $\pm 10\%$  X7R - Non Mag  
(CTI  $\geq 600$ )

## DC Bias Characteristics

Insufficient data exists to automatically calculate dc bias data for this specific part number.

Please contact your local sales office and our engineering teams will be happy to look at requests for part specific data.

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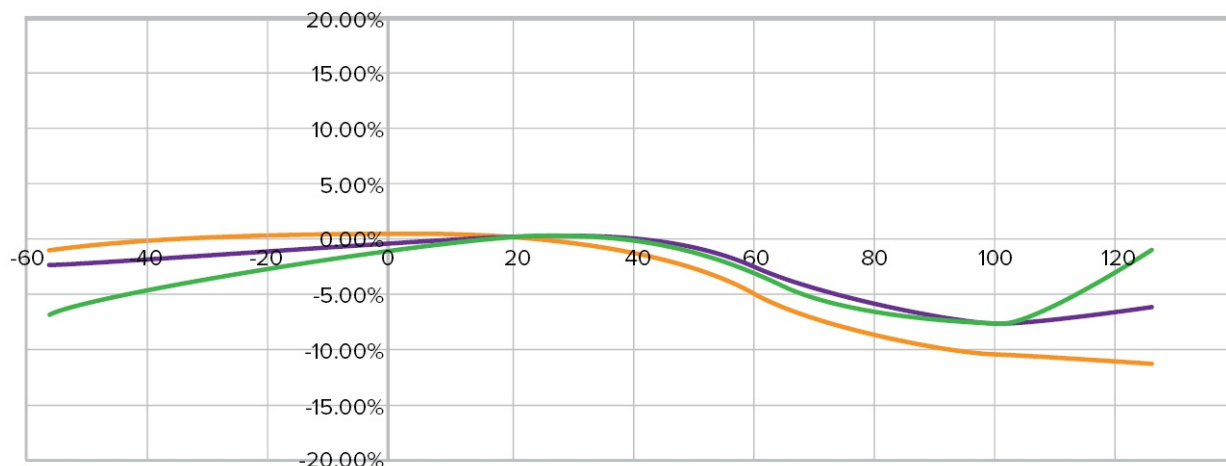
Date: Wednesday, July 02, 2025

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**Part Number:** 040220500103KXTFM2

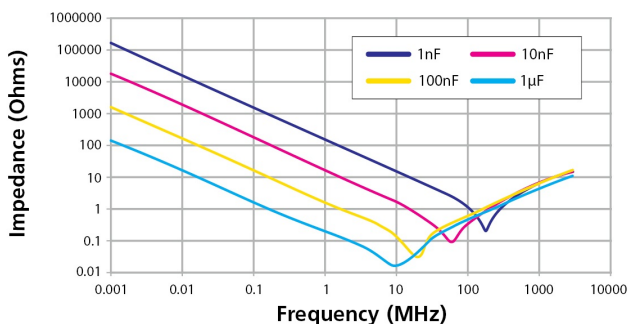
**Description:** 0402 50Vdc 10nF  $\pm 10\%$  X7R - Non Mag (CTI  $\geq 600$ )

**Typical Capacitance Change vs Temperature**

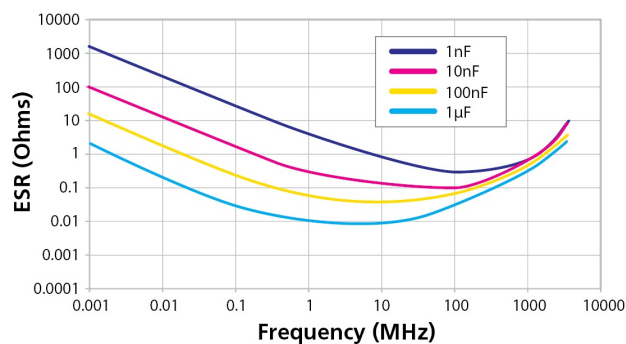


Typical TC Curves for X7R capacitors showing different dielectric types

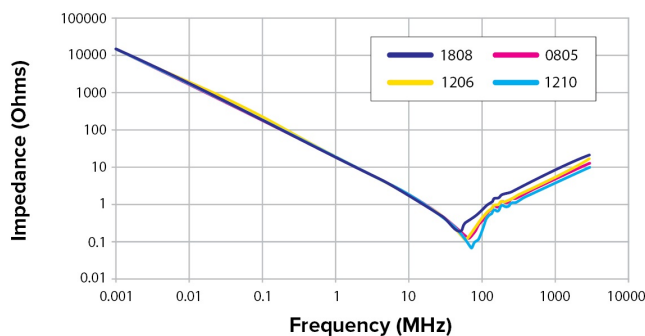
Stable X7R Dielectric



Stable X7R Dielectric



Stable X7R Dielectric — 10nF



Typical Performance Data - X7R

For part specific data, please contact your local sales office  
This data is for reference only and does not constitute a specification.

Complex

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