µClamp0551ZV

µClamp®

1-Line ESD & Surge Protection

Description

µClamp0551ZV diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They feature large cross-sectional area junctions for conducting high transient currents.

µClamp0551ZV is in a DFN 1.0 x 0.6 x 0.25mm 2-lead package. Leads are spaced at a pitch of 0.65mm. Each device will protect one unidirectional line operating at 5.5 volts. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

Features

- High ESD withstand Voltage
  - IEC 61000-4-2 (ESD): 30kV (Contact), 30kV (Air)
- Protects one I/O or power line
- High peak pulse current capability: 100A (tp = 8/20µs)
- Working voltage: 5.5V
- Low ESD clamping voltage
- Solid-state silicon-avalanche technology

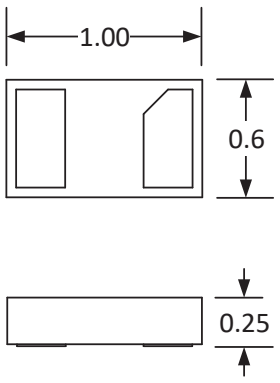
Applications

- Cellular Handsets & Accessories
- Battery Protection
- Notebooks & Handhelds
- Voltage Bus Protection

Mechanical Characteristics

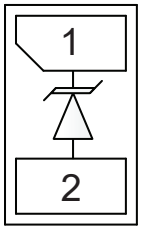
- Package : DFN 1.0 x 0.6 x 0.25mm 2-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish : Pb-Free
- Molding compound flammability rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

Package Dimension



Nominal Dimensions in mm

Functional Schematic



DFN 1.00 x 0.60 x 0.25 mm 2-Lead (Bottom View)

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20µs)	P_{PK}	1200	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	100	A
ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±30	kV
ESD per IEC 61000-4-2 (Air)(1)		±30	
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

All data taken from Pin 1 to 2 unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}				5.5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	5.8	7.0	7.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5.5V		10	100	nA
Clamping Voltage	V_C	I_{PP} = 40A, t_p = 8/20 µs		8.3	9.5	V
		I_{PP} = 100A, t_p = 8/20 µs		10.5	12.0	
ESD Clamping Voltage(2)	V_C	I_{TLP} = 4A, t_p = 0.2/100ns (TLP)		7		V
		I_{TLP} = 16A, t_p = 0.2/100ns (TLP)		7.5		
Dynamic Resistance(2),(3)	R_{DYN}	t_p = 0.2/100ns (TLP)		0.03		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		400	500	pF

Notes:

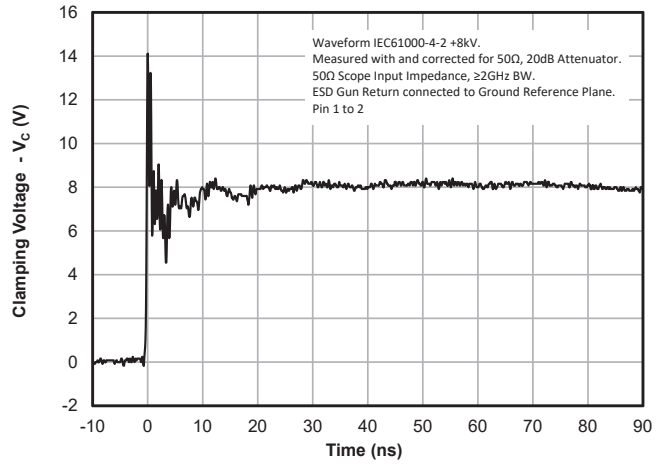
(1): ESD Gun return path to Ground Reference Plane (GRP)

(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

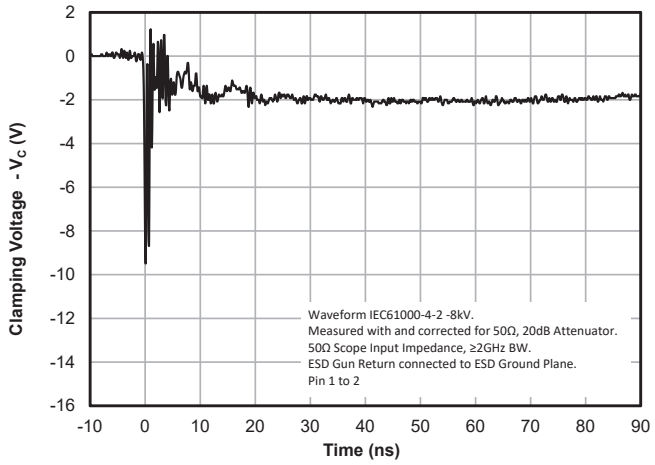
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

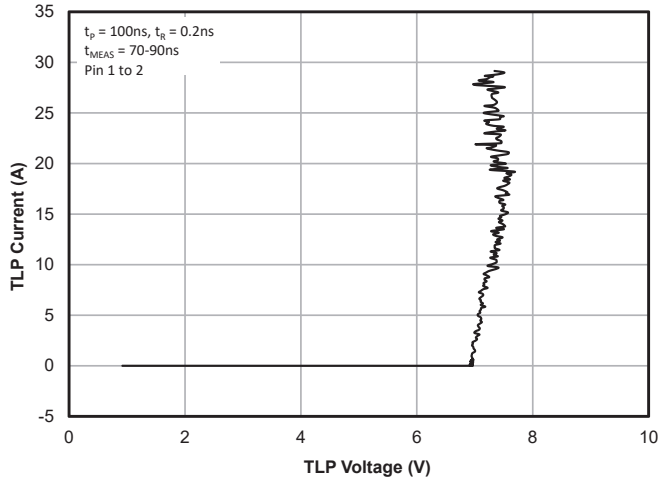
ESD Clamping (+8kV Contact per IEC 61000-4-2)



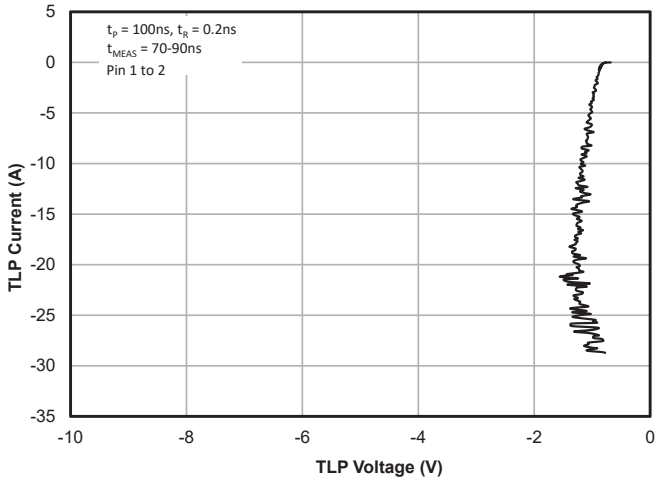
ESD Clamping (-8kV Contact per IEC 61000-4-2)



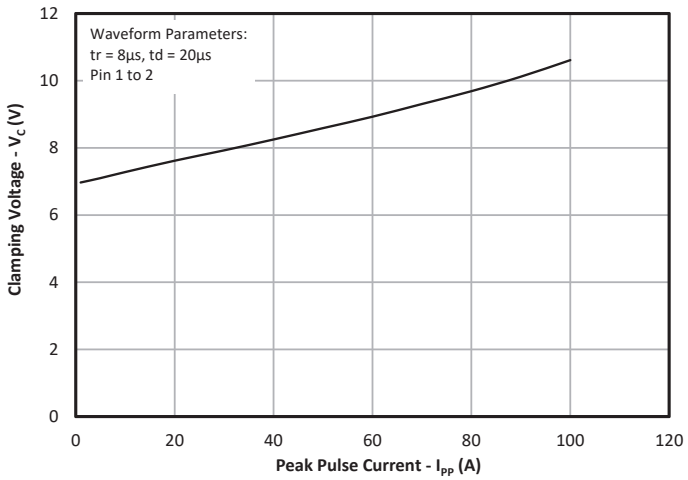
TLP Characteristics (Positive Pulse)



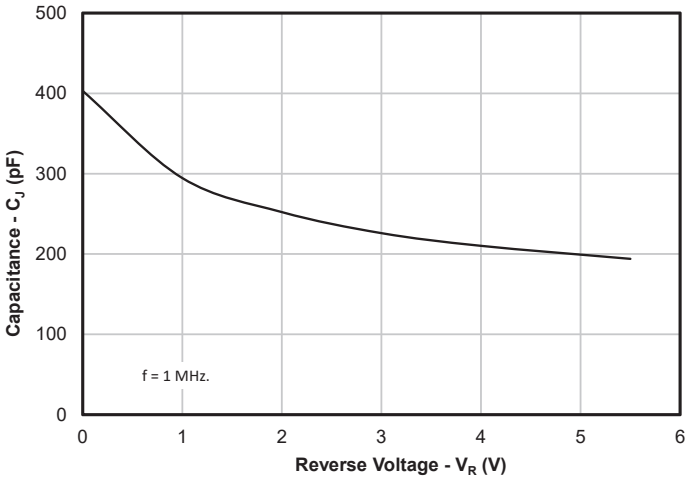
TLP Characteristics (Negative Pulse)



Surge Clamping Characteristic (tp= 8/20µs)



Capacitance vs. Reverse Voltage



Applications Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors determining the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.100mm (0.004") or 0.125mm (0.005") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern

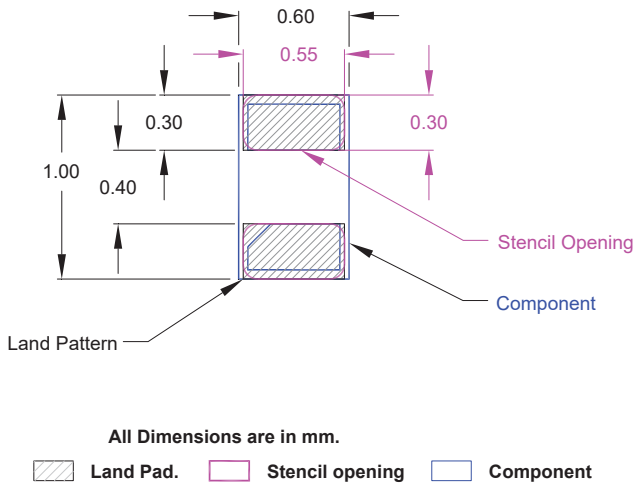
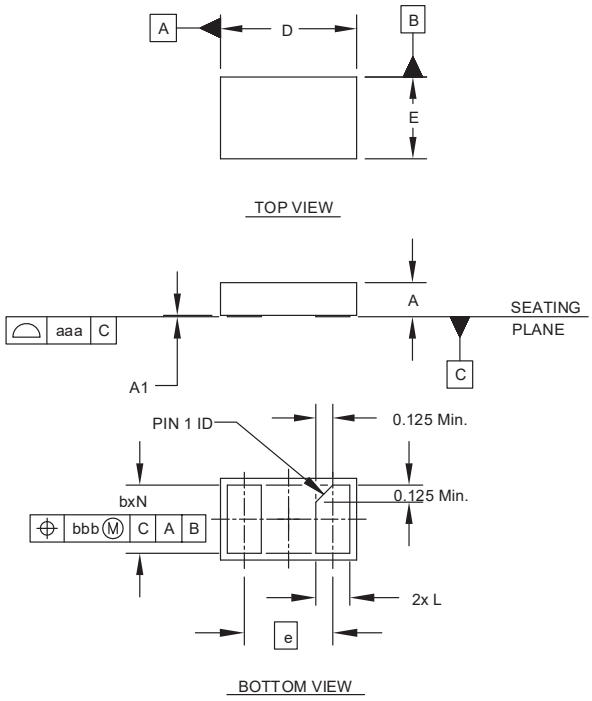


Figure 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.100mm (0.004") or 0.125mm (0.005")
Solder Paste Type	Type 4 or Type 5
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	SMD or NSMD
PCB Pad Finish	OSP or NiAu

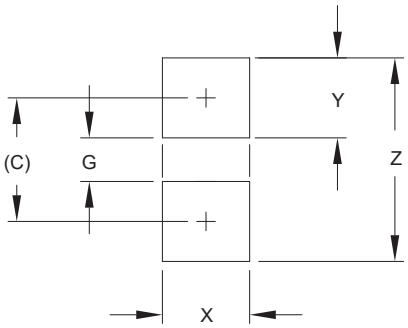
Outline Drawing - DFN 1.00 x 0.60 x 0.25mm 2-Lead



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.00	0.010	0.050
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

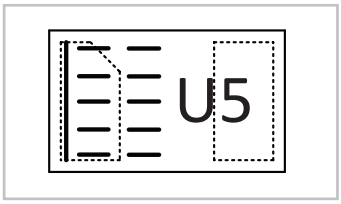
Landing Pattern - DFN 1.00 x 0.60 x 0.25mm 2-Lead



DIMENSIONS	
DIM	MILLIMETERS
C	(0.85)
G	0.30
X	0.60
Y	0.55
Z	1.40

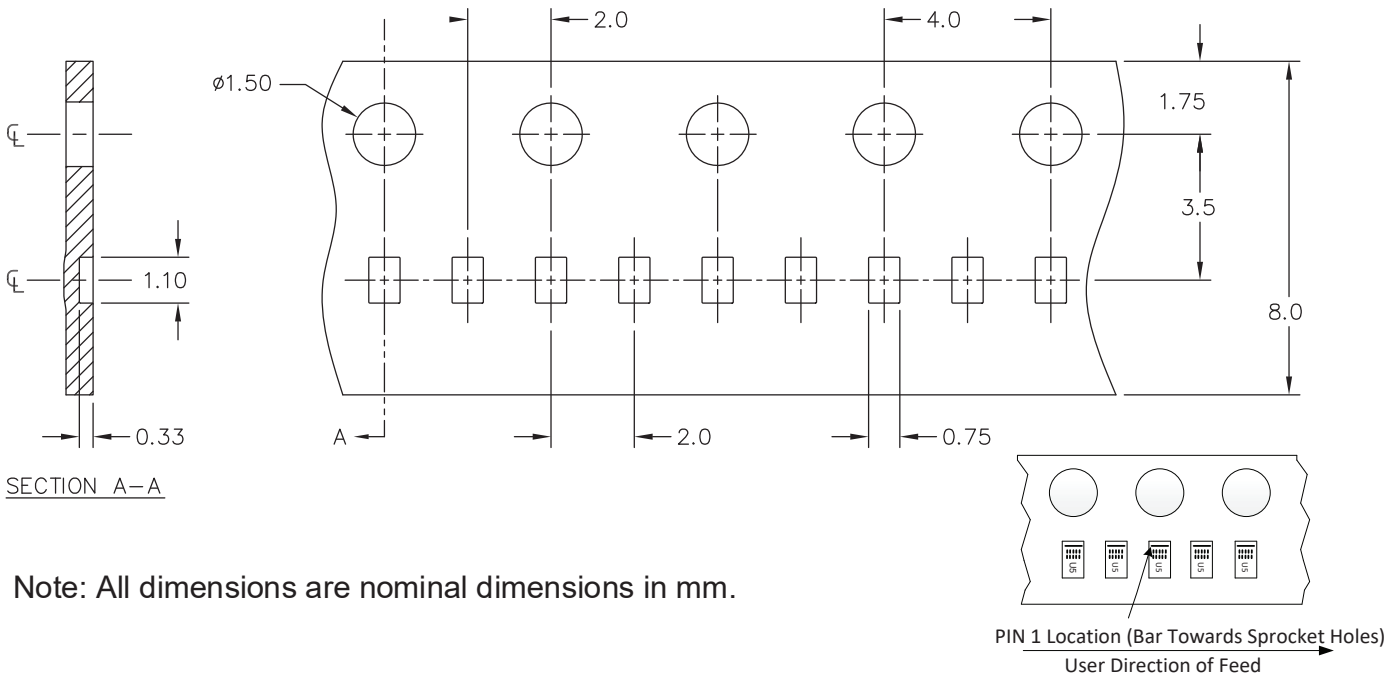
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes:
(1) Marking will also include line matrix date code
(2) Bar indicates Pin 1 location

Tape and Reel Specification



Note: All dimensions are nominal dimensions in mm.

Order Information

PART NUMBER	QTY PER REEL	REEL SIZE
µClamp0551ZV.F	15,000	7"

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