

Description

RClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD & EOS. RClamp1251ZA features extremely good ESD protection characteristics highlighted by low typical dynamic resistance of 0.08 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (+/-20kV contact per IEC 61000-4-2). Low maximum capacitance (0.6pF at $V_R=0V$) minimizes loading on sensitive circuits.

RClamp1251ZA Leads have a lead free finish. The combination of small size and high ESD surge capability makes them ideal for use in portable applications.

Applications

- USB 3.0/ USB 3.1 Gen 1
- USB Type-C
- MIPI/MDDI
- MHL
- FM antenna
- Wearables

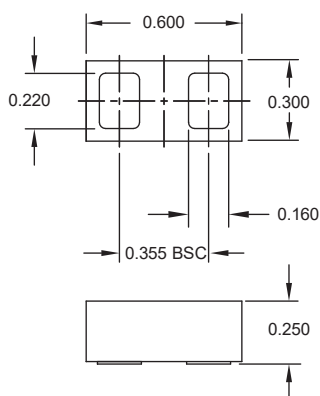
Features

- High ESD withstand Voltage
 - IEC 61000-4-2 (ESD): $\pm 20kV$ (Contact), $\pm 25kV$ (Air)
 - IEC 61000-4-5 (Lightning): 20A ($t_p = 8/20\mu s$)
- Ultra-small package
- Protects one data line
- Low ESD clamping voltage
- Working voltage: 12V
- Low capacitance: 0.6pF maximum
- Low leakage current
- Low dynamic resistance: 0.08Ω (typ)
- Solid-state silicon-avalanche technology

Mechanical Characteristics

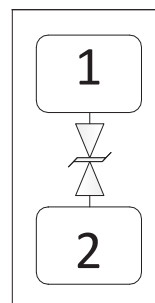
- Package: DFN 0.60x0.30x0.25mm-2 Lead
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Lead Finish: Pb-Free
- Marking: Marking code
- Packaging: Tape and Reel

Package Dimension



Nominal Dimensions in mm

Schematic & Pin Configuration



DFN 0.60 x 0.30 x 0.25mm 2-Lead (Bottom View)

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20μs)	P_{PK}	130	W
Peak Pulse Current (tp = 8/20μs)	I_{PP}	20	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	±20	kV
ESD per IEC 61000-4-2 (Air) ⁽¹⁾		±25	
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	13	14.8	18	V
Reverse Leakage Current	I_R	$V_{RWM} = 12V$		<10	50	nA
Clamping Voltage ⁽²⁾	V_C	tp = 1.2/50μs (Voltage), 8/20μs (Current) Combination Waveform, $R_s = 2\ \Omega$, $I_{PP} = 20A$		5.4	6.5	V
ESD Clamping Voltage ⁽³⁾	V_C	$I_{TLP} = 4A$, $t_p = 0.2/100ns$ (TLP)		2.8		V
		$I_{TLP} = 16A$, $t_p = 0.2/100ns$ (TLP)		3.7		
Dynamic Resistance ^{(3),(4)}	R_{DYN}	$t_p = 0.2/100ns$ (TLP)		0.08		Ω
Junction Capacitance	C_J	$V_R = 0V$, $f = 1MHz$		0.42	0.6	pF

Notes:

(1) ESD gun return path connected to ESD ground plane.

(2) Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, $R_s = 2\ \Omega$. Clamping is defined as the clamping voltage after the device snaps back to a conducting state.

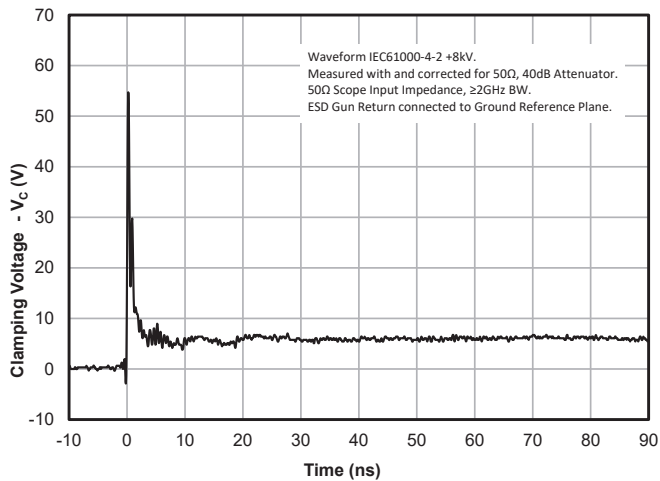
(3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

(4) Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$

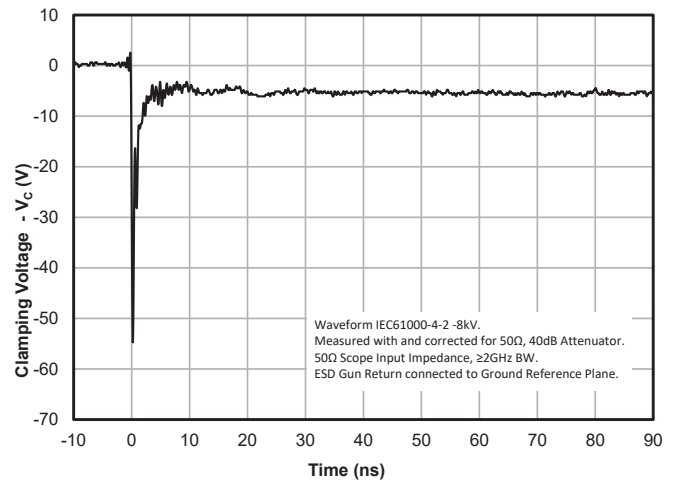
(5): This device was tested and characterized for 15V DC operation.

Typical Characteristics

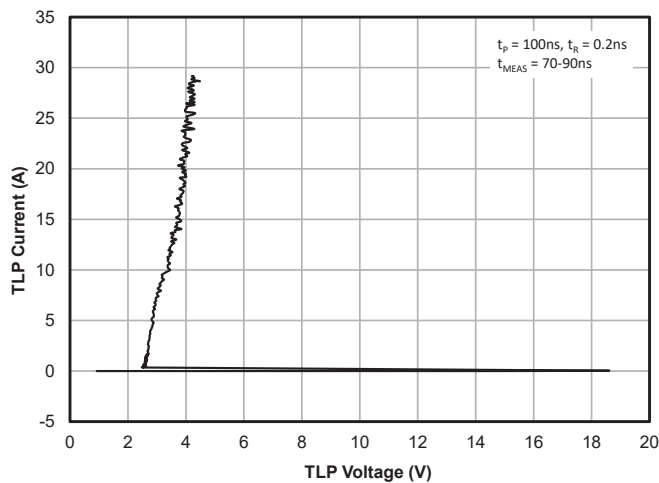
ESD Clamping (8kV Contact per IEC 61000-4-2)



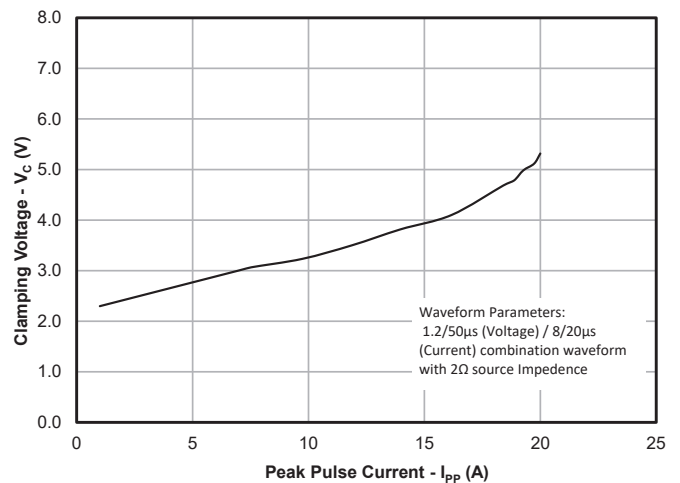
ESD Clamping (-8kV Contact per IEC 61000-4-2)



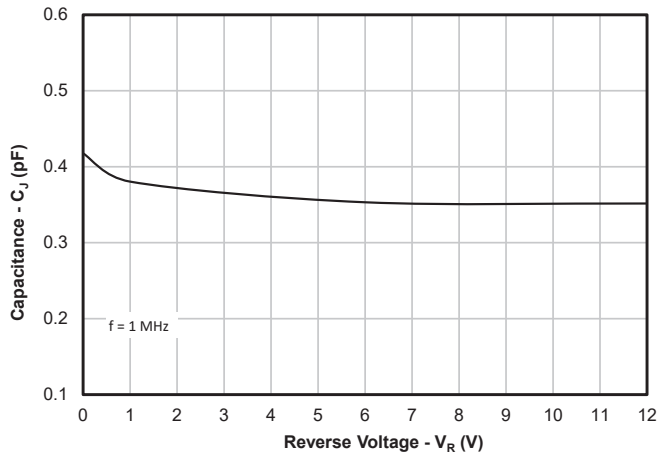
TLP Characteristics (Positive Pulse)



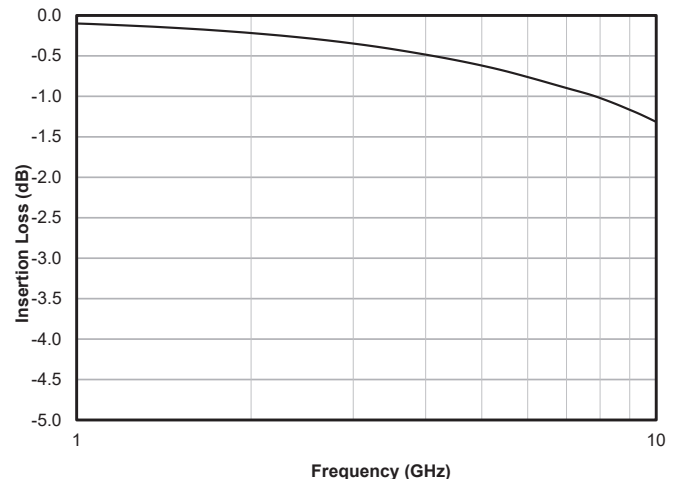
Clamping Voltage Waveform ($t_p=1.2/50\mu$ s)



Capacitance vs. Reverse Voltage



Insertion Loss - S21



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

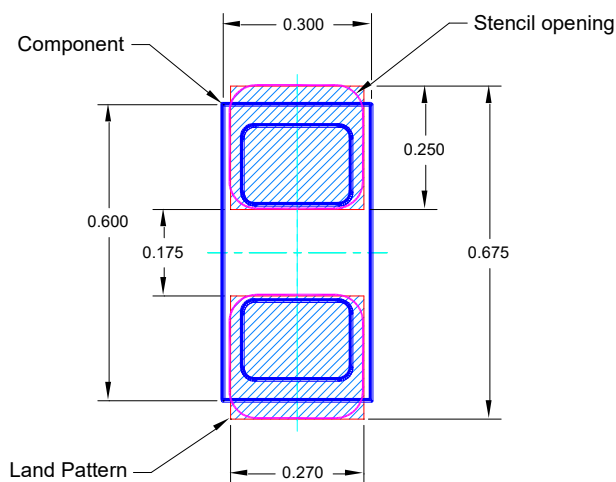
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended.

Recommended Mounting Pattern



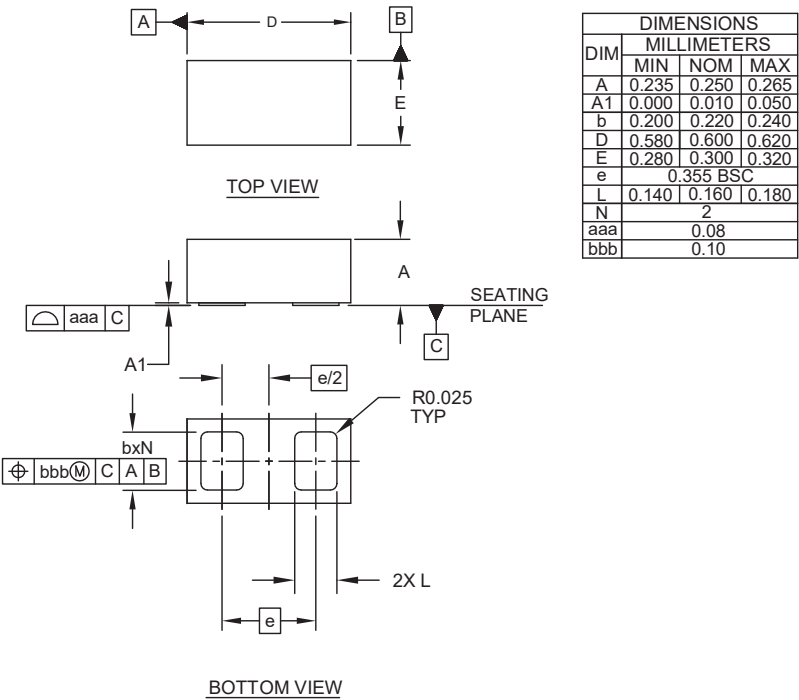
All Dimensions are in mm.

Land Pad. Stencil opening Component

Table 1 - Assembly Guidelines

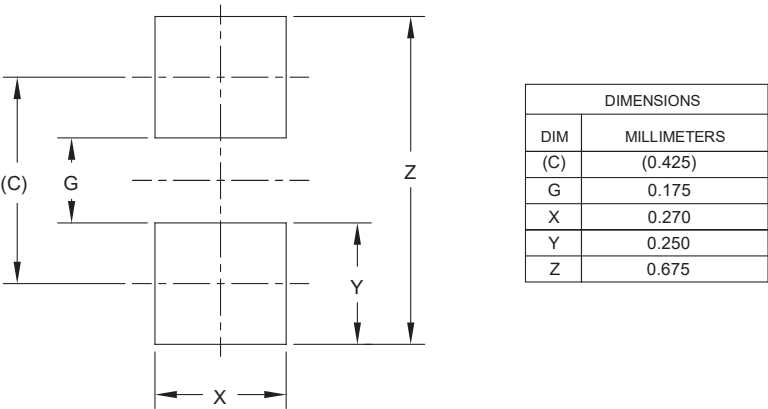
Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 0.60 x 0.30 x 0.25mm 2-Lead



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Landing Pattern - DFN 0.60 x 0.30 x 0.25mm 2-Lead



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.



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