µClamp1221ZA

Ultra Small µClamp®
1-Line ESD and EOS Protection

Description

µClamp1221ZA is specifically designed to protect sensitive electronics from damage or latch-up due to ESD and surge. It features large cross-sectional area junctions for conducting high transient currents. µClamp1221ZA offers desirable characteristics for board level protection, including fast response time, low operating and clamping voltage, and no device degradation.

µClamp1221ZA is in a DFN 0.60 x 0.30 x 0.25mm 2-Lead package. Leads are finished with Pb-Free. Each device will protect one line operating at 12 volts.

Features

- High ESD withstand Voltage
  - IEC 61000-4-2 (ESD): ±30kV (Contact), ±30kV (Air)
  - IEC 61000-4-5 (Lightning): 15A (8/20µs)
- Protects one data line or power line
- Ultra-small package
- Low leakage current: <50nA (V_R=12V)
- Working voltage: ±12V
- Low dynamic resistance: 0.13 Ω (typical)
- Solid-State Silicon-Avalanche Technology

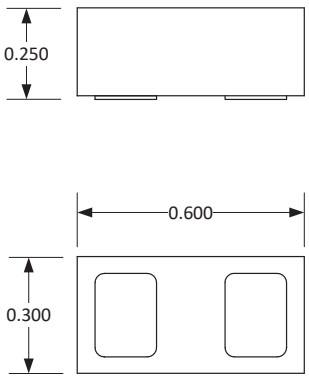
Applications

- USB Type-C (CC/SBU lines)
- Cellular Handsets & Accessories
- Computers and peripherals
- Notebooks
- Portable Instruments

Mechanical Characteristics

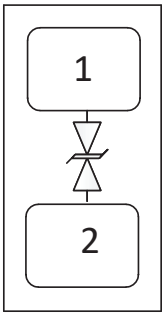
- Package: DFN 0.60 x 0.30 x 0.25mm 2-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking: Marking Code
- Packaging: Tape and Reel

Package Dimension



Nominal Dimensions in mm

Schematic & Pin Configuration



DFN 0.60 x 0.30 x 0.25mm 2-Lead (Bottom View)

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp = 8/20µs)	P_{PK}	285	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	15	A
ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±30	kV
ESD per IEC 61000-4-2 (Air)(1)		±30	
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	13	14.2	16	V
Reverse Leakage Current	I_R	V_{RWM} = 12V			50	nA
Holding Voltage	V_H	t_p = 0.2/100ns (TLP)	12			V
Clamping Voltage	V_C	I_{PP} = 15A, t_p = 8/20 µs		16.2	19	V
ESD Clamping Voltage(2)	V_C	I_{TLP} = 4A, t_p = 0.2/100ns (TLP)		13.2		V
		I_{TLP} = 16A, t_p = 0.2/100ns (TLP)		14.7		
Dynamic Resistance(2),(3)	R_{DYN}	t_p = 0.2/100ns (TLP)		0.13		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		23.5	30	pF

Notes:

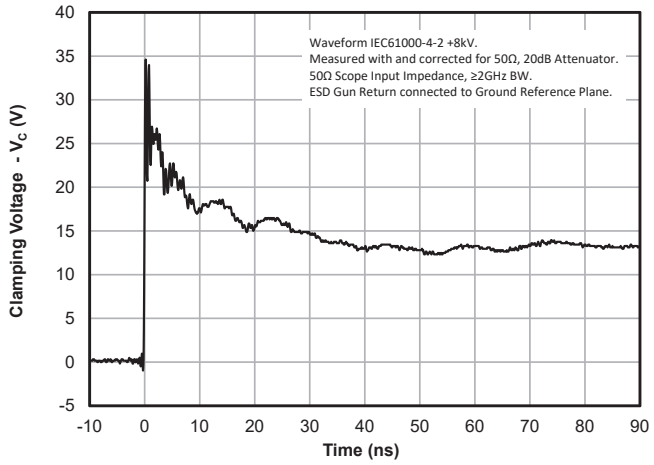
(1): ESD Gun return path to Ground Reference Plane (GRP).

(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

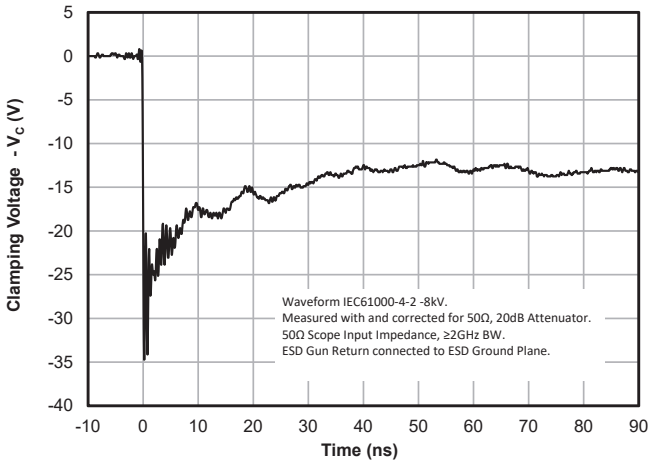
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A.

Typical Characteristics

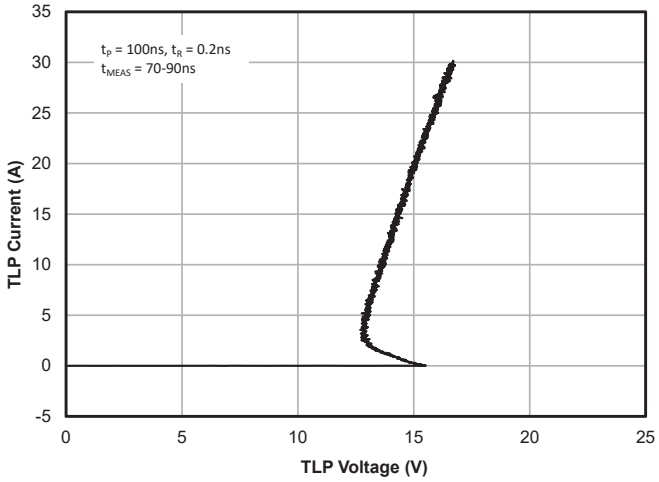
ESD Clamping (+8kV Contact per IEC 61000-4-2)



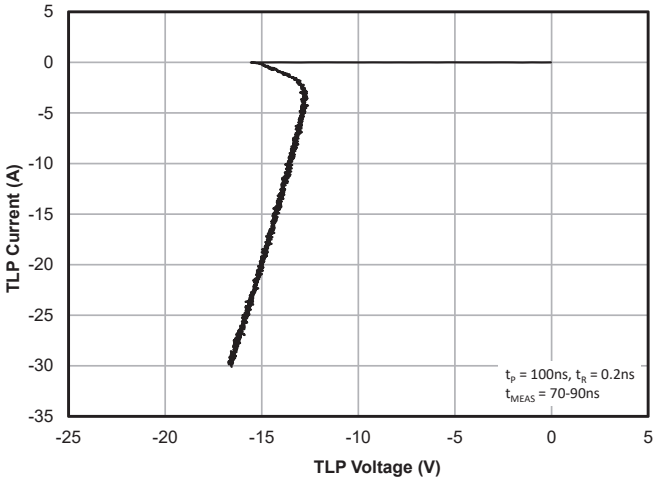
ESD Clamping (-8kV Contact per IEC 61000-4-2)



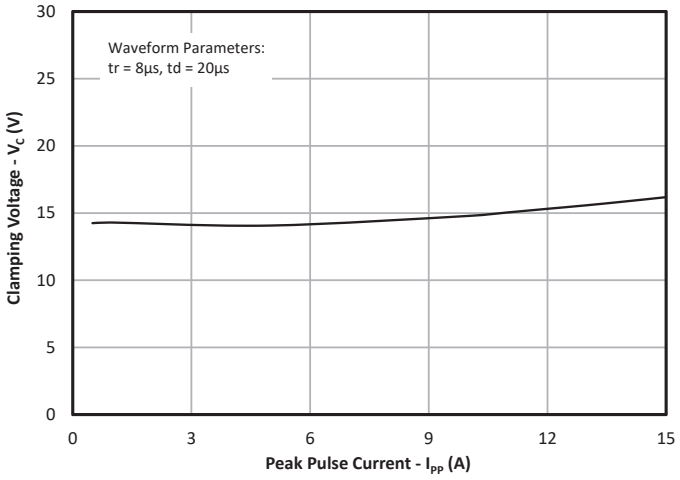
TLP Characteristics (Positive Pulse)



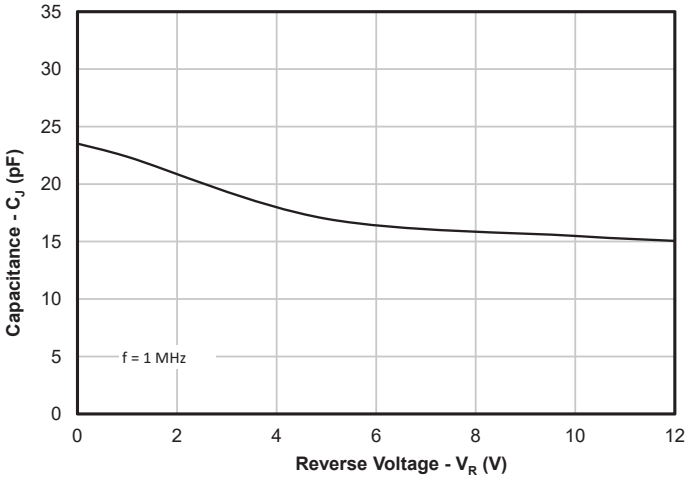
TLP Characteristics (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current (tp=8/20 µs)



Capacitance vs. Reverse Voltage



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended.

Recommended Mounting Pattern

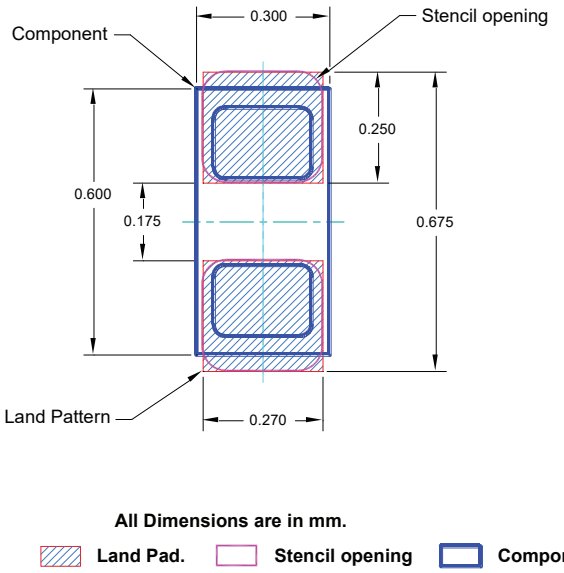
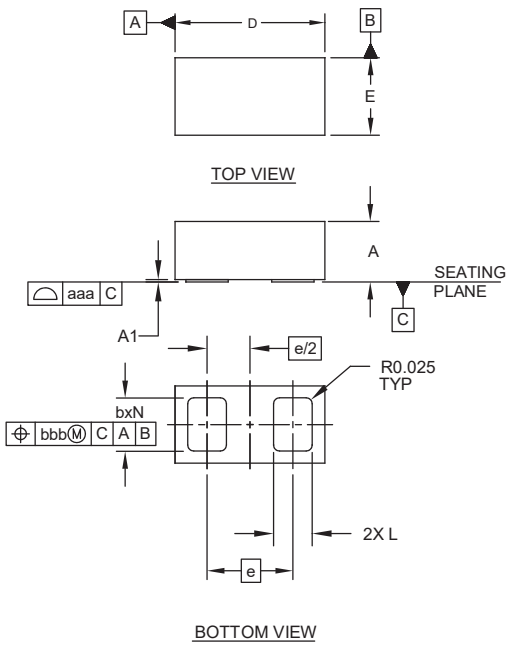


Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

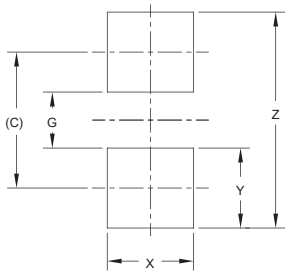
Outline Drawing - DFN 0.60 x 0.30 x 0.25mm 2-Lead



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Landing Pattern - DFN 0.60 x 0.30 x 0.25mm 2-Lead



DIMENSIONS	
DIM	MILLIMETERS
(C)	(0.425)
G	0.175
X	0.270
Y	0.250
Z	0.675

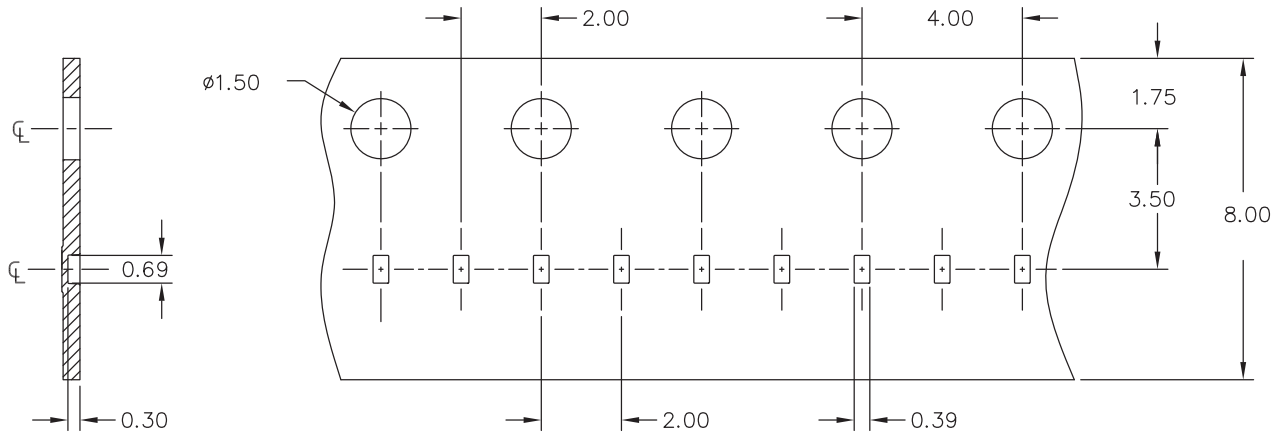
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

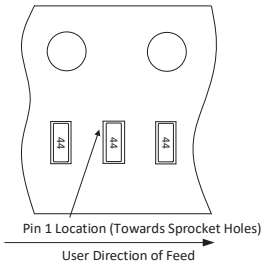
Marking Code

Note: Device is electrically symmetrical.

Tape and Reel Specification



Note: All dimensions are nominal dimensions in mm.



Order Information

PART NUMBER	QTY PER REEL	REEL SIZE
µClamp1221ZA.F	15,000	7"

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