RDIMM DDR5 5600 16GB Datasheet

(SQR-RD5N16G5K6HZZG)

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Revision History

Rev	Date	Modification
1.0	27th June, 2024	Official release

1. Description

DDR5 R-DIMM							
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	side	ECC
SQR-RD5N16G5K6HZZG (Hynix 2Gx8(16Gb))	16GB	PC5-5600	2Gx80	10	1	2	Y

2. Features

- Key Parameter

Industry Nomenclature	tCK (ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
PC5-5600	0.357	16.00	16.00	32.00	48.00

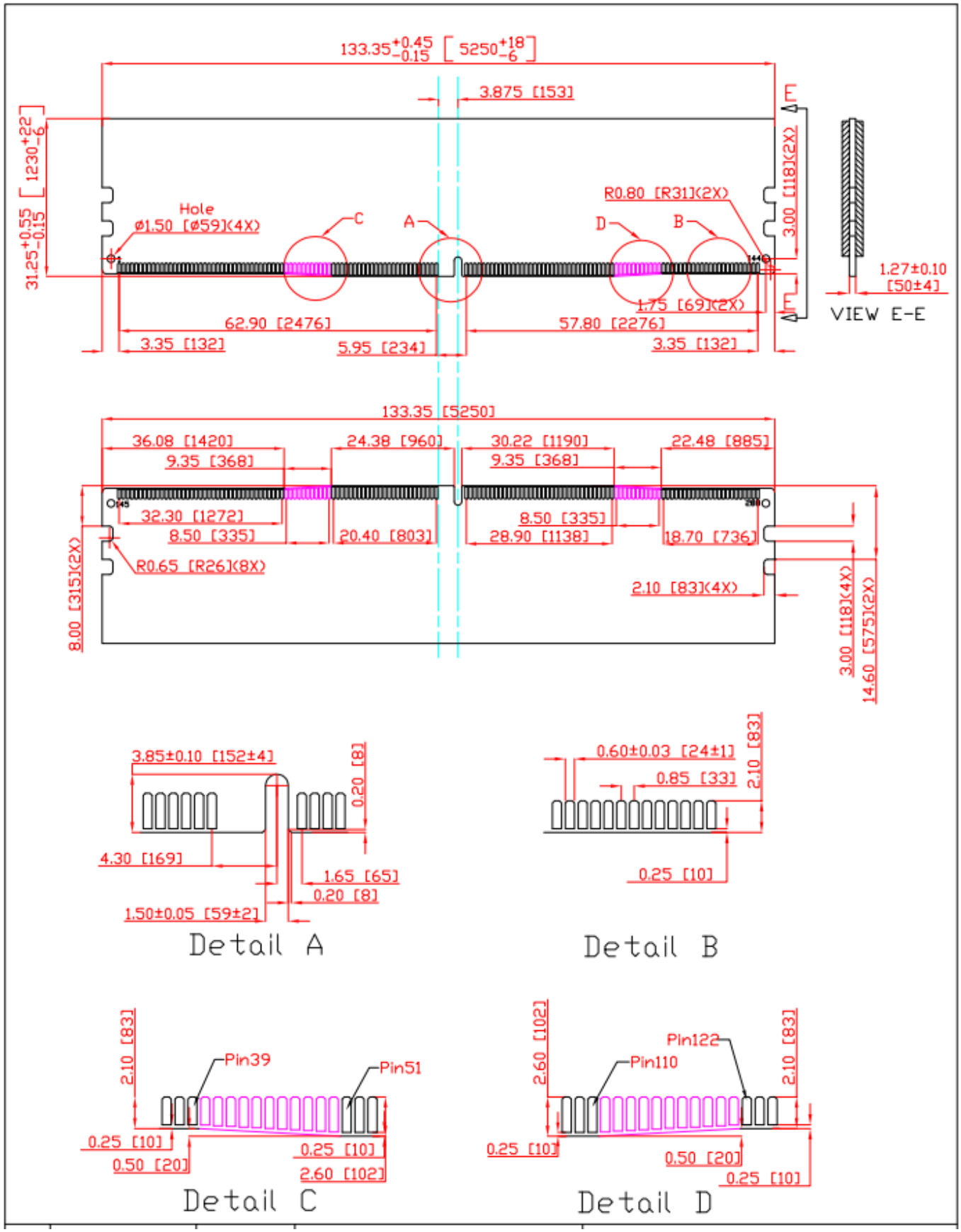
Supported Data Transfer Rate				
Industry Nomenclature	CL=36	CL=40	CL=42	CL=46
PC5-5600	4400	4800	5200	5600

- tRFC parameter by Density

Parameter	16Gb	Unit
tRFC1,min	295	ns
tRFC2,min	160	ns
tRFCsb,min	130	ns

- JEDEC Standard 288-pin Dual In-Line Memory Module
- Cl-tRCD-tRP: 46-45-45
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50
- Operating temperature Tcase: 0-95°C
  - tREFI 3.9us for 0°C ≤Tcase < 85°C
  - tREFI 1.95us for 85°C < Tcase ≤ 95°C
- On-Die ECC
- PMIC on DIMM, VIN_Bulk input supply range: 4.25V to 15.0V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

3. Dimension


133.35 +0.45 -0.15 [5250 +18 -6]
3.875 [153]
31.25 +0.55 -0.15 [1230 +22 -6]
Hole
ø1.50 [ø59](4X)
C
A
D
B
R0.80 [R31](2X)
3.00 [118](2X)
1.75 [69](2X)
62.90 [2476]
3.35 [132]
5.95 [234]
57.80 [2276]
3.35 [132]
1.27±0.10
[50±4]
VIEW E-E
133.35 [5250]
36.08 [1420]
9.35 [368]
24.38 [960]
30.22 [1190]
9.35 [368]
22.48 [885]
32.30 [1272]
8.50 [335]
20.40 [803]
8.50 [335]
28.90 [1138]
18.70 [736]
R0.65 [R26](8X)
2.10 [83](4X)
8.00 [315](2X)
3.00 [118](4X)
14.60 [575](2X)
3.85±0.10 [152±4]
0.20 [8]
4.30 [169]
1.65 [65]
0.20 [8]
1.50±0.05 [59±2]
Detail A
0.60±0.03 [24±1]
0.85 [33]
2.10 [83]
0.25 [10]
Detail B
2.10 [83]
Pin39
Pin51
0.25 [10]
0.50 [20]
0.25 [10]
2.60 [102]
Detail C
2.60 [102]
Pin122
Pin110
2.10 [83]
0.25 [10]
0.50 [20]
0.25 [10]
Detail D

Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

4. Pin Descriptions

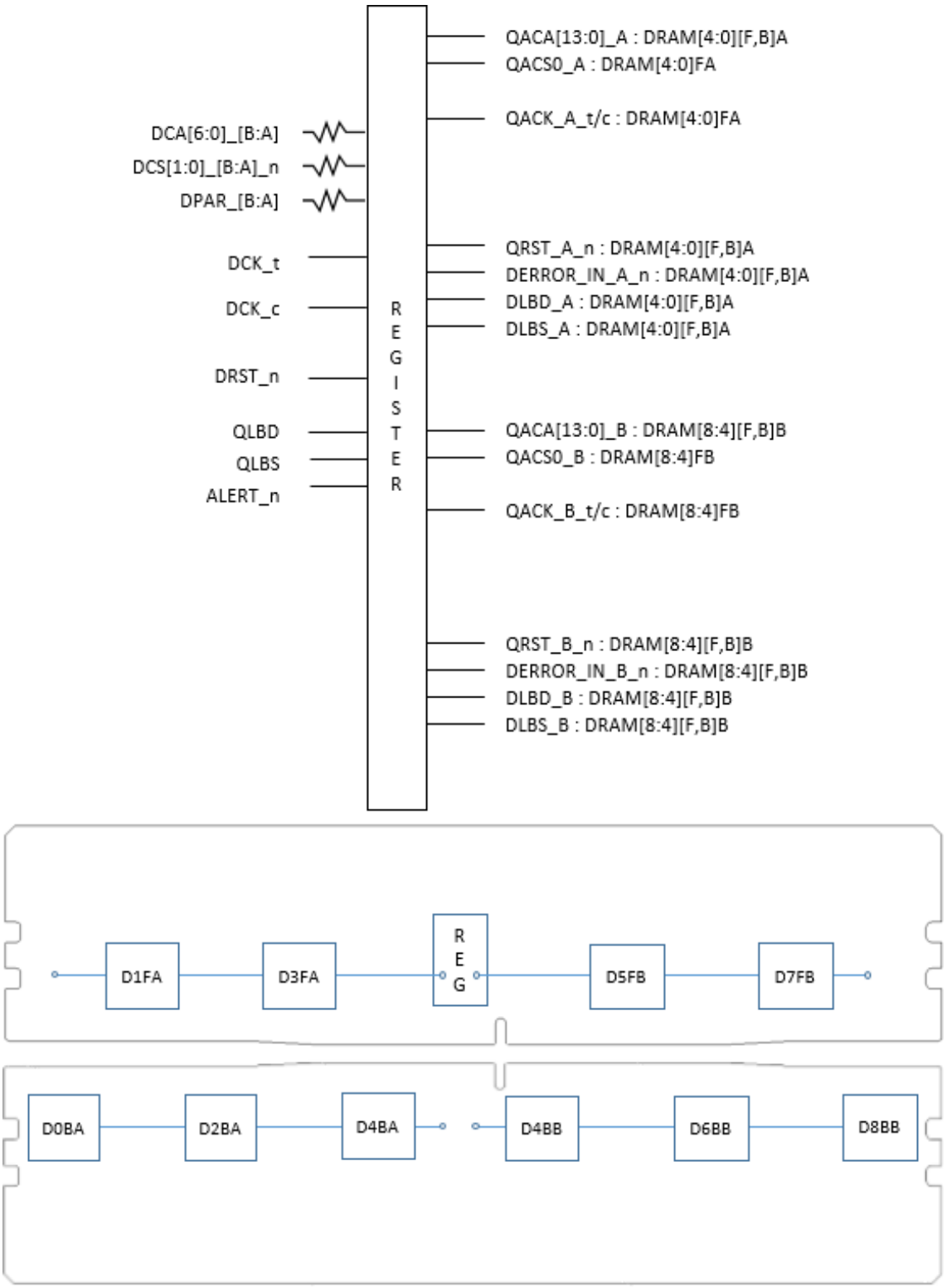
Pin Name	Description	Pin Name	Description
CA0_A - CA6_A	Register command address input to channel A. (DDR)	CA0_B - CA6_B	Register command address input to channel B. (DDR)
CS0_A_n - CS1_A_n	DIMM Rank Select Lines input for chan-nel A.	CS0_B_n - CS1_B_n	DIMM Rank Select Lines input for chan-nel B.
DQ0_A - DQ31_A	DIMM memory data bus for channel A.	DQ0_B - DQ31_B	DIMM memory data bus for channel B.
CB0_A - CB7_A	DIMM ECC check bits for channel A.	CB0_B - CB7_B	DIMM ECC check bits for channel B.
TDQS0_A_t- TDQS9_A_t	Dummy loads for mixed populations ofx4 based and x8 based RDIMMs in channel A. (positive line of differential pair)	TDQS0_B_t- TDQS9_B_t	Dummy loads for mixed populations ofx4 based and x8 based RDIMMs in channel B. (positive line of differential pair)
TDQS0_A_c- TDQS9_A_c	Dummy loads for mixed populations ofx4 based and x8 based RDIMMs in channel A. (negative line of differential pair)	TDQS0_B_c- TDQS9_B_c	Dummy loads for mixed populations ofx4 based and x8 based RDIMMs in channel B. (negative line of differentialpair)
DQS0_A_t - DQS9_A_t	Data Buffer data strobes in channel A.(positive line of differential pair)	DQS0_B_t - DQS9_B_t	Data Buffer data strobes in channel B.(positive line of differential pair)
DQS0_A_c - DQS9_A_c	Data Buffer data strobes in channel A.(negative line of differential pair)	DQS0_B_c - DQS9_B_c	Data Buffer data strobes in channel B.(negative line of differential pair)
PAR_A	Register parity input for channel A.	PAR_B	Register parity input for channel B.
RSP_A_n	Response signal for NVDIMM-P(channel A). Asynchronous, active-LOW, pulse-width modulated signal from DIMM to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists.	RSP_B_n	Response signal for NVDIMM-P(channel B). Asynchronous, active-LOW, pulse-width modulated signal from DIMM to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists.
VIN_BULK	12 V power input supply pin to the PMIC.	VSS	Power supply return (ground)
VIN_MGMT	3.3 V power input supply pin to the PMIC for VOUT_1.8V & VOUT_1.0V LDO output,side band management access, internal memory read opera-tion.	PWR_GOOD / FAIL_n	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regula- tors and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low
SCL	Side-band bus serial bus clock for SPD-Hub.	ALERT_n	Register ALERT_n output
SDA	Side-band bus serial data line for SPD-Hub.	RESET_n	Set Register and SDRAMs to a Known State
SAA	Side-band bus Host ID and Hub devicetype ID selection.	LBD	Loopback Data Inputs to register
CK_t	Register clock input (positive line of dif-ferential pair)	LBS	Loopback Strobe Inputs to register
CK_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

5. Pin Assignments

288-Pin DDR5 RDIMM Front Side						288-Pin DDR5 RDIMM Back Side					
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	12V_1	49	DQ29_A	97	VSS	145	12V_2	193	VSS	241	DQS4_B_t
2	RFU0	50	VSS	98	CB0_B	146	12V_3	194	DQ31_A	242	VSS
3	VIN_MGMT	51	CB0_A	99	VSS	147	P_GOOD/FAIL_n	195	VSS	243	CB2_B
4	HSCL	52	VSS	100	CB1_B	148	SA0	196	CB2_A	244	VSS
5	HSDA	53	CB1_A	101	VSS	149	SA1/RFU	197	VSS	245	CB3_B
6	RFU/Vpp	54	VSS	102	DQ0_B	150	VSS	198	CB3_A	246	VSS
7	RFU1	55	DQS4_A_c	103	VSS	151	DIMM_EN/RFU	199	VSS	247	DQ2_B
8	VSS	56	DQS4_A_t	104	DQ1_B	152	RFU8	200	RFU9	248	VSS
9	DQ0_A	57	VSS	105	VSS	153	VSS	201	VSS	249	DQ3_B
10	VSS	58	CS0_A_n	106	DQS0_B_c	154	DQ2_A	202	CS1_A_n	250	VSS
11	DQ1_A	59	CA0_A	107	DQS0_B_t	155	VSS	203	CA1_A	251	DM0_B_n
12	VSS	60	VSS	108	VSS	156	DQ3_A	204	VSS	252	VSS
13	DQS0_A_c	61	CA2_A	109	DQ4_B	157	VSS	205	CA3_A	253	DQ6_B
14	DQS0_A_t	62	CA4_A	110	VSS	158	DM0_A_n	206	CA5_A	254	VSS
15	VSS	63	VSS	111	DQ5_B	159	VSS	207	VSS	255	DQ7_B
16	DQ4_A	64	CA6_A	112	VSS	160	DQ6_A	208	CA7_A	256	VSS
17	VSS	65	CA8_A	113	DQ8_B	161	VSS	209	CA9_A	257	DQ10_B
18	DQ5_A	66	VSS	114	VSS	162	DQ7_A	210	VSS	258	VSS
19	VSS	67	CA10_A	115	DQ9_B	163	VSS	211	CA11_A	259	DQ11_B
20	DQ8_A	68	CA12_A	116	VSS	164	DQ10_A	212	RFU10	260	VSS
21	VSS	69	VSS	117	DM1_B_n	165	VSS	213	VSS	261	DQS1_B_c
22	DQ9_A	70	CK0_A_t	118	VSS	166	DQ11_A	214	CK1_A_t	262	DQS1_B_t
23	VSS	71	CK0_A_c	119	DQ12_B	167	VSS	215	CK1_A_c	263	VSS
24	DM1_A_n	72	VSS	120	VSS	168	DQS1_A_c	216	VSS	264	DQ14_B
25	VSS	73	CK0_B_t	121	DQ13_B	169	DQS1_A_t	217	CK1_B_t	265	VSS
26	DQ12_A	74	CK0_B_c	122	VSS	170	VSS	218	CK1_B_c	266	DQ15_B
27	VSS	75	VSS	123	DQ16_B	171	DQ14_A	219	VSS	267	VSS
28	DQ13_A	76	VDD0	124	VSS	172	VSS	220	VDD6	268	DQ18_B
29	VSS	77	VDD1	125	DQ17_B	173	DQ15_A	221	VDD7	269	VSS
30	DQ16_A	78	VDD2	126	VSS	174	VSS	222	VDD8	270	DQ19_B
31	VSS	79	VDD3	127	DQS2_B_c	175	DQ18_A	223	VDD9	271	VSS
32	DQ17_A	80	VDD4	128	DQS2_B_t	176	VSS	224	VDD10	272	DM2_B_n
33	VSS	81	VDD5	129	VSS	177	DQ19_A	225	VDD11	273	VSS
34	DQS2_A_c	82	ALERT_n	130	DQ20_B	178	VSS	226	RESET_n	274	DQ22_B
35	DQS2_A_t	83	VSS	131	VSS	179	DM2_A_n	227	VSS	275	VSS
36	VSS	84	CA12_B	132	DQ21_B	180	VSS	228	RFU11	276	DQ23_B
37	DQ20_A	85	CA10_B	133	VSS	181	DQ22_A	229	CA11_B	277	VSS
38	VSS	86	VSS	134	DQ24_B	182	VSS	230	VSS	278	DQ26_B
39	DQ21_A	87	CA8_B	135	VSS	183	DQ23_A	231	CA9_B	279	VSS
40	VSS	88	CA6_B	136	DQ25_B	184	VSS	232	CA7_B	280	DQ27_B
41	DQ24_A	89	VSS	137	VSS	185	DQ26_A	233	VSS	281	VSS
42	VSS	90	CA4_B	138	DM3_B_n	186	VSS	234	CA5_B	282	DQS3_B_c
43	DQ25_A	91	CA2_B	139	VSS	187	DQ27_A	235	CA3_B	283	DQS3_B_t
44	VSS	92	VSS	140	DQ28_B	188	VSS	236	VSS	284	VSS
45	DM3_A_n	93	CA0_B	141	VSS	189	DQS3_A_c	237	CA1_B	285	DQ30_B
46	VSS	94	CS0_B_n	142	DQ29_B	190	DQS3_A_t	238	CS1_B_n	286	VSS
47	DQ28_A	95	VSS	143	VSS	191	VSS	239	VSS	287	DQ31_B
48	VSS	96	RFU5	144	VDD_SENSE	192	DQ30_A	240	DQS4_B_c	288	VSS

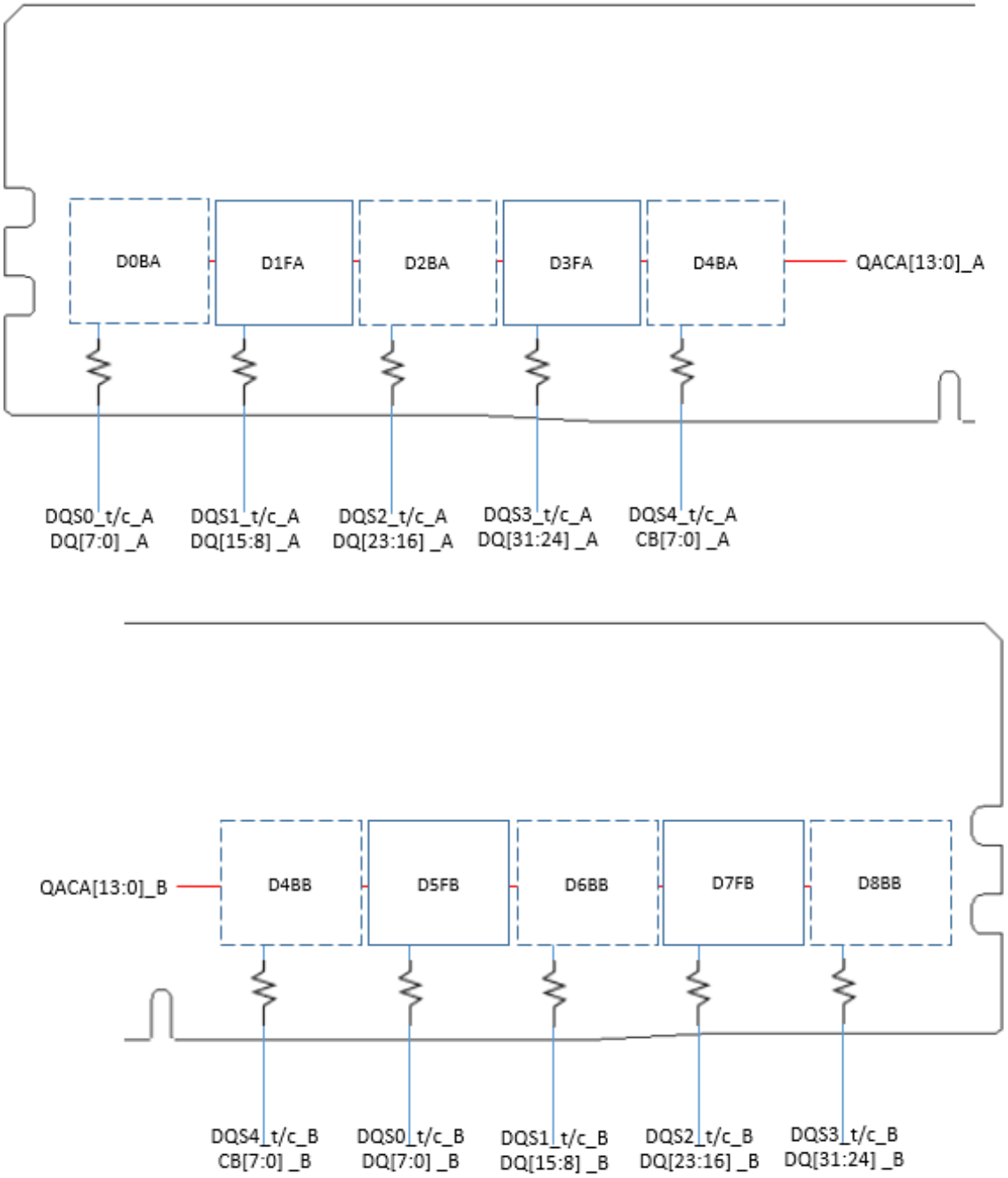
6. Block Diagram

16GB 2Gx80 Module (1Rank of x8) RDIMM



Note :

1. Unless otherwise noted resistors are 15 Ω±5 %.



Note :

1. Unless otherwise noted, resistor values are 15 Ω ±5%.
2. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

7. Thermal Characteristics

Symbol	Parameter		Rating	Units	Note
T_C	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2,3
		Extended Temp.	85 to 95	°C	1,2,3,4
T_{STG}	Storage Temperature		-55 to 100	°C	5
HSTG	Non-operating storage relative humidity (non-condensing)		5 to 95	%	

Note:
1. Maximum operating case temperature; Tc is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum Tc during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum Tc during operation.
4. If Tc exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

8. IDD, IDDQ and IPP Specifications

Symbol	Description	Value (Typical)		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current	878	69	mA
IDD0F	Operating Four Bank Active-Precharge Current	1220	140	mA
IDD2N	Precharge Standby Current	760	40	mA
IDD2P	Precharge Power-Down Current	681	35	mA
IDD3N	Active Standby Current	1450	149	mA
IDD3P	Active Power-Down Current	1370	138	mA
IDD4R	Operating Burst Read Current	3003	180	mA
IDD4W	Operating Burst Write Current	3380	206	mA
IDD5B	Burst Refresh Current (Normal Refresh Mode)	2540	450	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	1320	450	mA
IDD6E	Self Refresh Current: Extended Temperature Range	763	85	mA
IDD7	Operating Bank Interleave Read Current	3370	528	mA
IDD8	Maximum Power Saving Deep Power Down Current	510	35	mA

9. Timing Parameters

Parameter	Symbol	5600		6000		6400		Unit
		Min	Max	Min	Max	Min	Max	
Clock Timing								
Average clock period	tCK,AVG	0.357		0.333		0.312		ns
Command and Address Timing								
Read to Read command delay for same bank group	tCCD_L	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
WRITE to WRITE command delay for same bank group	tCCD_L_WR	32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		nCK
WRITE to WRITE command delay for same bank group, second WRITE not RMW	tCCD_L_WR2	16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		nCK
Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF	tCCD_S	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	tRRD_S,2K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	tRRD_S,1K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	tRRD_L,2K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	tRRD_L,1K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
Four activate window for 2KB page size	tFAW,2K	40nCK, 14.280ns (MAX)		40nCK, 13.333ns (MAX)		40nCK, 12.500ns (MAX)		ns
Four activate window for 1KB page size	tFAW,1K	32nCK, 11.428ns (MAX)		32nCK, 10.666ns (MAX)		32nCK, 10.000ns (MAX)		ns
Delay from start of internal WRITE transaction to internal READ command for different bank group	tWTR_S	2.5		2.5		2.5		ns
Delay from start of internal WRITE transaction to internal READ command for same bank group	tWTR_L	10		10		10		ns
Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank	tWTRA	tWR-tRTP		tWR-tRTP		tWR-tRTP		ns
Internal READ command to PRECHARGE command delay	tRTP	7.5		7.5		7.5		ns
PRECHARGE to PRECHARGE delay	tPPD	2		2		2		nCK
WRITE recovery time	tWR	30		30		30		ns

10. SPD

Byte Number	Function Described	Function supported	Hex Value
0	Number of Bytes in SPD Device	1024 Bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	RDIMM	01
4	First SDRAM Density and Package	Monolithic 16Gb	04
5	First SDRAM Addressing	10 columns/16 rows	00
6	First SDRAM I/O Width	x8	20
7	First SDRAM Bank Groups & Banks Per Bank Group	8BGs / 4Banks per BG	62
8	Second SDRAM Density and Package	N/A	00
9	Second SDRAM Addressing	N/A	00
10	Second SDRAM I/O Width	N/A	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	N/A	00
12	SDRAM BL32 & Post Package Repair	BL32 supported /sPPR Undo/Lock not supported	10
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for 4-phase internal clock(s)	02
14	SDRAM Fault Handling	Writeback suppression supported/ Bounded Fault supported	05
15	Reserved	Reserved	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	Standard	00
20	SDRAM Minimum Cycle Time (t_{CKAVG}min), Least Significant Byte	357ps	65
21	SDRAM Minimum Cycle Time (t_{CKAVG}min), Most Significant Byte	357ps	01
22	SDRAM Maximum Cycle Time (t_{CKAVG}max), Least Significant Byte	1010ps	F2
23	SDRAM Maximum Cycle Time (t_{CKAVG}max), Most Significant Byte	1010ps	03
24	CAS Latencies Supported, First Byte	22,26,28,30,32,36,40,42,46,50	7A
25	CAS Latencies Supported, Second Byte	22,26,28,30,32,36,40,42,46,50	AD
26	CAS Latencies Supported, Third Byte	22,26,28,30,32,36,40,42,46,50	00
27	CAS Latencies Supported, Fourth Byte	22,26,28,30,32,36,40,42,46,50	00
28	CAS Latencies Supported, Fifth Byte	22,26,28,30,32,36,40,42,46,50	00
29	Reserved	Reserved	00
30	SDRAM Minimum CAS Latency Time (t_{AA}min), Least Significant Byte	16000ps	80
31	SDRAM Minimum CAS Latency Time (t_{AA}min), Most Significant Byte	16000ps	3E
32	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Least Significant Byte	16000ps	80
33	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Most Significant Byte	16000ps	3E
34	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Least Significant Byte	16000ps	80
35	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Most Significant Byte	16000ps	3E
36	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	32000ps	00

37	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Most Significant Byte	32000ps	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	48000ps	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Most Significant Byte	48000ps	BB
40	SDRAM Minimum Write Recovery Time (t_{WR}min), Least Significant Byte	30000ps	30
41	SDRAM Minimum Write Recovery Time (t_{WR}min), Most Significant Byte	30000ps	75
42	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Least Significant Byte	295ns	27
43	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Most Significant Byte	295ns	01
44	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Least Significant Byte	160ns	A0
45	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Most Significant Byte	160ns	00
46	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}min, t_{RFCsb}_slr min), Least Significant Byte	130ns	82
47	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}_dlr min), Most Significant Byte	130ns	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Least Significant Byte	N/A	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Most Significant Byte	N/A	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Least Significant Byte	N/A	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Most Significant Byte	N/A	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Least Significant Byte	N/A	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Most Significant Byte	N/A	00
54	SDRAM Refresh Management, First Byte, First SDRAM	N/A	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	N/A	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	N/A	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	N/A	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	N/A	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	N/A	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	N/A	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	N/A	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	N/A	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	N/A	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	N/A	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	N/A	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	N/A	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	N/A	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	N/A	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	N/A	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Least Significant Byte	5000ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Most Significant Byte	5000ps	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Lower Clock Limit	8nCK	08

73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Least Significant Byte	5000ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Most Significant Byte	5000ps	13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	8nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Least Significant Byte	20000ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Most Significant Byte	20000ps	4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Lower Clock Limit	32nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Least Significant Byte	10000ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Most Significant Byte	10000ps	27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Lower Clock Limit	16nCK	10
82	SDRAM Minimum Four Activate Window (t_{FAW}min), Least Significant Byte	11428ps	A4
83	SDRAM Minimum Four Activate Window (t_{FAW}min), Most Significant Byte	11428ps	2C
84	SDRAM Minimum Four Activate Window (t_{FAW}min), Lower Clock Limit	32nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Least Significant Byte	10000ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Most Significant Byte	10000ps	27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Lower Clock Limit	16nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Least Significant Byte	2500ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Most Significant Byte	2500ps	09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Lower Clock Limit	4nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Least Significant Byte	7500ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Most Significant Byte	7500ps	1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Lower Clock Limit	12nCK	0C
94~127	Reserved -- must be coded as 0x00	Reserved	00
128~191	Reserved for future use	Reserved	00
192	SPD Revision for SPD bytes 192~447	Revision 1.0	10
193	Hashing Sequence	No authentication	00
194	SPD Manufacturer ID Code, First Byte	IDT (Renesas)	80
195	SPD Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
196	SPD Device Type	IDT (Renesas)	80
197	SPD Device Revision Number	IDT (Renesas)	12
198	PMIC 0 Manufacturer ID Code, First Byte	IDT (Renesas)	80
199	PMIC 0 Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
200	PMIC 0 Device Type	IDT (Renesas)	80
201	PMIC 0 Revision Number	IDT (Renesas)	31
202	PMIC 1 Manufacturer ID Code, First Byte	N/A	00
203	PMIC 1 Manufacturer ID Code, Second Byte	N/A	00

204	PMIC 1 Device Type	N/A	00
205	PMIC 1 Revision Number	N/A	00
206	PMIC 2 Manufacturer ID Code, First Byte	N/A	00
207	PMIC 2 Manufacturer ID Code, Second Byte	N/A	00
208	PMIC 2 Device Type	N/A	00
209	PMIC 2 Revision Number	N/A	00
210	Thermal Sensor Manufacturer ID Code, First Byte	IDT (Renesas)	80
211	Thermal Sensor Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
212	Thermal Sensor Device Type	TS0/TS1 Installed	C0
213	Thermal Sensor Revision Number	IDT (Renesas)	02
214	DRAM Specification Level	Reserved	00
215	SPD Specification Level	N/A	00
216	PMIC0 Specification Level	N/A	00
217	PMIC1 Specification Level	N/A	00
218	PMIC2 Specification Level	N/A	00
219	TS Specification Level	N/A	00
220	DIMM Specification Level	N/A	00
221~229	Reserved	Reserved	00
230	Module Nominal Height	31 < height <= 32 mm	11
231	Module Maximum Thickness	2 < thickness <= 3 mm Back side 1 < thickness <= 2 mm Front side	21
232	Reference Raw Card Used	R/C D rev 0	03
233	DIMM Attributes	Tc 0 to +95 °C, 1row	81
234	Module Organization	Symmetrical 1 Package Rank	00
235	Memory Channel Bus Width	2 channels, 40 bits per channel	32
236~239	Reserved	Reserved	00
240	Registering Clock Driver Manufacturer ID Code, First Byte	IDT (Renesas)	80
241	Registering Clock Driver Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
242	Register Device Type	DDR5RCD02 Installed	81
243	Register Revision Number	IDT (Renesas)	10
244~247	Reserved	Reserved	00
248	RCD-RW08 Clock Driver Enable	BCK_t/BCK_c Disabled QACK_t/QACK_c Enabled	2E
249	RCD-RW09 Output Address and Control Enable	QBCS[1:0]_n output Disabled BCS_n, BCOM[2:0] and BRST_n outputs Disabled(RDIMM), QBCA outputs Disabled	4A
250	RCD-RW0A QCK Driver Characteristics	Reserved	FF
251	RCD-RW0B	Reserved	00
252	RCD-RW0C QxCA and QxCS_n Driver Characteristics	Moderate Drive	11
253~447	Reserved for future use	Reserved	00
448~509	Reserved for future use	Reserved	00
510~511	CRC for SPD bytes 0~509	CRC	-
512	Module Manufacturer ID Code, First Byte	Advantech	8A

513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Made in Taiwan	02
515~516	Module Manufacturing Date		-
517~520	Module Serial Number		-
521~550	Module Part Number	SQR-RD5N16G5K6HZZG	53 51 52 2D 52 44 35 4E 31 36 47 35 4B 36 48 5A 5A 47 20 20 20 20 20 20 20 20 20 20 20 20 20 20
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte	SKhynix	80
553	DRAM Manufacturer ID Code, Second Byte	Skhynix	AD
554	DRAM Stepping	Undefined (No Stepping Number Provided)	FF
555~639	Manufacturer's Specific Data		-
640~703	End User Programmable	Reserved	00
704~767	End User Programmable	Reserved	00
768~831	End User Programmable	Reserved	00
832~895	End User Programmable	Reserved	00
896~959	End User Programmable	Reserved	00
960~1023	End User Programmable	Reserved	00

11. Appendix: Part Number Table

Product	Advantech PN
SQRAM 16GB R-DDR5-5600 2Gx8 Hynix (0~95)	**SQR-RD5N16G5K6HZZG**