swissbit®

Product Data Sheet

Industrial CFast Card

F-86 Series

SATA Gen3 – 6.0 Gbit/s, 3D pSLC

Commercial and Industrial Temperature Grade

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Made in Germany

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F-86 Series – Industrial CFast Card
10 GBytes up to 160 GBytes

1. Product Summary

- **Capacities:** 10 GBytes, 20 GBytes, 40 GBytes, 80 GBytes, 160 GBytes (3D pSLC)
- **Form Factor:** CFast-Sized Solid State Drive (36.4 mm x 42.8 mm x 3.6 mm)
- **Interface[1]:** SATA Gen3 – 6 Gbit/s (Gen2 – 3 Gbit/s and Gen1 – 1.5 Gbit/s backward compatible)
- **Command Sets:** Supports ATA/ATAPI-8 and ACS-4
- **CFast 2.0 compliant**
- **Performance:**
  - Burst Transfer Rate: Up to 600 MBytes/s in SATA Gen3 – 6.0 Gbit/s
  - Read Performance: Sequential Read up to 372 MBytes/s, Random Read 4K up to 13,100 IOPS
  - Write Performance: Sequential Write up to 223 MBytes/s, Random Write 4K up to 8,300 IOPS
- **Operating Temperature Range[2]:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3 V ± 5%
- **Power (160 GBytes) typ:**
  - Read (Active): 1,090 mW
  - Write (Active): 810 mW
  - Idle: 191 mW
  - Slumber: 50 mW
  - DEVSLP: 2.6 mW
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Endurance in DiskWritesPerDay (DWPD):**
  - JEDEC Enterprise Workload: up to 2.7
  - JEDEC Client Workload: up to 13
- **Shock/Vibration:** 500 *g* / 20 *g*
- **High-Performance Dual Core 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Triple-Level Cell (TLC) 3D NAND Flash in pSLC mode
  - Flexible BCH and GCC ECC engines provide superior error correction performance
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 2,000,000 hours @ 25 °C
  - Data Reliability: < 1 non-recoverable error per 10^{16} bits read
  - 30 µinch Gold-Plated Connector

[1] The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.
[2] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 120 °C (industrial temperature drive) and 105 °C (commercial temperature drive) respectively.

2. Product Features

- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Optimized FW algorithms especially for high read access and long data retention applications:
  - Proven power fail management for highest reliability
  - Near Miss ECC technology
    Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes the ECC margin level and refreshes data if necessary.
  - Read Disturb Management
    Read commands are monitored and the data is refreshed when critical numbers are reached.
  - Wear Leveling technology
    Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. This guarantees the maximum write endurance of the device.
  - Data Care Management
    An interruptible background process controls the user data for read disturb effects or high temperature related retention degradation and refreshes data if necessary.
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
- TRIM and NCQ Support
- ATA Security Feature Set Support
- DEVSLP Compatible
- In-Field Firmware Update[3]
- Enterprise-Grade Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- End-to-End (E2E) Data Path Protection
- Advanced protection against radiation and soft-errors by SRAM ECC and low-alpha package
- AES-128/256 encryption support with CBC and XTS modes (on request)
- TCG Opal 2.0 and secure boot feature (on request)
- On-die temperature sensor
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS 6 compliance
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK

[3] The support of In-Field FW update capabilities of host systems is recommended.

3. Ordering Information

Table 1: Standard Product List

Capacity	Part number
10 GBytes	SFCA010GHxA01Tf-t-cc-2yP-STD
20 GBytes	SFCA020GHxA01Tf-t-cc-2yP-STD
40 GBytes	SFCA040GHxA02Tf-t-cc-2yP-STD
80 GBytes	SFCA080GHxA01Tf-t-cc-2yP-STD
160 GBytes	SFCA160GHxA02Tf-t-cc-2yP-STD

x = product generation; f = flash generation; t = temperature grade; c = configuration; y = firmware revision

Table 2: Available Part Numbers

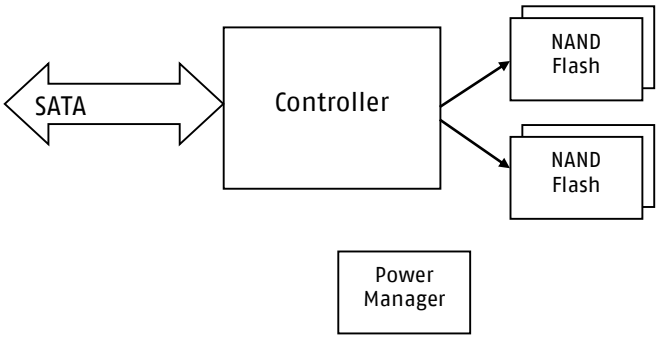
Gen3 Flash		
Capacity	**Commercial 0 °C to 70 °C**	**Industrial -40 °C to 85 °C**
10 GBytes	SFCA010GH1A01T0-C-5S-21P-STD	SFCA010GH1A01T0-I-5S-21P-STD
	SFCA010GH1A01T0-C-5S-22P-STD	SFCA010GH1A01T0-I-5S-22P-STD
20 GBytes	SFCA020GH1A01T0-C-6B-21P-STD	SFCA020GH1A01T0-I-6B-21P-STD
	SFCA020GH1A01T0-C-6B-22P-STD	SFCA020GH1A01T0-I-6B-22P-STD
40 GBytes	SFCA040GH1A02T0-C-6B-21P-STD	SFCA040GH1A02T0-I-6B-21P-STD
	SFCA040GH1A02T0-C-6B-22P-STD	SFCA040GH1A02T0-I-6B-22P-STD
80 GBytes	SFCA080GH1A01T0-C-8C-21P-STD	SFCA080GH1A01T0-I-8C-21P-STD
	SFCA080GH1A01T0-C-8C-22P-STD	SFCA080GH1A01T0-I-8C-22P-STD
160 GBytes	SFCA160GH1A02T0-C-8C-21P-STD	SFCA160GH1A02T0-I-8C-21P-STD
	SFCA160GH1A02T0-C-8C-22P-STD	SFCA160GH1A02T0-I-8C-22P-STD

Gen5 Flash		
Capacity	**Commercial 0 °C to 70 °C**	**Industrial -40 °C to 85 °C**
20 GBytes	-	SFCA020GH1A01TB-I-CA-21P-STD
40 GBytes	-	SFCA040GH1A01TB-I-EB-21P-STD
80 GBytes	-	SFCA080GH1A01TB-I-VC-21P-STD
160 GBytes	-	SFCA160GH1A02TB-I-VC-21P-STD

4. Product Description

The Swissbit F-86 Solid State Drive (SSD) leverages the CFast SATA industry-standard form factor and connectivity as well as support for AES encryption, end-to-end (E2E) security, and TCG OPAL standards. Combined with a SATA Gen3 controller and Triple-Level Cell (TLC) 3D NAND flash technology, the F-86 realizes a robust non-volatile storage solution for today's embedded storage applications. The flash is managed as pseudo Single-Level Cell (pSLC) flash, providing an optimal balance of endurance and performance. A functional block diagram of the F-86 SSD is provided below in Figure 1.

Figure 1: F-86 SATA Functional Block Diagram



The F-86 SSD incorporates two existing industry standards into a single product: the CompactFlash™ (CF) card form factor and the Serial ATA (SATA) interface commonly used with hard disk drives (HDDs) and SSDs. The interface consists of a female 7-pin SATA data connector and a female 17-pin power connector. Because standard SATA hard drives use male connectors, an adaptor is required to replace drives with CFast cards. CFast cards can be used to replace HDDs, SSDs, and Compact Flash™ cards in applications requiring smaller form factors, high endurance, and the ability to withstand shock, vibration, extreme temperatures (-40°C to 85°C), high altitude, and rough environmental conditions. The Swissbit CFast™ cards provide rugged storage for embedded and industrial systems where performance, data and system reliability, power fail protection, and flexibility are important design considerations.

The on-board SATA Gen3 controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support SATA Gen3 (6 Gbit/s) interface speeds and is fully backward compatible with SATA Gen2 (3 Gbit/s) and SATA Gen1 (1.5 Gbit/s) to enable the broadest possible range of platform compatibility. The controller utilizes two 32-bit RISC microprocessor cores, providing an optimum balance between read/write performance, Data Care Management and power fail protection.

Swissbit's F-86 SSDs deliver an impressive IOPS rate and endurance by combining TLC 3D NAND flash technology in pSLC mode with a high-end controller architecture, firmware and an optimized configuration. The SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance). This performance is achieved through the 2-channel NAND flash controller interface that supports ONFI and Toggle 2 (400 MT/s) interface speeds. In addition, the F-86 series features Swissbit's proven power fail safety and support for the ATA security feature set, NCQ, TRIM, advanced wear leveling, bad block management and in-field firmware updates.

The on-controller flexible BCH and GCC ECC engine provides superior error correction performance. This engine, combined with Swissbit's Data Care Management firmware, provides active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, and Dynamic Block Remapping.

The risk of data loss as a result of an unexpected power fail event is mitigated using a robust sequence of voltage regulators, capacitors, and detectors designed to ensure a graceful shutdown of the controller and NAND flash array. The combination of hardware and firmware power fail features prevents the possibility of resident data being corrupted during an unexpected power failure.

Related Documentation

- Serial ATA International Organization Serial ATA Revision 3.0 (http://www.serialata.org)
- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8) (http://www.t13.org)
- AT Attachment Interface Document, American National Standards Institute, X3.298-1997
- CFast™ Specification Revision 2.0-12/04/2012

4.1 Performance Specifications

The F-86 sequential and random read/write performance values are detailed in the following Table 3.

Table 3: Read/Write Performance[4]

Gen3 Flash				
Capacity	**Sequential Read (MBPS)**	**Sequential Write (MBPS)**	**Random Read 4K (IOPS)**	**Random Write 4K (IOPS)**
10 GBytes	244	84	4,400	2,500
20 GBytes	311	155	8,700	5,000
40 GBytes	372	223	13,100	8,300
80 GBytes	371	214	12,900	7,900
160 GBytes	371	216	12,900	7,900

Table 4: Read/Write Performance[5]

Gen5 Flash				
Capacity	**Sequential Read (MBPS)**	**Sequential Write (MBPS)**	**Random Read 4K (IOPS)**	**Random Write 4K (IOPS)**
20 GBytes	262	144	6,500	4,200
40 GBytes	345	243	11,700	7,700
80 GBytes	394	280	16,200	10,000
160 GBytes	395	280	16,300	10,100

[4] The values are measured using Crystal Disk Mark 7.0.0. Performance depends on flash type and number, file/cluster size, burst speed, and previously executed workload and can vary in some range. A cluster size of at least 32kB is recommended for highest performance.
[5] The values are measured using Crystal Disk Mark 8.0.1. Performance depends on flash type and number, file/cluster size, burst speed, and previously executed workload and can vary in some range. A cluster size of at least 32kB is recommended for highest performance.

4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in the following Table 5.

Table 5: Current Consumption[6]

Gen3 Flash								
Capacity	Sequential Read	Sequential Write	Random Read 4K	Random Write 4K	Idle	Slumber	DEVSLP	Unit
10 GBytes	240	175	150	150	59	15	0.8	mA
20 GBytes	280	220	170	170	59	15	0.8	
40 GBytes	310	265	190	180	59	15	0.8	
80 GBytes	300	240	185	170	59	15	0.8	
160 GBytes	330	245	190	175	58	15	0.8	

Table 6: Current Consumption[6]

Gen5 Flash								
Capacity	Sequential Read	Sequential Write	Random Read 4K	Random Write 4K	Idle	Slumber	DEVSLP	Unit
20 GBytes	300	220	165	160	60	18	0.6	mA
40 GBytes	335	275	195	185	60	22	0.6	
80 GBytes	410	285	255	190	59	22	0.6	
160 GBytes	420	295	260	195	65	22	0.6	

Current values are typical and has +/-5% tolerance. Max current consumption according to CFast specification (Power level 0). Host shall support same power level.

Typically 5 minutes after power on or 30 days permanent operating, the device performs a background data care management, that needs up to 310mA.

[6] All values are the typical values recorded running Crystal Disk Mark 7.0.0 for read/write operations at 25 °C, with nominal supply voltage and SATA transfer rate 6Gb/s.

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions for the F-86 SSD are provided in the following Table 7.

Table 7: Recommended Operating Conditions[7]

Parameter	Value
Commercial Operating Temperature	0 °C to 70 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V ± 5%

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in the following Table 8.

Table 8: Recommended Storage Conditions[8]

Parameter	Value
Commercial Storage Temperature	-40 °C to 85 °C
Storage Temperature (Commercial / Industrial model)	-40 °C to 85 °C

4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in the following Table 9.

Table 9: Shock, Vibration and Humidity

Parameter	Value
Non-Operating Shock	500 *g*, 0.5 ms pulse duration, half-sine wave (JESD22-B104 Profile A)
Non-Operating Vibration	20 *g*, 80-2,000 Hz, 3 axes, 12 cycles (MIL-STD-810G M514.6)
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B)

4.4 Regulatory Compliance

The F-86 devices comply with the directives and standards listed in the following Table 10.

Table 10: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE - 2014/30/EU FCC - 47 CFR Part 15 UKCA - S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

[7] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 120°C (industrial temperature drive) and 105 °C (commercial temperature drive) respectively.

[8] The data retention time at temperature above 40 °C is reduced. Swissbit can provide more data and support on request.

4.5 Mechanical Specifications

The F-86 SSD consists of a flash controller and NAND flash memory devices. The controller interfaces with a host system, allowing data to be written to and read from the flash memory array. The SSD has a PCIe mini connector with a SATA interface. Physical dimensions are detailed in the following Table 11. Figure 3 on page 14 illustrates the F-86 dimensions.

Table 11: Physical Dimensions

Physical Dimensions		Unit
Length	36.40±0.15	mm
Width	42.80±0.10	
Thickness (Max)	3.60	
Weight (Max Capacity)	7	g

4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in the following Table 12. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 12: Reliability

Parameter	Value
MTBF (at 25 °C)	> 2,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10^{16} Bits read
Data Retention (up to 40 °C)[9]	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytesWritten (TBW) and DriveWritesPerDay (DWPD) for the different application scenarios as shown is provided in the following Table 13.

Table 13: Endurance[10, 11]

Gen3 Flash						
Capacity	Sequential		Client[12]		Enterprise	
	TBW[13]	DWPD[14]	TBW[13]	DWPD[14]	TBW[13]	DWPD[14]
10 GBytes	245	22	125	11.4	29	2.6
20 GBytes	488	22	250	11.4	60	2.7
40 GBytes	974	22	500	11.4	117	2.6
80 GBytes	1,940	22	1,016	11.6	230	2.6
160 GBytes	3,890	22	2,330	13.3	445	2.5

Table 14: Endurance[10, 11]

Gen5 Flash						
Capacity	Sequential		Client[12]		Enterprise	
	TBW[13]	DWPD[14]	TBW[13]	DWPD[14]	TBW[13]	DWPD[14]
20 GBytes	488	22	195	8.9	57	2.6
40 GBytes	974	22	390	8.9	115	2.6
80 GBytes	1,940	22	781	8.9	242	2.8
160 GBytes	3,890	22	1,962	11.2	475	2.7

[9] NAND Flash data retention and endurance characteristics are defined according to JEDEC JESD47 and JESD22. The endurance limits of the storage shall be monitored by the life time information and simulated before field usage by the customer.

[10] Client and Enterprise workloads follow the JEDEC JESD219 standard. Enterprise workload values are measured based on 168 hours of runtime. 1 TByte = 10^{12} bytes

[11] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

[12] Because the JEDEC master trace file for the Client workload is designed for capacities ≥ 64 GBytes, the TBW and DWPD values for the capacities below 64 GBytes are estimates

[13] 3D TLC in pSLC mode – BCH 60bit correction per 1 Kbyte implemented

[14] DWPD values are based on a service life of 5 years. DWPD values with consideration of the limited lifetime warranty period of the storage device according to the used flash type and device capacity. Customer workload with higher DWPD values contributes to an earlier EOL of the storage device.

4.7 Drive Geometry Specification

The values for each capacity are shown in the following Table 15.

Table 15: Drive Geometry

Raw Capacity	User Capacity[15]	Default cylinders	Default heads	Default sectors	Sectors drive	Total addressable Bytes
32 GBytes	10 GBytes	16,383*)	16	63	19,556,208	10,012,778,496
64 GBytes	20 GBytes	16,383*)	16	63	39,091,248	20,014,718,976
128 GBytes	40 GBytes	16,383*)	16	63	78,161,328	40,018,599,936
256 GBytes	80 GBytes	16,383*)	16	63	156,301,488	80,026,361,856
512 GBytes	160 GBytes	16,383*)	16	63	312,581,808	160,041,885,696

*) The CHS access is limited to about 8GB. Above 8GB the drive must be addressed in LBA mode.

[15] 1 GByte = 10^9 bytes

5. Electrical Interface

The CFast card is connected with a standard 7-pin SATA connector and a standard 17-pin power connector. The signal/pin assignments and descriptions are listed in Table 16.

Figure 2: F-86 CFast Connector

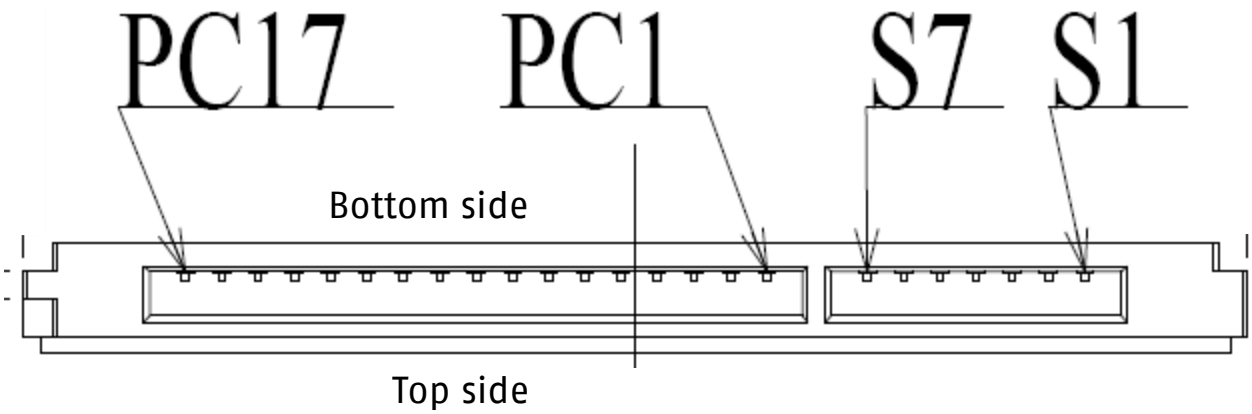


Table 16: Pin Assignment, Name, and Description

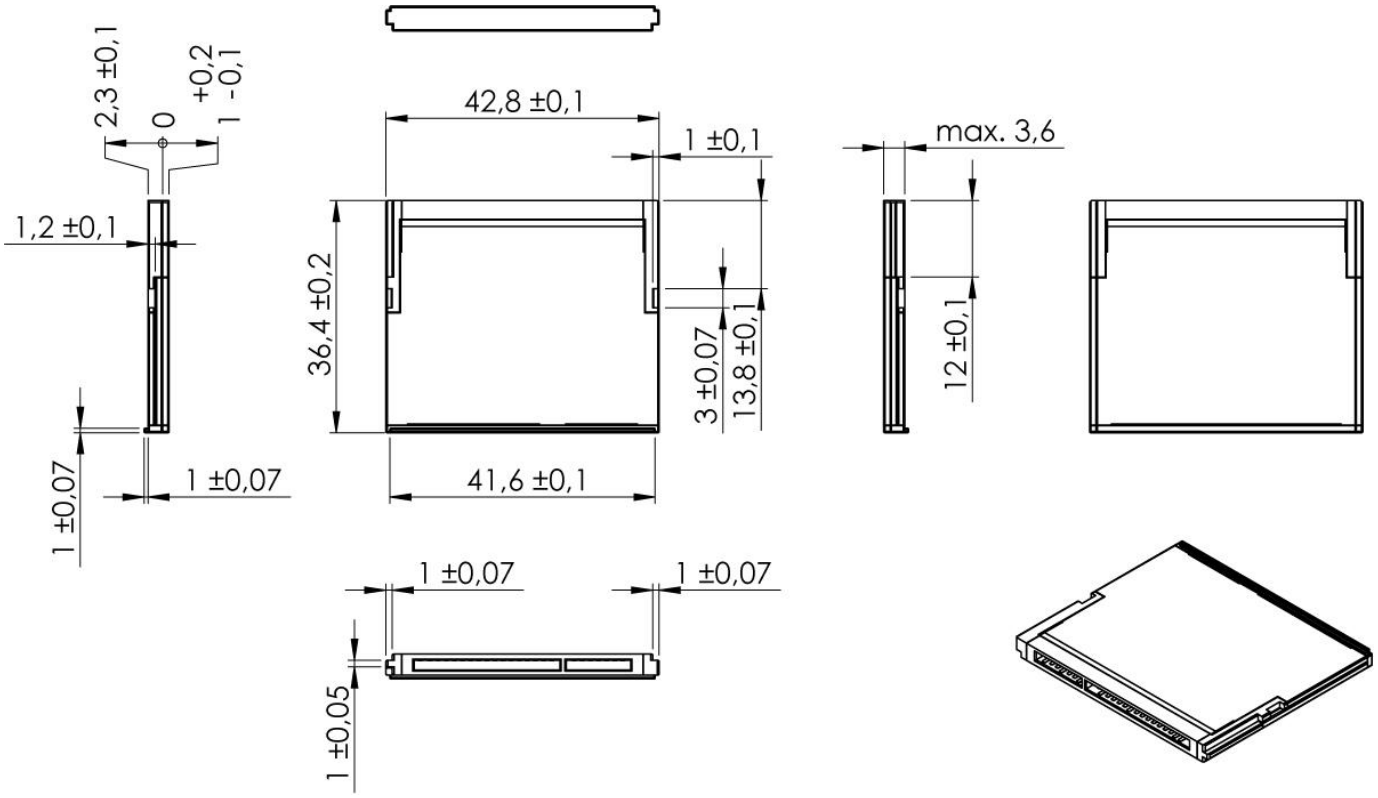
Pin	Signal Name	Description
S1	SGround	Signal Ground
S2	A+	+ Differential Device Receive Signal
S3	A-	- Differential Device Receive Signal
S4	SGround	Signal Ground
S5	B-	- Differential Device Transmit Signal
S6	B+	+ Differential Device Transmit Signal
S7	SGround	Signal Ground
PC1	CDI[16]	Card Detect In
PC2	PGround	Power Ground
PC3	DEVSLP	DEVSLP Input
PC4-PC6	NC	No Connect
PC7	PGround	Power Ground
PC8	LED1	No Connect, optional Device acitivity output
PC9	LED2	No Connect, optional SATA Link output
PC10	NC	No Connect, optional Write Protect input
PC11	NC	
PC12	IFDet	Card Output, Connected to GND
PC13-PC14	3.3 V	Device Power 3.3 V
PC15-PC16	PGround	Power Ground
PC17	CDO[16]	Card Detect Out

[16] CDI and CDO are physically shorted together in the device.

6. Package Mechanical

NOTE: The dimensions in the following figure are the maximum values based on the CFast specification. For the product dimensions, see the Mechanical Specifications section on page 10.

Figure 3: CFast SSD Drive Dimensions in mm [in]



7. ATA Commands

This section provides information on the ATA commands supported by the SSD. The commands are issued to the device by loading the required registers in the command block with the supplied parameter and then writing the command code to the register. For backward compatibility, some commands are implemented as a "no operation". See the following Table 17 for a list of ATA commands the device supports. For details about setting up the command registers, see the latest ATA Specification.

Table 17: ATA Command Set

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute Device Diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Read DMA	C8h	DMA
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
Write Verify	3Ch	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Download Microcode	92h	PIO data-out
Download Microcode DMA	93h	DMA
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

Command	Code	Protocol
S.M.A.R.T. Feature Set		
S.M.A.R.T. Disable Operations	B0h (FR=D9h)	Non-data
S.M.A.R.T. Enable/Disable Autosave	B0h (FR=D2h)	Non-data
S.M.A.R.T. Enable Operations	B0h (FR=D8h)	Non-data
S.M.A.R.T. Read Data	B0h (FR=D0h)	PIO data-in
S.M.A.R.T. Read Log	B0h (FR=D5h)	PIO data-in
S.M.A.R.T. Read Remap Data	B0h (FR=E0h)	PIO data-in
S.M.A.R.T. Read Thresholds	B0h (FR=D1h)	PIO data-in
S.M.A.R.T. Read Wear Level Data	B0h (FR=E1h)	PIO data-in
S.M.A.R.T. Return Status	B0h (FR=DAh)	Non-data
S.M.A.R.T. Write Log	B0h (FR=D6h)	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-Bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Log Ext	2Fh	PIO data-in
Read Log DMA Ext	47h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Log Ext	3Fh	PIO data out
Write Log DMA Ext	57h	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
CFA Feature Set		

Command	Code	Protocol
Erase Sector(s)	C0h	Non-data
Request sense	03h	Non-data
Translate sector	87h	PIO data-out
Write Multiple w/o Erase	CDh	PIO data-out
Write Sector(s) w/o Erase	38h	PIO data-out
Others		
Data Set Management	06h	DMA
Seek	70h-7Fh	Non-data
Erase All Blocks	C3h	Non-data

8. Identify Device Information

The following Table 18 describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

Table 18: Identify Device Information

Word(s)	Default Value	Total Bytes	Data Field Type Information
0	0040h*	2	Standard configuration (fixed)
1	XXXXh	2	Default number of cylinders
2	C837h	2	Specific configuration
3	0010h	2	Default number of heads
4-5	0000h	4	Obsolete
6	003Fh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXX*	20	Serial number in ASCII (right-justified)
20-22	0000h	6	Obsolete
23-26	XXXX*	8	Firmware revision in ASCII (big-endian byte order in Word)
27-46	XXXX*	40	Model number in ASCII (left-justified)
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	4000h	2	Trusted Computing feature set
49	0F00h*	2	Standby timer, DMA, LBA, IORDY supported
50	4001h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode 0
52	0000h	2	Obsolete
53	0007h*	2	Data Fields 54 to 58, 64 to 70, and 88 are valid
54	XXXXh	2	Current numbers of cylinders
55	0010h	2	Current numbers of heads
56	003Fh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in LBAs (Word 57 = LSW, Word 58 = MSW)
59	010X*	2	Multiple sector setting is valid
60-61	XXXXh	4	Total number of sectors addressable in LBA mode

Word(s)	Default Value	Total Bytes	Data Field Type Information
62	0000h	2	Obsolete
63	0007h*	2	Multiword DMA transfer support modes 2, 1 and 0
64	0003h	2	Advanced PIO modes supported
65	0078h*	2	Minimum Multiword DMA transfer cycle time per Word
66	0078h*	2	Recommended Multiword DMA transfer cycle time
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69	C120h*	2	CFast, Deterministic read after DSM Trim, Download Microcode DMA supported
70-74	0000h	10	Reserved
75	001Fh	1	Queue depth
76	E30Eh	2	SATA capabilities
77	00C6h	2	Additional SATA capabilities
78	015Eh	2	SATA feature support
79	0044h*	2	SATA features enabled (host changeable)
80	0FE0h	2	Major revision
81	0000h	2	Minor revision
82-84	746Bh* 7509h* 4061h*	6	Features/command sets supported
85-87	7469h* F409h* 4061h *	6	Features/command sets enabled (host changeable)
88	017F*	2	UDMA mode supported
89	0002h*	2	Time for security erase unit completion
90	0002h*	4	Time for enhanced security erase completion
91	0000h	2	Power Management
92	0000h*	2	Master password revision code
93-99	0000h*	14	Reserved
100-103	XXXXh	8	Max user LBA48 address feature set
104	0000h	2	Reserved
105	0001h	2	Maximum number of 512-bytes blocks per Data Set Management command
106	4000h	2	Sector size
107-118	0000h	24	Reserved (WWN)
119-120	4008h 4008h	4	Command set supported settings Command set features enabled (may change in operation)
121-127	0000h	14	Reserved
128	0029h*	2	Security status (may change in operation)
129-153	XXXXh	50	Reserved (vendor specific)
154-159	XXXXh	12	Vendor specific string. "Swissbit " for STD product variants
160	0000h	2	Reserved
161	8202h	2	CFast specification major version 2, ACTPM supported
162-164	0000h	6	Reserved

Word(s)	Default Value	Total Bytes	Data Field Type Information
165	80XXh*	2	CFast Card Operating Temperature Range. 8020h for commercial grade (0 to 70°C) 8058h for industrial grade (-40 to 85°C)
166-168	0000h	6	Reserved
169	0001h	2	Data Set Management supported
170-208	0000h	78	Reserved
209	4000h	2	Logical block alignment
210-216	0000h	14	Reserved
217	0001h*	2	Nominal media rotation rate: Solid State Device
218-221	0000h	8	Reserved
222	11FFh	2	Transport major revision
223-254	0000h	64	Reserved
255	XXA5h	2	Integrity Word

* Standard values for full functionality are listed. Values depend on device configuration.

9. S.M.A.R.T. Functionality

The F-86 SSD fully supports the ATA Specification for Self-Monitoring, Analysis and Reporting Technology (S.M.A.R.T.).

9.1 S.M.A.R.T. Subcommands

The following Table 19 lists the supported S.M.A.R.T. subcommands and the Features register values.
The device aborts any S.M.A.R.T. subcommands with Features register values not listed in Table 19.

Table 19: S.M.A.R.T. Features Supported

Features	Operation
D0h	S.M.A.R.T. Read Data
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/Disable Autosave
D5h	S.M.A.R.T. Read Log
D6h	S.M.A.R.T. Write Log
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status
E0h	S.M.A.R.T. Read Remap Data
E1h	S.M.A.R.T. Read Wear Level Data

9.2 S.M.A.R.T. Read Data

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following Table 20 for the data structure of this sector.

Table 20: S.M.A.R.T. Data Structure

Byte(s)	Value	Description
0–1	0100h	S.M.A.R.T. structure version
2–361	XXXXh	Attribute entries 1 to 30 (see Table 21)
362	00h	Off-line data collection status (no off-line data collection started)
363	00h	Self-test execution status byte (self-test completed)
364–365	0000h	Total time, in seconds, to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368–369	0003h	S.M.A.R.T. capabilities
370	00h	Error logging capability
371	00h	Vendor specific
372	00h	Short self-test routine recommended polling time, in minutes
373	00h	Extended self-test routine recommended polling time, in minutes
374–510	XXXXh	Reserved (vendor specific)
511	XXh	Data structure checksum

9.3 S.M.A.R.T. Attribute Entry Structure

Each attribute entry consists of 12 bytes. See the following Table 21 for the data structure of each entry.

Table 21: Attribute Entry

0	XXh	Attribute ID (see Table 22)
1–2	XXXXh	Flags (little-endian) X=2 Advisory type; X=3 Prefail type
3	XXh	Attribute value as a percentage (64h=100%)
4	XXh	Worst value as a percentage (64h=100%)
5–11	XXXXh	Raw value (little-endian)

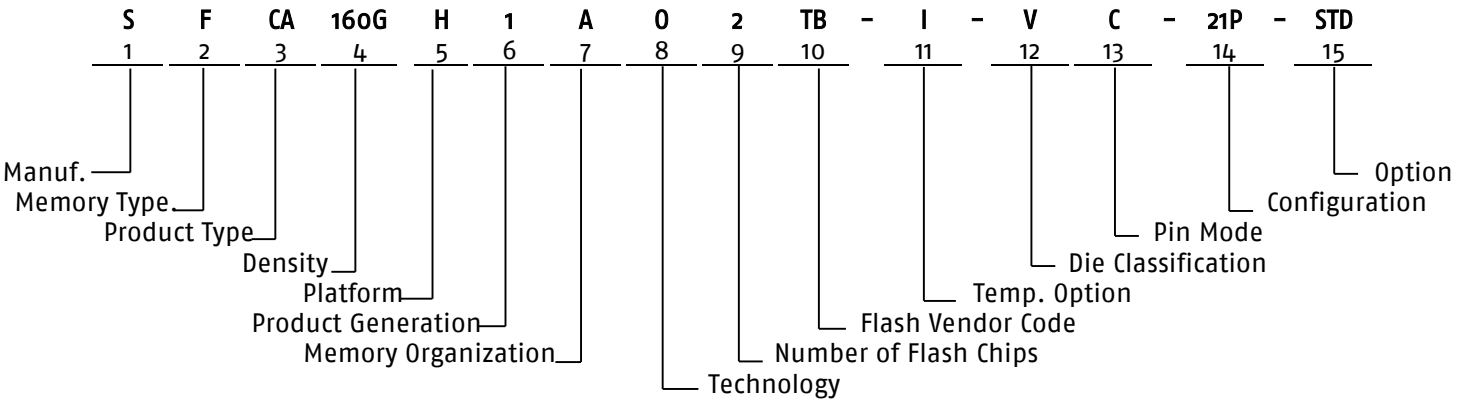
9.4 S.M.A.R.T. Attributes

The F-86 drives support the S.M.A.R.T. attributes listed in the following Table 22.

Table 22: S.M.A.R.T. Attributes

ID	Value	Worst	Threshold	Attribute	Description
0x09	100	100	0	Power On Hours	Power On Hours
0x0C	100	100	0	Power On Counter	Total number of power cycles the device encountered
0xA5	100	100	0	Maximum Erase Count	Maximum erase count on data storage blocks
0xA7	100	100	0	Total Flash Block Erases	Average erase count on data storage blocks
0xA8	100	100	0	Rated Erase Count	Rated Erase Count (target PE cycles) on data storage blocks
0xA9	100	100	0	Power On Data Repairs	Number of uncorrectable errors encountered during a power up event
0xB8	100	100	0	E2E Error Count Flash to SATA	End-to-end data path protection error count from flash to SATA interface
0xB9	100	100	0	E2E Error Count SATA to Flash	End-to-end data path protection error count from SATA interface to flash
0xC2	X °C	Max °C	0	Temperature Status	On-chip temperature sensor value (degrees Celsius) The raw value shows the current temperature in the first byte, the lowest temperature ever recorded in the second byte and the maximum temperature ever recorded in the third byte. All temperature bytes are signed.
0xC3	100	100	0	Flash ECC recovered	Total number of times the device required the read-retry process to recover data.
0xC4	X%	X%	25	Spare Block Status	Total Spare block count. The first three bytes of the raw value show the initial count and the next three bytes show the remaining spare block count.
0xC6	100	100	0	Uncorrectable ECC Errors	Total number of uncorrectable ECC errors that have occurred on flash read commands during firmware runtime
0xC7	100	100	0	Communication Errors	Host interface CRC error count
0xC8	100	100	0	SATA COM Reset	SATA COM reset counter
0xD5	X%	X%	25	Spare Block Count Worst	Spare block count of the worst channel. The drive will switch to read-only mode if 0 is reached. The first three bytes of the raw value show the initial count and the next three bytes show the remaining spare block count.
0xD7	X%	X%	0	Currently trimmed area	The percentage of device content that is currently in the trimmed state. There is no raw value.
0xE5	X%	X%	1	Total Flash Block Erases	The number of flash block erases that have been performed. Value and Worst show the remaining life.
0xE8	100	100	0	Total Read Count	The total number of sectors read from flash
0xF1	100	100	0	Total Host LBAs Written	The total number of host sectors written, in units of 32MB (65,536 sectors).
0xF2	100	100	0	Total Host LBAs Read	The total number of host sectors read, in units of 32MB (65,536 sectors).
0xF8	X%	X%	0	Remaining Erase Life Time	Percent of flash life remaining based upon the number of P/E cycles consumed

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

CFast Interface	CA

10.4 Density

10 GBytes	010G
20 GBytes	020G
40 GBytes	040G
80 GBytes	080G
160 GBytes	160G

10.5 Platform

CFast SSD	H

10.6 Product Generation

Product Generation	1

10.7 Memory Organization

x8	A

10.8 Technology

F-86 Series	0

10.9 Number of Flash Chips

1 Flash	1
2 Flash	2

10.10 Flash Code

Toshiba / Kioxia Gen3	T0
Toshiba / Kioxia Gen5	TB

10.11 Temperature Option

Commercial Temperature Range: 0 °C to 70 °C	C
Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

3D TLC MONO (single die package)	5
3D TLC DDP (dual die package)	6
3D TLC ODP (oct die package)	8
3D TLC MONO (single die package)	C
3D TLC DDP (dual die package)	E
3D TLC QDP (quad die package)	V

10.13 Pin Mode

	TSOP	BGA
Single nCE	S	A
Dual nCE	*	B
Quad nCE	*	C

*Not Available

10.14 Drive configuration XYZ

X = Type

Drive Mode	PIO	DMA Support	X
Fix	Yes	Yes	2

Y = Firmware Revision

FW Revision	Y
Firmware 1	1

Z = Feature

Feature	Z
pSLC	P

10.15 Option

Standard	STD

11. Swissbit CFast SATA SSD Marking Specification

11.1 Top View

Figure 4: F-86 top view

11.2 Bottom View

Figure 5: F-86 bottom view

11.3 Print on the label

Figure 6: F-86 label details

12. Revision History

Table 23: Document Revision History

Date	Revision	Description	Revision Details
12-NOV-2020	1.00	Initial release	Doc. req. no. 4169
18-NOV-2020	1.01	Adjusted performance values in product summary	Doc. req. no. 4188
12-FEB-2021	1.02	Updated performance, endurance and power values	Doc. req. no. 4439
02-FEB-2022	1.03	Updated product illustrations (UKCA), regulatory compliance table, S.M.A.R.T. attributes and footer (doc. classification).	Doc. req. no. 5216
28-JUN-2022	1.04	Adjusted S.M.A.R.T. attributes	Doc. req. no. 5536
13-FEB-2024	1.05	Added Flash Gen5 products to the data sheet	Doc. req. no. 6887
20-JUN-2024	1.06	Adjusted S.M.A.R.T. attributes (ID: [0Ch]; [A7h]; [A9h]; [C4h]; [C7h]; [D7h]; [E5h]; [E8h])	Doc. req. no. 7194
01-JUL-2024	1.07	Adjusted Gen5 PN	Doc. req. no. 7224
09-JUL-2024	1.08	Available Part Numbers table has been updated	Doc. req. no. 7248
02-APR-2025	1.09	Adjusted S.M.A.R.T. attributes	-